Active Current Transformer Circuits for Low Distortion Sensing in Switched Mode Power Converters

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***Abstract*—The current transformer (CT) is frequently used for sensing applications in switched mode power converters. Advantages are that galvanic isolation is inherently incorporated, bandwidth is high, losses are low and that a high-amplitude output signal may be derived. Because of this combination of advantages it may be preferred to other current sensing technologies such as the Hall-effect sensor or the sense resistance. However, it exhibits some limitations. A compromise exists between the amplitude of the output signal and the distortion present in it due to droop. Droop results as some of the input current under measurement diverts away from the "ideal" transformer within the CT's equivalent circuit and into its magnetizing branch. In addition, where the CT is used for sensing unidirectional current pulses, the duty cycle of the pulses has to be restricted if saturation of its core material is to be avoided. This paper describes techniques based on the incorporation of an active load and synchronous rectification for reducing the distortion due to droop and allowing operation at extended duty cycles. Experimental results are given for a dual transformer arrangement used to sense the choke current drawn by a boost converter circuit.**

***Index Terms*—Current transformer, droop, duty cycle, synchronous rectification.**

I. Introduction

THE CURRENT transformer (CT) [1] is frequently used in switched mode power converters so that peak or average current-mode control or limiting may be implemented [2], [3]. Advantages are that galvanic isolation is inherently incorporated, bandwidth is high, losses are low, and that a high-amplitude output signal may be derived. This last feature is particularly desirable in switched mode power converters where a high level of ambient electrical interference may be present due to switching transients. However, a limitation of the CT is that distortion in the form of droop in the output signal is present as some of the input current under measurement diverts away from the "ideal" transformer within the CT's equivalent circuit and into its magnetizing branch. Also, where the CT is used for sensing unidirectional current pulses, the duty cycle of the pulses has to be restricted if saturation of the CT's core material is to be avoided. Design compromises are required to reduce this distortion. Methods for countering these limitations using an active output stage in conjunction with synchronous rectification (SR) are introduced in this paper. Essentially, the active stage is realized using a simple op-amp circuit. This circuit maintains zero voltage across the secondary terminals of the CT thus minimizing the emf applied across its magnetizing branch. Active output stages based on op-amp circuitry have been described in [4] for low-frequency ac current measurement in the range from 30 to 5 kHz. In [4], improved accuracy is achieved by compensating for the effects of the CT's leakage impedances on the emf applied across its magnetizing branch. However, in this paper the simplified version described above is utilized as the principal technique investigated is the incorporation of SR to enhance the performance of CTs in applications where their output signals have to be rectified. The active load and SR are initially discussed in schemes for ac current sensing and unidirectional current pulse sensing respectively. They are then introduced into a scheme for sensing the choke current in a single-ended power converter topology by means of the dual transformer method described in [3] and [5]. The choke current may, however, be measured using a single CT in series with it. Although the CT is not inherently able to sense dc currents, this may be achieved using one of two principal techniques. Periodic resetting circuitry may be used as described in [1] or the secondary winding may be incorporated into an LR multivibrator circuit which is used to detect asymmetrical excitation of the CT's core material and provide a compensating current [6], [7]. A variant of the latter technique uses a CT with a tertiary winding in conjunction with two MOSFETs [8]. However, where periodic resetting or incorporation into a multivibrator circuit is implemented, the bandwidth is low and effective peak current control or limiting may not be attainable. The dual transformer method may therefore be preferred. In this paper the effect of introducing an active load in conjunction with SR is experimentally evaluated in a dual transformer arrangement used to measure the choke current drawn by a boost converter.

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II. Review of Current Transformer Operation

Fig. 1(a) depicts a commonly described transformer equivalent circuit. This is simplified to that shown in Fig. 1(b), where, in addition to the ideal transformer, only the inductive leg of the magnetizing branch (L_m) and the resistance of the secondary winding (R_2, denoted in Fig. 1(b) and in subsequent figures by R_{Cu}) are shown. As the CT is effectively fed from a current source, i_p, and not a voltage source, the primary winding resistance and leakage inductance (R_1 and L_1) are assumed not

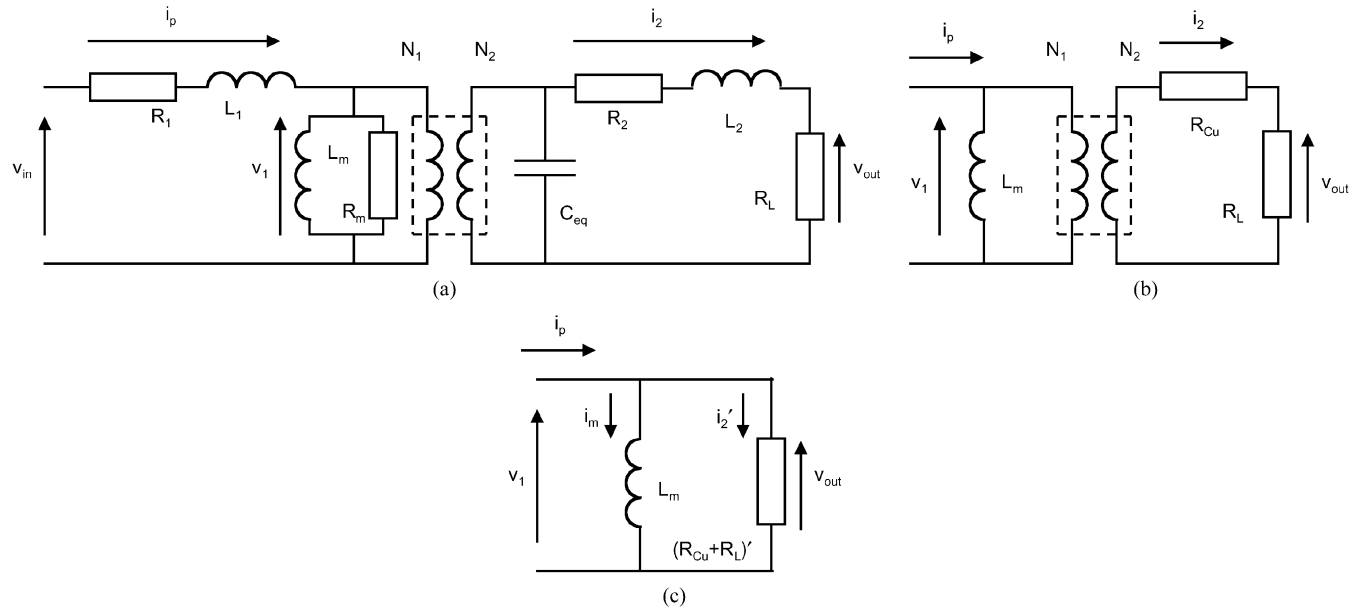

Fig. 1. Transformer equivalent circuits: (a) transformer equivalent circuit showing parasitic elements, (b) current transformer simplified equivalent circuit, and (c) equivalent circuit from (b) with load referred to primary side.

to affect the voltage $(\mathrm{v_1})$ across the magnetizing branch of the transformer. The flux density excursion in a transformer used for current sensing is normally small and the resistive leg $(\mathrm{R_m})$ of the magnetizing branch used to model core losses is therefore neglected. The secondary leakage inductance $(\mathrm{L_2})$ is neglected as it is assumed that the transformer is constructed with a toroidal core carrying a secondary winding with evenly spaced turns. A toroidal core shape is normally preferred in switched mode CT applications, since, in addition to the low achievable leakage inductance, no gaps are introduced into the magnetic circuit and the high intrinsic permeability of the core material is therefore retained.

In high-frequency measurement applications short rise-times are required and the interaction of the leakage inductances, winding resistances and parasitic capacitances of the CT may have to be taken account of [9]. If the CT is constructed as described above, the rise-time is normally satisfactory for power control applications. However, the equivalent parasitic capacitances, shown lumped together as "$\mathrm{C_{eq}}$" in Fig. 1(a), may prevent the CT from resetting fully under conditions of high frequency and duty cycle unless an active reset technique is used. This is addressed in [5] and is discussed further below. A high-permeability material is normally used to maximize the magnetizing inductance and therefore reduce droop as described above. Several corollaries, described in [9], result when such a material is used, that is, one with a high ratio of Zinc to Manganese in the dopant. These are relatively high core losses, a low saturation flux density and a low Curie Temperature and are not normally problematic in a CT due to the low flux density excursion.

The sum of the resistance of the secondary winding, $\mathrm{R_{Cu}}$, and the load resistance, $\mathrm{R_L}$, may be referred to the CT's primary side to give the circuit shown in Fig. 1(c) where

$$(\mathrm{R_{Cu}} + \mathrm{R_L})' = (\mathrm{N_1}/\mathrm{N_2})^2(\mathrm{R_{Cu}} + \mathrm{R_L}). \tag{1}$$

Ideally, the referred secondary current, i_2', in this referred resistance is equal to the primary current, $\mathrm{i_p}$. However, as the transformer's magnetizing inductance, $\mathrm{L_m}$, lies in parallel with this resistance, as shown in Fig. 1(c), it draws some of the primary current which would otherwise flow as referred secondary current. If the primary current undergoes a step change from zero to $\mathrm{I_p}$ at $\mathrm{t} = 0, \mathrm{i}_2'$ decays according to

$$\mathrm{i}_2' = \mathrm{I_p e^{-t/\tau}}. \tag{2}$$

Alternatively expressed, as $\mathrm{i}_2' = (\mathrm{N_2}/\mathrm{N_1})\mathrm{i_2}$ then

$$\mathrm{i_2} = (\mathrm{N_1}/\mathrm{N_2})\mathrm{I_p e^{-t/\tau}}. \tag{3}$$

It can be seen from (3) that the output current in the load resistance decays exponentially toward zero from its initial value of 100% of i_p' where i_p' is the primary current referred to the secondary side, given by $(\mathrm{N_1}/\mathrm{N_2})\mathrm{i_P}$. The time constant, τ, is given by

$$\tau = \mathrm{L_m}/(\mathrm{R_{Cu}} + \mathrm{R_L})'. \tag{4}$$

Normally $\mathrm{R_{Cu}}$ is much smaller than $\mathrm{R_L}$ and may be neglected when calculating τ. $\mathrm{L_m}$ is given by

$$\mathrm{L_m} = \mathrm{A_e}\mu_0\mu_\mathrm{r}\mathrm{N_1^2}/\mathrm{l_e} \tag{5}$$

$\mathrm{A_e}\mu_0\mu_\mathrm{r}/\mathrm{l_e}$ is given by the core's inductance factor, $\mathrm{A_L}$. For a small (c.10 mm outside diameter) ferrite core $\mathrm{A_L}$ is typically 2500 nH per turn squared. $\mathrm{N_1}$ is normally one and therefore $\mathrm{L_m}$ is 2500 nH. N2 is typically 100. If the primary current is 10 A then the secondary current is, ideally, 100 mA. To develop an output voltage of 1 V a load resistance of 10 Ω is therefore required. This refers to the primary side to give 1 mΩ and a CT time constant, τ, of 2.5 ms from (4) if $\mathrm{R_{Cu}'}$ is neglected.

For a given set of transformer parameters ($\mu_\mathrm{r}, \mathrm{A_e}, \mathrm{l_e}, \mathrm{N_1}$ and $\mathrm{N_2}$), this decay can be made slower by reducing the resistance

of R_L and therefore increasing τ. However, the voltage, v_{out}, developed across R_L by i_2 is now reduced.

III. Incorporation of Active Loads and Synchronous Rectification

A. Active Load Used for Bidirectional AC Current Sensing

A CT is often used to sense the bidirectional ac current in the primary winding of a power transformer utilized in a half-bridge or full-bridge switched mode power converter. A typical current waveform is shown in Fig. 2(a). CT core reset circuitry is not required when used in this application as the waveform has 180° symmetry, and the positive and negative volt–second products applied across the CT's magnetizing branch over one cycle are therefore identical.

Instead of connecting a load resistance (R_L), directly across the secondary winding of the CT, as shown in Fig. 2(b), thereby forming the equivalent circuit shown in Fig. 1(b) and (c), the circuit shown in Fig. 2(c) may be implemented. The CT's secondary current flows into the node connected to the op-amp's inverting terminal. The op-amp is connected in an inverting configuration and maintains its inverting terminal at virtually the same potential as its noninverting terminal which is connected to the other end of the CT's secondary winding. As both ends of this winding are held at virtually the same potential by the feedback action of the op-amp, there is effectively a short-circuit across it.

The referred resistance, R', seen in parallel with the magnetizing branch on the primary side of the CT, is now reduced from $(R_{Cu} + R_L)'$ to R'_{Cu}

$$R' = (N_1/N_2)^2 R_{Cu} \tag{6}$$

and hence, τ is now increased from $L_m/(R_{Cu} + R_L)'$ to

$$\tau = L_m/R_{Cu}.' \tag{7}$$

The op-amp develops a voltage across R_F equal to $i_2 R_F$. Where required, TR1 and TR2 act as a class B current amplifier to ensure that sufficient current may be driven through R_F to hold the op-amp's inverting terminal at virtual ground. A class AB configuration may be preferred where the "crossover" distortion of the class B stage is excessive.

A practical consideration taken into account is that it may be necessary to high-pass filter the circuit's output voltage. As the input impedance of the circuit feeding the op-amp is very low, being the CT's secondary winding resistance (R_{Cu}) in the steady-state, TR1 or TR2 may have to source a large offset current to satisfy any offset voltage present at the op-amp's inputs. To remove the resultant offset voltage present across R_F, a high-pass filter (R_f, C_f) is used.

Unlike the arrangement shown in Fig. 2(b), the voltage across R_F cannot be directly bridge-rectified in order to compare both positive and negative excursions with a maximum peak current set level, as it is referenced to ground. However, rectifying the signal in this way, as described in [1], is in any case undesirable as the rectifier diode voltage drops would be reflected back to the CT's primary winding, thereby forcing current into its magnetizing branch. As an alternative, a "window detection" arrangement of two comparators may be used to realize a practical peak current detection circuit [10]. Their outputs are connected in a "wired-OR" configuration.

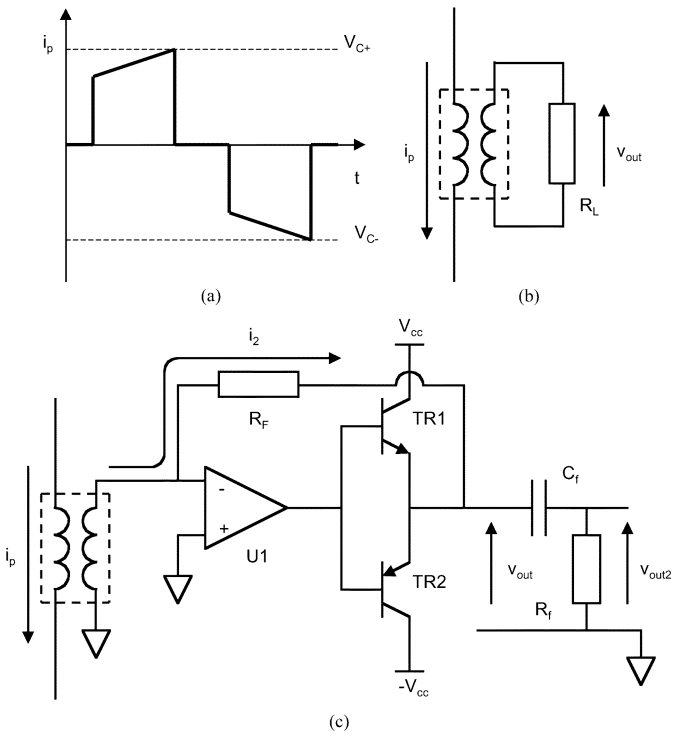

Fig. 2. Bidirectional current sensing: (a) typical bidirectional current waveform, (b) current transformer with load resistance, and (c) current transformer with active output stage.

When a positive current excursion produces a voltage above V_{C+} or a negative excursion produces a voltage below V_{C-}, the respective comparator output sinks current and produces a low output signal which is used to terminate the pulse driving the switching devices. A negative reference level may be derived from a positive reference level by means of an op-amp in an inverting configuration, thereby avoiding the addition of a second voltage reference. Ramp reference waveforms may be applied to the comparators where slope compensation is required.

B. Active Load Used for Unidirectional Current Pulse Sensing

Fig. 3(a) shows a scheme used to sense unidirectional current pulses such as the current in the power device in a single-ended power converter, for example, the buck or boost converter or isolated-output topologies such as the forward or flyback converters. Unlike the bidirectional sensing circuit shown in Fig. 2, rectification of the CT's output is, in this case, required. A typical waveform is shown in Fig. 3(b). In the circuit shown in Fig. 3(a), a negative output voltage appears across R_L when the power device, TR1, conducts. D1 may be included to reset the CT's core material using a suitable voltage clamp when TR1 is off. During this interval the rectifier diode (D2) prevents the reset voltage from being applied to the load resistance. D1 prevents the reset voltage from being applied to the CT when TR1 is on. The duty cycle at which TR1 operates has to be restricted to a maximum value to allow the CT sufficient time to reset. This is discussed further below.

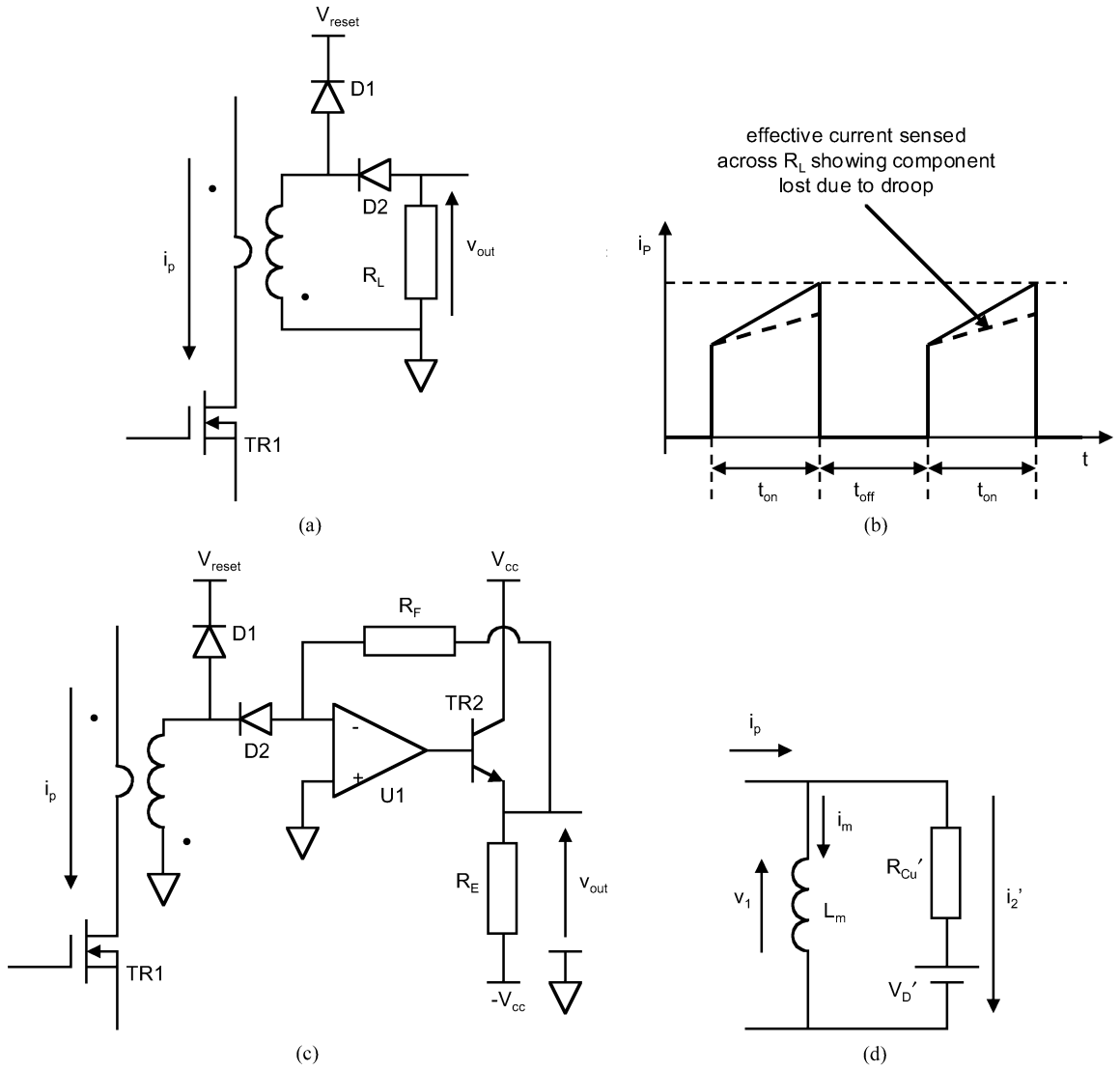

Fig. 3. Unidirectional current pulse sensing: (a) unidirectional current pulse sensing with load resistance, (b) typical unidirectional current pulse waveform, (c) unidirectional current pulse sensing with active load, and (d) equivalent circuit from Fig. 3(c) with load referred to primary side.

Instead of a load resistance, an active output stage can be added as shown in Fig. 3(c). Where required, TR2 acts as a class A current amplifier to ensure that the CT's secondary current may be driven through $\mathrm{R_F}$. However, even with the load resistance negated, the rectifier diode, D2, still produces a voltage drop $(\mathrm{V_D})$ which is reflected back to the CT's primary side leading to droop. Fig. 3(d) shows the CT's equivalent circuit when used in this mode. In this case the droop is not exponential but may be taken as linear if the effect of $\mathrm{R_{Cu}}$ is sufficiently small in comparison with that of D2 to be neglected. The magnetizing current, $\mathrm{i_m}$, is given by

$$\mathrm{i_m(t) = (V'_D t)/L_m} \tag{8}$$

where $\mathrm{V'_D}$, the referred diode voltage drop, is given by

$$\mathrm{V'_D = V_D(N_1/N_2).} \tag{9}$$

C. Active Load and Synchronous Rectification Used for Unidirectional Current Pulse Sensing

In Fig. 4, synchronous rectification (SR) [11], realized using a MOSFET (TR3), is introduced in place of the passive rectifier diode (D2 in Fig. 3(c)) to counteract droop and allow operation at an improved duty cycle. TR3 is turned on at the same time as the power switch, TR1, and conducts in reverse to provide a low resistance path for the CT's secondary current to flow into the op-amp circuit. When TR1 is held off, TR3 is also held off and prevents the reset voltage appearing across the secondary winding of the CT from being applied to the op-amp. The droop resulting from this scheme is given by (3) where, in this case, τ is given by

$$\tau = \mathrm{L_m/(R_{Cu} + R_{DS(on)}).'} \tag{10}$$

$\mathrm{R_{DS(on)}}$ is the on-state resistance of the MOSFET and is assumed to be identical when both forward and reverse biased. In the case of a small-signal low-voltage MOSFET, $\mathrm{R_{DS(on)}}$ is

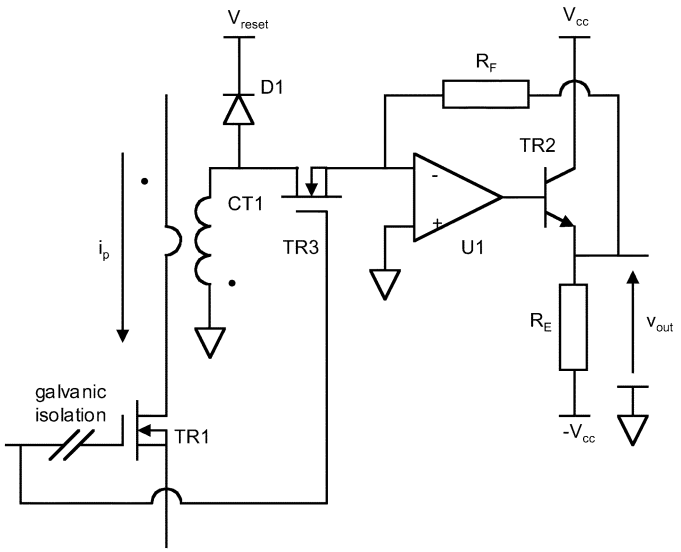

Fig. 4. Unidirectional current pulse sensing circuit with active load and synchronous rectification.

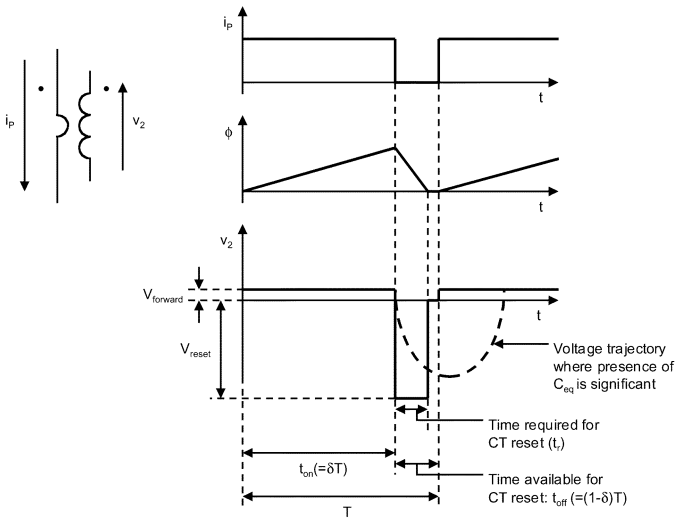

Fig. 5. CT reset waveforms.

typically between 100 and 500 mΩ. The droop caused by the voltage drop incurred by the CT's secondary current (typically 10–100 mA) flowing in this resistance is therefore lower than that across a pn diode (approximately 600 mV) or a Schottky Diode (approximately 400 mV).

As shown in Fig. 4, TR1 may be driven via a galvanically isolated barrier, for example an opto-isolator. The drive signal applied to the primary side of this barrier may be used to drive TR3. The inherent isolation between power and control circuits provided by the CT is therefore retained.

Apart from reduced droop, a further advantage of SR is that for a given reset voltage $(\mathrm{V_{reset}})$ a CT may be operated at a higher duty cycle than if a passive diode were used to rectify its output voltage. Reset waveforms are shown in Fig. 5. In accordance with Faraday's Law, to prevent the CT's core material from saturating the following restriction must be observed to ensure that a sufficient volt–second product is available to reset it by returning the core flux (ϕ in Fig. 5) to zero each cycle

$$\mathrm{t_{on}V_{forward}} \leq \mathrm{t_{off}V_{reset}} \tag{11}$$

where $\mathrm{V_{forward}}$ is the voltage drop across the CT's secondary winding during its on-time when it is driving current into the load impedance. $\mathrm{t_{on}}$ and $\mathrm{t_{off}}$ are given by $\delta\mathrm{T}$ and $(1-\delta)\mathrm{T}$, respectively

$$\delta\mathrm{TV_{forward}} \leq (1-\delta)\mathrm{TV_{reset}}. \tag{12}$$

This rearranges to give the maximum allowable duty cycle $(\delta_{\max})$

$$\delta_{\max} = \mathrm{V_{reset}}/(\mathrm{V_{forward}} + \mathrm{V_{reset}}). \tag{13}$$

As $\mathrm{V_{forward}}$ is now lower than previously, δ can be increased closer to 100%. The parasitic capacitance lying in parallel with the CT's secondary winding (shown as $\mathrm{C_{eq}}$ in Fig. 1) may, however, render (13) inappropriate. Instead of the current in the CT's secondary magnetizing inductance $(\mathrm{L_{m2}})$ ramping down linearly at turn-off, $\mathrm{C_{eq}}$ and $\mathrm{L_{m2}}$ form a lightly damped resonant circuit. Due to the effect of $\mathrm{C_{eq}}$, the maximum voltage appearing may be sufficiently well defined for a reset voltage clamp not to be required. Provided the rectifier element can support this voltage, omitting the clamp is preferred as its presence reduces the volt–second product applied across the CT at reset. Neglecting signs, the voltage appearing across the CT's secondary winding is given by

$$\mathrm{v_c(t)} = \sqrt{(\mathrm{L_{m2}/C_{eq}})}\mathrm{I_m}\sin\omega_{\mathrm{r}}\mathrm{t} \tag{14}$$

where $\mathrm{I_m}$ is the magnetizing current at power switch turn-off and ω_{r} is given by $\sqrt{\mathrm{L_{m2}C_{eq}}}$. The current, $\mathrm{i_m(t)}$, leads this voltage by $\pi/2$ radians and is given by

$$\mathrm{i_m(t)} = \mathrm{I_m}\cos\omega_{\mathrm{r}}\mathrm{t}. \tag{15}$$

The CT is reset when $\mathrm{i_m(t)} = 0$, that is, when a quarter-period has elapsed and $\mathrm{t} = \pi/2\omega_{\mathrm{r}}$. A resistor, $\mathrm{R_E}$, is shown in the emitter of TR2 in Figs. 3(c) and 4. This is because when the CT is resetting and the rectifier (D2 or TR3, respectively) is not conducting, a small negative voltage may be required at the op-amp's inverting terminal to satisfy any worst-case offset voltage present. TR2 cannot sink current and the op-amp output may saturate at the negative rail voltage. This resistor allows a negative voltage to appear and therefore prevents the op-amp's output from going to the negative rail trying to source this voltage. The op-amp's transient response, when the load current is re-applied, is therefore improved as its output voltage has to slew less before settling as it is pre-positioned at approximately 0.7 V above signal ground. The resistance of $\mathrm{R_E}$ is selected so that its power dissipation is not excessive but so that forward biasing of the base-emitter junction of TR2 is ensured during CT off-times.

Fig. 6 shows the dual transformer arrangement used to sense the input (choke) current drawn by a boost converter. Typical current waveforms are shown in Fig. 7. CT1 and CT2 are located such that they sense the switch and diode currents respectively. The voltage across the load resistance, $\mathrm{R_L}$, is ideally at all times proportional to the choke current being sensed, assuming that the reverse recovery current conducted by D1 and the off-state leakage currents conducted by D1 and TR1 may be regarded as negligible. Polarities of the CT connections shown

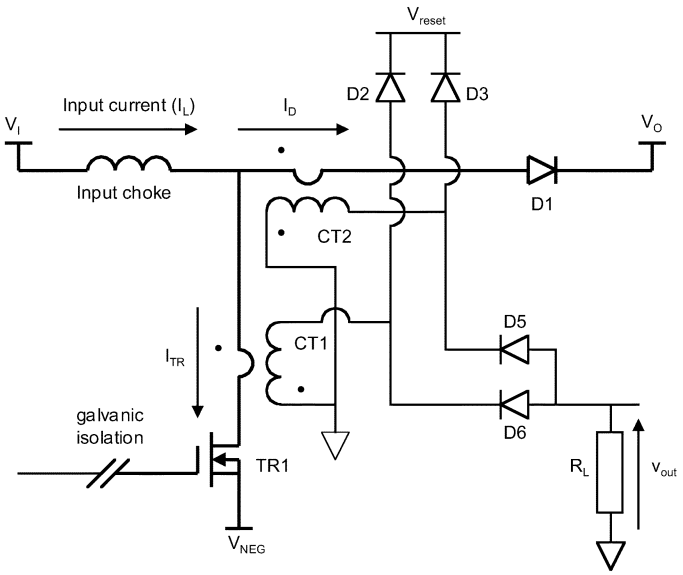

Fig. 6. Dual transformer technique used for sensing input current in boost converter.

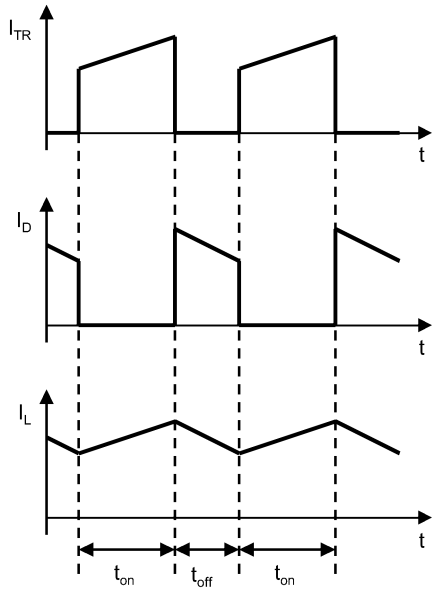

Fig. 7. Typical current waveforms in power converter switch, diode and choke.

are such that a negative voltage is developed across $\mathrm{R_L}$. The same principle may also be used for sensing the choke current in the buck converter. The boost converter topology is commonly used to realize power factor correction (PFC) circuits. In this application accurate sensing of the input current drawn is normally necessary to ensure low distortion. The dual transformer arrangement is advantageous here as, unlike the sense resistor technique, galvanic isolation is inherent and losses are low for a given output signal magnitude. In PFC circuits, an average current control loop is usually implemented without including an inner peak current control loop. However, peak current limiting is usually incorporated to protect the power switch against transient over-currents. The high bandwidth of the dual transformer technique is therefore particularly advantageous in this application when compared to the schemes described in [1], [6]–[8].

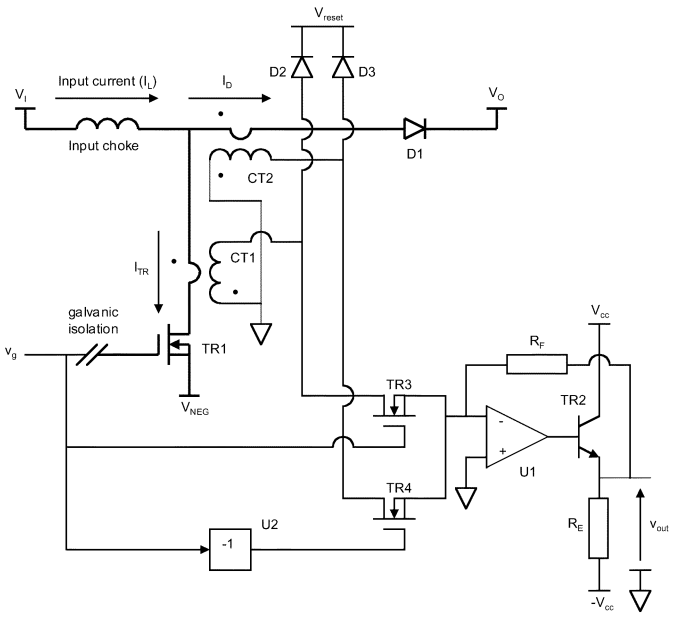

Fig. 8. Dual transformer technique using active output stage with synchronous rectification.

Fig. 8 shows an arrangement [12] where the circuit shown in Fig. 6 is adapted to incorporate an active load and SR. TR3 is turned on when the power device is on and TR4 is turned on when it is off. TR3 is driven with the same low-voltage signal used to drive the power switching device, TR1, prior to the isolation barrier and TR4 is driven with a complementary signal as shown.

The dual transformer technique imposes maximum and minimum duty cycle restrictions on the operation of TR1 due to the requirement to reset both CT1 and CT2, respectively. An exception may occur when the converter enters the discontinuous current mode of operation and a minimum duty cycle is not required to reset CT2. Where SR is introduced, duty cycles closer to 0 and 100% for a given reset voltage are expected as given by (13).

Where a boost converter is used for PFC, a power switch duty cycle up to 100% is desirable when the input voltage crosses through zero in order to reduce crossover or "cusp" distortion. When a CT is used in series with the power switch, a compromise exists between avoiding this form of distortion and that due to CT saturation as the power switch's duty cycle approaches 100% and sensing is lost [13].

MOSFETs with logic-level gates may be used as the SR elements. The arrangements in Figs. 5 and 8 use N-channel MOSFETs. Compared to the use of P-channel MOSFETs this provides two principal advantages. First, their gates may be driven with positive-going signals referenced to signal ground. Second, for a given silicon area the on-state resistance is lower. The complexity and cost introduced is minimal due to their simple drive requirements as they are voltage driven and may be referenced to the same ground rail as the converter's control circuit. They may also be driven from the same signal used to drive the power-switching device prior to isolation. Typical industry-standard packages used for commercially available

MOSFETs are the SOT23 and SOT323 outlines. These packages are also used for the passive rectifier diodes which would conventionally be used. SR may therefore be incorporated into a sensing scheme with no increase in the circuit's "footprint" area or volume being required.

IV. Experimental Results

Three schemes are discussed in this paper, for bidirectional ac, unidirectional current pulse, and dual transformer choke current sensing. Experimental results are given for the dual transformer current sensing circuit, as this circuit incorporates and demonstrates the principal features introduced, the active load and SR.

Two CTs were assembled using Ferroxcube TN9/6/3 toroidal cores in 3E25 material, wound with 100 turns of 0.25-mm diameter enameled copper wire forming the secondary winding. The primary "winding" was in each case a single conductor passed once through the CT's aperture. The secondary magnetizing inductances of both CTs were measured at 13.1 mH using a model 6425 Precision Component Analyzer manufactured by Wayne Kerr, Ltd. This inductance refers to the CT's primary side to give a primary magnetizing inductance of 1.31 μH. The resistance of each CTs' secondary winding was established at 0.53 Ω using the "four-wire" measurement technique. 1N4148 diodes and ZVN4306A MOSFETs were used as the passive diodes and synchronous rectifiers, respectively. The op-amp (U1) was a NE5534A type. A ZTX451 bipolar transistor used in location TR2. The power device (TR1), in this case a MOSFET, was driven via an isolation barrier based around a TLP2200 high-speed opto-isolator. A ± 12-V rail was used to supply this circuitry. The $+12$-V rail was also used as the CT reset voltage (V_{reset}). A 74 ac series gate (U2) operating from a $+5$-V rail was used to invert the signal used to drive TR4.

A boost converter, as shown in Fig. 6, was arranged. The input current was set using a constant current source. Losses in power components prevented a very high output voltage from being developed when operated at a high duty cycle. The dual transformer arrangement is used for experimentation as its expected output is, ideally, constant regardless of the duty cycle applied with respect to either CT. Recalculation of the expected output voltage value to account for variation in the duty cycle is therefore not required. A drop in the expected value is taken as indicating the onset of incomplete reset in that CT operating at the higher duty cycle.

A first experiment was conducted with an average current of 10 A conducted by the choke with the power switch operating at a duty factor of 50%. The switching frequency was varied. The effective current detected against frequency is tabulated in Fig. 9 for the following three conditions.

1) A load resistance is fed directly by means of rectifying diodes as shown in Fig. 6.
2) An active output stage is fed by means of rectifying diodes. This is the arrangement shown in Fig. 6 but with the load resistor, R_L, replaced with the op-amp stage shown in Fig. 8.
3) An active output stage is fed by means of synchronous rectifiers as shown in Fig. 8.

f(kHz)	(I) Output voltage (V): Passive Load	(II) Output voltage (V): Active Load Only	(III) Output voltage (V): Active Load with Synchronous Rectification
0.3	-	-	4.45
0.4	-	-	4.73
0.5	-	-	4.78
0.6	-	-	4.82
0.7	-	-	4.85
0.8	-	-	4.86
0.9	-	-	4.87
1	-	-	4.89
2	-	-	4.92
3	-	-	4.94
4	-	-	4.93
5	-	4.69	4.97
10	1.99	4.87	4.97
20	3.71	4.94	4.98
30	4.62	4.94	4.98
40	4.72	4.95	4.98
50	4.77	4.97	4.99
60	4.80	4.97	4.98
80	4.84	-	4.95
100	4.87	-	4.94

Fig. 9. Effect of cumulatively adding active and synchronous rectification stages to dual transformer current sensing circuit.

The load, R_L, or op-amp feedback resistance, R_F, as applicable, was in each case set at 50 Ω. A suitable capacitance was placed in parallel with this resistance to filter out the switching frequency ripple voltage to obtain the average dc value. The intended gain of the circuits was therefore 500 mV/A ideally giving an output voltage, V_{out}, of 5 V for 10-A sensed current. An HTP50 closed-loop Hall-effect sensor manufactured by LEM-HEME was used to accurately calibrate the current under measurement.

A second experiment was conducted where, again with the choke current set at 10 A, but with a fixed frequency of 25 kHz, the duty cycle of the converter was varied for the following two conditions.

1) An active output stage is fed by means of rectifying diodes. This is the arrangement shown in Fig. 6 but with the load resistor, R_L, replaced with the op-amp stage shown in Fig. 8.
2) An active output stage is fed by means of synchronous rectifiers as shown in Fig. 8.

It can be seen from Fig. 9 that the low-frequency performance of the dual transformer arrangement is progressively enhanced by means of cumulatively adding active and SR stages. This is attributed to the reduction in droop in the currents sensed in the converter's transistor and diode paths. When used with SR, a decline in the output signal is seen at above approximately 60–80 kHz. Some factors are expected to degrade performance at raised frequencies. The capacitances of the SR devices are added to the CT's parasitic capacitance and the CT secondary conductor resistance is expected to rise due to the skin effect. The effective mismatching between the propagation delays through the power switch and the SR devices is expected to be greater as these delays occupy a greater proportion of the switching period. Referring to Fig. 10, it can be seen that adding SR increases the allowable duty cycle at which the CT is used. Figs. 11 and 12 show oscillograms of the resetting behavior of the CT when used with passive diode rectification (condition I) at duty cycles of 50% and 92%, respectively. At 92% duty

Duty Factor, δ (%)	(I) Output Voltage (V): Active Load Only	(II) Output Voltage (V): Active Load and Synchronous Rectification
50	4.94	4.95
55	4.93	4.95
60	4.93	4.96
65	4.93	4.96
70	4.92	4.96
75	4.92	4.96
80	4.92	4.95
90	4.92	4.95
91	4.91	4.93
92	4.90	4.92
93	3.51	4.90
94	3.10	4.89
95	2.55	4.84
96	-	4.75
97	-	4.62

Fig. 10. Effect of adding synchronous rectification on distortion as duty cycle of power switch is increased.

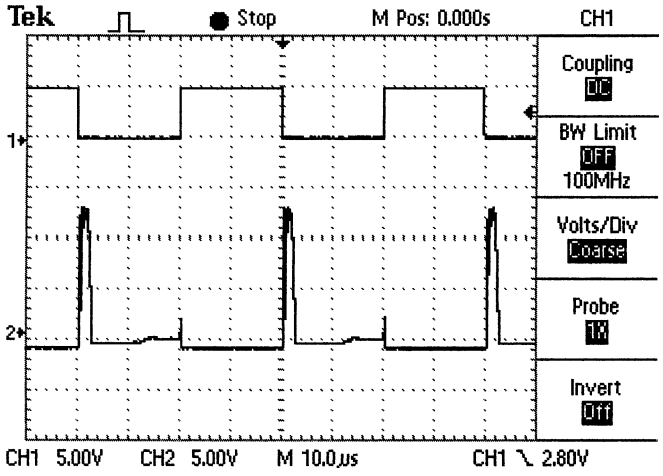

Fig. 11. Drive signal (upper trace) and CT secondary voltage (lower trace) with diode rectification at $\delta = 50\%$.

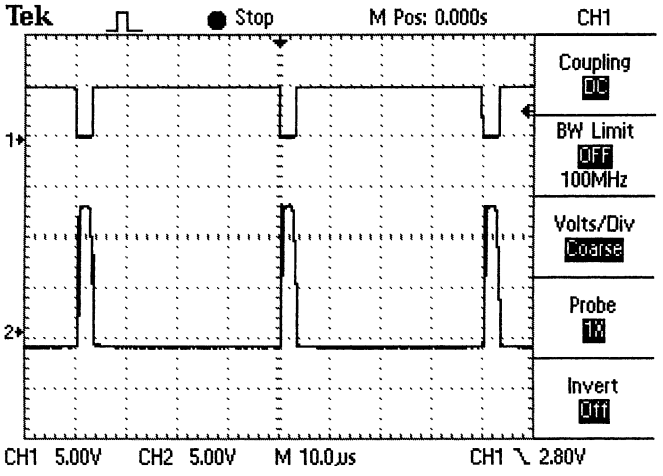

Fig. 12. Drive signal (upper trace) and CT secondary voltage (lower trace) with diode rectification at $\delta = 92\%$ (onset of incomplete reset).

cycle incomplete resetting is arbitrarily deemed to take place as the measured output signal is 1% less than that ideally expected.

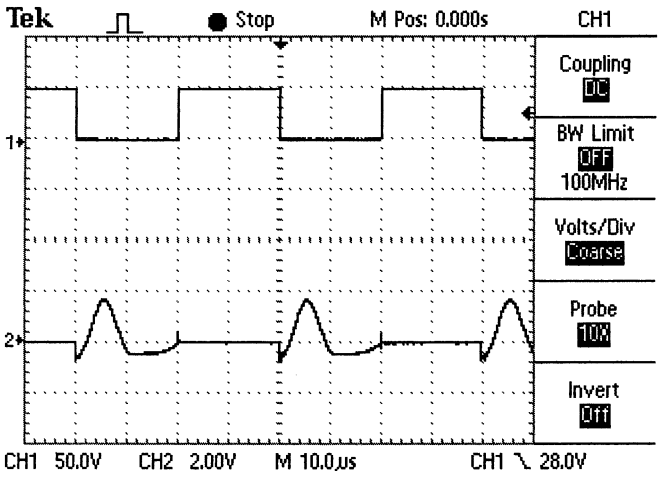

Fig. 13. Drive signal (upper trace) and CT secondary voltage (lower trace) with SR at $\delta = 50\%$.

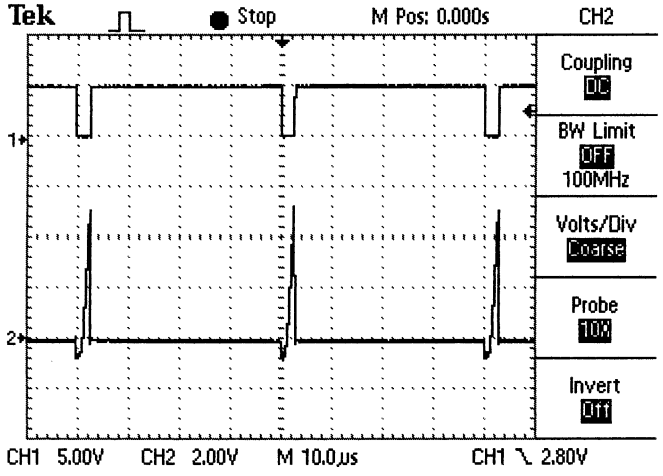

Fig. 14. Drive signal (upper trace) and CT secondary voltage (lower trace) with SR at $\delta = 94\%$ (onset of incomplete reset.

The upper traces show the drive signal $(\mathrm{v_g})$ applied to TR1 prior to the isolation barrier and the lower traces show the voltage across CT1.

The voltage across CT1 is approximately -0.6 V when it is conducting in the forward direction. This is due to the rectifier diode's voltage drop. It can be seen that the rectangular approximation of the CTs resetting behavior shown in Fig. 5 is appropriate in this case. The effective voltage appearing across the CT's secondary winding is calculated from

$$\mathrm{V_{forward}} = \mathrm{I_2 R_{Cu}} + \mathrm{V_D} \tag{16}$$

where $\mathrm{I_2}$ is 100 mA, $\mathrm{R_{Cu}}$ is 0.53 Ω, and $\mathrm{V_D}$ is taken as 650 mV. $\mathrm{V_{forward}}$ is therefore 703 mV. This and the reset voltage of 12 V are put into (13) to give a predicted maximum duty cycle of 94%. The measured maximum allowable duty cycle of 92% is therefore less than that predicted. This is attributed to $\mathrm{R_{Cu}}$ being higher than that measured under dc conditions due to the skin effect.

Figs. 13 and 14 show oscillograms of the resetting behavior of the CT when used with SR (condition II) at duty cycles of 50% and 94%, respectively. At 94% duty cycle CT reset is taken as incomplete as the output signal is, again, 1% less than that ideally

expected. The response in this case is effectively oscillatory as shown in Fig. 5 due to the augmentation of C_{eq} by the inter-terminal capacitance of the SR MOSFET, in this case its common source output capacitance (C_{oss}). The rectangular approximation shown in Fig. 5 is therefore not appropriate. The oscillatory frequency is approximately 450 krads/s. Note the change of scale in the lower trace showing the voltage across CT1 from 5-V/div. to 2-V/div. From manufacturer's data C_{oss} is estimated at 500 pF for $V_{DS} \approx 0$ V. Combining this with the measured value of L_{m2} (13.1 mH), ω_r is calculated at 391 krads/s. There is therefore approximate agreement between the measured and expected values of ω_r. At power switch turn-off the voltage across CT1 undergoes a step change from its new $V_{forward}$ value of $\approx$0 V to ≈ -0.6 V. This is due to the SR MOSFET turning off before the power device due to the lower propagation delay in its drive path when compared to the power device. This causes the current through the SR MOSFET to pass momentarily through its intrinsic diode. After the first half-cycle has elapsed this diode again conducts for an interval due to the resonant voltage trying to change direction.

Referring to Fig. 13, it can be seen that the quarter-period of the reset waveform is approximately 3.5 μs. The switching frequency of 25 kHz used has a period of 40μs. A maximum duty cycle of 91% is therefore predicted. However, the measured duty cycle is higher at 94%. When SR is implemented the equivalent capacitance, C_{eq}, defining ω_r is now dominated by C_{oss}. This capacitance is nonlinear, falling with applied voltage. As the pulse width is increased more magnetizing current is switched into C_{eq} at power device turn-off leading to a higher voltage oscillation. This in turn leads to a higher frequency oscillation with a shorter quarter-period as C_{eq} has a lower effective value. For a given MOSFET, C_{oss} may be approximated as inversely proportional to $R_{DS(on)}$. Using a device with a higher $R_{DS(on)}$ with a consequently lower C_{oss} value may be preferred to allow operation at an enhanced duty cycle if the higher droop incurred is allowable. Similarly, the value of L_{m2} may be reduced to enhance the duty cycle at the expense of increased droop. With regard to the waveforms shown in Figs. 13 and 14, it can be seen that D2 and D3 are now effectively redundant. The reset voltage developed across the CT's output is readily supported by a signal-level MOSFET. In order to fully exploit the extended duty cycle attainable with SR, active resetting is required to maximize the voltage applied to the CT's secondary winding during its off-time thereby rendering (13) appropriate for predicting the CT's maximum duty cycle.

In the circuits described above, the outputs of both CTs are synchronously rectified. In a boost converter, if the choke current is continuous, then the duty cycle at which the switch operates is

$$\delta = 1 - V_I/V_O \tag{17}$$

where V_I and V_O are the input and output voltages, respectively. When the boost converter operates in a single phase PFC application V_I is given by $|V_p \sin \omega t|$, and therefore, varies between zero and V_p. V_O is usually set at approximately 10% more than the peak value, V_p, of V_I. From (17) it can be seen that δ should ideally vary between 100% and 9% as V_I changes. The duty cycle at which the diode conducts consequently varies between 0% and no more than 91%. With reference to Fig. 10, it is therefore concluded that, in a boost converter used for PFC, CT saturation may be avoided if only the power switch CT's secondary current is synchronously rectified and the power diode CT's secondary current is rectified in the normal way. The inverter gate (U2) and TR4 shown in Fig. 8 may therefore be dispensed with.

V. Conclusion

Techniques using CTs have been discussed for the sensing of both bidirectional and unidirectional pulse and choke currents in switched mode power converters. These techniques include the use of an active load and, in the case of unidirectional current pulse and choke current sensing, the introduction of synchronous rectification of the CTs' output signals in place of conventional passive diode rectification.

For a given CT, experimentation using the dual transformer technique for choke current sensing in a boost converter topology has shown that the distortion attributable to droop may be reduced by successively adding active output stages and SR. It has also been shown that CT operation may be extended closer to a duty cycle of 100%. A result of this is that restrictions other than CT reset may define the maximum duty cycle, for example, power device gate driver limitations, snubber circuit reset requirements and the need to provide "dead-times" elsewhere in the control circuitry.

When implementing SR, the MOSFET's common source output capacitance has to be taken into account as it lowers the resonant frequency of the CT and therefore increases the time which would otherwise be required for reset. If this capacitance is excessive in conjunction with respect to the CT's secondary magnetizing inductance, introducing SR in the place of passive rectification may have the adverse effect of reducing the CT's allowable duty cycle at high switching frequencies.

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