Zero-Voltage-Switching (ZVS) Two-Stage Approaches with Output Current Sharing for 48V Input DC-DC Converter

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Abstract – **Low-voltage on-board DC-DC converters are increasingly required to have high efficiency and fast transient response. In this paper, two-stage DC-DC converter architecture is proposed to achieve fast transient response while operating at high efficiencies, which feature soft switching, self-current-sharing capability and simplified self-driven techniques for the synchronous rectifiers.**

Keywords – Two-stage, zero-voltage switching, current sharing, half bridge, full bridge, synchronous rectifier, self-driven SR

I. INTRODUCTION

According to the Intel roadmap, microprocessors requiring 1V and 100~130A will be available in the market in the next two years [1]. This increase of load current and reduction of its voltage is also accompanied by an increased transient current slew rate at the processor power bus. Most of today's Voltage Regulator Modules (VRMs) draw power from the 12 V output of a silver box and use non-isolated buck converters as on-board VRMs to satisfy the load power requirements [1-4]. In this case, as the required output voltage becomes lower, higher voltage step-down ratio is required, resulting in small duty cycle, low efficiency and asymmetric transient responses.

With the increase of the required power level, the 12V input bus voltage may not be able to satisfy the requirements. Thus, 48V input-voltage isolated converters are potential candidates for the next generation of low-voltage converters and VRMs [4], especially for "servers" and "workstations" of computer systems. In the 48V input-voltage converters, isolation transformers are utilized to step down the input voltage. As a result, the duty cycle can be optimized and better converter efficiency is expected. Moreover, the 48V voltage bus reduces the distribution conduction losses and the required input capacitance becomes smaller.

With the stringent high-current, low-voltage and fast transient requirements of VRMs two-stage structure is a potential candidate approach for 48V input converters. The first stage provides an isolated intermediate voltage bus, and the second stage can be optimized to achieve faster transient response and better efficiency. Furthermore, the first stage is allowed to operate at lower frequency to keep higher overall efficiency, while the second stage is designed to operate as higher frequency to meet the transient requirements.

In two stage converters, the state-of-the-art 12V VRM techniques may be employed in the second stage converters. However, in the interleaved multi-channel buck converters, the switches operate at hard switching conditions. Thus, the switching losses increase with the increase of the switching frequency. In this paper, a two-stage soft-switching concept is proposed, which allows both the first stage and the second stage to operate at Zero-Voltage Switching (ZVS) condition.

Based on this concept, the half-bridge topology is employed as the first stage with the fixed 0.5 complementary duty cycles. Both switches operate at zero-voltage switching because of the small dead time between the two drive signals of switches. For the second stage, a non-isolated complementary half bridge and a Duty-Cycle-Shifted (DCS) [5] non-isolated ZVS half bridge are proposed to achieve soft switching for the second-stage switches. Therefore, all switches in both stages operate at soft switching. Moreover, the non-isolated DCS controlled converter has a novel current sharing capability under voltage-mode control, which is suited for low-voltage and high-current output converters. In addition, self-driven synchronous rectifiers are utilized for both stages to improve the rectification efficiency and simplify the driving circuits.

The next section describes the proposed topology with its main switching waveforms. Section III presents experimental results and the conclusion is given in Section IV.

II. PROPOSED TWO-STAGE APPROACHES FOR 48V DC-DC CONVERTERS

For 48V nominal input voltage DC-DC converters, the electrical isolation is generally required. In two-stage converter approaches, the isolation transformer may be used in the first stage or second stage. If the transformer is used in the second stage, the first stage topology may be Buck or Boost converter, and second stage may be full bridge, half bridge, forward or push pull. Wherein the first stage provides a regulated voltage bus for the second stage, and

the second stage steps down the voltage and provides electrical isolation. This configuration is suitable for wide input voltage range.

On the other hand, the isolation transformer can be placed in the first stage while the second stage is non-isolated. Such two-stage converter configuration is shown in Fig. 1, where the first stage provides step-down intermediate voltage bus and transformer isolation. If the input voltage is relatively fixed at 48V, there is no need to regulate the intermediate voltage, such that open-loop control can be used for the first stage. If the input voltage is variable, e.g. 42~52V, the non-isolated feed-forward loop control can be used to roughly regulate the intermediate bus voltage [8], which is simpler than feedback control. At this case, the first stage functions as a "DC transformer," and topologies such as full-bridge, half-bridge, forward and push-pull can be used. The second stage is designed to tightly regulate the output voltage and meet the transient requirements, where state-of-the-art 12V multi-channel VRMs or other non-isolated buck-derived converters may be employed. It should be noted that intermediate bus voltage should be optimized according to the value of output voltage and converter power level.

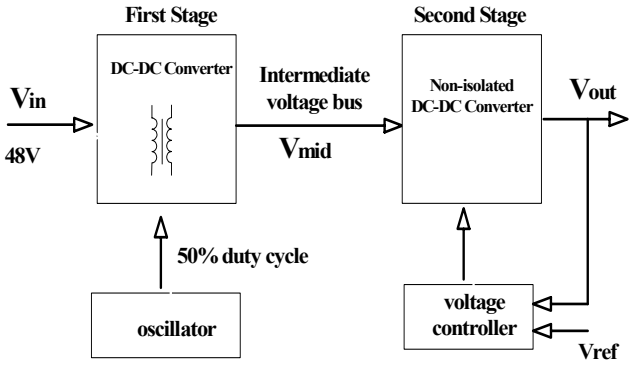


Fig.1: Two-Stage Approach for High Step-Down Fast Transient Converter

A. *First Stage – Open-Loop Controlled ZVS Half Bridge with Self-Driven Synchronous Rectifiers:*

In many cases, the converter input voltage is relatively fixed at 48V, thus the first stage may operate with open-loop control, offering a transformer isolation and step-down intermediate voltage bus. Thus an open-loop controlled 50 percent-duty-cycle half-bridge DC-DC converter, shown in Fig. 2, can be employed as first stage. The driving signals of switches S_1 and S_2 are complementarily generated with nearly 50 percent duty cycle. There are no asymmetric penalties since the duty cycle is always symmetric, which means the voltage and current stresses in the corresponding components are symmetric. Because of the small dead time and the transformer leakage inductance, ZVS can be achieved for both switches, and the leakage-inductance-related ringing is eliminated. Moreover, on the secondary, synchronous rectifiers can be easily driven via extra transformer windings with minimal body diodes losses, thanks to the 50 percent duty cycle. The key waveforms of the asymmetric half-bridge DC-DC converter are shown in the Fig. 3.

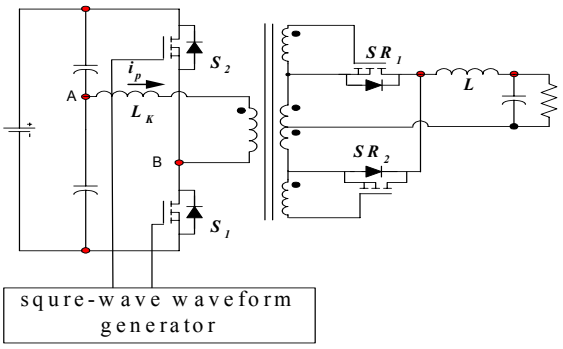


Fig. 2: Asymmetric HB ZVS DC-DC Converter

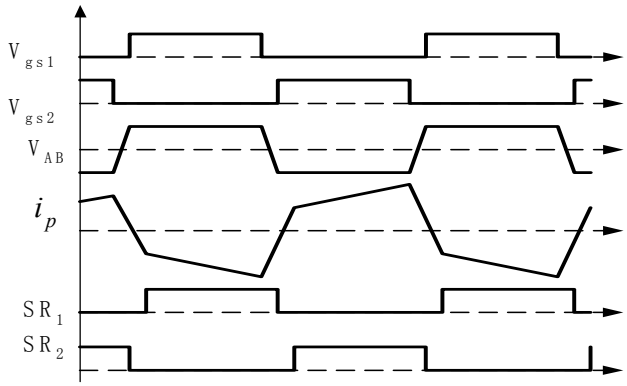


Fig. 3: Waveforms of Asymmetric HB DC-DC Converter

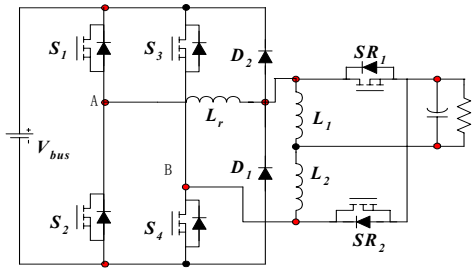
B. *Second Stage – A Family of Non-Isolated ZVS DC-DC Converters:*

State-of-the-art 12V multi-channel VRMs can be directly employed in the second stage. However, all switches in the VRMs operate at hard-switching conditions, and the small duty cycle results in higher switching and conduction losses. In this section, a family of non-isolated ZVS topologies is proposed for the second stage to reduce the switching losses, where the main difference from conventional topologies is that the isolation transformers are removed and the circuitry is simplified. A non-isolated full bridge DC-DC converter is shown in Fig. 4(a), where the full bridge is controlled with the phase-shift scheme to achieve ZVS for all switches. The duty cycle D (0<D<0.5) may operate at nearly 50 percent to reduce circulating losses since the intermediate voltage is fixed. The output voltage can be expressed as:

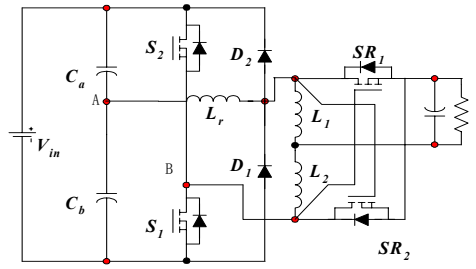
$$V_{out} = V_{bus} D \quad (0<D<0.5) \qquad (1)$$

Where V_{bus} is the intermediate bus voltage that depends on the required output voltage, and D is effective duty cycle. For example, if the required output voltage is 3.3V, for a duty cycle of 0.4 in the steady state, the intermediate voltage bus can be selected as 8.25V.

Inductor Lr is added as a resonant inductance to discharge switches junction capacitance to achieve ZVS. In addition, Lr is used to limit di/dt to reduce reverse-recovery peak current through the secondary-side body diodes. In addition, schottky diodes D_1 and D_2 as shown in Fig. 4 are used to clamp the voltage spikes of SRs, such that the SRs voltage stresses are significantly reduced and FETs with lower voltage rating can be used as SRs to reduce the conduction losses.



(a) Non-Isolated Full Bridge DC-DC Converter



(b) Non-Isolated Half-Bridge DC-DC Converter

Fig. 4: A Family of Non-Isolated ZVS DC-DC Converters

Another non-isolated topology shown in Fig. 4(b) is the asymmetric ZVS half-bridge with a current doubler rectifier. Lr, D1 and D2 in the converter have the same function as in the full-bridge DC-DC converter shown in Fig. 4(a). In fact, a current doubler rectifier is a kind of two-channel buck converter, and thus it has advantages of interleaved buck converters, such as current ripple cancellation and good transient response. With asymmetric control, the topology of Fig. 4(b) has two major advantages over a conventional two-channel interleaved buck converter: (1) ZVS can be achieved and (2) self-driven synchronous rectifiers can be used to simplify the SR drive circuitry and reduce cost.

The output voltage is expressed as:

$$V_{out} = V_{bus} D(1-D) \qquad (0<D<0.5) \qquad (2)$$

It is noted that half bridge DC-DC converter has higher step-down ratio compared to the full bridge. Thus, it has lower output voltage at the same input voltage bus. Half bridge DC-DC converter is suited for low-voltage high-current application because of less transformer primary turns, since secondary winding is generally one turn for low voltage output.

Taking into account the duty cycle losses, one may assume that the secondary-side maximum available duty cycle is 0.45. At 9V intermediate bus voltage, the output voltage is around 2V. Since higher intermediate bus voltage may reduce the conduction losses, a non-isolated coupled-current-doubler topology can be introduced to achieve higher intermediate bus voltage [7].

However, the asymmetric non-isolated half bridge has uneven current and voltage stresses distributed in the corresponding components. The reverse voltage stresses across two synchronous rectifiers (SRs) are expressed as:

$$V_{SR1} = V_{in}(1-D_1) \qquad (0<D<0.5) \qquad (3)$$

$$V_{SR2} = V_{in} D_1 \qquad (0<D<0.5) \qquad (4)$$

The rms currents through the two synchronous rectifiers (SRs) are expressed as:

$$I_{SR1} = I_o \sqrt{1-D_1} \qquad (0<D<0.5) \qquad (5)$$

$$I_{SR2} = I_o \sqrt{D_1} \qquad (0<D<0.5) \qquad (6)$$

From equations (3)~(6), it can be noticed that the higher voltage rating SR carries higher rms current, which leads to asymmetric thermal distribution and thus degrades the rectification efficiency and reliability. Moreover, the current stresses on primary-side switch S_1 and S_2 are uneven.

C. *Second Stage – Non-Isolated Duty-Cycle-Shifted ZVS Half-Bridge DC-DC Converters:*

As discussed above, non-isolated asymmetric half bridge can achieve ZVS for both switches. However, when the duty cycle goes asymmetric, voltage stresses and current stresses are unevenly distributed. Besides, the converter transient response depends on capacitance of the capacitors C_a and C_b.

A Duty-Cycle-Shifted (DCS) ZVS half-bridge DC-DC converter was proposed [5]. As a second-stage candidate topology, the non-isolated DCS ZVS half-bridge DC-DC converter is proposed as shown in Fig. 5, with its corresponding key waveforms shown in the Fig. 6. In order to charge/discharge the junction capacitance, a resonant inductor Lr is added to achieve ZVS.

It should be noted that the drive signal of switch S_2 is shifted left and be close to the falling edge of drive signal of switch S_1, such that switch S_2 can be turned on at ZVS. During the on-time period of switch S_2, switch S_3 is turned on at Zero-Current Switching (ZCS). Thus, the energy in the resonant inductor Lr will be trapped through D_3 and S_3 when switch S_2 turns off. Before switch S_1 is turned on, switch S_3 is turned off to release the energy to discharge junction capacitance and create a ZVS condition for switch S_1. Therefore, all switches in the converter operate at soft-switching conditions. In addition, the asymmetric penalties of asymmetric control HB converter are eliminated thanks to

the equal duty cycle applied to the two primary-side main switches.

An interesting feature of the non-isolated DCS controlled half-bridge converter is that it has self current-sharing capability, i.e. even if the inductors DCR and SRs on-resistance values are asymmetric, the average currents in the two inductors and SRs always stay identical. Therefore, no current sharing control is needed, even under voltage mode control. As matter of fact, this current-balance feature can be verified by use of an average state-space concept [9]. By solving the averaged state-space equation, the average currents through the two inductors are:

$$I_{L1} = \frac{d_2}{d_1 + d_2} I_o \qquad (7)$$

$$I_{L2} = \frac{d_1}{d_1 + d_2} I_o \qquad (8)$$

Where d_1 and d_2 are applied duty cycles of switch S_1 and S_2, respectively. Note that the inductors ESR and SRs resistance have no impact on the inductor currents. Since the duty cycles are symmetrically applied to switches, d1 should be equal to d_2, and currents in inductors are always equal despite asymmetric inductor DCR and SRs on-resistance values. In fact, self-current-sharing is an attractive advantage especially for high-current low-voltage applications. Moreover, because the steady-state duty cycle is designed close to 50 percent, S_3 and D_3 have a very small portion of period to carry current and the conduction losses on that branch are very small.

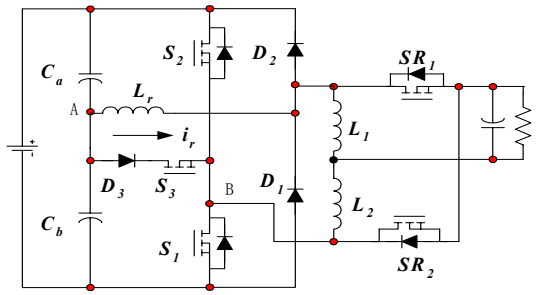


Fig. 5: Non-Isolated DCS Topology

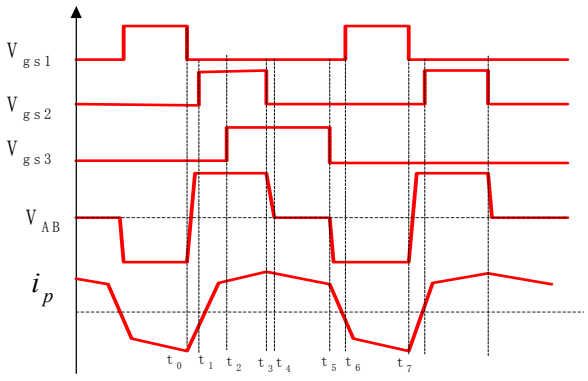
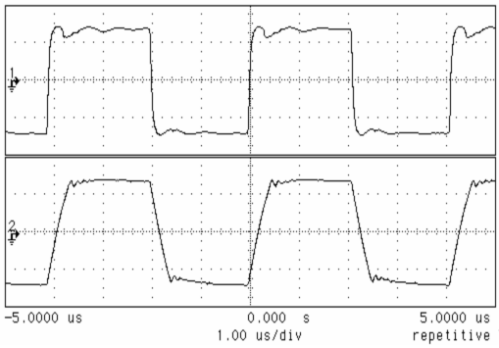


Fig. 6: Key Waveforms

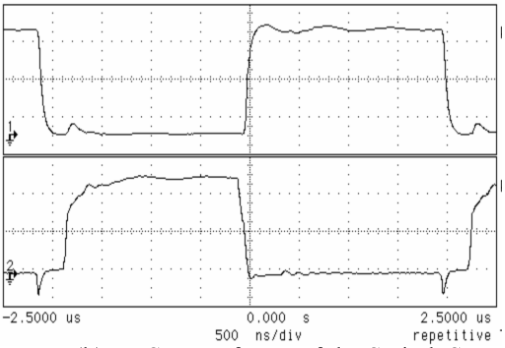
Because the duty cycle is closed to 0.5, good current ripple cancellation can be achieved and the output voltage ripple can be very small. Bulky capacitor may be removed if the converter has sufficiently high bandwidth.

III. EXPERIMENTAL RESULTS

A prototype with the topology shown in Fig. 2 and with 48V input voltage and 10V/10A output was built in the laboratory for experimental verification. 50 percent fixed-duty-cycle signals are applied to the two main switches. Fig. 7 (a) shows the transformer primary voltage and current waveforms. It can be observed that the current waveform is very clean. ZVS turn-on behavior of switch S_1 is clearly shown in Fig. 7 (b).



(a) Transformer primary-side voltage and Current (top trace: 20V/div; bottom trace: 5A/div)

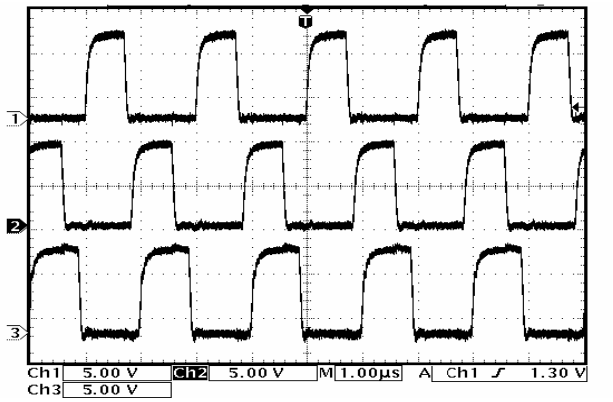


(b) ZVS Waveforms of the Switch S_1 (top trace Vds 20V/div; bottom trace Vgs: 5v/div)

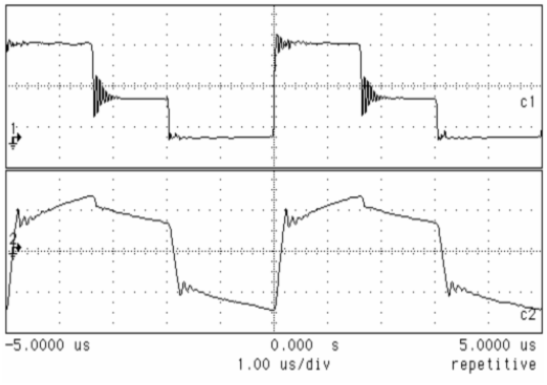
Fig. 7: Experimental Results of the First-Stage Converter

The second-stage converter shown in Fig. 5 is separately built with 10V input and 1.8V/30A output. Fig. 8 shows corresponding experimental results. Fig. 8(a) shows the gate signals of switches S_1, S_2 and S_3, while Fig 8(b) shows waveforms of S_1 drain-to-source voltage and current through resonant inductor Lr. Fig. 8(c) shows the ZVS waveforms of switch S_1. Note that ZVS range of switch S_2 is wider than S_1, because the energy in the output inductor current can be utilized to achieve ZVS for switch S_2 while

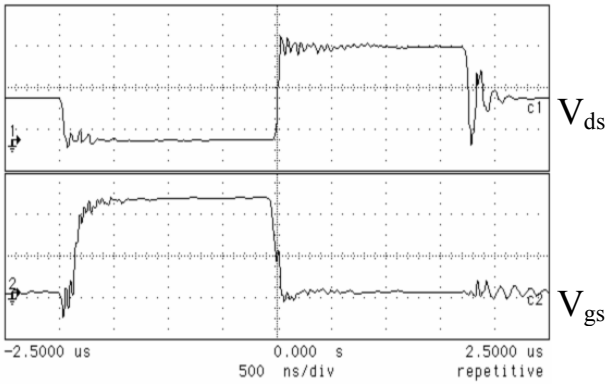
energy in the resonant inductor Lr is utilized for ZVS of switch S_1.



(a) Gate Signals
(from top to bottom $S_1 \sim S_3$: 5V/div)



(b) Vds1 Voltage and Inductor Lr Current i_r



(c) S_1 ZVS Waveforms

Fig. 8: Experimental Results of the Non-Isolated DCS ZVS HB DC-DC Converters

IV. CONCLUSION

A two-stage approach for 48V DC-DC conversion was proposed in the paper, where an open-loop-controlled ZVS isolated half-bridge DC-DC converter is used as the first stage, and a non-isolated DCS-controlled ZVS HB DC-DC converter and a non-isolated asymmetric ZVS HB DC-DC converter are proposed for the second stage. In this two-stage scheme, both stages operate at ZVS conditions, which provide a potential to allow converters to operate at higher switching frequencies to meet the high-density and fast-transient requirements. Initial experimental results verified the two-stage DC-DC converter concept.

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