

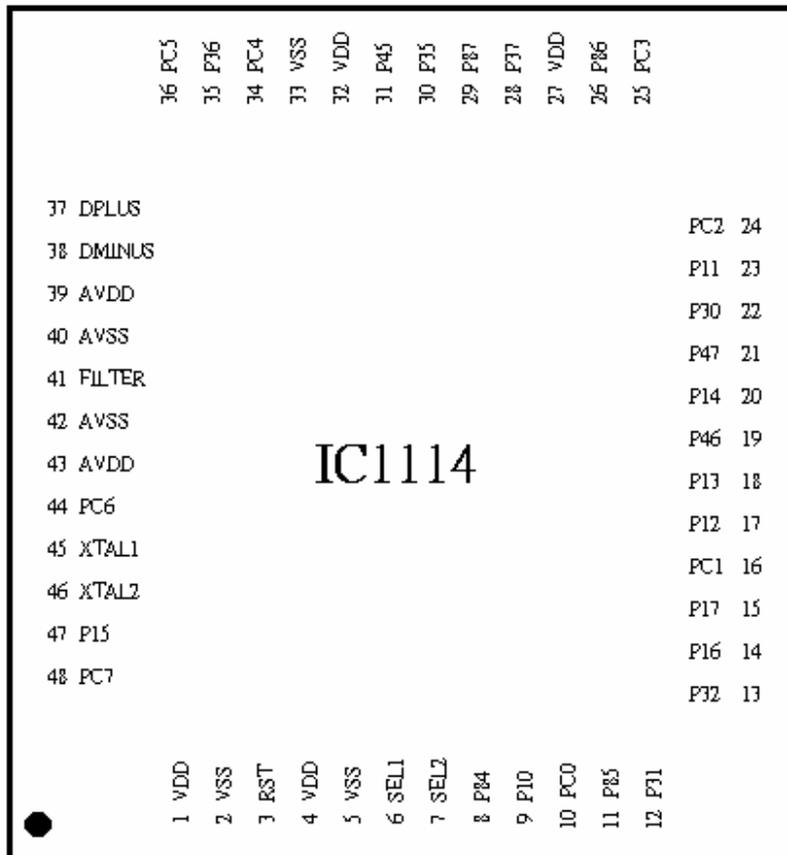


1. FEATURES

- High speed 8-bit micro-controller with 4 system clocks per machine cycle
- Instruction-set compatible with MCS-51
- Embedded 32K-byte program FLASH ROM for product quick delivery. In System Programming, ISP is supported by either USB or I2C port.
- Built in fixed address 256 bytes data RAM.
- Built in floating address 4608 bytes data RAM
- Extra 1K bytes CPU data RAM space available by disable central control block function.
- System power saving mode ready, idle & power down modes.
- Three programmable 16-bit timer/counter and watchdog timer.
- Compliant with USB Specification Rev.1.1 supports full speed (12Mbits/sec), one device address and four endpoints. (Including control, interrupt, bulk in and bulk out endpoints)
- Built in ICSI in-house bi-directional parallel port for quick data transfer. Both master and slave modes are supported.
- Master/Slave IIC and UART/RS-232 interface for external device communication.
- Smart Media Card/NAND type flash chip interface complies with Smart Media Specification Rev.1.1 and Smart Media Identify Number Specification Version 1.1
- Built-in hardware ECC (Error Correction Code) check for Smart Media Card/NAND type flash chip.
- 3.0~3.6V supply.
- 48LQFP packages is available.



2. PIN INFORMATION



2.1.1. PIN FUNCTION DESCRIPTION

Function	Signal Name	IO	Pin Number	Description
Parallel Port	PP_D0	IO_TR	10	Parallel port data bus bit 0. Share with PC0
	PP_D1	IO_TR	16	Parallel port data bus bit 1. Share with PC1
	PP_D2	IO_TR	24	Parallel port data bus bit 2. Share with PC2
	PP_D3	IO_TR	25	Parallel port data bus bit 3. Share with PC3
	PP_D4	IO_TR	34	Parallel port data bus bit 4. Share with PC4
	PP_D5	IO_TR	36	Parallel port data bus bit 5. Share with PC5
	PP_D6	IO_TR	44	Parallel port data bus bit 6. Share with PC6
	PP_D7	IO_TR	48	Parallel port data bus bit 7. Share with PC7
	PP_RW	IO_PU	12	Parallel port read/write trigger, active high. Share with P31
	PP_RDY	IO_PU	22	Parallel port READY signal, active high. Share with P30
	PP_EN	IO_TR	30	Parallel port enable, active high. Share with P35

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Function	Signal Name	IO	Pin Number	Description
	PP_DIR	IO_PU	31	Parallel port direction control. Share with P45
SM Card	SM_D0	IO_TR	10	SM card data bus bit 0. Share with PC0
	SM_D1	IO_TR	16	SM card data bus bit 1. Share with PC1
	SM_D2	IO_TR	24	SM card data bus bit 2. Share with PC2
	SM_D3	IO_TR	25	SM card data bus bit 3. Share with PC3
	SM_D4	IO_TR	34	SM card data bus bit 4. Share with PC4
	SM_D5	IO_TR	36	SM card data bus bit 5. Share with PC5
	SM_D6	IO_TR	44	SM card data bus bit 6. Share with PC6
	SM_D7	IO_TR	48	SM card data bus bit 7. Share with PC7
	SM_CD1	IO_PU	8	Card detect pin, active low. Share with P84
	SM_CLE	IO_PU	31	Command latch enable, active high. Share with P45
	SM_RNB	IO_PU	19	Ready/Busy. Share with P46
	SM_ALE	IO_PU	21	Address latch enable, active high. Share with P47
	SM_RD	IO_TR	11	Read enable, active low. Share with P85
	SM_WR	IO_TR	26	Write enable, active low. Share with P86
	SM_WP	IO_TR	29	Write protect, active low. Share with P87
Master/Slave IIC	IIC_CL	IO_PU	12	IIC clock. Share with P31
	IIC_DA	IO_PU	22	IIC data. Share with P30
UART	TXD	IO_PU	12	Serial output. Share with P31
	RXD	IO_PU	22	Serial input. Share with P30
Timer/counter	T1	IO_TR	30	External pin for timer 1. Share with P35
	T2	IO_TR	9	External counter clock input for timer 2. Share with P10
	T2EX	IO_TR	23	External counter enable for timer 2. Share with P11
EXT interrupt	INT0	IO_PU	13	External interrupt 0. Share with P32
	P10	IO_TR	9	Port 1 bit 0.
	P11	IO_TR	23	Port 1 bit 1.
	P12	IO_TR	17	Port 1 bit 2.
	P13	IO_TR	18	Port 1 bit 3.
	P14	IO_TR	20	Port 1 bit 4.
	P15	IO_TR	47	Port 1 bit 5.
	P16	IO_TR	14	Port 1 bit 6.
	P17	IO_TR	15	Port 1 bit 7.
	P30	IO_PU	22	Port 3 bit 0.
	P31	IO_PU	12	Port 3 bit 1.
	P32	IO_PU	13	Port 3 bit 2.
	P35	IO_PU	30	Port 3 bit 5.
	P36	IO_PU	35	Port 3 bit 6.
	P37	IO_PU	28	Port 3 bit 7.
	P45	IO_PU	31	Port 4 bit 5.
	P46	IO_PU	19	Port 4 bit 6.
	P47	IO_PU	21	Port 4 bit 7.
	P84	IO_PU	8	Port 8 bit 4.
	P85	IO_TR	11	Port 8 bit 5.
	P86	IO_TR	26	Port 8 bit 6.
	P87	IO_TR	29	Port 8 bit 7.
	PC0	IO_TR	9	Port C bit 0.
	PC1	IO_TR	23	Port C bit 1.

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Function	Signal Name	IO	Pin Number	Description
	PC2	IO_TR	17	Port C bit 2.
	PC3	IO_TR	18	Port C bit 3.
	PC4	IO_TR	20	Port C bit 4.
	PC5	IO_TR	47	Port C bit 5.
	PC6	IO_TR	14	Port C bit 6.
	PC7	IO_TR	15	Port C bit 7.
PLL	FILTER	O	41	External loop filter pin, a capacitor is connected between this pin and analog ground
USB	DPLUS	IO	37	USB DPLUS pin
	DMINUS	IO	38	USB DMINUS pin
XTAL	XTAL1	I	45	XTAL oscillator input pin
	XTAL2	O	46	XTAL oscillator output pin
Power	AVDD	P	39/43	Analog 3.3V
	AVSS	P	40/42	Analog ground
Power	VSS	P	2/5/33	Digital ground pin
	VDD	P	1/4/27/32	Digital 3.3V
	RST	I	3	System reset pin, Shmmit trigger
SELCLK	SEL1	I	6	CPU clock select pin 1
	SEL2	I	7	CPU clock select pin 2

Note :

- After reset, all extra function is disabling. When extra function enable, that I/O is in input or output mode is dependent on pin function.
- Ports are GPIO and input after reset, and still a GPIO if the extra function does not turn on by software. The initial state of GPIO is High, LOW, or TRI-STATE, which is dependent on I/O cell as IO_PU, IO_PD or IO_TR.
- SEL [2:1]=00, 01, or 10 CPU clock is 12Mhz, 24Mhz or 48Mhz. SEL [2:1]=11 is reserved.
- Connect 1.2 Mohm between XTAL1 and XTAL2.
- Connect 820 pF between FILTER and VSS.



3. FUNCTION DESCRIPTION

IC1114 includes a turbo 80T32 CPU core, 32K-byte internal program Flash-ROM, 5.5-bytes SRAM and many interface blocks. Including USB function, SM flash card interface, UART, NAND type flash chip interface, I2C master & slave blocks and high speed parallel port master & slave interface.

If turning on extra function, the data can be shared through central control block as Figure 1. Data can be transferred very effective and result a best performance in card reader and other application.

The IC1114 embedded full speed USB port as major bridges to talk to other host. IC1114 also provides both master and slave parallel port, UART port and I2C port for any extended function usage. For those early development or code always changing environment, IC1114 provides a flexible solution with embedded 32K bytes program Flash-ROM. User can update her/his ROM code by our built in ISP function. IC1114’s ISP function gives customer three different choices to take, via USB and I2C.

IC1114 can support CPU data memory space up to 5.5K bytes by turning off central control block. For that huge data RAM consumed application, this extra space can still be accessed by executing “MOVX” command.

For those more I/O ports required applications, IC1114 can provide up to 29 general I/O pins.

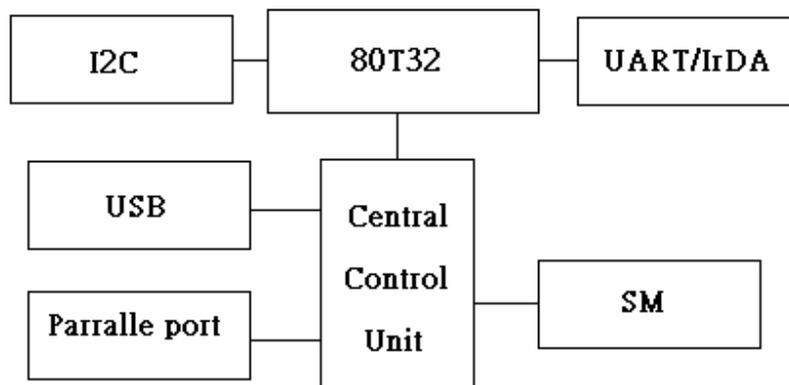


Figure 1. System block diagram



4. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Operating temperature under bias	0 to +70	°C
Storage temperature range	-65 to +125	°C
Voltage on I/O port	5.5	V
Voltage on any other pin to VSS	3.8	V

Stressing the device beyond the "Absolute Maximum Rating" may cause permanent damage. This is stress rating only. Operation beyond the "operating conditions" is not recommended and extended exposure beyond the "operating conditions" may affect device reliability.

OPERATING RANGES

Commercial devices case temperature	0 to +70 °C
VCC supply voltage	+3.0 to 3.6V
Input capacitor	5 pF
Input Voltage of I/O port	V _{SS} -0.3, 5.5V
Input Voltage of other pin	V _{SS} -0.3, V _{DD} +0.3
Oscillator frequency	12 MHz

Minimum D.C. input voltage is -0.5 V. During transitions, inputs may undershoot ,to -2.0 V for periods less than 20 ns. Maximum D.C. voltage on output pins is VCC+0.5 V, which may overshoot to VCC + 2.0 V for periods less than 20 ns.

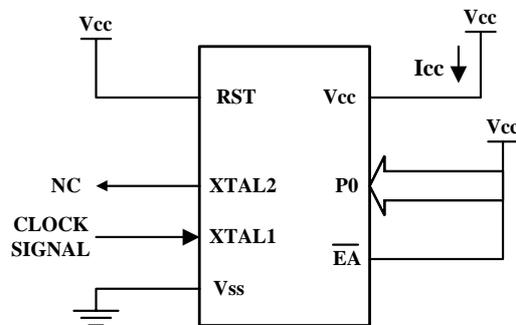


5. DC ELECTRICAL CHARACTERISTICS

($V_{DD}-V_{SS}= 3.6V$ to $3.0V$)

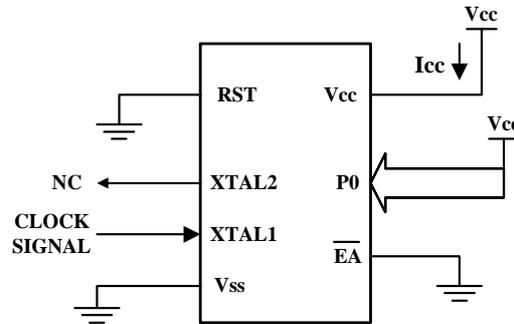
Symbol	Parameter	Min	Max	Unit	Test conditions
Vil	Input low voltage of GPIO	-0.5	0.8	V	
Vih	Input high voltage of GPIO	2.0	5.5	V	Vcc=3.0V
Vil1	Input low voltage (XTAL1)	-0.5	0.2Vcc - 0.3	V	
Vih1	Input high voltage (XTAL1)	0.7Vcc	Vcc+0.5	V	
Vsch+	RST positive Schmidt-trigger threshold voltage	2.0	Vcc+0.5	V	
Vsch-	RST negative Schmidt-trigger threshold voltage	0	0.8	V	
Vol	Output low voltage of USB		0.4	V	Iol=4.0mA, Vcc=3.0V
Voh	Output high voltage of USB	2.4		V	Ioh=4.0mA, Vcc=3.0V
Vol	Output low voltage of I/O port, RST	-	0.4	V	Iol=4.0mA, Vcc=3.0V
Voh	Output high voltage of I/O port, RST	2.4	-	V	Ioh=4.0mA Vcc=3.0V
Ili	Input leakage current	-10	+10	uA	Vin=0V or 3.6V
Ru	IO_PU pull up resister	50K	150K	ohm	
Icc active mode	12 MHz 24 MHz 48 MHz		20 30 40	mA mA mA	Vcc=3.6V, no load
Icci idle mode	12 MHz 24 MHz 48 MHz		3 4 4	mA mA mA	Vcc=3.6V, no load
Ipd	Current in power down mode		500	uA	Vcc=3.6V
Vdr	Minimum voltage to keep RAM data	2		V	

– Active mode

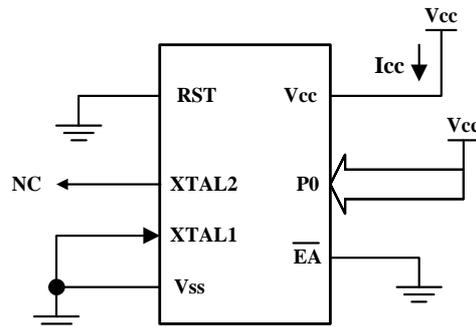




- Idle mode



- Power down mode ($V_{cc} = 2.0V$ to V_{cc})

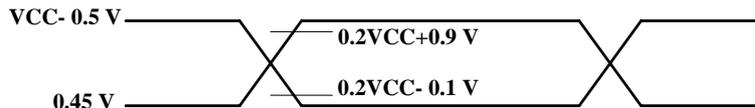




6. AC SPECIFICATION

CL=100 pF on all GPIO pins

6.1 A.C. TEST POINTS



A.C. inputs during testing are driven at VCC-0.5 for logic "1" and 0.45V for logic "0". Timing measurements are made at Vih min for logic "1" and max for a logic "0".

6.2 SERIAL PORT MODE 0 TIMING CHARACTERISTIC

PARAMETER	SYMBOL	MIN	MAX	UNITS
Serial Port Clock Cycle Time SM2=0 -> 12 clocks per cycle SM2=1 -> 4 clocks per cycle	t_{XLXL}	$12t_{CLCL}-10$ $4t_{CLCL}-10$	$12t_{CLCL}+10$ $4t_{CLCL}+10$	ns
Output Data Setup to Clock Rising Edge SM2=0 -> 12 clocks per cycle SM2=1 -> 4 clocks per cycle	t_{QVXH}	$10t_{CLCL}-10$ $3t_{CLCL}-10$	- -	ns
Output Data Hold to Clock Rising Edge SM2=0 -> 12 clocks per cycle SM2=1 -> 4 clocks per cycle	t_{XHGX}	$2t_{CLCL}-10$ $t_{CLCL}-10$	- -	ns
Input Data Hold after Clock Rising Edge SM2=0 -> 12 clocks per cycle SM2=1 -> 4 clocks per cycle	t_{XHDX}	t_{CLCL} t_{CLCL}	- -	ns
Clock Ring Edge to Input Data Valid SM2=0 -> 12 clocks per cycle SM2=1 -> 4 clocks per cycle	t_{XHDV}	- -	$11t_{CLCL}$ $3t_{CLCL}$	ns

6.3 CARD INTERFACE CHARACTERISTIC

PARAMETER	SYMBOL	MIN	MAX	UNITS
PP port Data input setup time	tDI _s		5	ns
PP port Data input hold time	tDI _h		5	ns
PP port Data output setup time	tD _s	20		ns
PP port Data output hold time	tD _h	20		ns
PP port DIR setup time	tDIR _s	20		ns
PP port DIR hold time	tDIR _h	20		ns
SM card Data input setup time	tDI _s		10	ns
SM card Data input hold time	tDI _h	0	-	ns
SM card Data output setup time	tD _s	100		ns



SM card Data output hold time	tDh	20		ns
SM card command setup time	tCMDs	100		ns
SM card command hold time	tCMDh	20		ns

6.4 EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Clock High Time	t _{CHCX}	8	-	-	ns
Clock Low Time	t _{CLCX}	8	-	-	ns
Clock Rise Time	t _{CLCH}	-	-	5	ns
Clock Fall Time	t _{CHCL}	-	-	5	ns

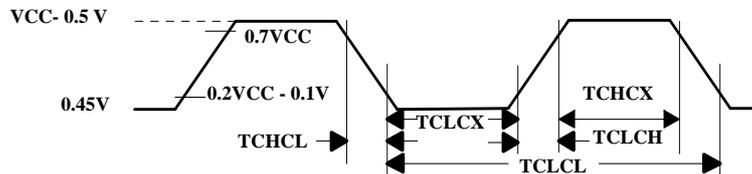


Figure 2. External clock drive waveform



7. TIMING DIAGRAM

7.1 SERIAL PORT MODE 0 TIMING

Serial Port (Synchronous Mode)

High Speed Operation SM2=1 => TxD Clock = XTAL/4

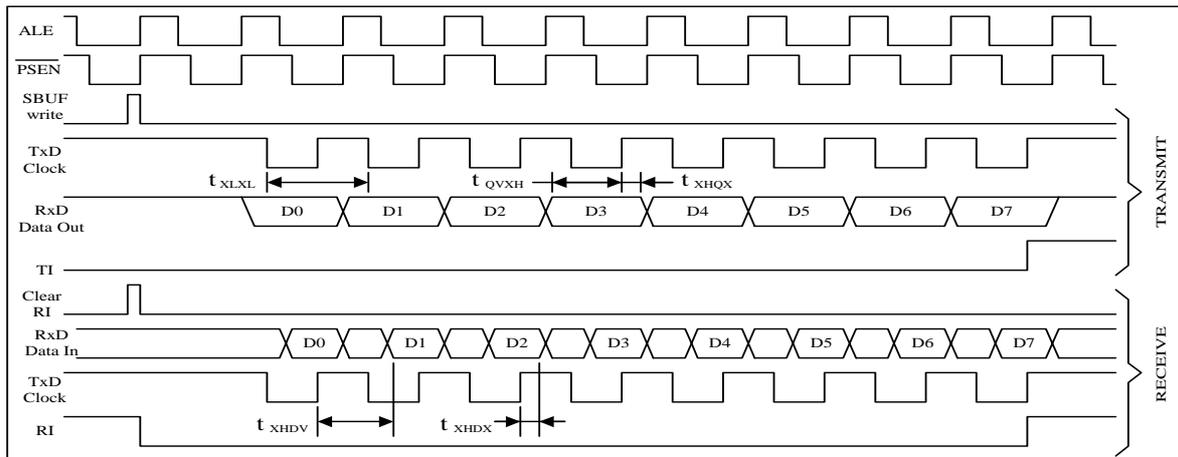


Figure 3. Serial port mode 0 timing at high speed operation

Serial Port (Synchronous Mode)

Standard Operation SM2=1 => TxD Clock = XTAL/12

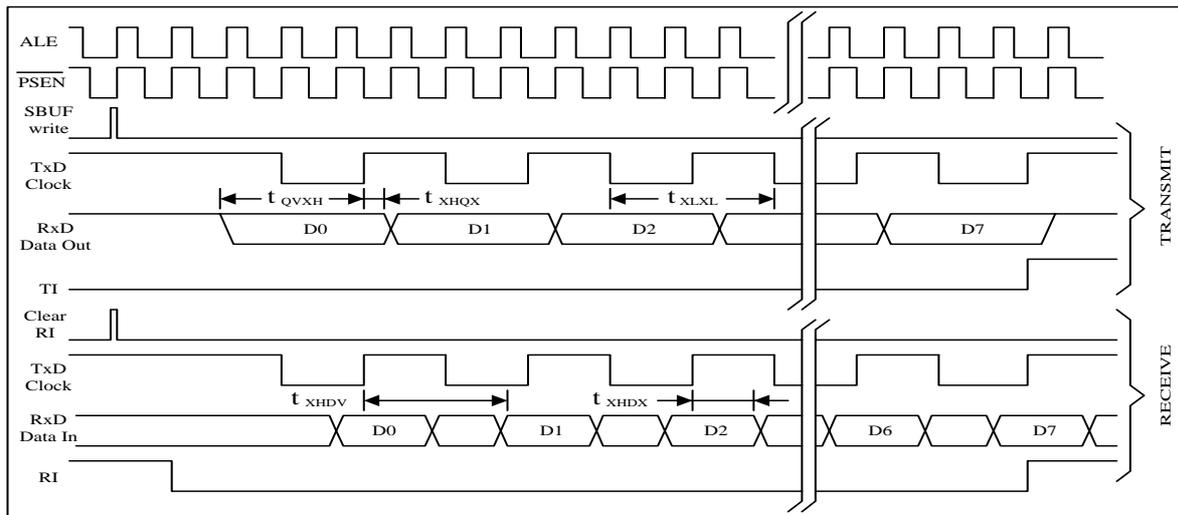


Figure 4. Serial port mode 0 timing at standard operation



7.2 CARD INTERFACE TIMING

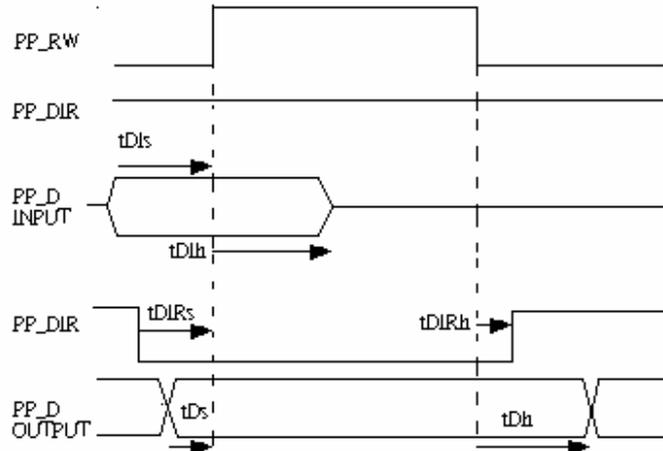


Figure 5 Parallel port read/write timing

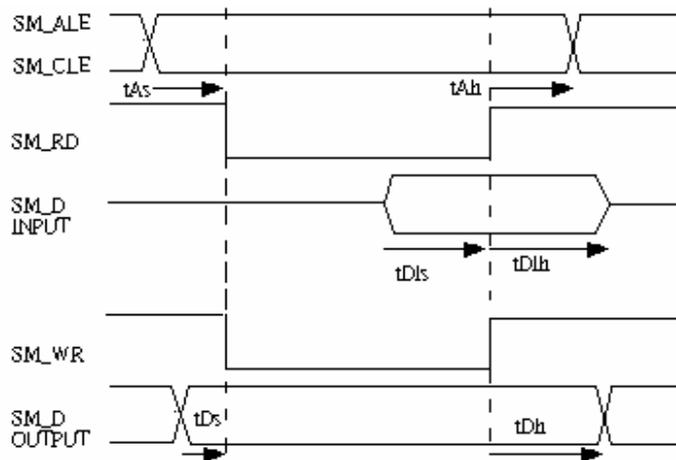


Figure 6 SM card read/write timing

IC1114-F48LQ



ORDERING INFORMATION

COMMERCIAL TEMPERATURE : 0 °C to +70 °C

Order Part Number	Package
IC1114-F48LQ	7*7*1.4mm LQFP



Integrated Circuit Solution Inc.

HEADQUARTER:
NO.2, TECHNOLOGY RD. V, SCIENCE-BASED INDUSTRIAL PARK,
HSIN-CHU, TAIWAN, R.O.C.
TEL: 886-3-5780333
FAX: 886-3-5783000

BRANCH OFFICE:
7F, NO. 106, SEC. 1, HSIN-TAI 5TH ROAD
HSICHIH TAIPEI COUNTY, TAIWAN, R.O.C.
TEL: 886-2-26962140
FAX: 886-2-26962252
<http://www.icsi.com.tw>