Coupled Inductor Improves Cross Regulation in Multiple **Output Forward Converters**

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ultiple output power converters suffer from cross regulation issues. This problem is present in ATX desktop power supplies where multiple output voltages of 5, 3.3, 12, -12, and -5 Vdc are required. Although all these outputs reference the same ground, cross regulation suffers from the fact that feedback control often references one output via an optocoupler for isolation. When a large load swing occurs on an output other than the sensed output, poor regulation can result. The coupled inductor is employed as a method of feeding back load swing information to the sensed winding to provide better regulation. The method for designing a coupled inductor for an ATX power supply can be applied to any multiple output forward converter.

Basic Multiple Output Forward Converter

The basic, multiple output, forward converter for today's ATX computer supply is shown in Figure 1. Note that only one output, the 5Vdc output is sensed. When using separate inductors for each output, poor regulation results in other outputs. Poor regulation will be greatest in outputs with large load swings, especially the 3.3Vdc output that sees load currents of up to 10A at a slew rate of 30% of rated current at 2.5A/µsec^[2]. The ATX must maintain a voltage above the minimum allowable 3.14Vdc during load swing situations. With separate

the transformer and inductor, the 5Vdc output would not see as much of a voltage reduction nor would it see it as quickly as the 3.3Vdc output would. Therefore it is likely that the 3.3Vdc output would fall out of regulation unless a feedback method is introduced. The purpose of coupled inductors is to relay current loading information directly through the inductor as shown The coupled inductor basic transformer

inductors in a standard multiple output design, the feed-

back would have to transmit from the 3.3Vdc output

through the 3.3V inductor, to the 3.3V secondary and couple to the 5V secondary through the 5Vdc inductor and

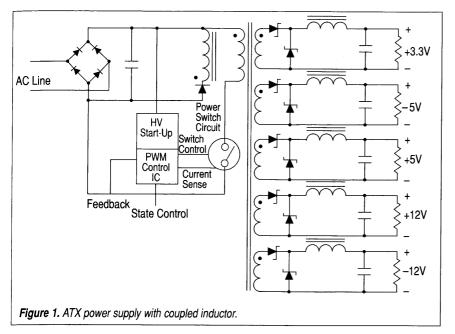
finally the feedback loop in order for the converter to

respond. By forcing the information to propagate through

design procedure involves reflection analysis using turns ratios to reflect the loads to the sensed 5Vdc output. The resulting loads are normalized to the 5Vdc output in order to calculate relative parameters, such as desired ripple current and leakage inductance values.

in Figure 1. The information is again relayed through magnetic coupling but not through the transformer like before, but through the inductor itself. Changes in load current will feedback to the 5V winding much faster and therefore the system will react quicker. Other benefits of the coupled inductor design are:

- One magnetic element for the coupled windings rather than one inductor per winding
- Reduced board space
- Confined areas of EMI generation
- Smaller output capacitors (if ripple currents are effectively steered)
- · Reduced cost. For all the coupled inductor design



benefits, there are some disadvantages. These include:

- Leakage inductance and its relation to ripple currents
- More difficult winding
- Confining the heat to one element rather than spreading it to several

inductors

Somewhat difficult design calculations

Coupled Inductor Design Basics

Before beginning design, it's best

to provide some basic rules. Further information can be found in^[1]. These are the basic rules of design that must be remembered with coupled inductors:

- The turns ratio of the inductor must match exactly the turns ratio of the transformer secondaries. This is the ratio between the output windings for the various outputs, not the ratio of the output winding to the primary.
- 2. It is best to steer the ripple current to the highest voltage winding as this winding usually has the largest allowable variation in output voltage. Therefore, the high voltage winding should have the lowest leakage inductance and be the closest winding to the inductor core.
- 3. For best results, reflect all of the windings to the feedback winding. With these rules in mind, one should revisit transformer theory prior to beginning the design. For this

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example we will refer to the feedback or main winding with a subscript of M and the subordinate winding with a subscript of R. Equations reference *Figure 2*.

The basic transformer voltage equation is:

$$\frac{V_{M}}{N_{M}} = \frac{V_{R}}{N_{R}} \tag{1}$$

From this we can calculate the voltage reflected to main winding M:

$$V_{\rm M} = \frac{V_{\rm R}}{N_{\rm R}} \times N_{\rm M} \tag{2}$$

Similarly, from the basic transformer current equation:

$$I_{M} \times N_{M} = I_{R} \times N_{R} \tag{3}$$

We can calculate the current reflected to main winding, M:

$$I_{M} = \frac{I_{R} \times N_{R}}{N_{M}} \tag{4}$$

These equations will be helpful in calculating voltage and current. How-

ever, to calculate inductors, capacitors, and resistances, use the impedance relationship. Impedance viewed from the main winding M is:

$$Z_{\rm M} = \frac{V_{\rm M}}{I_{\rm M}} \tag{5}$$

By substituting the reflected voltage and current equations developed earlier, the reflected impedance can be found to be:

be found to be:
$$Z'_{R} = \frac{V_{M}}{I_{M}} = \frac{\frac{V_{R}}{N_{R}} \times N_{M}}{\frac{I_{R} \times N_{R}}{N_{M}}}$$
 (6)

$$= \frac{V_R}{I_R} \times \left(\frac{N_M}{N_R}\right)^2 = Z_R \times \left(\frac{N_M}{N_R}\right)^2 = Z'_R$$

Often, the exact turns of the transformer are not known until the transformer is designed. However, the actual design can proceed if the turns ratio is substituted where the turns ratio, TR, is:

$$TR = \frac{N_{\rm M}}{N_{\rm R}} \tag{7}$$

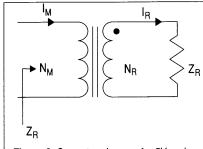


Figure 2. Current and power for 5V and 3.3V outputs.

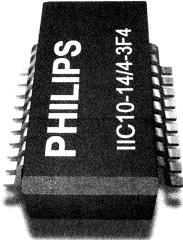
Transformer theory provides the following rules:

- 1. The voltage reflected to the main winding, M, is the voltage from the reflected winding, R, multiplied by the turns ratio TR. (Voltage is multiplied by TR.)
- 2. The current reflected to the main winding, M, is the current from the reflected winding, R, divided by the turns ratio, TR. (Current is divided by TR.)
- 3. The impedance reflected to the main winding, M, is the impedance from the reflected winding,

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Variable	Value
Estimated max rectified Input Vinmax=	407
Estimated min rectified input Vinmin=	240
Dmax=	0.51
Np/N5 = TR5p=	22.35
(Vo5+vSchott)*TR5p/Vinmax = DminNew=	0.30
(Vo5+vSchott)*TR5p/Vinnom = DminNom=	0.36
Np/N33 = TR33p=	32.34
Np/N12 = TR12p=	9.83
Np/NN12 = TRN12p=	9.83
Table 1 ATX nower converter mai	n naram-

Table 1. ATX power converter main parameters and turns ratio.

R, multiplied by the turns ratio, TR squared. (Impedance is multiplied by TR squared.)

These basic equations will assist in the design of the coupled inductor as well as its associated output parameters.

Coupled Inductor Design Details

Detailed design of the coupled inductor assumes that the transformer turns ratios have already been calculated. Then the duty cycle range is predicted over all input line voltages.

14 12 33A Ontbnt Crucent 6 8 8 10 10 10 10 10 10 10 10 10 10 10 10 10	- 3.3V Output Curre (amps) - Output Power (all outputs) 5 10	150 140 (M) 130 120 100 100 100 100 100
	5V Output Current	

Using the computation method described here results in the turns ratio values shown in Table 1.

Note that the calculations are from an EXCEL program and therefore are in EXCEL equation format. The specifications used for the 140W converter are shown in Table 2.

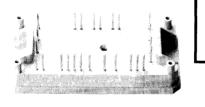
Also note that the combined power for the 5Vdc and 3.3Vdc outputs cannot exceed 90W as illustrated in Figure 3. The core energy calculation uses the maximum value of 90W, however, the windings must be calculated to

Max Current (amps)	Max Current Variable Names	Min Output Current (amps)	Min Current Variable Names	Output Voltage (VDC)	Output Ripple (Vp-p)	Output Range (%)	Minimum Output Voltage (VDC)	Maximum Output Voltage (VDC)	
18	I5max	1	I5min	5	0.05	0.05	4.75	5.25	
10	I33max	0.3	l33min	3.3	0.05	0.05	3.135	3.465	
4.5	I12max	0	l12min	12	0.12	0.05	11.4	12.6	
0.3	IN12max	0	IN12min	-12	0.12	0.1	-10.8	-13.2	
0.3	IN5max	0	IN5min	-5	0.05	0.1	-4.5	-5.5	
Table 2.	Table 2. ATX specification for a 140W converter.								

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		V _{RRM} (V)	IFAVM (A)	V _{CES} (V)	Ic90 (A)	V _{CES} (V)	Ic90 (A)
A 009	MUBW6-06A6 MUBW10-06A6 MUBW15-06A6 MUBW20-06A6 MUBW25-06A6 MUBW35-06A6	1200 1200 1200 1200 1200 1200	11 11 11 11 11 25	600 600 600 600 600	7 11 11 11 18 23	600 600 600 600 600	4.5 8 10 13 16 25
1200 V	MUBW4-12A6 MUBW10-12A6 MUBW15-12A6 MUBW30-12A6	1600 1600 1600 1600	11 11 25 25	1200 1200 1200 1200	2.5 2.5 8 9	1200 1200 1200 1200	2.4 8 11.5 17

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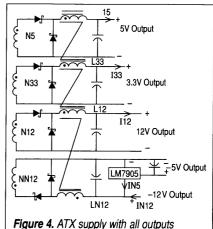
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handle the maximum current each output will see. The information in the table allows us to determine the maximum current a winding will see or determine the amount of current on the 5Vdc output based on the output current on the 3.3Vdc output.

The inductance of L5 is chosen using the EXCEL formula: L5fin = ((1-Dmin)*T*(Vo5+vSchott))/(IndPctMaxIo*I5max) (8)

Where the switching frequency, f =100kHz and therefore T = 10 (sec.

Now that the inductance value of the 5Vdc output is known from earlier calculations, inductance values for the other outputs are calculated using the turns ratio impedance principle developed earlier. Figures 4, 5, and 6 show how the windings reflected to the 5V winding. The prime symbol (') on the reflected windings means these windings have been normalized to the 5V winding. In this case, normalized means multiplied by the output turns



reflected to 5VDC the winding.

Variable	Inductance Formula Using Transformer Turns Ratios	Inductance (μΗ)	Leakage Percentage of Main Inductance (%)	Leakage Inductance (H)	Leakage Inductance (μΗ)	Leakage Inducctance (Normalized to 5V) (H)	Equation Used in Normalizing Leakage Inductance to 5 VDC Winding
		L		lk	lk	lk'	
L5fin		29.0	20%	5.79E-06	5.790	5.79E-06	
L33fin	=L5fin*(TR33p/TR5p)^2	60.6	25%	1.516E-05	15.162	7.238E-06	lk33'=lk33/(TR33p/TR5p)^2
L12fin	=L5fin*(TR12p/TR5p)^2	5.6	2%	5.79E-07	0.579	2.991E-06	lk12'=lk12/(TR12p/TR5p)^2
LN12fin	=L5fin*(TRN12p/TR5p)^2	5.6	10%	0.000005	5.000	2.583E-05	IkN12'=IkN12/(TRN12p/TR5p)^2
able 3. Leaka	age inductance values; actu	al and reflect	ed (normalized)).			· · · · · · · · · · · · · · · · · · ·

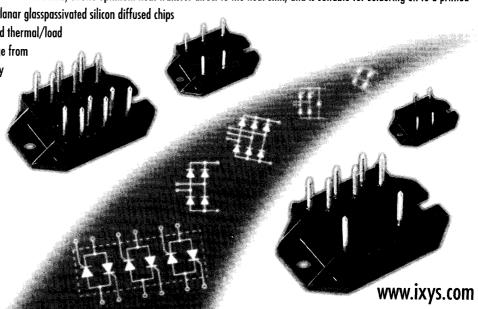
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ratios. Note from *Figures 4*, 5 and 6 that the –5Vdc output goes through a post regulator via the –12Vdc output. The –5Vdc output current is added to the –12Vdc output current for accuracy.

Table 4 shows the calculated inductance values as well as the EXCEL formulas used to find them. Note that a column of data titled "leakage inductance percentage of main inductance" is shown. These values were used to predict ripple currents in the

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final design so that minimum capacitor values could be calculated. The lowest percentage shown is 2% for the highest voltage winding. It was established earlier that the ripple current would be steered to this winding and therefore, it should have the lowest leakage. This provides the magnetics designer with some flexibility in designing the inductor and orienting windings for leakage. The ripple steering inductance will be determined in breadboard experimentation, and this ripple steering inductance

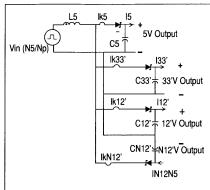


Figure 5. ATX reflected outputs of Figure 4 redrawn for better visualization.

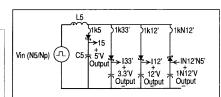


Figure 6. Inductor winding diagram for leakage optimization for ripple current steering.

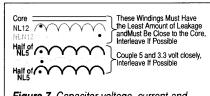


Figure 7. Capacitor voltage, current and inductor current.

tance could be a combination of the leakage inductance and an external series inductor. Similarly, the final output capacitance value will be a combination of available values, holdup time specifications, and final filtering of the output.

Based on the inductor calculations, the winding current and therefore wire size can be determined. This information is in *Table 5* (which was given to the magnetics design house).

More information needs to be given to the inductor designer in order to choose the proper core. The currents in all windings are reflected to the 5V winding. The reflected current squared is then multiplied by the inductance value, as shown in the *Table 6*.

Finally, for the purposes of steering the ripple current to the high voltage winding, a winding diagram is presented in *Figure* 7. The 12 VDC (NL12) winding will get most of the



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ripple current and must have the lowest leakage inductance and therefore be located closest to the core. The negative 12Vdc output (NLN12) is located next and finally the high current 5Vdc and 3.3Vdc windings are interleaved for close coupling and better regulation.

References

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- Provide Dramatic Performance Improvement," author not listed, page M7-1, Unitrode Power Supply Design Seminar SEM 800, Unitrode Semiconductor Products Division, Unitrode Corporation, 7 Continental Boulevard, P.O. Box 399, Merrimack, NH 03054, http://www.unitrode.com TEL: 603-424-2410 FAX: 603-424-3460
- 2. *Intel ATX Power Supply Design Guide*, Version 0.9 Intel Corporation
- 3. ATX 5Vdc and 3.3Vdc Output

- Current Maximum Values Based On 90W
- 4. ATX Outputs with Coupled Inductor
- 5. ATX Supply with all Outputs Reflected to 5VDC the Winding
- 6. ATX Reflected Outputs of *Figure 4* Redrawn for Better Visualization
- Inductor Winding Diagram for Leakage Optimization for Ripple Current Steering
- 8. Capacitor charge balance timing diagram

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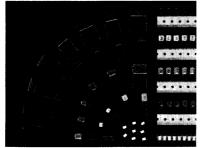
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APPENDIX: Capacitor Value Calculation Method

For the capacitor, the charge must be balanced. As shown in *Figure 8*, the shaded areas must be equal in area. The voltage across the capacitance is expressed in terms of this triangular area. The area product of current versus time is equivalent to the integral expression of the equation:

$$\int_{t_1}^{t_2} i_C \times dt = (shaded area)$$
 (9)

Where $i_C = Capacitor current$

The voltage across the capacitance is:

$$\Delta V_{oc} = \frac{1}{C} \times (area)$$
 (10)

The new expression becomes:

$$\Delta V_{oc} = \frac{1}{C} \times \frac{1}{2} \times \frac{1}{2} \Delta i_{L} \times \frac{1}{2} T_{s}$$
 (11)

Where D' = Duty cycle and T_s = SMPS Switching Period

Where $i_L = Inductor current$

The peak-to-peak inductor current s:

$$\Delta i_{L} = \frac{V_{o}}{I_{c}} D' \times T_{s}$$
 (12)

Time (dt) is:

$$t_2 - t_1 = \frac{1}{2} T_s \tag{13}$$

The final expressions for the ripple voltage due to capacitance is:

$$\Delta V_{oc} = \frac{1}{8} \times \frac{V_o}{LC} \times D' \times T_s^2$$
 (14)

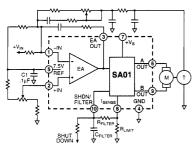
The final expressions for the total output ripple voltage is:



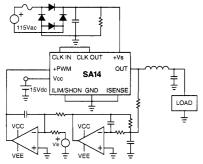
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$$\Delta V_o = i_C \times R_c + \frac{1}{8} \times \frac{V_o}{LC} \times D' \times T_s^2 \quad (15)$$

Where $R_c = \text{Capacitor ESR}$

By using the leakage calculated for each winding to predict the ripple steered to or from that winding along with the established capacitor equations, the capacitor values can be found. The calculated capacitor values are illustrated in the *Table 6*. The low ripple currents that result from the ripple steering produces low capacitor values and favorable ESR values. Final capacitor values will be much higher and LC filtering on the output will filter some of the ripple voltage that will occur across the ESR of the large capacitors.

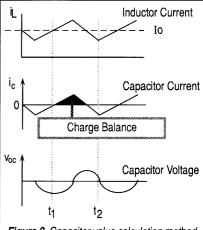


Figure 8. Capacitor value calculation method.

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Output Voltage of Converter (VDC)	Winding Label	Max Inductor Current (ADC)	Inductance (µH)	Turns Ratio (winding/5V)	Leakage Inductance (µH)	Comments
5	NL5	18	29.0	1.0	5.8	Leakage Can Be High for Ripple Steering But Coupling to 3.3 volt winding must be close
3.3	NL33	10	60.6	1.4	15.2	Leakage Can Be High for Ripple Steering But Cou- pling to 5 volt wind- ing must be close
12	NL12	4.5	5.6	0.4	0.6	Need Lowest Leak- age for Ripple Steering
-12	NLN12	0.6	5.6	0.4	5.0	Need Second Low- est Leakage for Ripple Steering

Table 4. Inductor values and parameters used to determine inductor windings.

L5	DC Current Reflected to 5V Winding (A)	DC Current In Reflected 5 volt Winding (Amps)	Inductor LI Squared Calculation
2.9E-05	34.71768	=l5max+l33max*(TR33p/TR5p)+ l12max*(TR12p/TR5p)+ (IN12max+lN5max)*(TRN12p/TR5p)	0.0348956

Table 5. Total inductor current reflected to the 5 VDC winding (used to determine core power).

3.3 0.323 0.467 1.17E-05 =iripple33/(8*f*Vo33ripl) 11.7	uge of verter S DC)	Normalized Iripple Steered by Leakage Inuctance (A p-p)	Actual Iripple Steered by Leakage Inductance (A p-p)	C _{o(min)} (F)	Capacitor Calculation Equations	C _{o(min)} μF	ESR max (ohms)
	5	0.404	0.404	1.01E-05	=iripple5/(8*f*Vo5ripl)	10.1	0.12
12 0.781 0.344 3.58E-06 =iripple12/(8*f*Vo12ripl) 3.6	.3	0.323	0.467	1.17E-05	=iripple33/(8*f*Vo33ripl)	11.7	0.11
	2	0.781	0.344	3.58E-06	=iripple12/(8*f*Vo12ripl)	3.6	0.35
-12 0.090 0.040 4.15E-07 =irippleN12/(8*f*VoN12ripl) 0.4	12	0.090	0.040	4.15E-07	=irippleN12/(8*f*VoN12ripl)	0.4	3.01