UC3842A/43A/44A/45A
High Performance Current Mode Controller

The UC3842A/43A/44A/45/A series are high performance fixed frequency current mode controllers. They are specifically designed for off-line and DC-to-DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature a trimmed oscillator for precise duty cycle control, a temperature compensated reference, high gain error amplifier, current sensing comparator, and a high current totem pole output ideally suited for driving a power MOSFET.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle-by-cycle current limiting, programmable output deadtime, and a latch for single pulse metering.

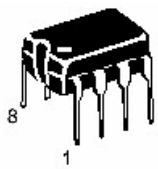
The UC3842A/44A has UVLO thresholds of 16V (on) and 10V (off), ideally suited for off-line converters.

The UC3843A/45A is tailored for lower voltage applications having UVLO thresholds of 8.5V(on) and 7.6(off).

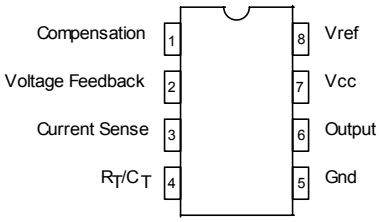
● FEATURE

1. Trimmed Oscillator Discharge Current for Precise Duty Cycle Control
2. Current Mode Operation to 500KHz
3. Automatic Feed Forward Compensation
4. Latching PWM for Cycle-By-Cycle Current Limiting
5. Internally Trimmed Reference with Undervoltage Lockout
6. High Current Totem Pole Output
7. Undervoltage Lockout with Hysteresis
8. Low Start-Up and Operating Current

● PIN ARRANGEMENT



PIN CONNECTIONS

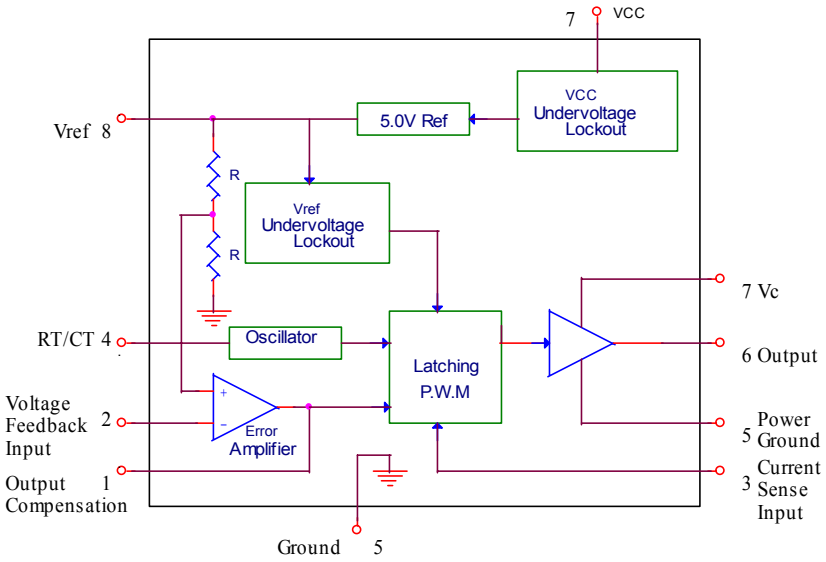


(Top View)

● ORDERING INFORMATION

Device	Temperature Range	Package
UC3842A	0℃~70℃	DIP-8
UC3842AS	0℃~70℃	SOP-8
UC3843A	0℃~70℃	DIP-8
UC3843AS	0℃~70℃	SOP-8
UC3844A	0℃~70℃	DIP-8
UC3844AS	0℃~70℃	SOP-8
UC3845A	0℃~70℃	DIP-8
UC3845AS	0℃~70℃	SOP-8

● BLOCK DIAGRAM



● ABSOLUTE MAXIMUM RATING

Rating	Symbol	Value	Unit
Total Power Supply and Zener Current	(Icc+Iz)	30	mA
Output Current Source or Sink (Note 1)	Io	1.0	A
Output Energy (Capacitive Load per Cycle)	W	5.0	μJ
Current Sense and Voltage Feedback Inputs	Vin	-0.3 to +5.5	V
Error Amp Output Sink Current	Io	10	mA
Power Dissipation and Thermal Characteristics			
SOP-8			
Maximum Power Dissipation @ T_A=25℃	P_D	862	mW
Thermal Resistance Junction to Air	$R_{\Theta JA}$	145	℃/W
DIP-8			
Maximum Power Dissipation @ T_A=25℃	P_D	1.25	W
Thermal Resistance Junction to Air	$R_{\Theta JA}$	100	℃/W
Operating Junction Temperature	T_J	+150	℃
Operating Ambient Temperature	T_A	0 to +70	℃
Storage Temperature Range	Tstg	-65 to +150	℃

● ELECTRICAL CHARACTERISTICS

(Vcc=15V[Note 2], R_T=10KΩ, C_T=3.3nF, T_A=T_{low} to T_{high} [Note 3] unless otherwise noted).

Characteristics	Symbol	Value			Unit
		Min	Typ	Max	
Reference Section					
Reference Output Voltage (Io=1.0mA, T_J=25℃)	Vref	4.9	5.0	5.1	V
Line Regulation (Vcc=12V to 25V)	Reg_{line}	-	6.0	20	mV
Load Regulation (Io=1.0mA to 20mA)	Reg_{load}	-	6.0	25	mV
Temperature Stability	Ts	-	0.2	-	mV/℃
Total Output Variation over Line, Load, and Temperature	Vref	4.82	-	5.18	V
Output Noise Voltage (f=10Hz~10KHz, T_J=25℃)	Vn	-	50	-	μV
Long Term Stability (T_A=125℃ for 1000 Hours)	S	-	5.0	-	mV
Output Short Circuit Current	Isc	-	-100	-180	mA
Oscillator Section					
Frequency T_J=25℃ T_A=T_{low} to T_{high}	fosc	 47 46	 52 -	 57 60	KHz
Frequency Change with Voltage Vcc=12V to 25V	Δfosc/ΔV	-	0.05	1.0	%
Frequency Change with Temperature T_A=T_{low} to T_{high}	Δfosc/ΔT	-	5.0	-	%
Oscillator Voltage Swing (Peak-to-Peak)	Vosc	-	1.6	-	V
Error Amplifier Section					
Voltage Feedback Input (Vo=2.5V)	V_{FB}	2.42	2.5	2.58	V
Input Bias Current (V_{FB}=2.7V)	I_{IB}	-	-0.1	-2.0	μA
Open-Loop Voltage Gain (Vo=2.0V to 4.0V)	A_{VOL}	65	90	-	dB
Unity Gain Bandwidth (T_J=25℃)	BW	0.7	1.0	-	MHz
Power Supply Rejection Radio Vcc=12V to 25V	PSRR	60	70	-	dB
Output Current Sink (Vo=1.1V, V_{FB}=2.7V) Source (Vo=5.0V, V_{FB}=2.3V)	 I_{sink} I_{Source}	 2.0 -0.5	 7 -1.0	 - -	mA
Output Voltage Swing High State (R_L=15K to ground, V_{FB}=2.3V) Low State (R_L=15K to Vref, V_{FB}=2.7V)	 V_{OH} V_{OL}	 5.0 -	 6.0 0.8	 - 1.1	V
Current Sense Section					
Current Sense Input Voltage Gain (Note 4&5)	A_v	2.85	3.0	3.15	V/V
Maximum Current Sense Input Threshold (Note 4)	V_{th}	0.9	1.0	1.1	V
Power Supply Rejection Radio Vcc=12V to 25V (Note4)	PSRR	-	70	-	dB
Input Bias Current	I_{IB}	-	-3.0	-10	μA

Propagation Delay (Current Sense Input to Output)	$t_{PLH(IN/OUT)}$	-	150	300	ns

Output Section

Output Voltage					
Low State (Isink=20mA)	V_{OL}	-	0.08	0.4	V
(Isink=200mA)		-	1.4	2.2	
High State (Isource=20mA)	V_{OH}	13	13.5	-	
(Isource=200mA)		12	13.0	-	
Output Voltage with UVLO Activated Vcc=6.0V, Isink=1.0mA	V_{OL}(UVLO)	-	0.1	1.1	V
Output Voltage Rise Time (C_L=1.0nF, T_J=25℃)	t_r	-	45	150	ns
Output Voltage Fall Time (C_L=1.0nF, T_J=25℃)	t_f	-	35	150	ns

Undervoltage Lockout Section

Start-Up Threshold	UC3842A/UC3844A	Vth	14.5	16	17.5	V
	UC3843A/UC3845A		7.8	8.4	9.0	
Minimum Operating Voltage After Turn-On	UC3842A/UC3844A	$Vcc_{(min)}$	8.5	10	11.5	V
	UC3843A/UC3845A		7.0	7.6	8.2	

PWM Section

Duty Cycle	UC3842A/UC3843A	DCmax	95	97	100	%
	UC3844A/UC3845A		47	48	50	
		DCmin			0	

Total Device

Start-Up Current (UC3842A/43A/44A/45A)	I_{ST}	-	0.17	0.3	mA
Operating Supply Current (V_{FB}=V_{sense}=0)	I_{CC}		14	17	mA
Power Supply Zener Voltage (Icc=25mA)	Vz	30	38	-	V

Note：1. Maximum Package power dissipation limits must be observed.
2. Adjust Vcc above the Start-Up threshold before setting to 15V.
3. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
T_{low}=0℃ for UC3842A/43A/44A/45A T_{high}=+70℃ for UC3842A/43A/44A/45A
4. This parameter is measured at the latch trip point with V_{FB}=0V.
5. Comparator gain is defined as：$Av=\frac{\Delta V\ Output\ Compensation}{\Delta V\ Output\ Sense\ Input}$

- **APPLICATION EXAMPLES**

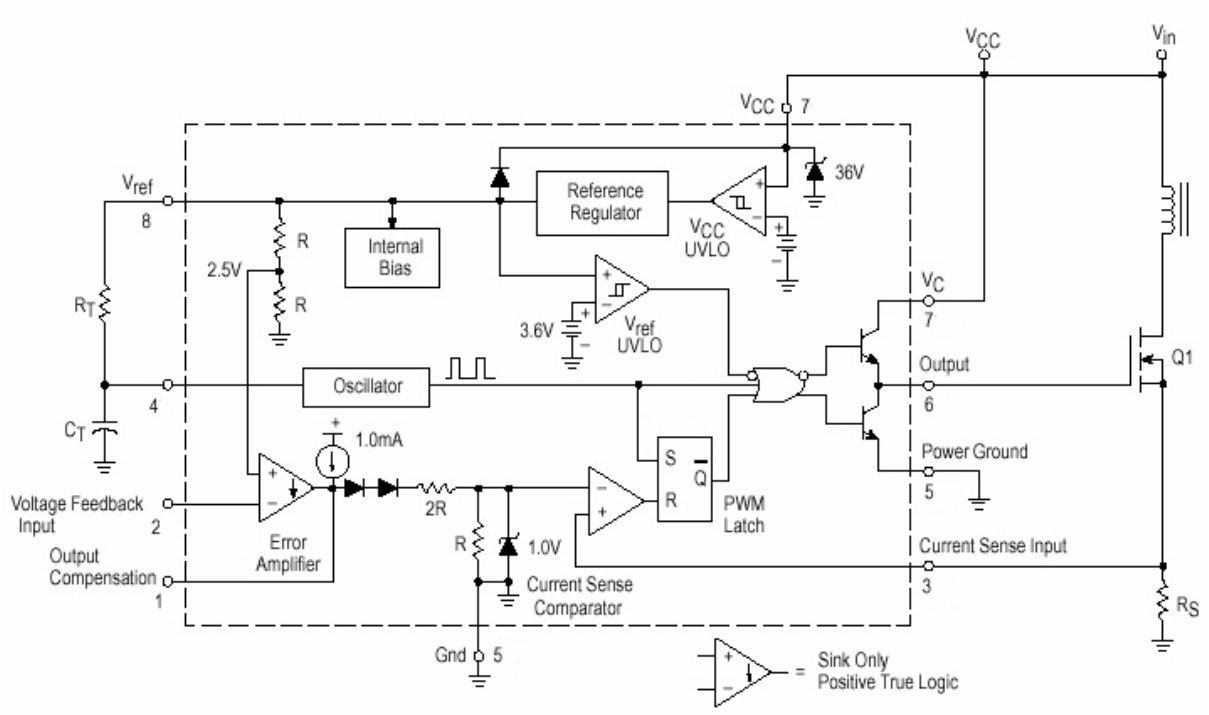


Fig 1.Representative Block Diagram

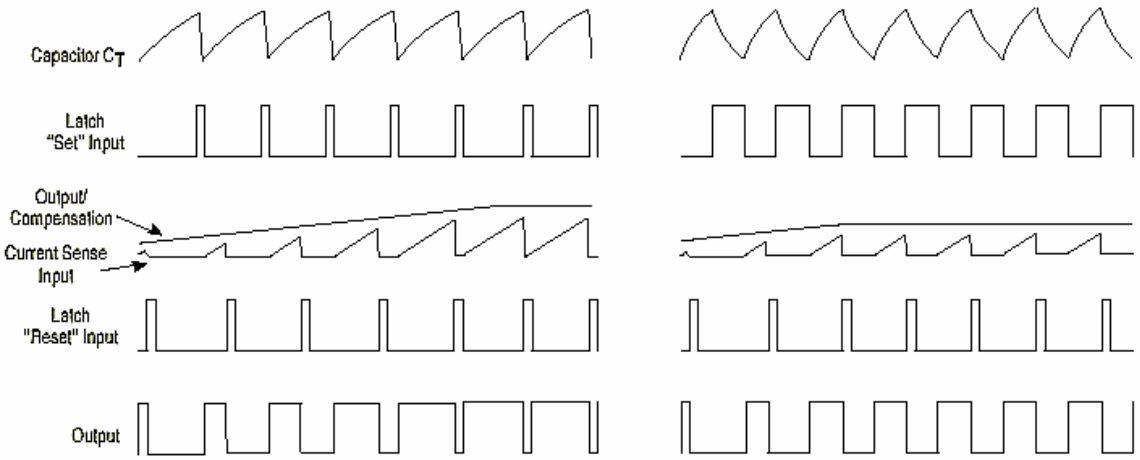
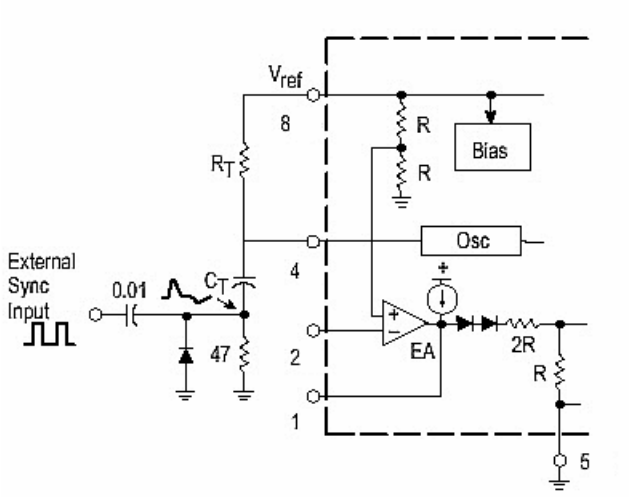


Fig 2.Timing Diagram



The diode clamp is required if the Sync amplitude is large enough to cause the bottom side of C_T to go more than 300 mV below ground.

Fig 3.External Clock Synchronization

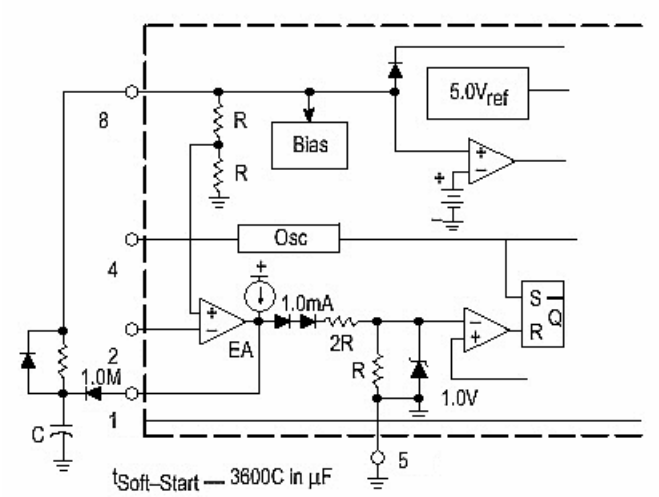
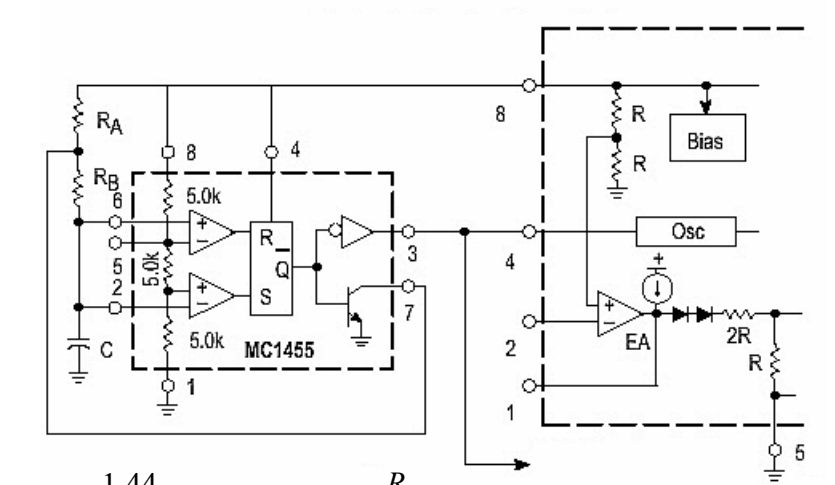


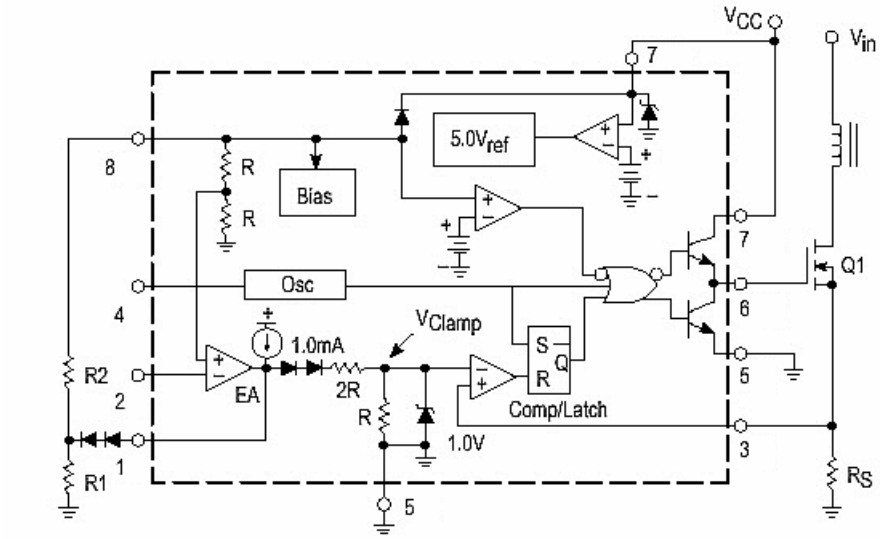
Fig 4.Soft-Start Circuit



$$f=\frac{1.44}{(R_A+2R_B)C} \qquad D_{max}=\frac{R_B}{R_A+2R_B}$$

To Additional UC3842's

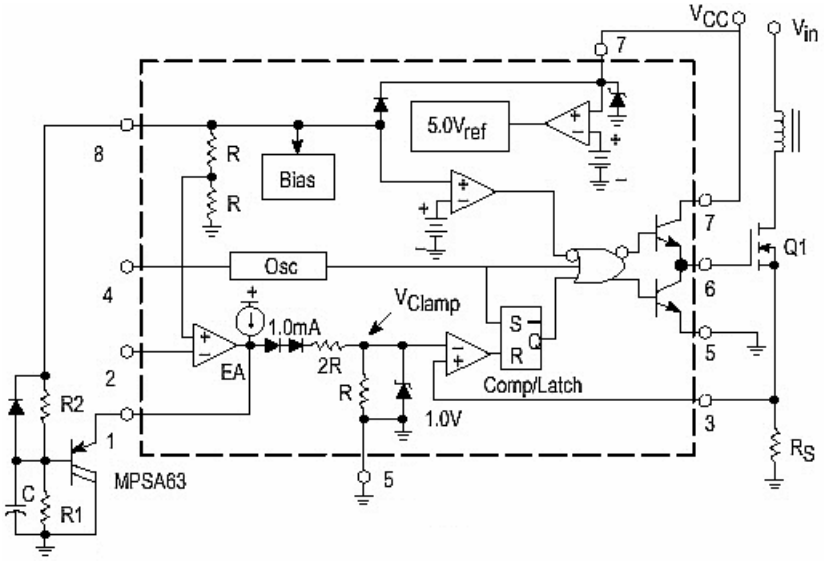
Fig 5.External Duty Cycle Clamp and Multi Unit Synchronization



$$Vclamp=\frac{1.67}{(\frac{R2}{R1}+1)}+0.33\times10\text{-}3(\frac{R1R2}{R1+R2}) \qquad Ipk(max)=\frac{VClamp}{RS}$$

Where:$0 \leqq V_{clamp} \leqq 1.0V$

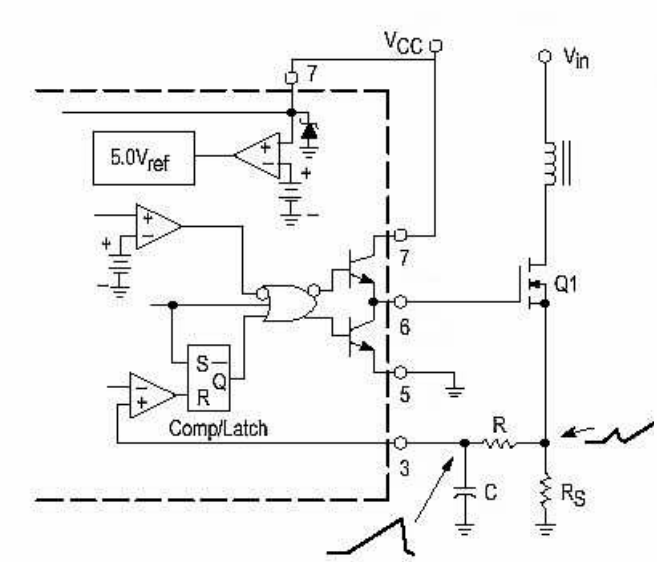
Fig 6.Adjustable Reduction of Clamp Level



$$V_{Clamp}=\frac{1.67}{(\frac{R2}{R1}+1)} \qquad Ipk(max)=\frac{VClamp}{RS} \qquad \text{Where:} 0 \leqq V_{Clamp} \leqq 1.0V$$

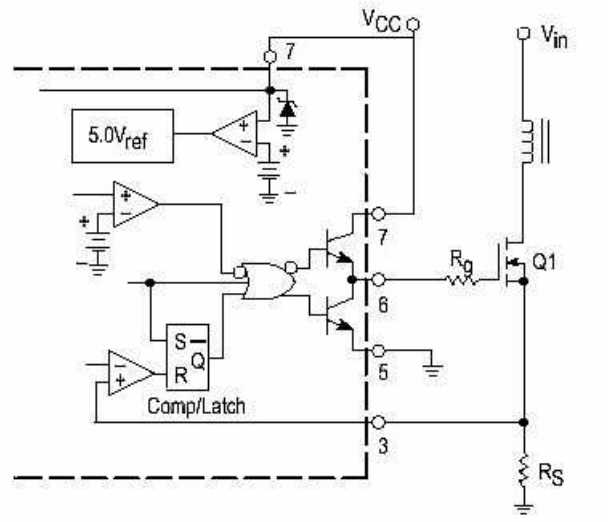
$$t_{softstart}=-\ln\left[1-\frac{Vc}{3V_{Clamp}}\right]C\frac{R1R2}{R1+R2}$$

Fig 7.Adjustable Buffered Reduction of Clamp Level with Soft-Start



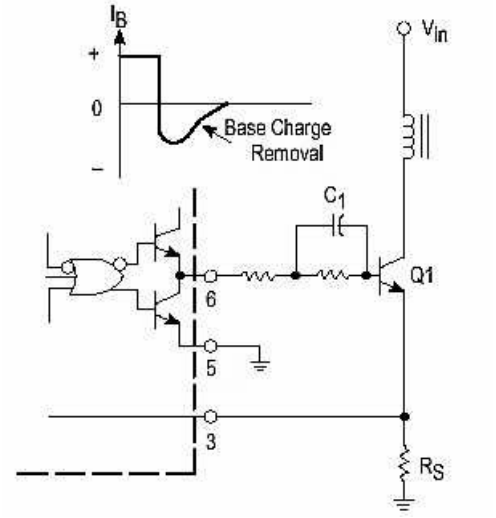
The addition of the RC filter will eliminate instability caused by the leading edge spike on the current waveform.

Fig 8.Current Waveform Spike Suppression



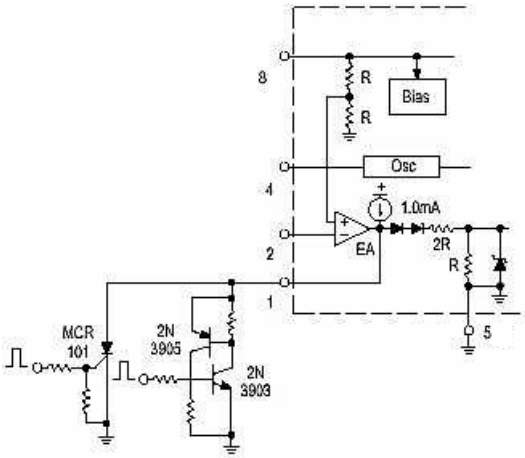
Series gate resistor R_g will damp any high frequency parasitic oscillations caused by the MOSFET input capacitance and any series wiring inductance in the gate-source circuit.

Fig 9.MOSFET Parasitic Oscillations



The totem-pole output can furnish negative base current for enhanced transistor turn-off, with the addition of capacitor C1.

Fig 10.Bipolar Transistor Drive



The MCR101 SCR must be selected for a holding of less than 0.5mA at $T_{A(min)}$.The simple two transistor circuit can be used in placed of the SCR as shown. All resistor are 10K.

Fig 11.Latched Shutdown

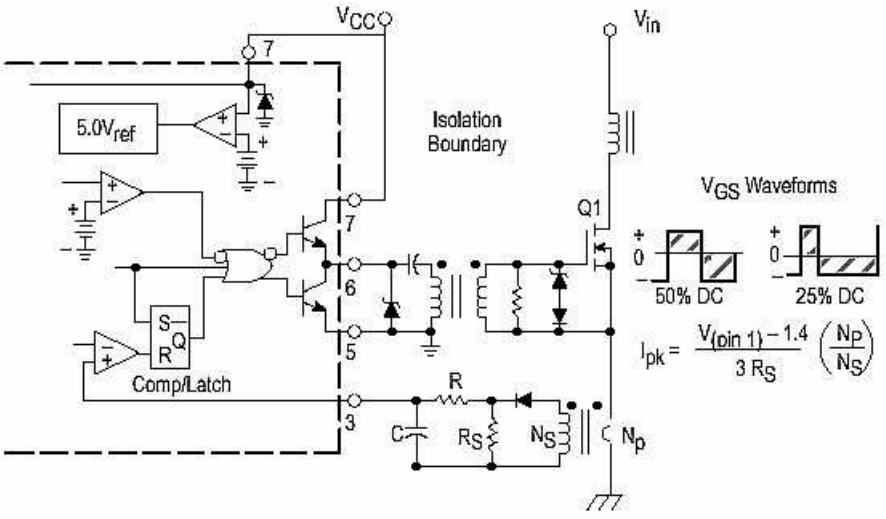
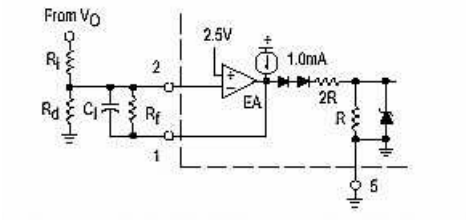
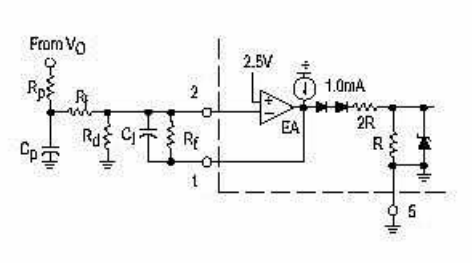


Fig 12.Isolated MOSFET Drive





$R_f \geqq 8.8K$

Error Amp compensation circuit for stabilizing any current-mode topology except for boost and flyback converters operating with continuous inductor current.

Error Amp compensation circuit for stabilizing current-mode topology except for boost and flyback operating with continuous inductor current.

Fig 13.Error Amplifier Compensation

OPERATING DESCRIPTION

The UC3842A/43A/44A/45A series are high performance, fixed frequency, current mode controllers. They are specifically designed for Off-Line and dc-to-dc converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Fig 1.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. Capacitor C_T is charged from the 5.0 V reference through resistor R_T to approximately 2.8V and discharged to 1.2V by an internal current sink. During the discharge of C_T, the oscillator generates and internal blanking pulse that holds the center input of the NOR gate high. This causes the Output to be in a low state , thus producing a controlled amount of output deadtime. Note that many values of R_T and C_T will give the same oscillator frequency but only one combination will yield a specific output deadtime at a given frequency. The oscillator thresholds are temperature compensated, and the discharge current is trimmed and guaranteed to within±10% at T_J=25℃. These internal circuit refinemens minimize variations of oscillator frequency and maximum output duty cycle.

In many noise sensitive applications it may be desirable to frequency-lock the converter to an external system clock. This can be accomplished by applying a clock signal to the circuit shown in Fig 3 . For reliable locking, the free-running oscillator frequency should be set about 10% less than the clock frequency. A method for multi unit synchronization is shown in Fig 5. By tailoring the clock waveform, accurate Output duty cycle clamping can be achieved.

Error Amplifier

A fully compensated Error Amplifier with access to the inverting input and output is provided. It features a typical dc voltage gain of 90dB, and a unity gain bandwidth of 1.0MHz with 57 degrees of phase margin(Fig 19). The noninverting input is internally biased at 2.5V and is not pinned out. The converter output voltage is typically divided down and monitored by the inverting input. The maximum input bias current is –2.0 μA which can cause an output voltage error that is equal to the product of the input bias current and the equivalent input divider source resistance.

The Error Amp Output(Pin 1) is provide for external loop compensation(Fig 11). The output voltage is offset by two diode drops (≒1.4V) and divided by three before it connects to the inverting input of the Current Sense Comparator. This guarantees that no drive pulses appear at the Output (Pin 6) when Pin 1 is at its lowest state(V_{OL}). This occurs when the power supply is operating and the load is removed, or at the beginning of a soft-start interval (Fig 4,Fig 7). The Error Amp minimum feedback resistance is limited by the amplifier's source current (0.5mA) and the required output voltgae (V_{OH}) to reach the comparator's 1.0V clamp level:

$$R_{f(min)} \fallingdotseq \frac{3.0(1.0V)+1.4V}{0.5mA} = 8800\,\Omega$$

Current Sense Comparator and PWM Latch

The UC3842A/43A/44A/45A operate as a current mode controller, whereby output switch conduction is initiated by the oscillator and terminated when the peak inductor current reaches the threshold level established by the Error Amplifier Output/Compensation(Pin 1). Thus the error signal controls the peak inductor current on a cycle-by-cycle basis. The current Sense Comparator PWM Latch configuration used ensures that only a single pulse appears at the Output during any given oscillator cycle. The inductor current is converted to a voltage by inserting the ground referenced sense resistor R_S in series with the source of output switch Q1. This voltage is monitored by the Current Sense Input (Pin 3) and compared a level derived from the Error Amp Output . The peak inductor current under normal operating conditions is controlled by the voltage at pin 1 where:

$$I_{pk} = \frac{\mathbf{V_{(Pin\,1)} - 1.4V}}{\mathbf{3R_S}}$$

Abnormal operating conditions occur when the power supply output is overloaded or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.0V. Therefore the maximum peak switch current is:

$$I_{pk(max)} = \frac{\mathbf{1.0V}}{\mathbf{R_S}}$$

When designing a high power switching regulator it becomes desirable to reduce the internal clamp voltage in order to keep the power dissipation of R_S to a reasonable level. A simple method to adjust this voltage is shown in Fig 6.The two external diodes are used to compensate the internal diodes yielding a constant clamp voltage over temperature. Erratic operation due to noise pickup can result if there is an excessive reduction of the $I_{pk(max)}$ clamp voltage.

A narrow spike on the leading edge of the current waveform can usually be observed and may cause the power supply to exhibit an instability when the output is lightly loaded. This spike is due to the power transformer interwinding capacitance and output rectifier recovery time. The addition of an RC filter on the Current Sense Input with a time constant that approximates the spike duration will usually eliminate the instability; refer to Fig 8.

Pin	Function	Description
1	Compensation	This pin is Error Amplifier output and is made available for loop Compensation.
2	Voltage Feedback	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	Current Sense	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	R_T/C_T	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor R_T to V_{ref} and capacitor C_T to ground. Operation to 500kHz is possible.
5	Gnd	This pin is the combined control circuitry and power ground.
6	Output	This output directly drivers the gate of a power MOSFET. Peak currents up to 1.0A are sourced and sunk by this pin.
7	V_{CC}	This pin is the positive supply of the control IC.
8	V_{ref}	This is the reference output. It provides charging current for capacitor C_T through resistor R_T.

Undervoltage Lockout

Two undervoltage lockout comparators have been incorporated to guarantee that the IC is fully functional before the output stage is enabled. The positive power supply terminal (V_{CC}) and the reference output (V_{ref}) are each monitored by separate comparators. Each has built-in hysteresis to prevent erratic output behavior as their respective thresholds are crossed. The V_{CC} comparator upper and lower thresholds are 16V/10V for the UC3842A/44A and 8.4V/7.6V for UC3843A/45A. The V_{ref} comparator upper and lower thresholds are 3.6V/3.4V. The large hysteresis and low startup current of the UC3842A/44A make it ideally suited in off-line converter applications where efficient bootstrap startup techniques are required. The UC3843A/45A are intended for lower voltage dc to dc converter applications. A 36V zener is connected as a shunt regulator from V_{CC} to ground. Its purpose is to protect the IC from excessive voltage that can occur during system startup. The minimum operating voltage for the UC3842A/44A is 11V and 8.2V for the UC3843A/45A.

Output

These devices contain a single totem pole output stage that was specifically designed for direct drive of power MOSFETs. It's capable of up to ±1.0A peak drive current and has a typical rise and fall time of 50ns with a 1.0nF load. Additional internal circuitry has been added to keep the Output in a sinking mode whenever an eliminates the need for an external pull-down resistor.

Reference

The 5.0V bandgap reference is trimmed to ±2.0% tolerance at T_J=25℃ on the UC3842A/43A/44A and UC3845A. It's primary purpose is to supply charging current to the oscillator timing capacitor. The reference has short circuit protection and is capable of providing is excess of 20mA for powering additional control system circuitry.

DESIGN CONSIDERATIONS

Do not attempt to construct the converter on wire-wrap or plug-in prototype board. High Frequency circuit layout techniques are imperative to prevent pulsewidth jitter. This is usually caused by excessive noise pick-up imposed on the Current Sense or Voltage Feedback inputs. Noise immunity can be improved by lowering circuit impedances at these points. The printed circuit layout should contain a ground plane with low-current signal and high-current switch and output grounds returning on separate paths back to the input filter capacitor. Ceramic bypass capacitors (0.1 μF) connected directly to V_{CC}, V_C, and V_{ref} may be required depending upon circuit layout. This provides a low impedance path for filtering the high frequency noise. All high current loops should be kept as short as possible using heavy copper runs to minimize radiated EMI. The Error Amp compensation circuitry and the converter output voltage divider should be located close to the IC and as far as possible from the power switch and other noise generating components.

Current mode converters can exhibit subharmonic oscillations when operating at a duty cycle greater than 50% with continuous inductor current. This instability is independent of the regulators closed-loop characteristics and is caused by the simultaneous operating conditions of fixed frequency and peak current detecting. Fig (14A) shows the phenomenon graphically. At t_0, switch conduction begins, causing the inductor current to rise at a slope of m_1. This slope is a function of the input voltage divided by the inductance. At t_1, the Current Sense Input reaches the threshold established by the control voltage. This causes the switch to turn off and the current to decay at a slope of m_2 until the next oscillator cycle. The unstable condition can be shown if a perturbation is added to the control voltage, resulting is a small ΔI (dashed line). With a fixed oscillator period, the current decay time is reduced, and the minimum current at switch turn-on (t_2) is increased by $\Delta I + \Delta I\, m2/m1$. The minimum current at the next cycle (t_3) decreases to $(\Delta I + \Delta I m2/m1)(m2/m1)$. This perturbation is multiplied by m2*m1 on each succeeding cycle, alternately increasing and decreasing the inductor current at switch turn-on. Several oscillator cycles may be required before the inductor current reaches zero causing the process to commence again. If m_2/m_1 is greater than 1, the converter will be unstable. Fig(14B) shows that by adding an artificial ramp that is synchronized with the PWM clock to the control voltage, the ΔI perturbation will decrease to zero on succeeding cycles. This compensation ramp(m_3) must have a slope equal to or slightly greater than $m_2/2$ for stability. With $m_2/2$ slope compensation, the average inductor current follows the control voltage yielding true current mode operation. The compensating ramp can be derived from the oscillator and add to either the Voltage Feedback or Current Sense inputs .

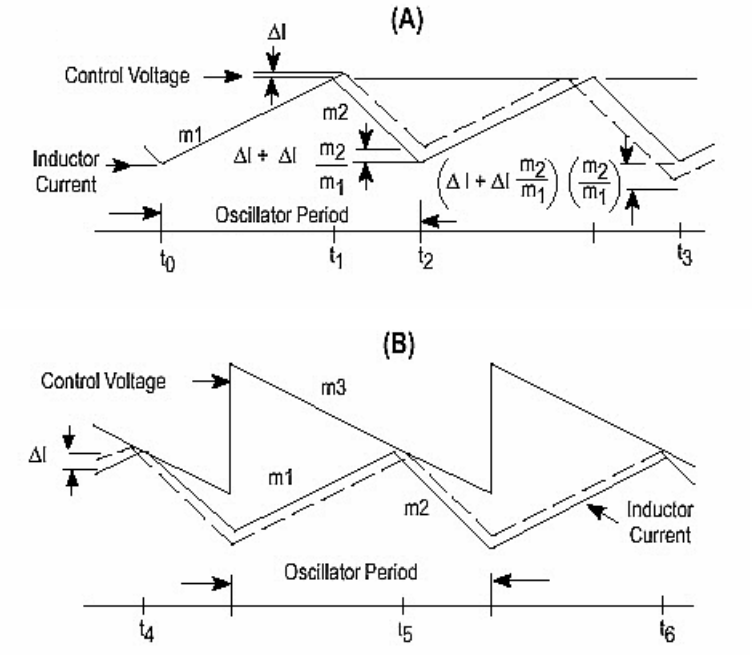

(A)
ΔI
Control Voltage
m2
m1
Inductor Current
ΔI + ΔI m2/m1
(ΔI + ΔI m2/m1)(m2/m1)
Oscillator Period
t0
t1
t2
t3
(B)
Control Voltage
m3
ΔI
m1
m2
Inductor Current
Oscillator Period
t4
t5
t6

Fig .14

- **ELECTRICAL CHARACTERISTICS CURVES**

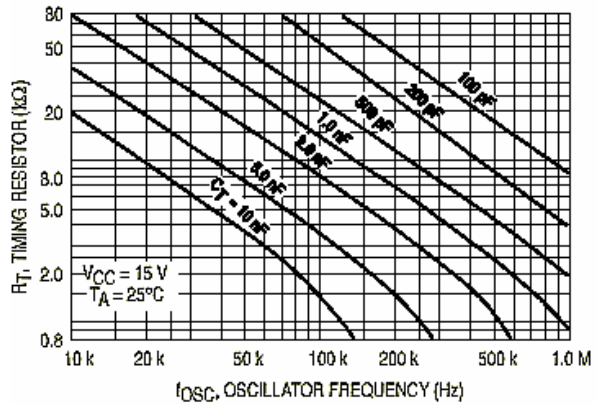


Fig 15.Timing resistor versus oscillator frequency

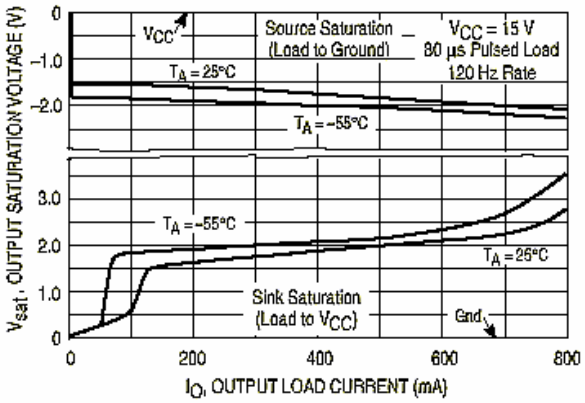


Fig 16.Output saturation voltage versus load current

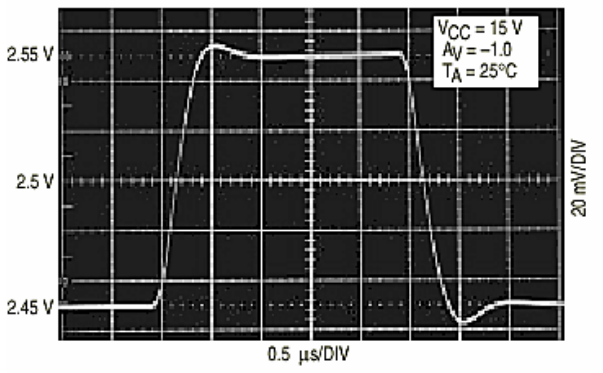


Fig 17.Error amp small signal transient response

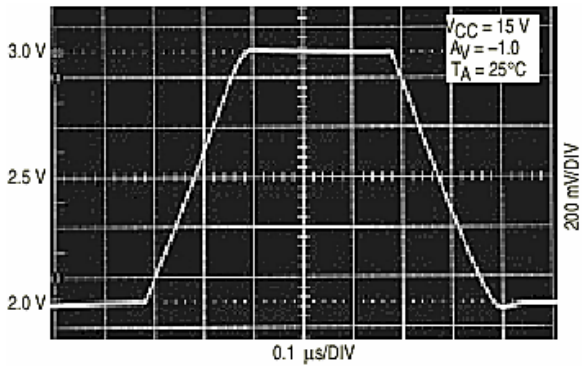
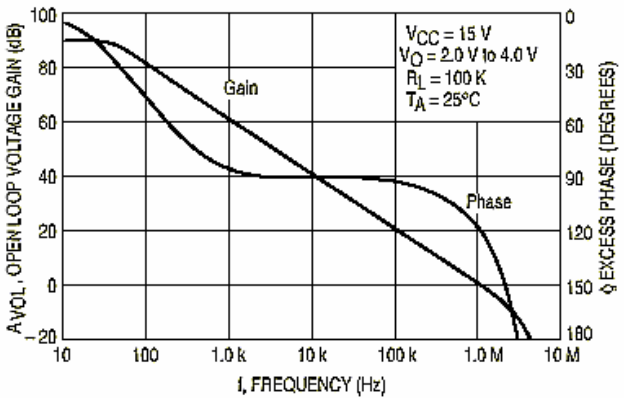


Fig 18.Error amp large signal transient response



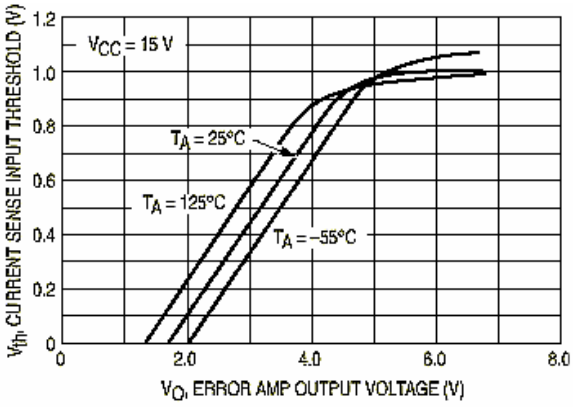
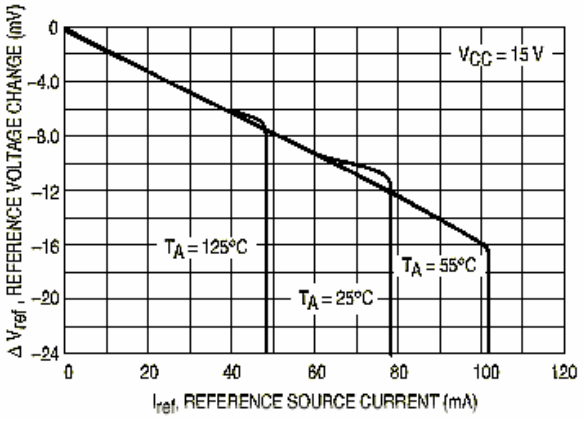


Fig 19.Error amp open-loop gain and phase versus frequency

Fig 20.Current sense input threshold versus error amp output voltage



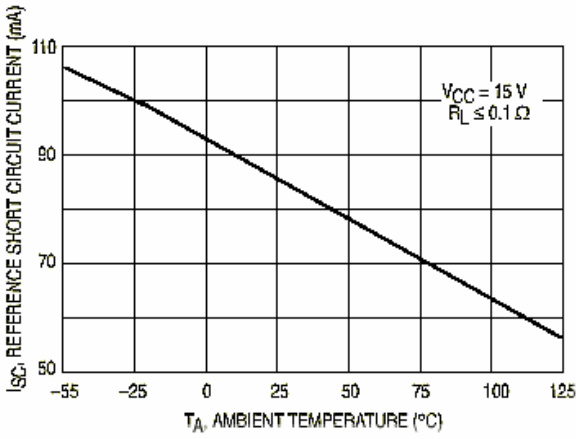
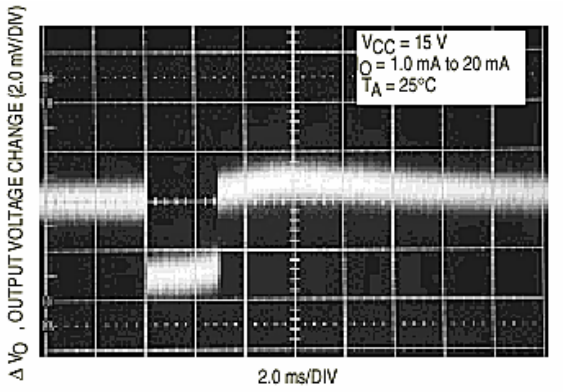


Fig 21.Refrence voltage change versus source current

Fig 22.Reference short circuit current versus temperature



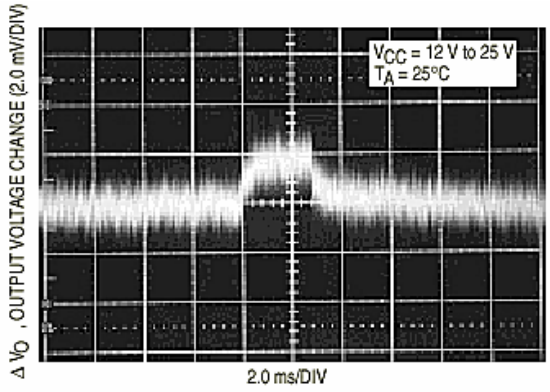
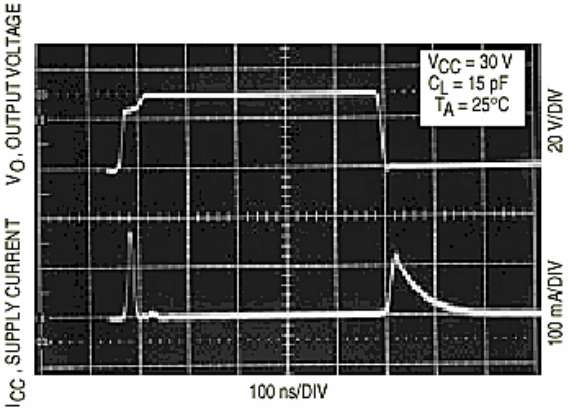


Fig 23.Reference load regulation

Fig 24.Reference line regulation



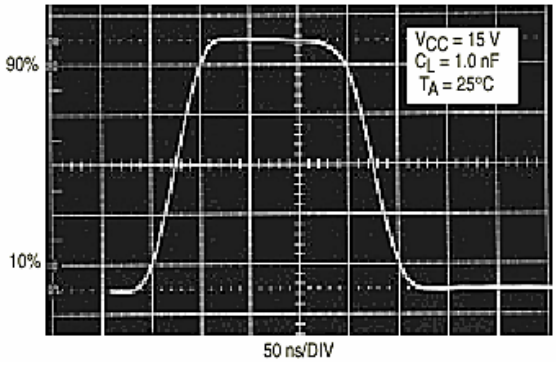
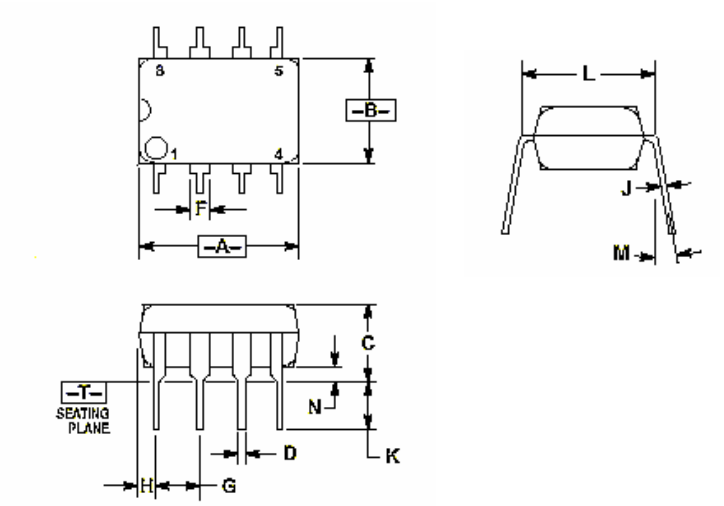


Fig 25.Output cross conduction **Fig 26.Output waveform**

- **EXTERNAL DIMENSIONS**

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	--	10°	--	10°
N	0.76	1.01	0.030	0.040



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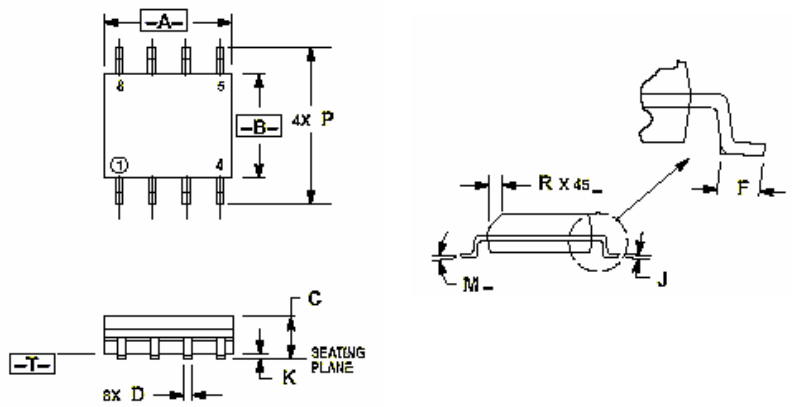
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	5.00	5.20	0.196	0.205
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019



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