

SYNOPSYS

# Advanced HDL Design Training On Xilinx FPGA

version 3.3

Speaker : Elmer Chiang

Xilinx Taiwan

©1999 Synopsys, Inc. Synopsys is a registered trademark and FPGA Express is a registered trademark of Synopsys, Inc.



# Chapter 1

## FPGA *Express* v3.3

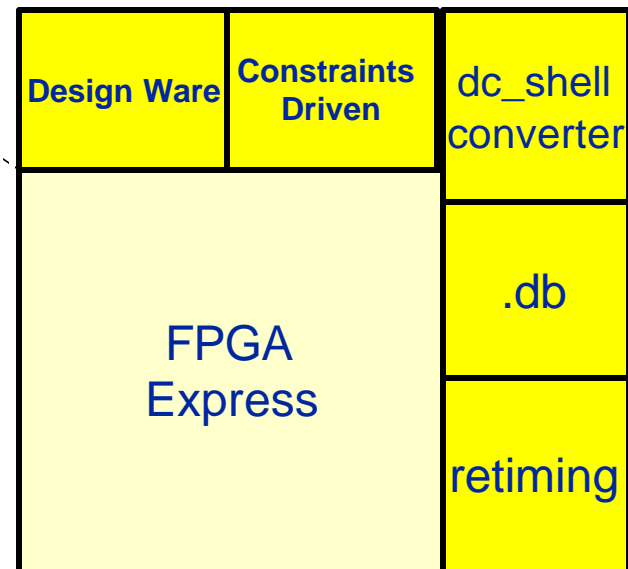
### Overview

# What is FPGA Express and Compiler II?

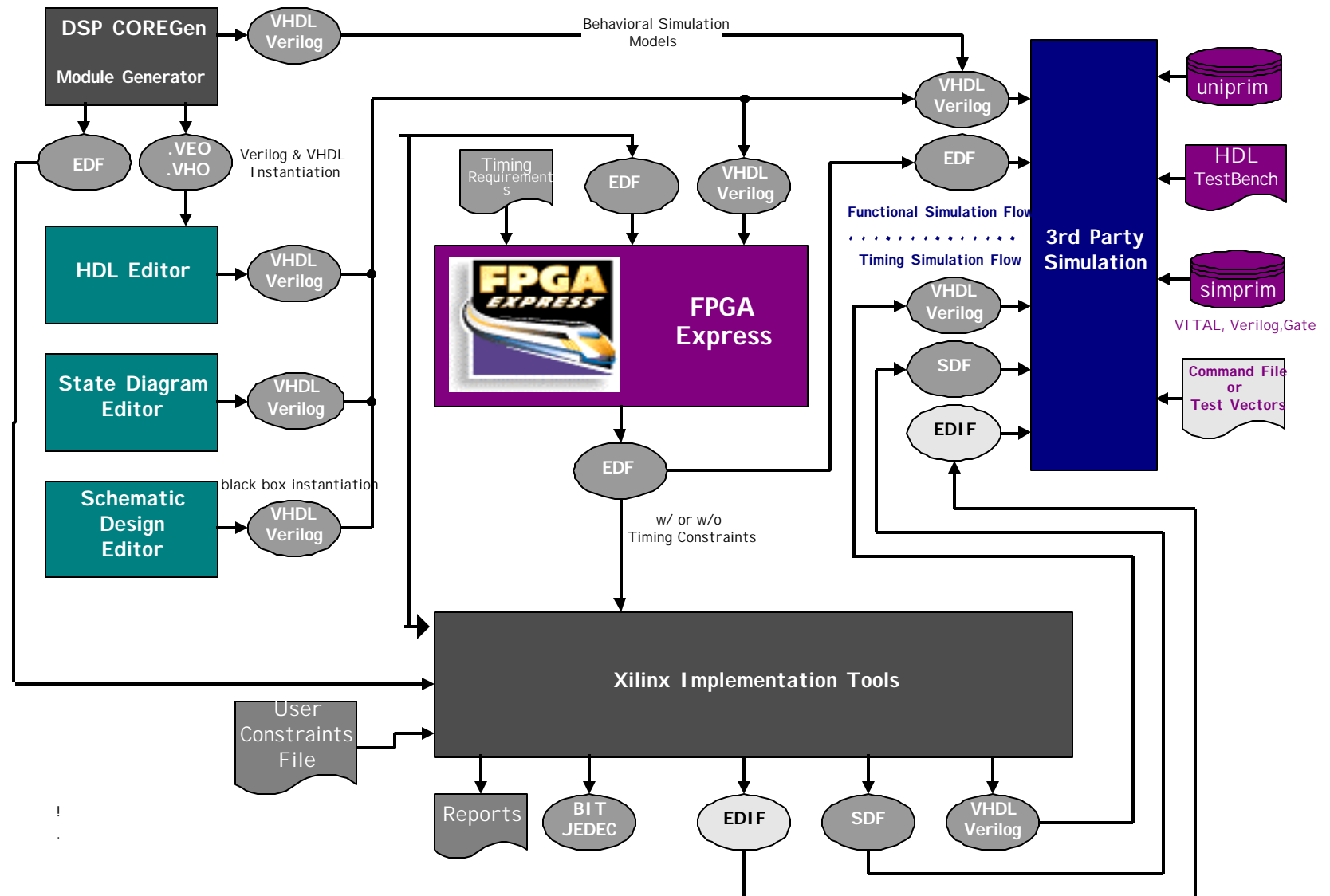
## ***FPGA Express***

- Push-Button Flow
- Industry-Standard HDLs
- Industry-Leading QoR
- Built-In Static Timing Analyzer
- Schematic Viewer
- Integration with P&R tools

## ***FPGA Compiler II***



# FPGA Express Flow



# FPGA Express Features ...

- ◆ FPGA Express Technology
  - Constraint Entry GUI
  - Automatic I/O Pad and Global Signal Mapping
  - Built-in Timing Analyzer
  - Built-in Module Generation (Fast Carry, RLOC)
  - Resource Sharing
  - Hierarchy Control
  - Schematic Viewer called Vista

# What's New in Express v3.3

- ◆ dont\_touch
  - instructs Express to not re-optimize instantiated modules
  - available via Constraint GUI, HDL attribute, script command in FE\_SHELL
- ◆ Virtex architectural support additions
  - SRL16 inference
  - ROM inference

# Simple Four Step Design Process

The screenshot displays the FPGA Express software interface with the following components:

- Design Sources:** A tree view showing the project files, including `lab3`, `WORK`, and various Verilog files like `bernie_counter.v`, `bernie_ff.v`, `bernie_shiftr.v`, `bitunstuff.v`, `bnkreg.v`, and `eopdetect.v`. A blue circle labeled "1 Analyze Files" is placed over this panel.
- Chips:** A list of available chips, with `Xilinx XC4000: 4013XLPQ160V-3` selected. A blue circle labeled "4 Optimize" is placed over this panel.
- Create Implementation - bernie\_counter:** A dialog box for configuring the implementation. It includes fields for `Implementation Name` (set to `bernie_counter`), `Target device` (Vendor: `Xilinx`, Device: `4028EXHQ208`, Family: `XC4000`, Speed grade: `ex-2`), `Optimize for` (radio buttons for `Speed` and `Area`), `Effort` (radio buttons for `High` and `Low`), `Clock frequency` (set to `50` MHz), and a checkbox for `Do not insert I/O pads`. A blue circle labeled "2 Select Device" is placed over the `Device` dropdown menu.
- lab3.exp - rxd [Constraints]:** A dialog box for entering constraints. It has tabs for `Clocks`, `Paths`, `Ports`, `Modules`, and `Xilinx Options`. The `Ports` tab is active, showing a table of constraints. A blue circle labeled "3 Enter Constraints" is placed over the `Output Delay (ns)` column.

Name	Direction	Input Delay (ns)	Output Delay (ns)
<default>			
DPLUS	input	20/(RC, CLK)	
DMINS	input	20/(RC, CLK)	
PIDBUS<7>	output		20/(RC, CLK)
PIDBUS<6>	output		20/(RC, CLK)



# Constraint Entry ...

- ◆ Synthesis -> Edit Constraints...

## Define Clocks

PERIOD / RISE / FALL

## Define Time Constraint

FROM : TO

Sub-Paths

## Define Port Attributes

DELAY

PULLUP / PULLDOWN

SLEW / Global Buffers

Pin Locations

## Define Hierarchy Preservation

Eliminate / Preserve

Operator Sharing

Optimize / Effort

## Xilinx Constraints

Implementation Tool Target

GSR Usage

	Name	Direction	Input Delay (ns)	Output Delay (ns)	Global Buffer
1	<default>				AUTOMATIC
2	RST	input	20/(RC, CLK)		
3	CLK	input	20/(RC, CLK)		
4	DPLUS	input	20/(RC, CLK)		
5	DMINS	input	20/(RC, CLK)		
6	PIDBUS<7>	output		20/(RC, CLK)	
7	PIDBUS<6>	output		20/(RC, CLK)	
8	PIDBUS<5>	output		20/(RC, CLK)	
9	PIDBUS<4>	output		20/(RC, CLK)	
10	PIDBUS<3>	output		20/(RC, CLK)	
11	PIDBUS<2>	output		20/(RC, CLK)	
12	PIDBUS<1>	output		20/(RC, CLK)	
13	PIDBUS<0>	output		20/(RC, CLK)	
14	DATABUS<7>	output		20/(RC, CLK)	
15	DATABUS<6>	output		20/(RC, CLK)	
16	DATABUS<5>	output		20/(RC, CLK)	

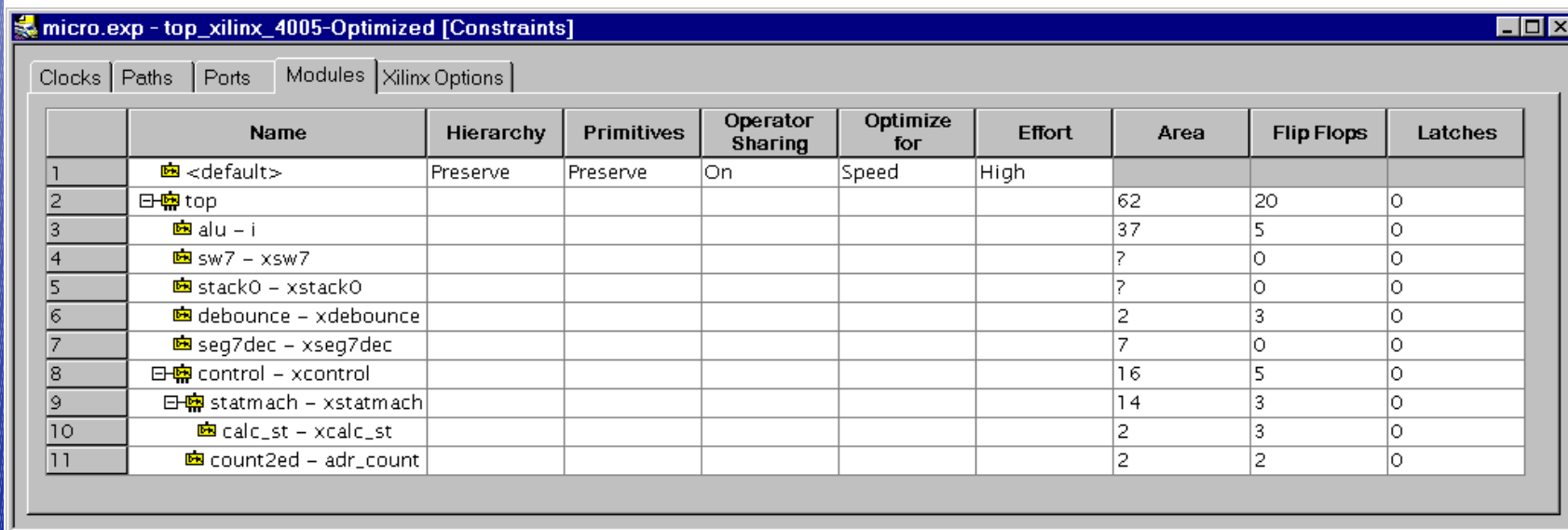


# How are the Constraints used?

- ◆ FPGA Express passes the constraints to the output .NCF file
- ◆ The exact value of the timing constraint is not directly used for synthesis optimization
  - Speed or Area selection under constraint editor's module tab is used for selecting the type of optimization to perform on the sections of the design
- ◆ FPGA Express creates Xilinx recommended constraints:
  - Periods and Offsets for global constraints
  - FROM:TO for fast, slow, or multi-cycle paths

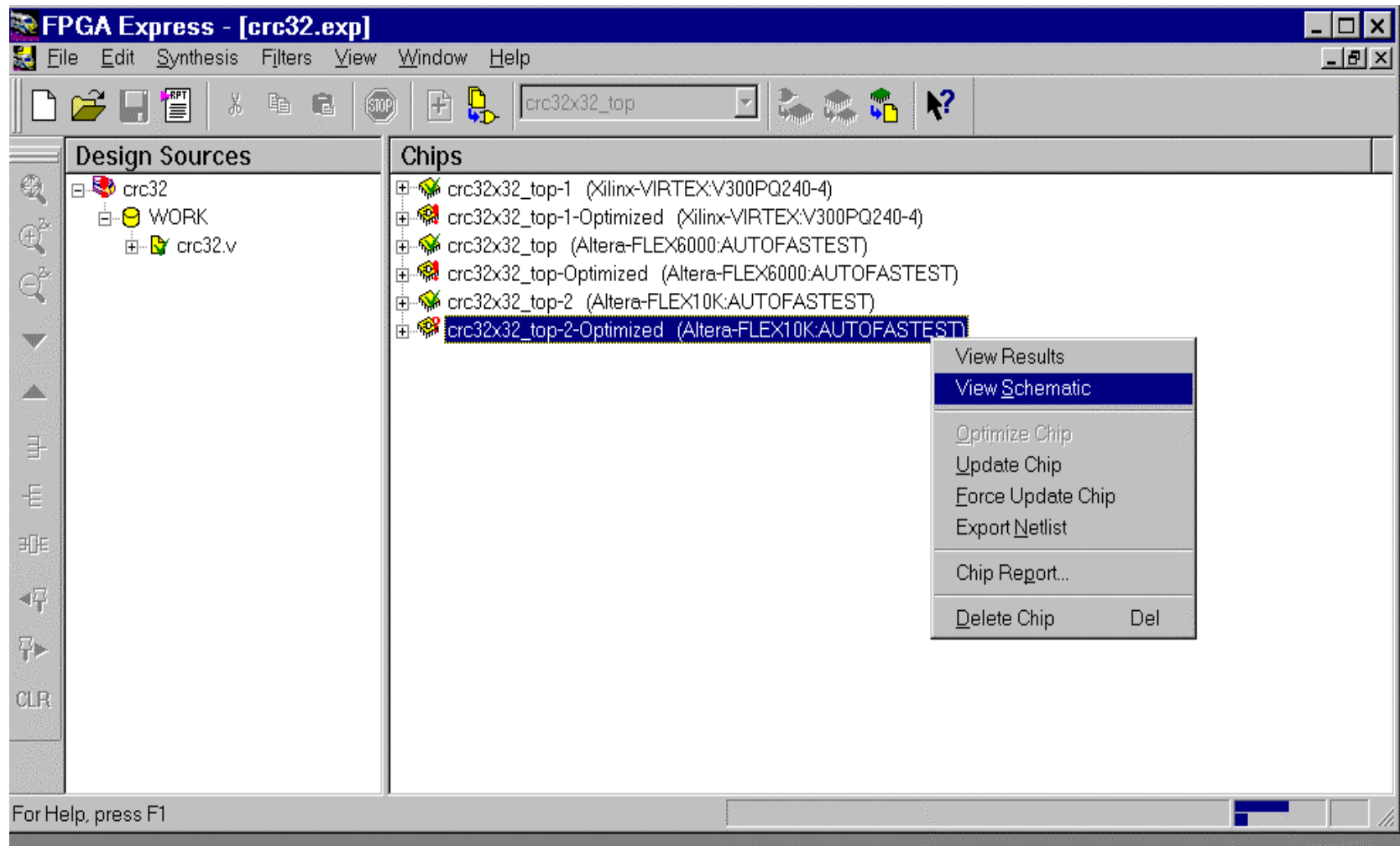
# Hierarchy Specification

- ◆ The module view lets the user "See" the design hierarchy
- ◆ Hierarchy Control is available you can preserve or eliminate level of hierarchy from optimization
- ◆ Operator Sharing, Speed/Area, Effort
- ◆ Primitive Control



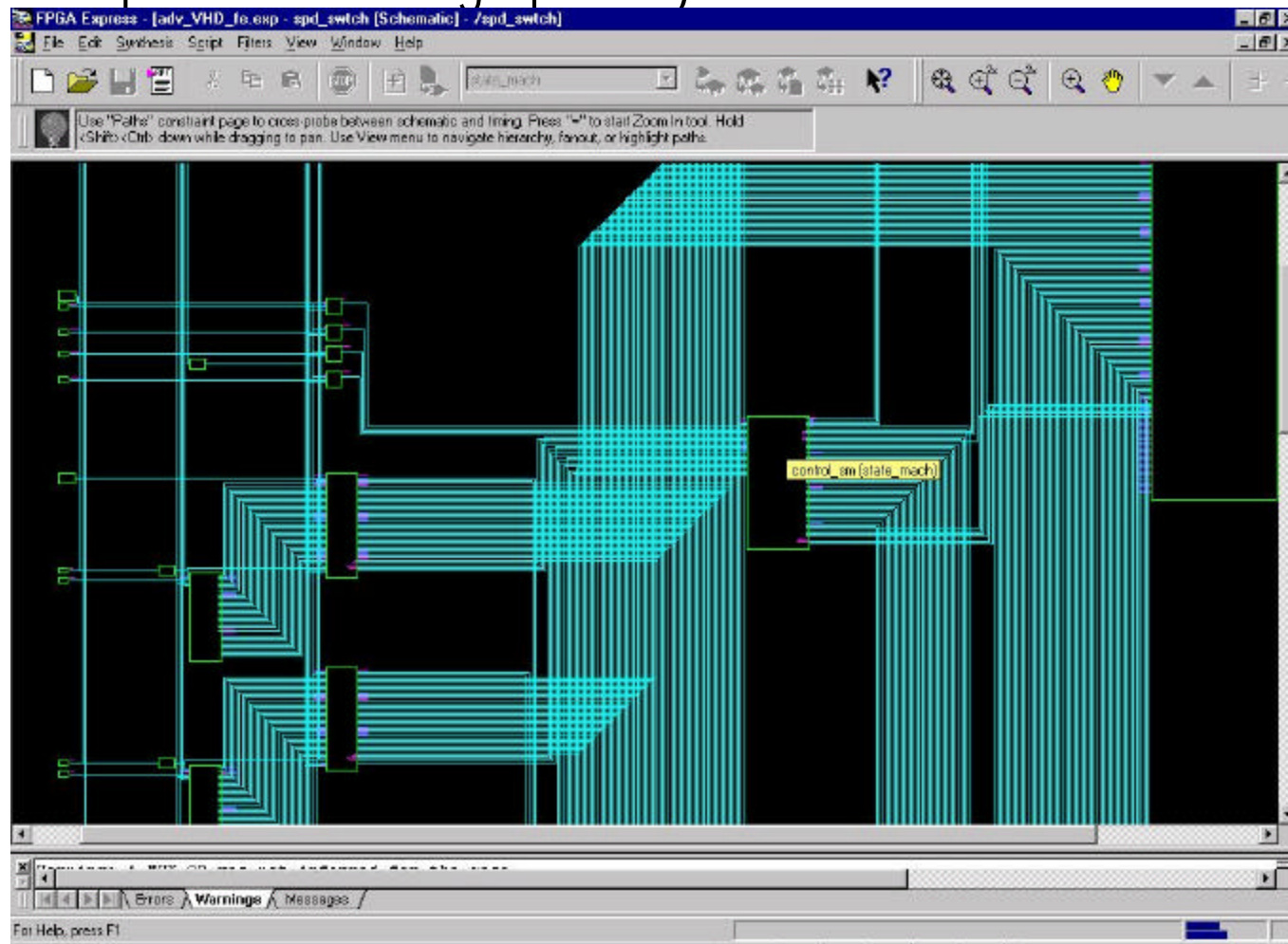
	Name	Hierarchy	Primitives	Operator Sharing	Optimize for	Effort	Area	Flip Flops	Latches
1	<default>	Preserve	Preserve	On	Speed	High			
2	top						62	20	0
3	alu - i						37	5	0
4	sw7 - xsw7						7	0	0
5	stack0 - xstack0						7	0	0
6	debounce - xdebounce						2	3	0
7	seg7dec - xseg7dec						7	0	0
8	control - xcontrol						16	5	0
9	statmach - xstatmach						14	3	0
10	calc_st - xcalc_st						2	3	0
11	count2ed - adr_count						2	2	0

# Invoking the Schematic Viewer



# Schematic Viewer: Vista

- ◆ The “Vista” Schematic Viewer allows you to see what FPGA express has built graphically

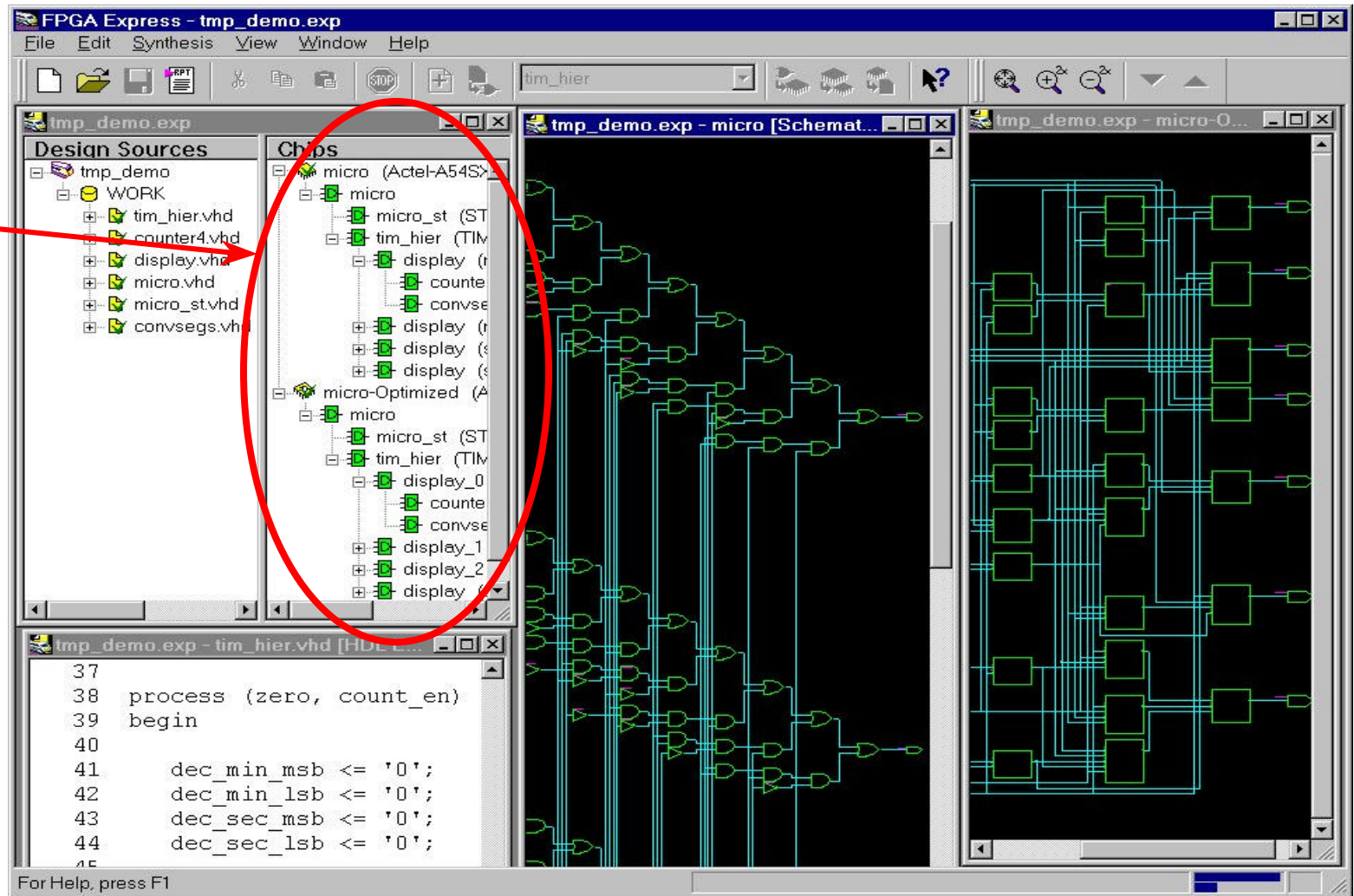


# Critical Path Analysis Tools

RTL/Gates

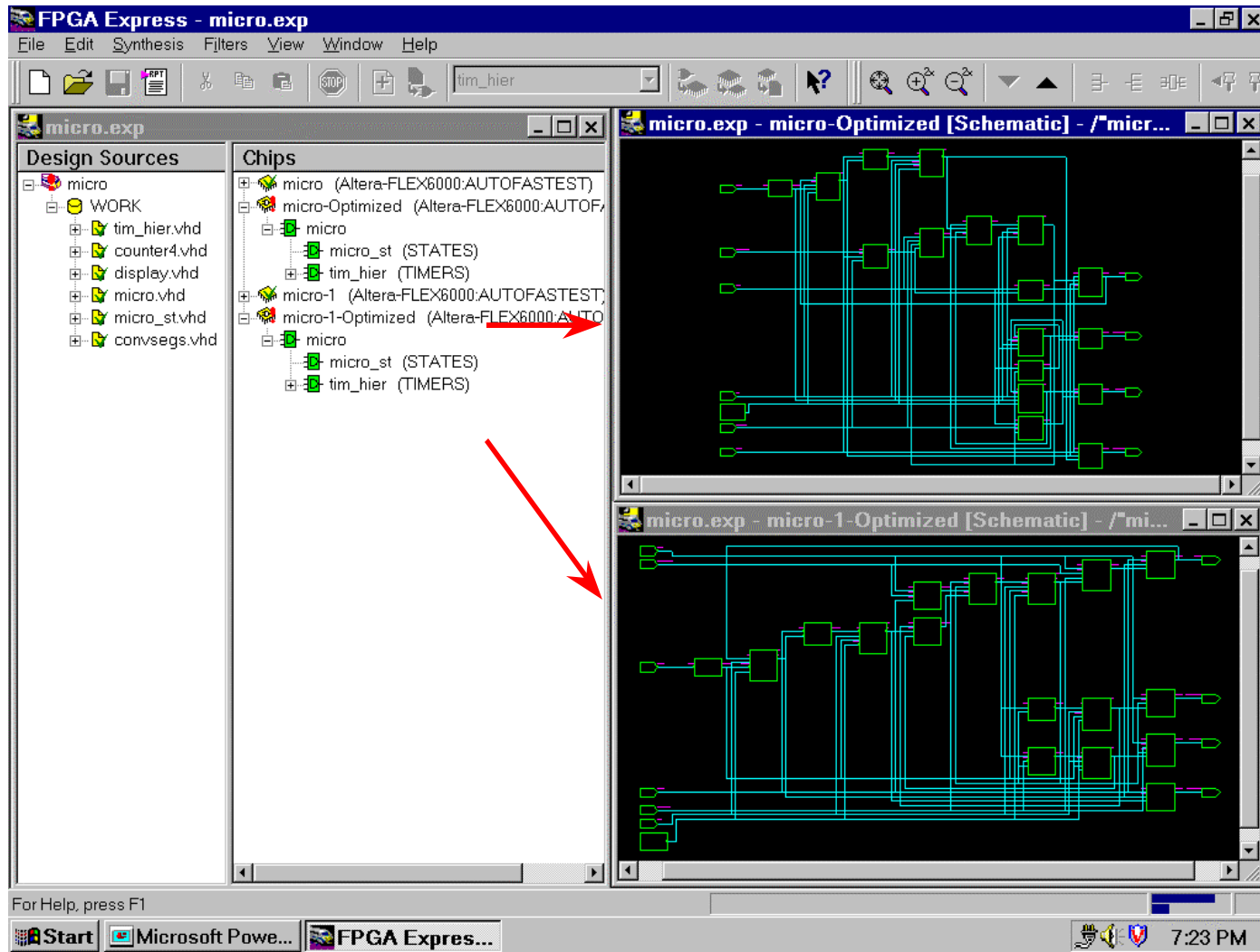
LUTs

Navigate via  
Hierarchy  
Browser  
or via  
Schematic





# Explore Design Alternatives

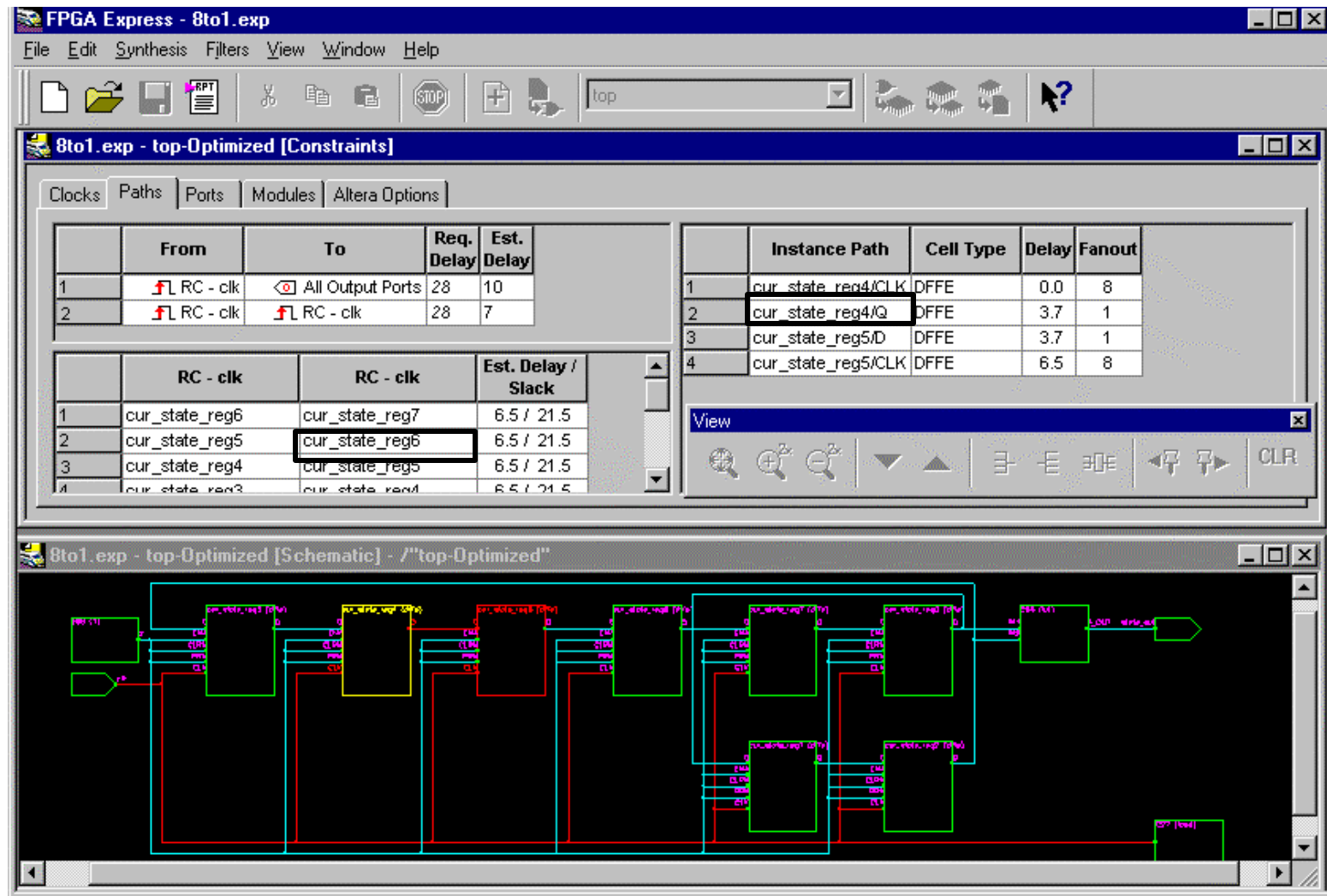


“Speed”

“Area”

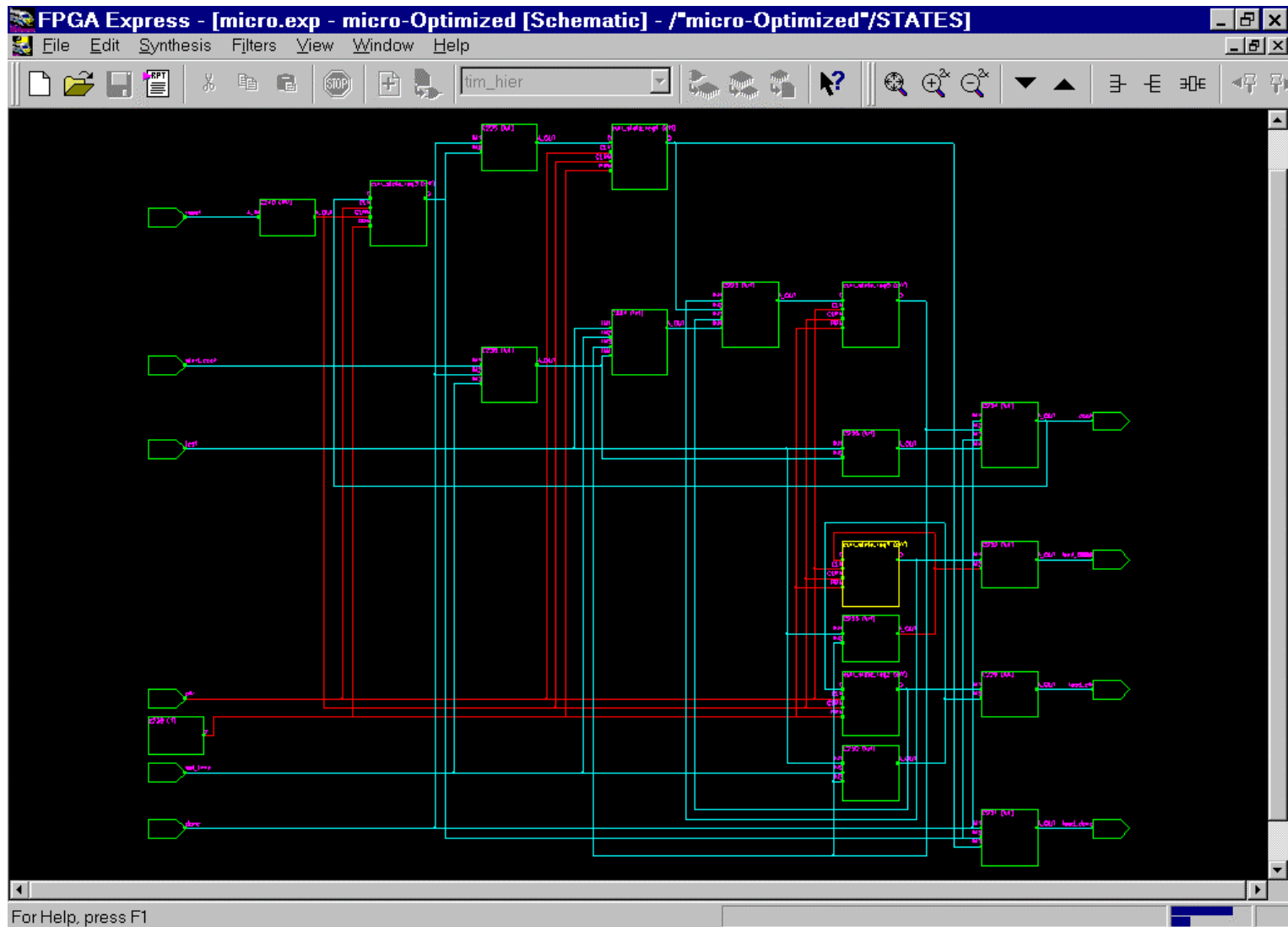


# Critical Path Analysis with VISTA





# Fan-in Analysis



Response	Percentage
Yes	78%
No	18%
Don't know	4%

