Advanced HDL Design Training On Xilinx FPGA

Speaker : Elmer Chiang

Xilinx Taiwan

Chapter 1

FPGA *Express* v3.3

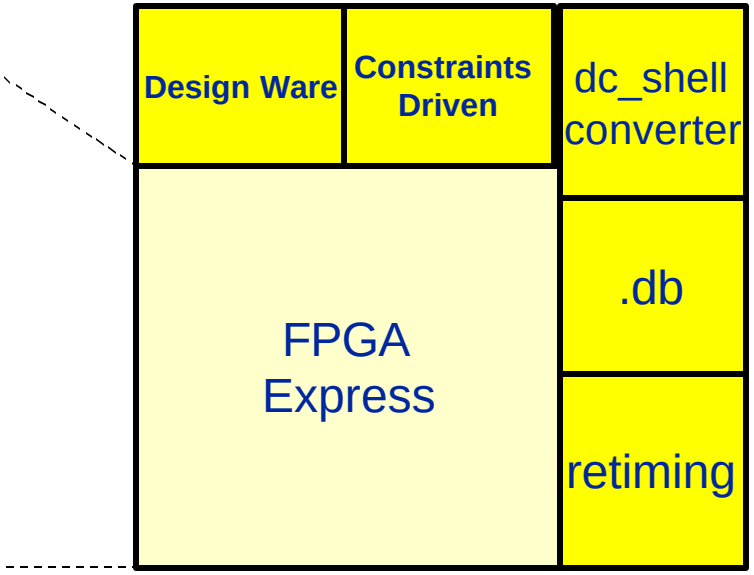
Overview

What is FPGA Express and Compiler II?

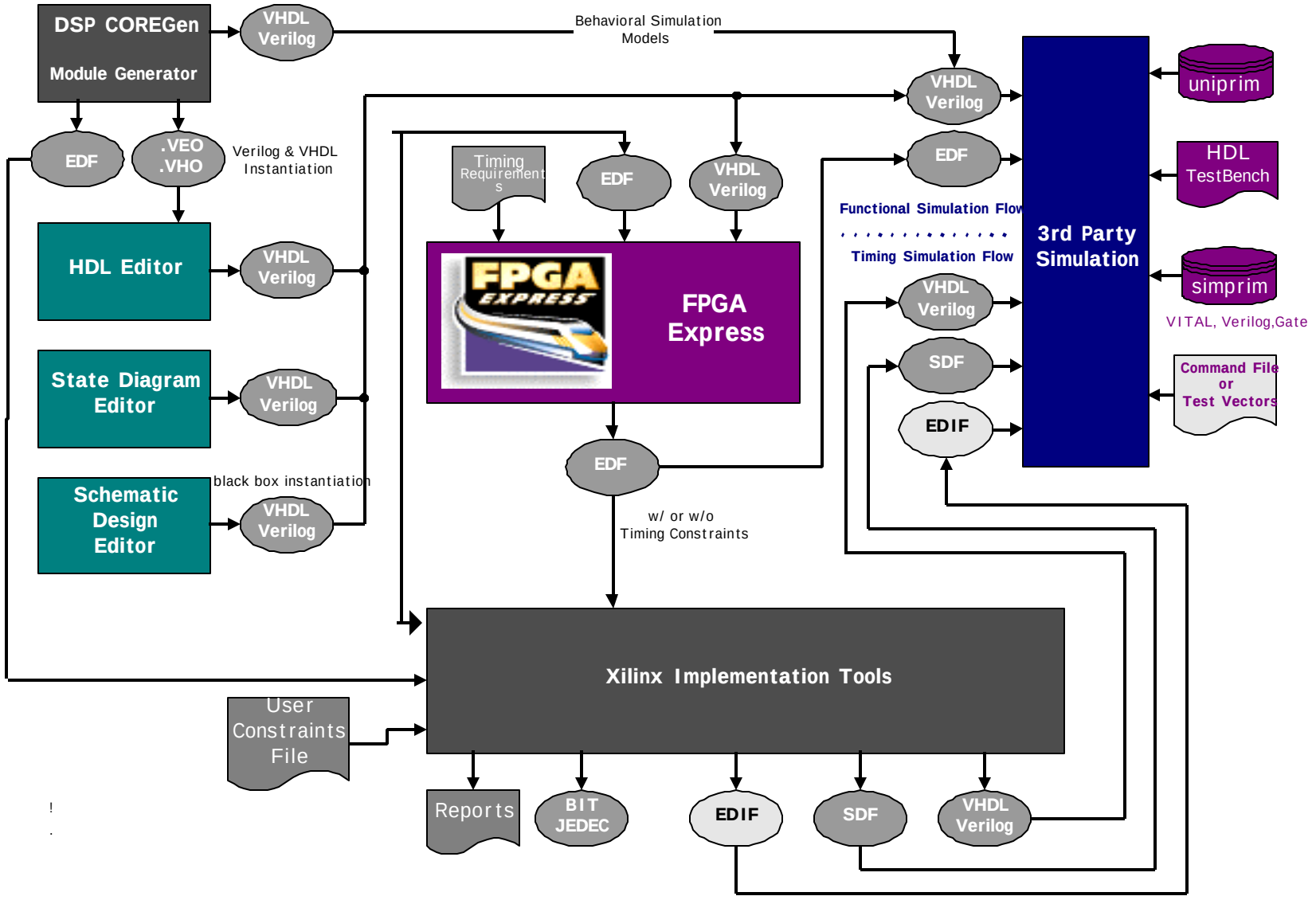
FPGA Express

- Push-Button Flow
- Industry-Standard HDLs
- Industry-Leading QoR
- Built-In Static Timing Analyzer
- Schematic Viewer
- Integration with P&R tools

FPGA Compiler II



FPGA Express Flow



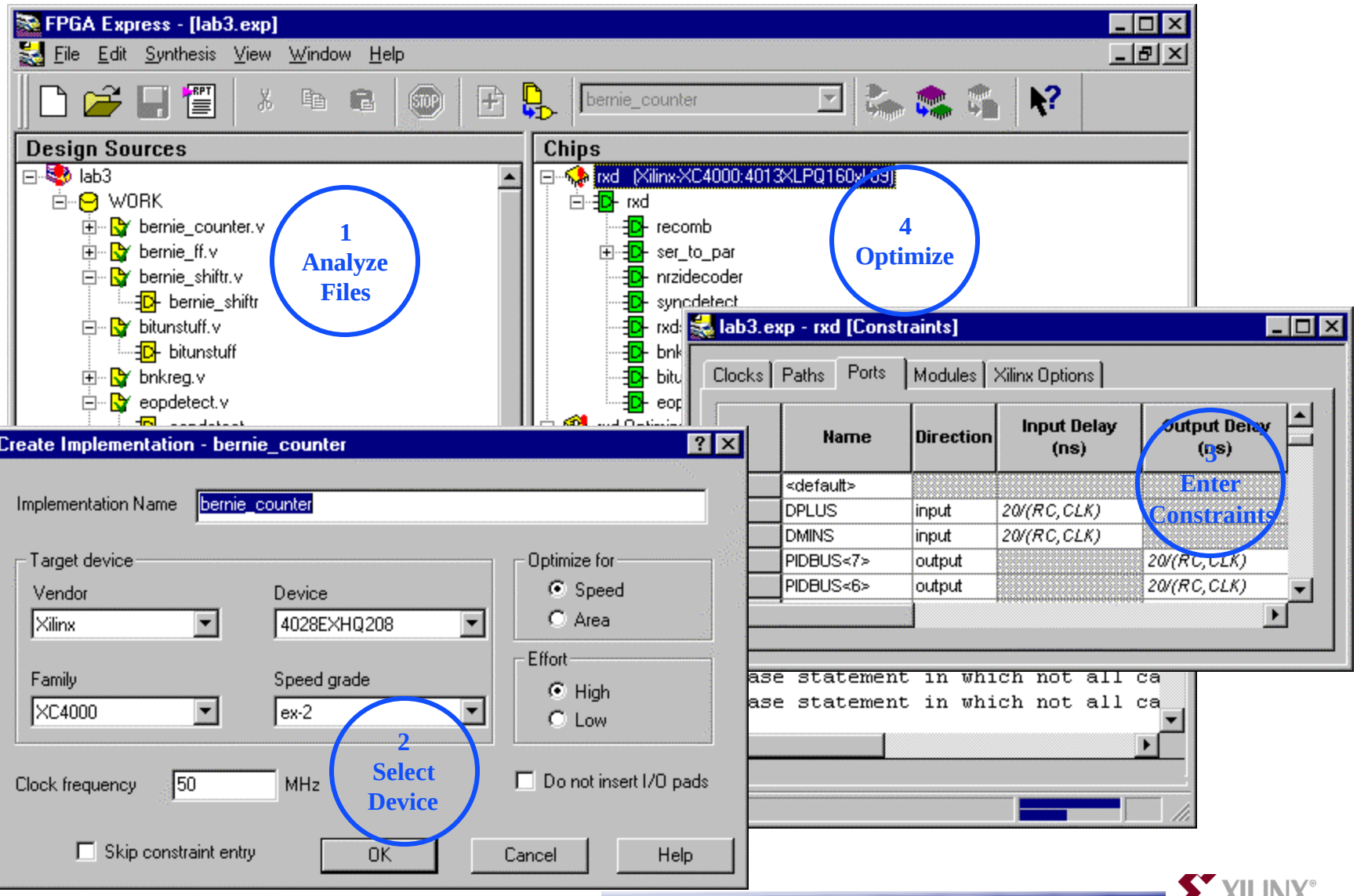
FPGA Express Features ...

- FPGA Express Technology
  - Constraint Entry GUI
  - Automatic I/O Pad and Global Signal Mapping
  - Built-in Timing Analyzer
  - Built-in Module Generation (Fast Carry, RLOC)
  - Resource Sharing
  - Hierarchy Control
  - Schematic Viewer called Vista

What's New in Express v3.3

- dont_touch
  - instructs Express to not re-optimize instantiated modules
  - available via Constraint GUI, HDL attribute, script command in FE_SHELL
- Virtex architectural support additions
  - SRL16 inference
  - ROM inference

Simple Four Step Design Process



Constraint Entry ...

- Synthesis -> Edit Constraints...

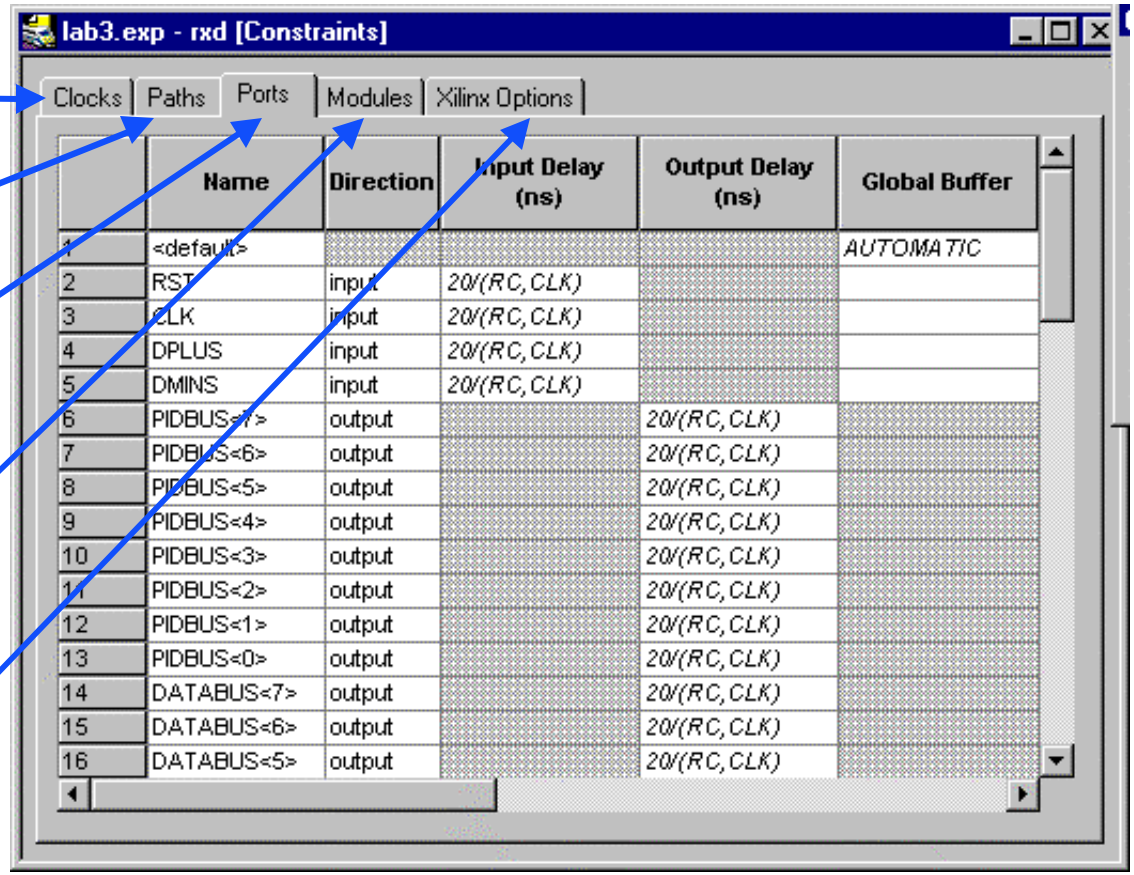
Define Clocks
PERIOD / RISE / FALL

Define Time Constraint
FROM : TO
Sub-Paths

Define Port Attributes
DELAY
PULLUP / PULLDOWN
SLEW / Global Buffers
Pin Locations

Define Hierarchy Preservation
Eliminate / Preserve
Operator Sharing
Optimize / Effort

Xilinx Constraints
Implementation Tool Target
GSR Usage



How are the Constraints used?

- FPGA Express passes the constraints to the output .NCF file
- The exact value of the timing constraint is not directly used for synthesis optimization
  - Speed or Area selection under constraint editor's module tab is used for selecting the type of optimization to perform on the sections of the design
- FPGA Express creates Xilinx recommended constraints:
  - Periods and Offsets for global constraints
  - FROM:TO for fast, slow, or multi-cycle paths

Hierarchy Specification

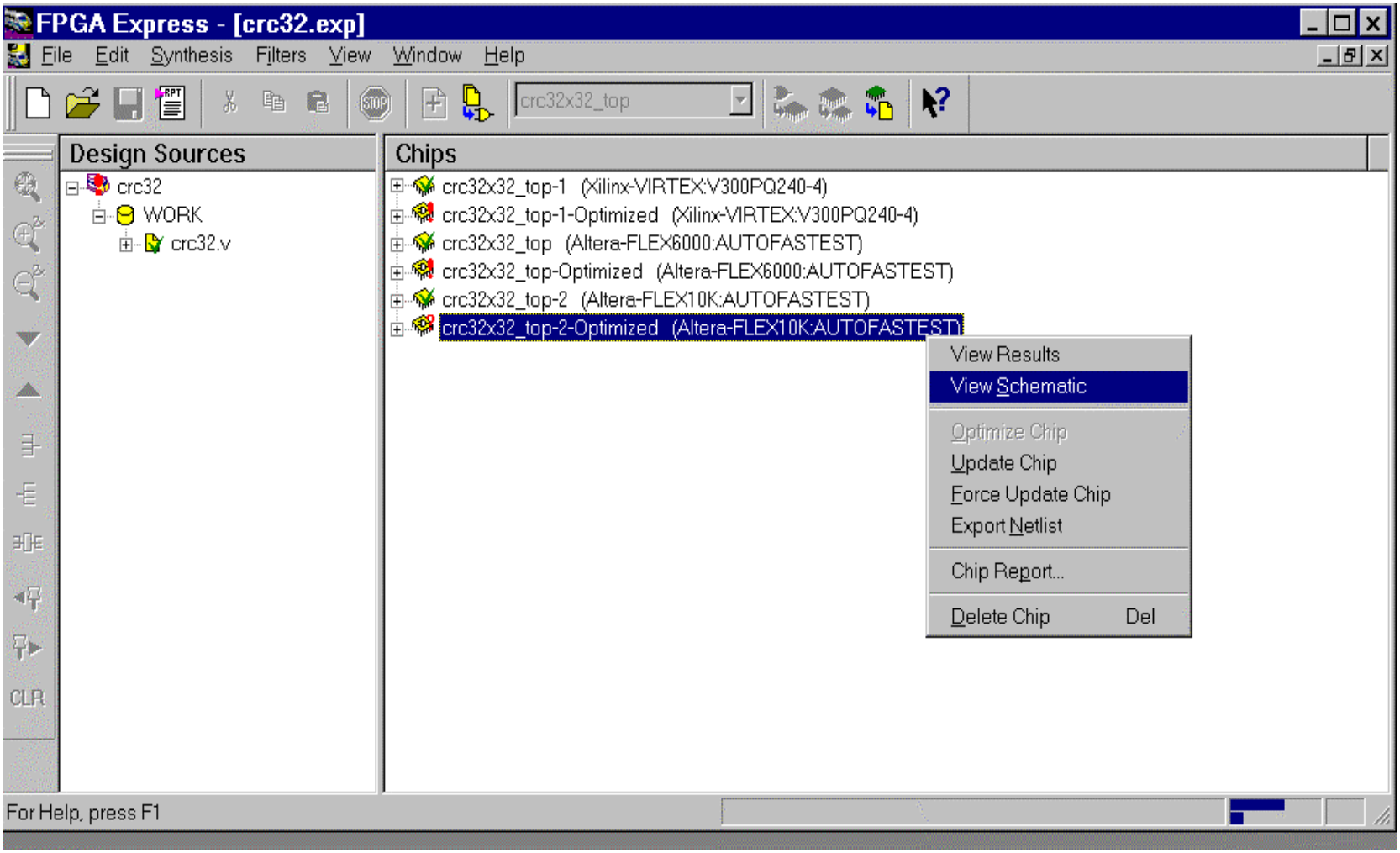
- The module view lets the user “See” the design hierarchy
- Hierarchy Control is available you can preserve or eliminate level of hierarchy from optimization
- Operator Sharing, Speed/Area, Effort
- Primitive Control

micro.exp - top_xilinx_4005-Optimized [Constraints]

Clocks | Paths | Ports | Modules | Xilinx Options

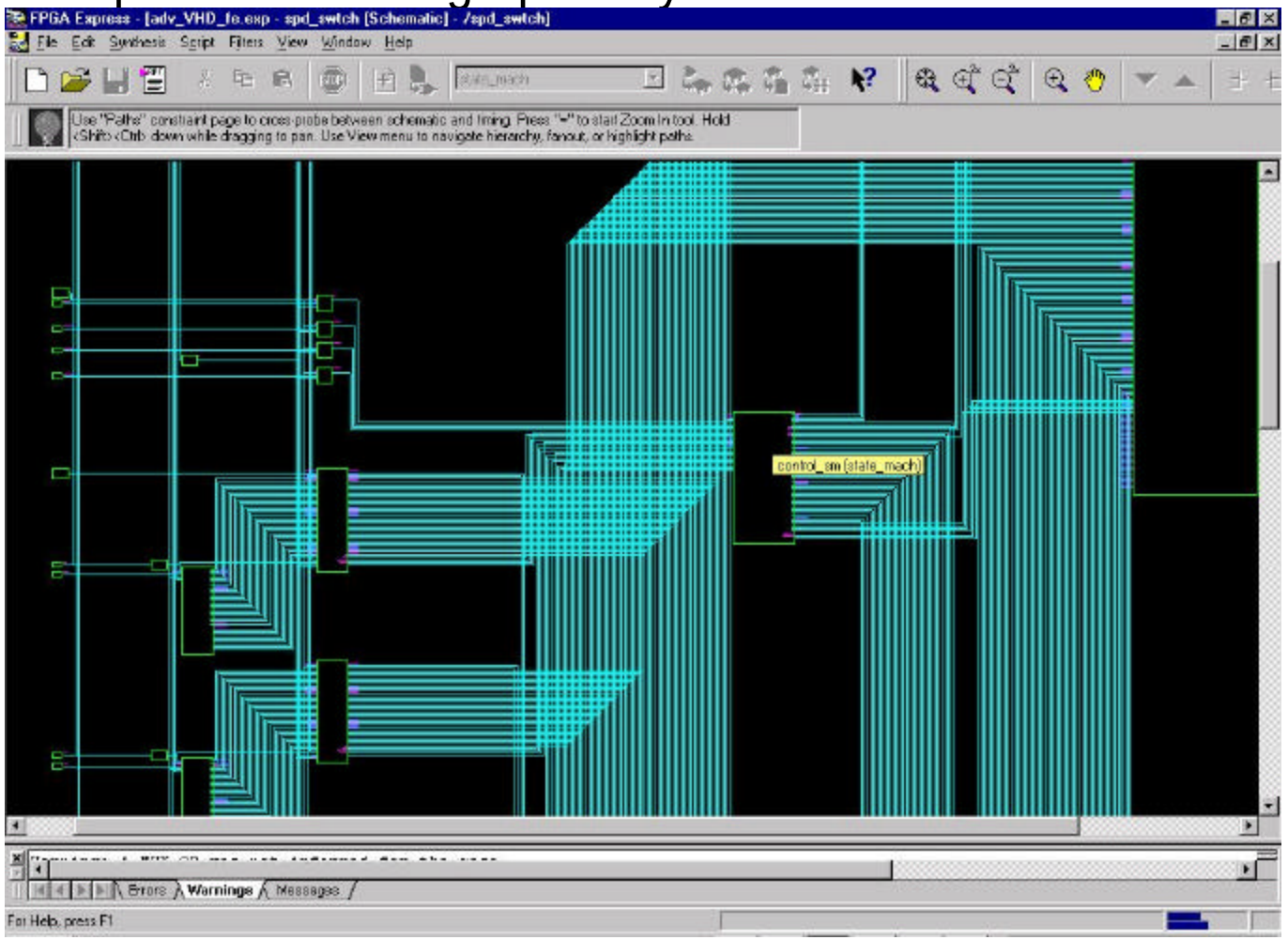
	Name	Hierarchy	Primitives	Operator Sharing	Optimize for	Effort	Area	Flip Flops	Latches
1	<default>	Preserve	Preserve	On	Speed	High			
2	top						62	20	0
3	alu – i						37	5	0
4	sw7 – xsw7						?	0	0
5	stack0 – xstack0						?	0	0
6	debounce – xdebounce						2	3	0
7	seg7dec – xseg7dec						7	0	0
8	control – xcontrol						16	5	0
9	statmach – xstatmach						14	3	0
10	calc_st – xcalc_st						2	3	0
11	count2ed – adr_count						2	2	0

Invoking the Schematic Viewer



Schematic Viewer: Vista

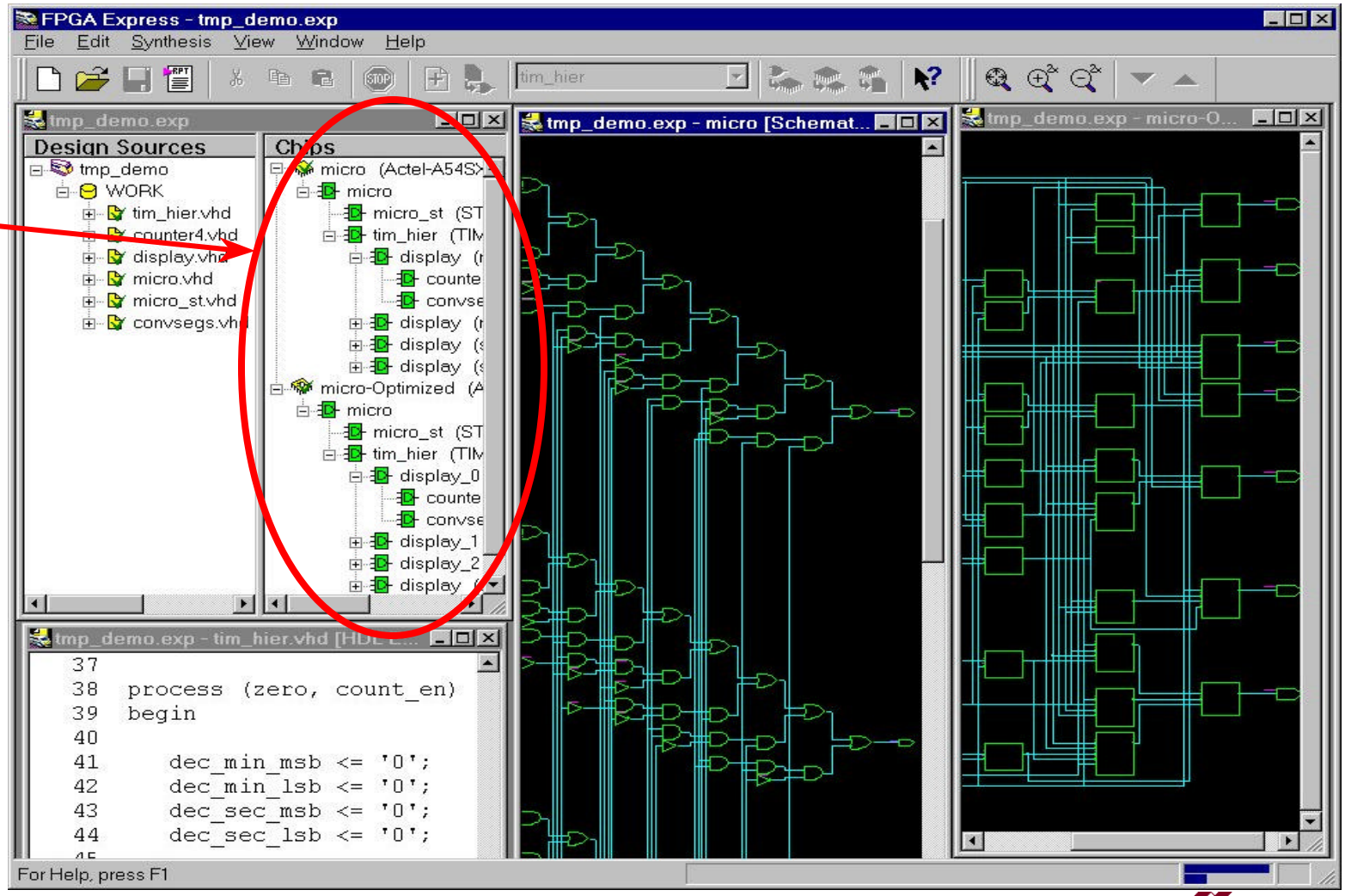
- The “Vista” Schematic Viewer allows you to see what FPGA express has built graphically



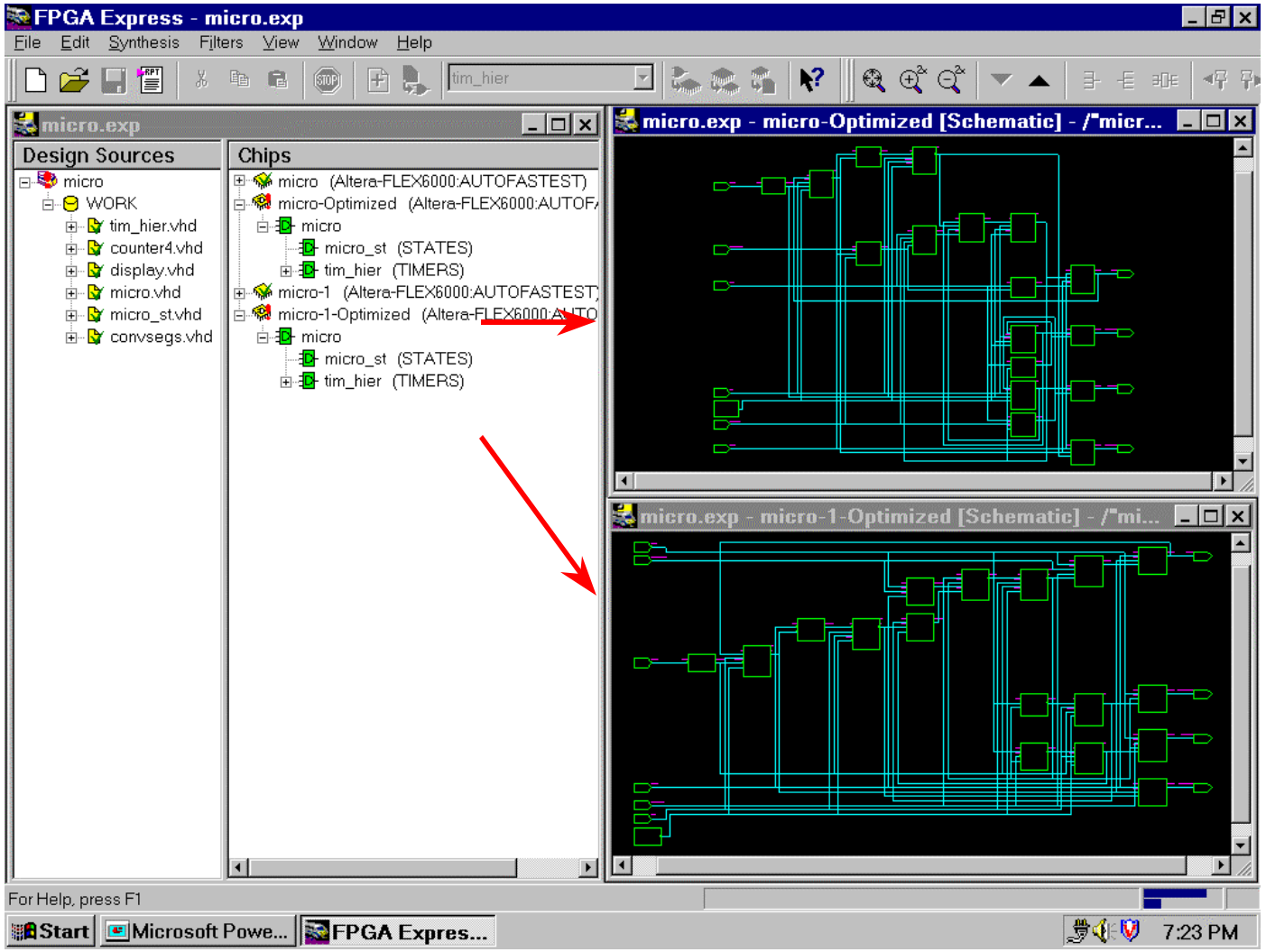
Critical Path Analysis Tools

RTL/Gates LUTs

Navigate via Hierarchy Browser or via Schematic



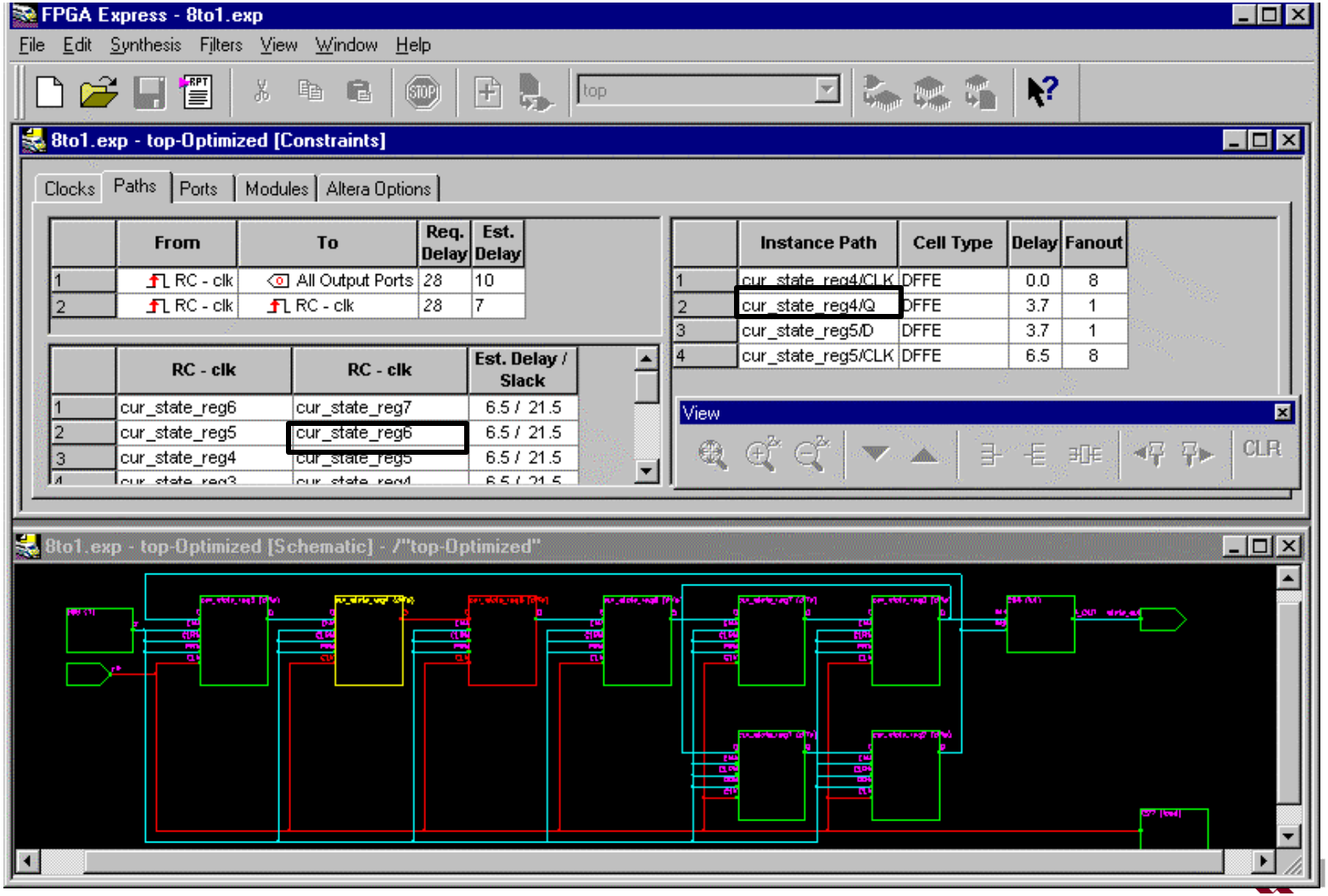
Explore Design Alternatives



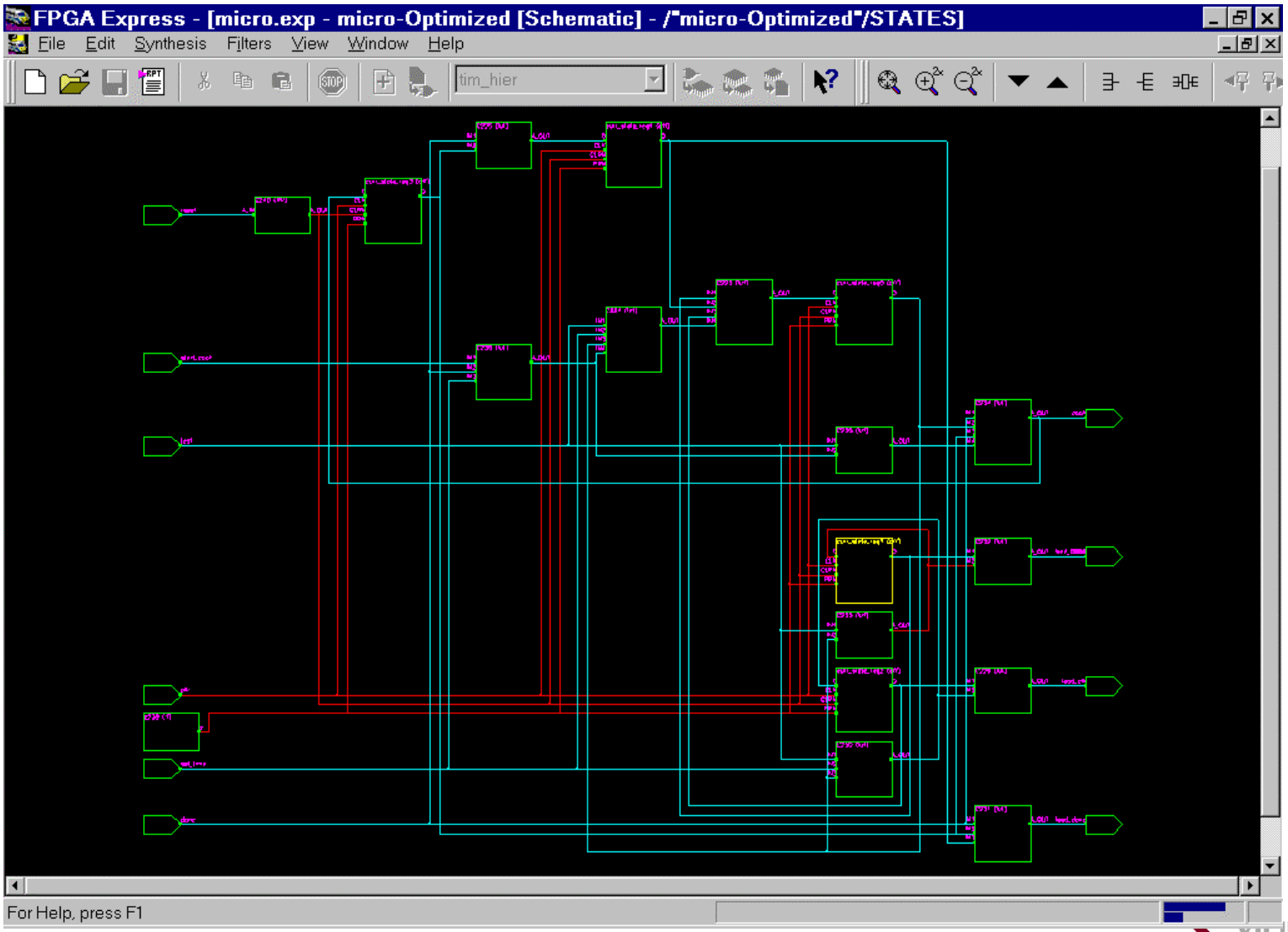
"Speed"

"Area"

Critical Path Analysis with VISTA



Fan-in Analysis



Fan-out Analysis