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APPLICATION NOTE

BI3101A CCFL BackLight Controller IC

Version 1.00

Jul. 25, 2001

Contents:

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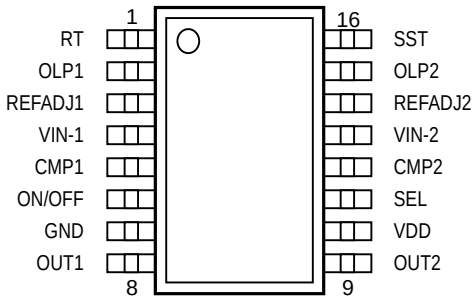
1. General Description

Features:

- Dual PWM Modulators
- Dual Independent Open Lamp Protection
- On/Off control
- Flexible Dimming Scheme
- Internal UVLO (Under Voltage Look Out) function
- CMOS Totem Pole output
- NMOS output driving
- SOP Packing



Pin Description:

Pin No.	Names	I/O	Description
1	RT		Operation frequency control
2	OLP1		A voltage sense input pin. If voltage level is less than 325 mV after a user defined period of time, the chip will shut down the OUT1 and PWM_1. A digital latch circuit latches this result. The latch condition will be released if the power be turned off and on again or disable the chip by setting the ON/OFF pin to off state.
3	REFADJ1		PWM_1 controller input, reference level adjustment pin of the error amplifier_1.
4	Vin-1		PWM_1 controller input, the inverting input of the error amplifier_1
5	CMP1		PWM_1 controller input, the output of the error amplifier_1
6	ON/OFF		Enable and disable Control. The chip only consumes the leakages current when it is disable. A ~ 80Kohm pull down resistor is integrated internally.
7	GND		Ground
8	OUT1		PWM_1 output, high active for driving NMOS load.
9	OUT2		PWM_2 output, high active for driving NMOS load.
10	VDD		Supply voltage
11	SEL		Soft -Start selection, a ground SEL makes BI3101A works as the same as BI3101. An internal pull-high resistor is integrated internally. A long period and programmable soft start control scheme is selected via floating SEL.
12	CMP2		PWM_2 controller input, the output of the error amplifier_2
13	Vin-2		PWM_2 controller input, the inverting input of the error amplifier_2
14	REFADJ2		PWM_2 controller input, reference level adjustment pin of the error amplifier_2.
15	OLP2		A voltage sense input pin. If voltage level is less than 325 mV after a user defined period of time, the chip will shut down the OUT2 and PWM_2. A digital latch circuit latches this result. The latch condition will be released if the power be turned off and on again or disable the chip by setting the ON/OFF pin to off state.
16	SST		The delay timer for enabling open lamp protection

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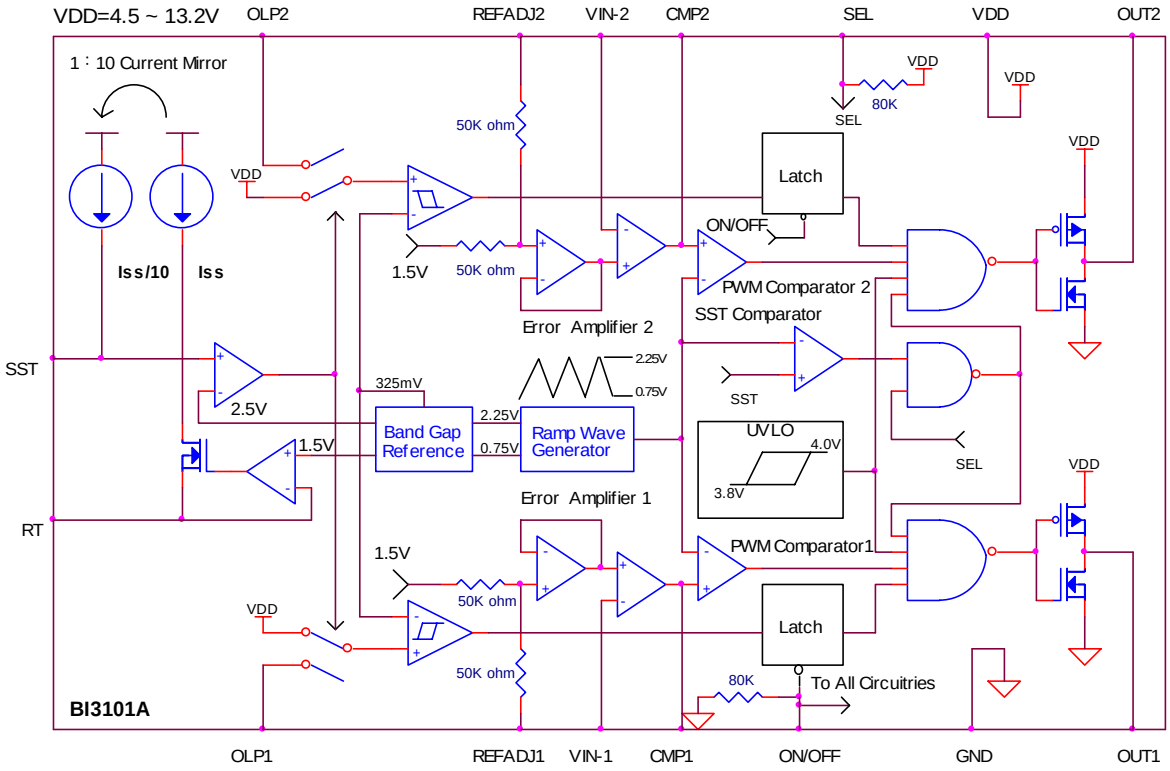
2. Functional Block Diagram



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3. DC/AC Characteristics

Parameter	Test Conditions	Min.	Typ.(Limits)	Max.	Unit
Reference Voltage					
Output voltage	Measure Vin+	1.425	1.5	1.575	V
Line regulation	VDD=4.5 ~ 13.2 V		2	20	mV
Under Voltage Look Out					
Upper threshold voltage	Ta=25℃	3.8	4	4.2	V
Hysteresis		0.1	0.2	0.3	V
Ramp Wave Generator					
Frequency	R_T=100K Ω	120	140	160	KHz
Operating Frequency	note 1	50		250	KHz
Output peak			2.25		V
Output valley			0.75		V
Error Amplifier					
Input voltage	note 1	0.75		2.25	V
Open loop gain		60	80		dB
Unit gain band width		1	1.5		MHz
SST Soft Start and Open Lamp Enable					
Output current	VDD=12V, Ta=25℃		1.5V/R_T		uA
Open lamp detection enable			2.5		V
Open Lamp Protection					
Open lamp detection lower threshold	VDD=12V, Ta=25℃		325		mV
Hysterisis			50		mV
Output					
CMOS output impedance	note 1		50		Ω
Rising Time	1000pF load,		110		ns
Falling Time	note 1		100		ns

Ta : ambient temperature.

Note 1: It is guaranteed by design not 100% tested.

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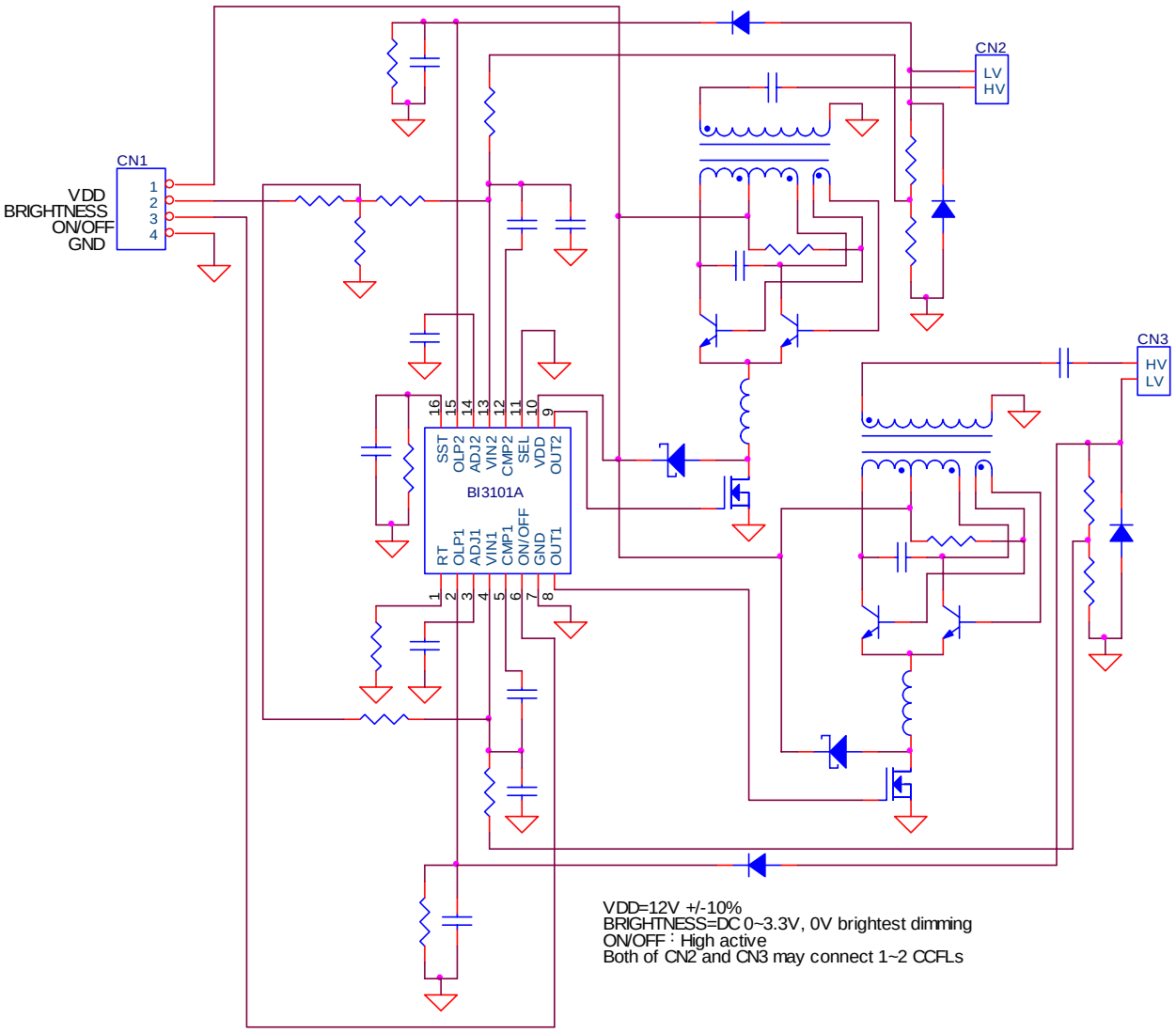
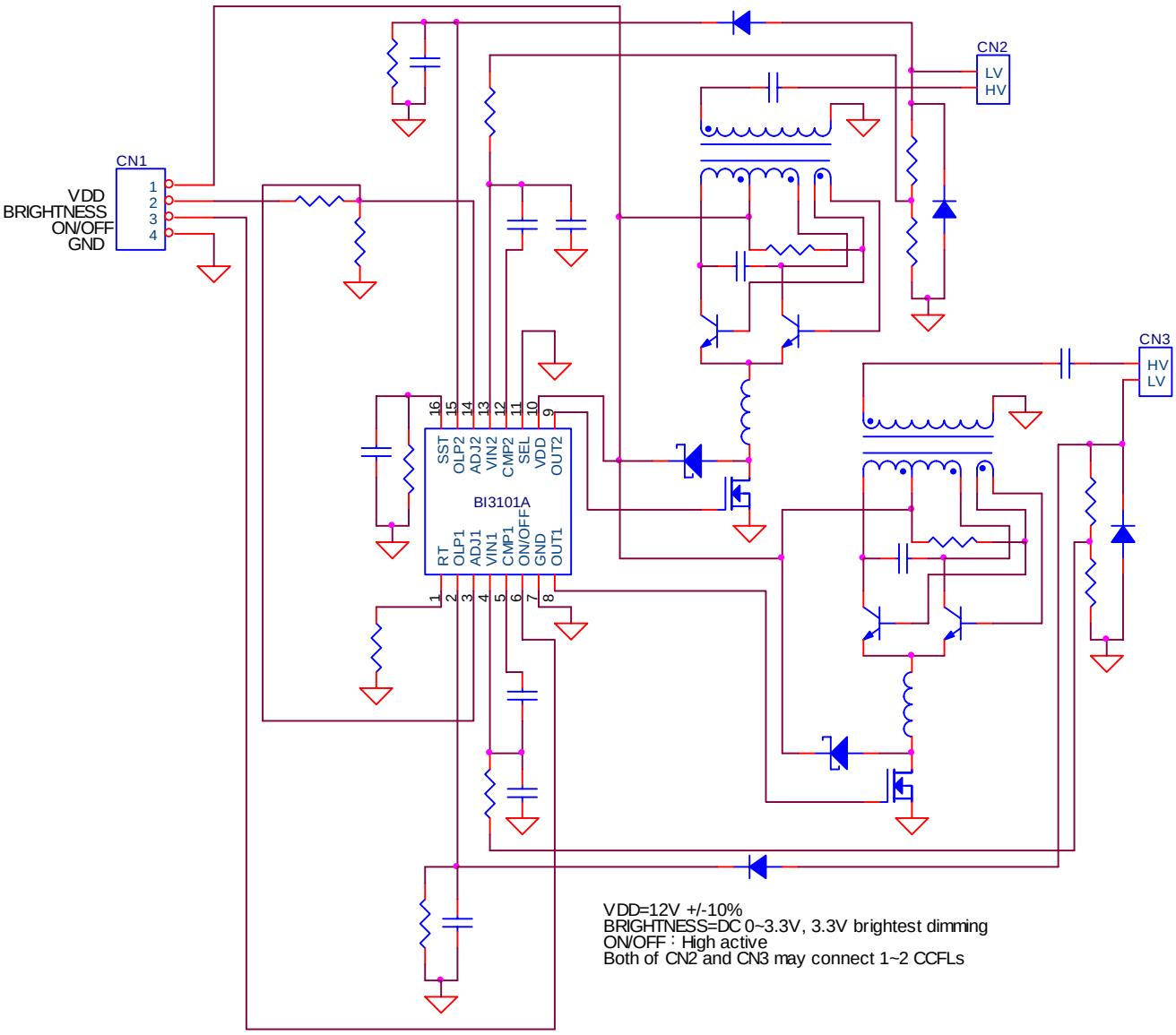
4. Application Information

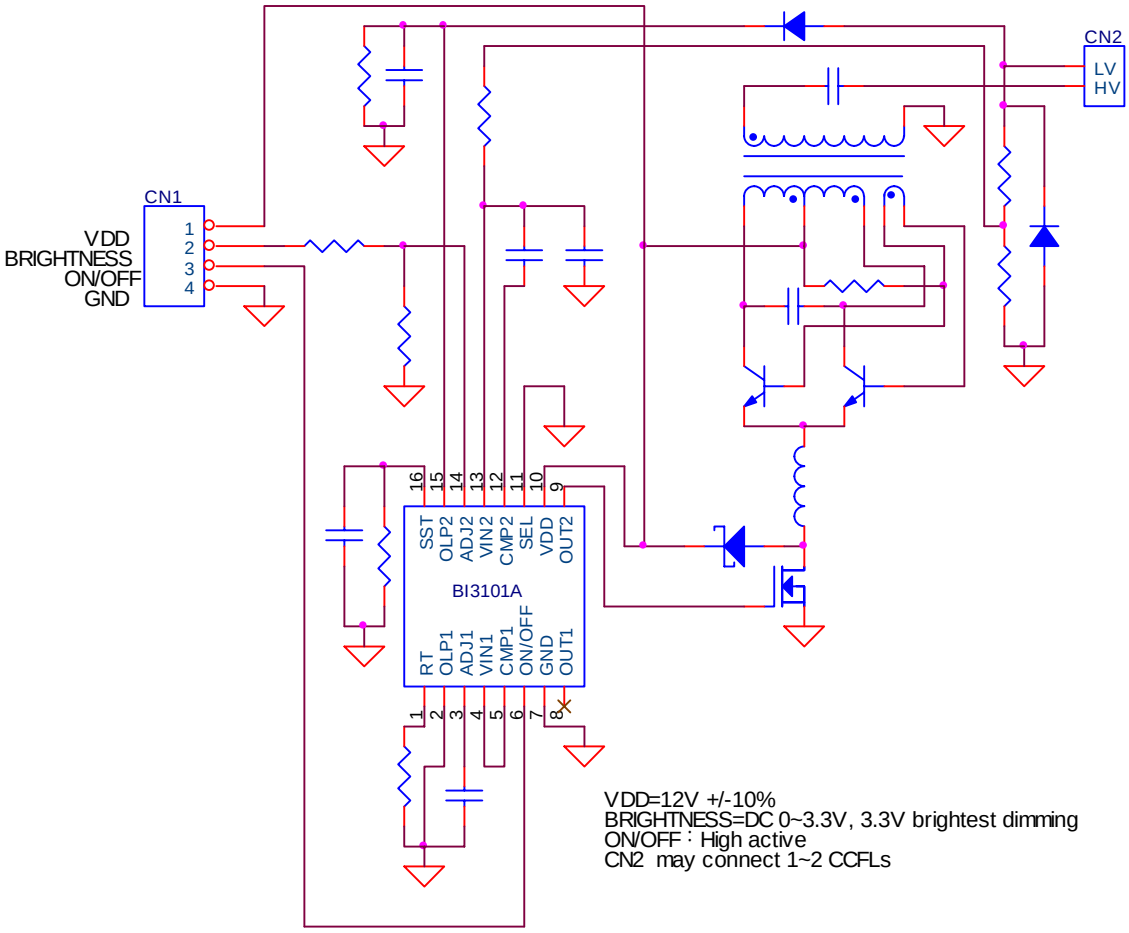
Example1: This is a typical design for 2 to 4 lamps system. ON/OFF control can turn off the lamps without shout the VDD down .



Example2: This is a different dimming scheme from Example 1, zero-volt-most-dark.



Example3: The independent design of open lamp protection makes BI3101A can used as a single PWM controller without consuming the extra power. A force-to-GND connection of OLP pin will shut down the circuit of PWM. This is an example of BI3101A operates as a single PWM modulator.



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5.Design Example

	ITEM	CONDITION	SPECIFICATION			UNITS
			MIN	TYP	MAX	
●	INPUT VOLTAGE	Ta = 25℃	10.8	12.0	13.2	Vdc
●	LAMP CURRENT/ CCFL	12V, Ta = 25℃	8.0	8.3	8.6	mArms
	(Vadj = 0V)					
●	FREQUENCY	12V, Ta = 25℃	40	42	44	KHz
●	OPEN OUTPUT	12V, Ta = 25℃, R = ∞	LATCH OFF			Vrms
●	LAMP CURRENT/ CCFL	12V, Ta = 25℃	2.0	2.3	2.6	mArms
	(Vadj = 5V)					
●	LAMP VOLTAGE	12V, Ta = 25℃	*	580	*	Vrms
●	OPEN VOLTAGE	12V, Ta = 25℃	1800	*	*	Vrms

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(1) Lamp Striking and Transformer:

The striking voltage is dependent on supply voltage and the turn ratio (TR) of transformer as following described.

$V_{STRIKE, rms} \leqq \pi * VDD_{(min.)} * TR / 2^{0.5}$

So, $TR \geq 2^{0.5} * V_{STRIKE, rms} / (\pi * VDD_{(min.)})$

In this case, $V_{STRIKE, rms} = 1800V_{rms}$, $VDD_{(min.)} = 10.8V$.

So, $TR_{(min.)} = 75$

The maximum power consumption of lamp is,

$V_{lamp} * I_{lamp} = 580V * 8.3mA = 4.814W$

(2) Setting the CCFL Striking Period:

The IC will monitor the OLP pin after the specified CCFL striking period. According the design of IC, the period is set as following equation,

$T_{STRIKE} = 16.67 * R_T * C_{SSt}$

Where $Iss = V_{RT} / (R_T * 10)$, $V_{RT} = 1.5V$

In this case, $R_T = 100Kohm$, $C_{SSt} = 1uF$

$T_{STRIKE} = 1.667sec$

(3) PWM Frequency Control Resistor R_T:

The frequency of PWM of IC BI3101A could be controlled as

F_{PWM} (KHz) = 14000 / R_T (Kohm)

A 100 Kohm R_T resistor is selected for this case. It results a 140KHz PWM frequency.

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(4) Ballast Capacitor:

In many practical designs, for minimizing current distortion caused by the non-linear behavior of the lamp, $V_{C(BALLAST)}$ is set to be around 1.5~ 2 times of V_{LAMP}. It means,

$V_{C(BALLAST)} = I_{LAMP} / (2 * \pi * F_{LAMP} * C_{BALLAST}) = k * V_{LAMP}$, k = 1.5 ~ 2

In this case, $I_{LAMP, typ}$ = 8.3mA, F_{LAMP} = 42KHz, V_{LAMP} = 580Vrms. A 33pF of capacitance makes a 1.7 times of lamp voltage drops on $C_{BALLAST}$ capacitor.

Smaller the $C_{BALLAST}$ will make more linear the lamp operation.

(5) Resonant Capacitor:

The primary and secondary circuits determine the resonant frequency of the Royer oscillator. When lamp voltage is low, a lower resistance load makes the resonance frequency very close to equation below

$F_{LAMP} = 1 / (2 * \pi * (Lp * (C_{RESONANT} + (TR^2 * C_{BALLAST})))^{0.5})$

In this case, assume Lp = 34uH, TR = 75, $C_{BALLAST}$ = 33pF, F_{LAMP} = 42KHz

Then 0.22uF $C_{RESONANT}$ induces a 42.879KHz oscillation.

(6) Transformer Wire Loss:

The current flow through the resistive transformer consumes power. The current of the primary I_{PRI} is

$V_{PRI} = V_{SEC} / TR$

And $V_{SEC} = ((V_{C(BALLAST)})^2 + (V_{LAMP})^2)^{0.5}$

The impedance of resonance tank is

$Z_{TANK} = (Lp / C_{RESONANT})^{0.5}$

Then $I_{PRI} = V_{PRI} / Z_{TANK} = ((V_{C(BALLAST)})^2 + (V_{LAMP})^2)^{0.5} / (TR * (Lp / C_{RESONANT})^{0.5})$

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In this case, I_{LAMP} = 8.3mA, V_{LAMP} = 580V, $C_{BALLAST}$ = 33pF, TR = 75, Lp = 34uH, $C_{RESONANT}$ = 0.22uF and F_{LAMP} = 42KHz

We obtain V_{SEC}=1116V, Z_{TANK}=12.43 ohm and I_{PRI} = 1.2A.

Then Transformer wire Loss = I_{PRI}^2 * Rp

(7) Buck Inductor:

If we consider the buck stage which works in continuous conduction mode and the NMOS transistor turn on time is t_{on} and turn off time is $t_{off,}$ then

V_{BUCK} * t_{on} = (VDD - V_{BUCK} + V_D) * t_{off}, where V_D is the voltage drop on the diode.

If t_{on} + t_{off} = T, then

(VDD -$V_{BUCK, ave}$ + V_D) / $V_{BUCK, ave}$ = t_{on} / (T - t_{on})

The maximum ripple occurs when PWM operating frequency and duty cycle are the minimum; VDD and lamp current are maximum.

The average buck voltage at maximum lamp current is

$V_{BUCK, ave}$ = VDD - V_{SEC} * $2^{0.5}$ / (TR * π)

In this case, VDD (max)=13.2V, V_{SEC} = 1116V, TR=75
And if we set PWM frequency = 140KHz

If V_D=0.6V, then the NMOS turn on time = 3.8 us

The resulted ripple current is
I_{RIP} = ton * $V_{BUCK, ave}$ / L1

Usually, a less than 50% ripple is required for buck design. In this case $I_{BUCK, rms}$=0.87A, so, the maximum ripple is ~ 400mA. It can be found the minimum L is 60uH. So, a 100uH inductor is selected for the buck stage.

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(8) Lamp Current Control and Dimming:

In this design example,

V_{ADJ} = 5V, then I_{LAMP} = 2.3 mA.

V_{ADJ} = 0V, then I_{LAMP} = 8.3 mA

So, if V_{ADJ} = 1.5V, then I_{LAMP} = 6.5 mA

In this case, we set V_{REF} = 1.5V

then the lamp current is

$I_{LAMP} = (V_{REF} + 0.5 * V_D) * \pi / (2^{0.5} * R_L)$, where V_{REF} = 1.5V and V_D = 0.7V

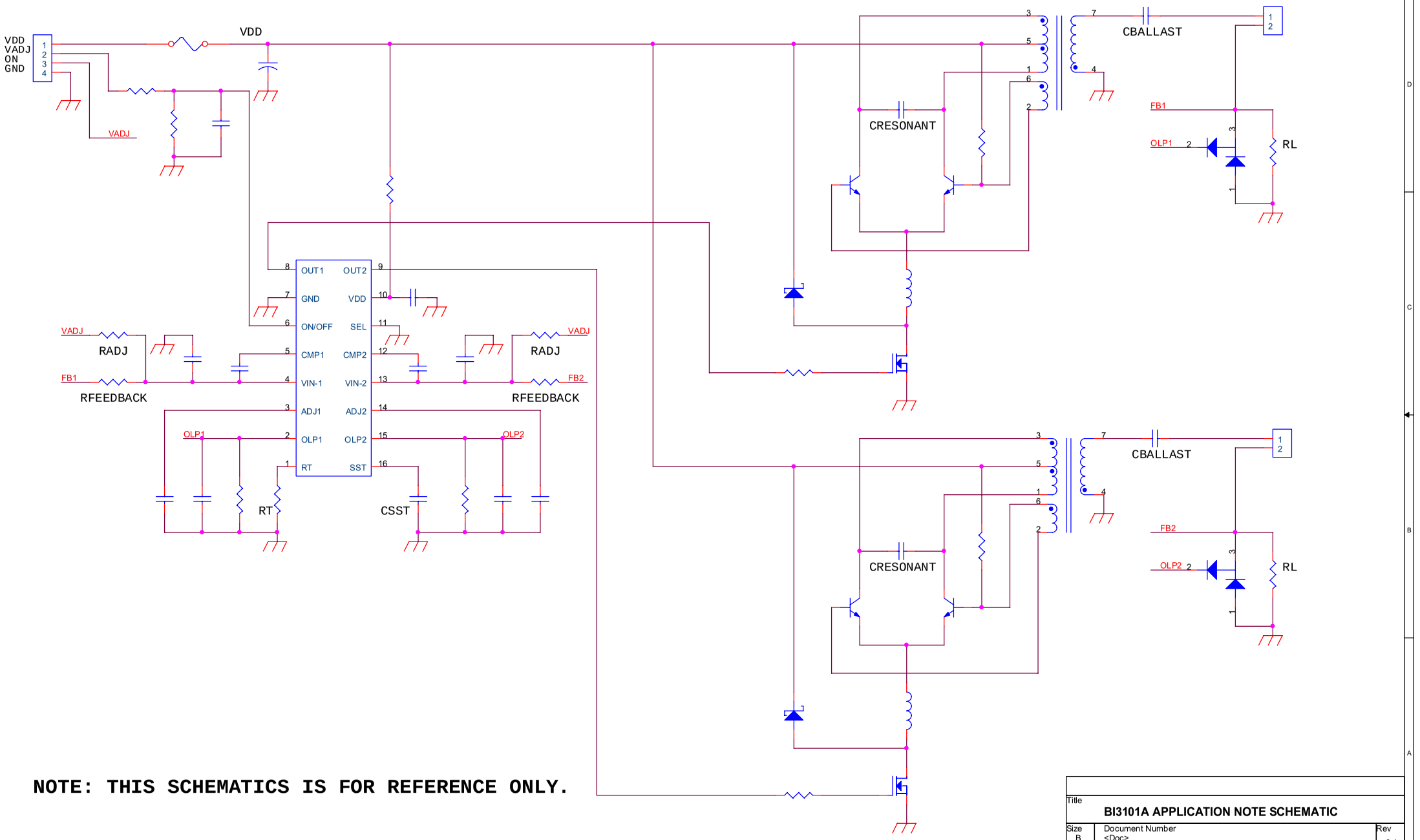
We can obtain R_L = 660 ohm

By using equation

$I_{LAMP} = (V_{REF} (R_{FEEDBACK} + R_{ADJ}) – V_{ADJ} * R_{FEEDBACK} + 0.5 * V_D * R_{ADJ}) * \pi / (2^{0.5} * R_L * R_{ADJ})$

where R_L = 660 ohm, V_{ADJ} = 5V => I_{LAMP} = 8.3 mA and V_{ADJ} = 0V => I_{LAMP} = 2.3 mA

So, if $R_{FEEDBACK}$ = 33K ohm then R_{ADJ} = 100K ohm



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