

Regulating Pulse Width Modulators

FEATURES

- Undervoltage Lockout with Hysteresis
- *Guaranteed* 1% 5.1V Reference
- *Guaranteed* 10mV/1000 Hr Long Term Stability
- Latching PWM
- 8V to 35V Operation
- 100Hz to 400kHz Oscillator
- 400mA Source and Sink Current

APPLICATIONS

- Switching Power Supplies
- Motor Speed Control
- Power Converters

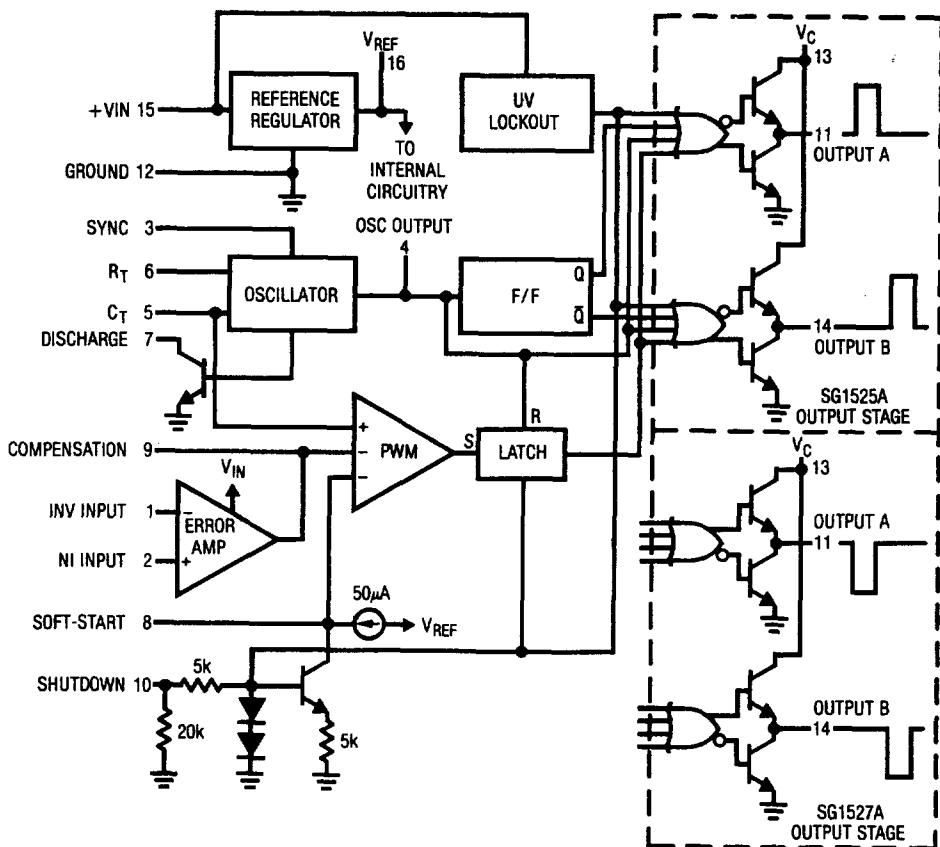
DESCRIPTION

The LT1525A and LT1527A are improved general purpose switching regulator control circuits. Included on the chip are a trimmed 1% voltage subsurface zener reference, oscillator, comparator and high current class B totem pole output drivers. Included in the design of the LT1525A are easy synchronization to an external clock, soft-start and adjustable deadtime control. A shutdown pin allows instantaneous shutdown.

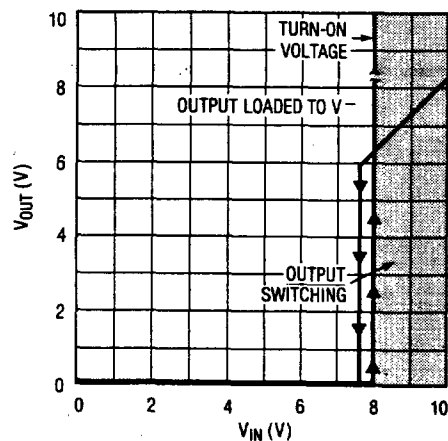
The LT1525A and LT1527A differ only in their output logic phasing. The LT1525A has a low output during the "off" state, while the LT1527A has a high output during the "off" state. Both devices have undervoltage lockout with about 0.5V hysteresis, giving reliable operation even with slowly varying supplies.

The combination of improved features and advanced processing for high reliability make Linear Technology's switching regulators a supreme choice.

BLOCK DIAGRAM



LT1525A Start-Up

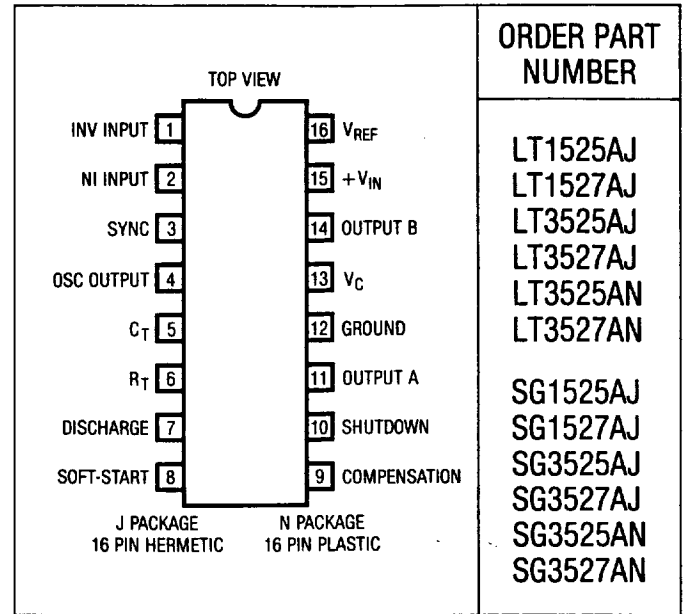


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage ($+V_{IN}$)	+40V
Logic Inputs	-0.3V to +5.5V
Analog Inputs	-0.3V to $+V_{IN}$
Output Current, Source or Sink	500mA
Reference Output Current	50mA
Oscillator Charging Current	5mA
Power Dissipation at $T_A = +25^\circ\text{C}$ (Note 2)	1000mW
Thermal Resistance: Junction to Ambient	100°C/W
Power Dissipation at $T_C = +25^\circ\text{C}$ (Note 3)	2000mW
Thermal Resistance: Junction to Case	60°C/W
Operating Temperature Range	
1525A, 1527A	-55°C to 150°C
3525A, 3527A	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

PACKAGE/ORDER INFORMATION



RECOMMENDED OPERATING CONDITIONS

(Note 4)

Input Voltage ($+V_{IN}$)	+8V to +35V	Reference Load Current	0mA to 20mA
Collector Supply Voltage (V_C)	+4.5V to +35V	Oscillator Frequency Range	100Hz to 400kHz
Sink/Source Load Current (Steady State)	0mA to 100mA	Oscillator Timing Resistor	2k Ω to 150k Ω
Sink/Source Load Current (Peak)	0mA to 400mA	Oscillator Timing Capacitor	0.001 μF to 0.1 μF
		Deadtime Resistor Range	0 Ω to 500 Ω

ELECTRICAL CHARACTERISTICS $V_{IN} = +20\text{V}$ unless otherwise noted

PARAMETER	CONDITIONS	LT1525A LT1527A			SG1525A SG1527A			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
REFERENCE SECTION									
Output Voltage	$T_j = 25^\circ\text{C}$	5.05	5.10	5.15	5.05	5.10	5.15	V	
Line Regulation	$V_{IN} = 8\text{V to } 35\text{V}$	●	5	10		10	20	mV	
Load Regulation	$I_L = 0\text{mA to } 20\text{mA}$	●	20	50		20	50	mV	
Temperature Stability		●	20	50		20	50	mV	
Total Output Variation	Line, Load, and Temperature	●	5.0	5.1	5.2	5.0	5.1	5.2	V
Short Circuit Current	$V_{REF} = 0, T_j = 25^\circ\text{C}$		80	100		80	100	mA	
Output Noise Voltage	10Hz $\leq f \leq$ 10kHz, $T_j = 25^\circ\text{C}$		40	200		40	200	μVrms	
Long Term Stability	$T_j = 125^\circ\text{C}$		1	10		20	50	mV/ $\sqrt{\text{Khr}}$	

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	LT1525A LT1527A			SG1525A SG1527A			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
OSCILLATOR SECTION (Note 6)									
Initial Accuracy	$T_J = 25^\circ\text{C}$ (Note 6)		2	6		2	6	%	
Voltage Stability	$V_{IN} = 8\text{V to } 35\text{V}$	●	0.5	1		0.3	1	%	
Temperature Stability		●	3	6		3	6	%	
Minimum Frequency	$R_T = 150\text{k}\Omega$, $C_T = 0.1\mu\text{F}$	●		100			100	Hz	
Maximum Frequency	$R_T = 2\text{k}\Omega$, $C_T = 1\text{nF}$	●	400			400		kHz	
Current Mirror	$I_{RT} = 2\text{mA}$	●	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude		●	3.0	3.5		3.0	3.5	V	
Clock Width	$T_J = 25^\circ\text{C}$		0.3	0.5	1	0.3	0.5	1	μs
Sync Threshold		●	1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V	●		1.0	2.5		1.0	2.5	mA
ERROR AMPLIFIER SECTION ($V_{CM} = 5.1\text{V}$)									
Input Offset Voltage		●	0.5	5		0.5	5	mV	
Input Bias Current		●	0.2	3		1	10	μA	
Input Offset Current		●		0.5			1	μA	
DC Open Loop Gain	$R_L \geq 10\text{M}\Omega$	●	70	80		60	75	dB	
Gain Bandwidth Product	$A_V = 0\text{dB}$, $T_J = 25^\circ\text{C}$ (Note 5)		1	2		1	2	MHz	
Output Low Level		●	0.2	0.5		0.2	0.5	V	
Output High Level		●	3.8	5.6		3.8	5.6	V	
Common Mode Rejection	$V_{CM} = 1.5\text{V to } 5.2\text{V}$	●	75	90		60	75	dB	
Supply Voltage Rejection	$V_{IN} = 8\text{V to } 35\text{V}$	●	75	90		50	60	dB	
PWM COMPARATOR									
Minimum Duty Cycle		●		0			0	%	
Maximum Duty Cycle		●	45	49		45	49	%	
Input Threshold	Zero Duty Cycle (Note 6)	●	0.6	0.9		0.6	0.9	V	
Input Threshold	Max Duty Cycle (Note 6)	●		3.3	3.6		3.3	3.6	V
Input Bias Current		●	0.05	1.0		0.05	1.0	μA	
SOFT-START SECTION									
Soft-Start Current	$V_{SHUTDOWN} = 0\text{V}$	●	25	50	80	25	50	80	μA
Soft-Start Voltage	$V_{SHUTDOWN} = 2\text{V}$	●		0.4	0.6		0.4	0.6	V
Shutdown Input Current	$V_{SHUTDOWN} = 2.5\text{V}$	●		0.4	1.0		0.4	1.0	mA
OUTPUT DRIVERS (Each Output) ($V_C = 20\text{V}$)									
Undervoltage Lockout Hysteresis			0.2	0.6	1	0.2	0.6	1	V
Output Low Level	$I_{SINK} = 20\text{mA}$	●		0.2	0.4		0.2	0.4	V
	$I_{SINK} = 100\text{mA}$	●		1.0	2.0		1.0	2.0	V
Output High Level	$I_{SOURCE} = 20\text{mA}$	●	18	19		18	19	V	
	$I_{SOURCE} = 100\text{mA}$	●	17	18		17	18	V	
Undervoltage Lockout	V_{COMP} and $V_{SS} = \text{High}$	●	6	7	8	6	7	8	V
Collector Leakage	$V_C = 35\text{V}$ (Note 7)	●			200			200	μA
Rise Time	$C_L = 1\text{nF}$, $T_J = 25^\circ\text{C}$ (Note 5)			100	600		100	600	ns
Fall Time	$C_L = 1\text{nF}$, $T_J = 25^\circ\text{C}$ (Note 5)			50	300		50	300	ns
Shutdown Delay	$V_{SD} = 3\text{V}$, $C_S = 0$, $T_J = 25^\circ\text{C}$ (Note 5)			0.2	0.5		0.2	0.5	μs
TOTAL STANDBY CURRENT									
Supply Current	$V_{IN} = 35\text{V}$	●		14	20		14	20	mA

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ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	LT3525A LT3527A			SG3525A SG3527A			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
REFERENCE SECTION									
Output Voltage	$T_J = 25^\circ\text{C}$		5.05	5.10	5.15	5.00	5.10	5.20	V
Line Regulation	$V_{IN} = 8\text{V to } 35\text{V}$	●		5	10		10	20	mV
Load Regulation	$I_L = 0\text{mA to } 20\text{mA}$	●		20	50		20	50	mV
Temperature Stability		●		20	50		20	50	mV
Total Output Variation	Line, Load, and Temperature	●	4.95	5.1	5.25	4.95		5.25	V
Short Circuit Current	$V_{REF} = 0, T_J = 25^\circ\text{C}$			80	100		80	100	mA
Output Noise Voltage	$10\text{Hz} \leq f \leq 10\text{kHz}, T_J = 25^\circ\text{C}$			40	100		40	200	μVrms
Long Term Stability	$T_J = 125^\circ\text{C}$			1	10		20	50	mV/khr
OSCILLATOR SECTION (Note 6)									
Initial Accuracy	$T_J = 25^\circ\text{C}$ (Note 6)			2	6		2	6	%
Voltage Stability	$V_{IN} = 8\text{V to } 35\text{V}$	●		0.5	2		1	2	%
Temperature Stability		●		3	6		3	6	%
Minimum Frequency	$R_T = 150\text{k}\Omega, C_T = 0.1\mu\text{F}$	●			100			100	Hz
Maximum Frequency	$R_T = 2\text{k}\Omega, C_T = 1\text{nF}$	●	400			400			kHz
Current Mirror	$I_{RT} = 2\text{mA}$	●	1.7	2.0	2.2	1.7	2.0	2.2	mA
Clock Amplitude		●	3.0	3.5		3.0	3.5		V
Clock Width	$T_J = 25^\circ\text{C}$		0.3	0.5	1.0	0.3	0.5	1.0	μs
Sync Threshold		●	1.2	2.0	2.8	1.2	2.0	2.8	V
Sync Input Current	Sync Voltage = 3.5V	●		1.0	2.5		1.0	2.5	mA
ERROR AMPLIFIER SECTION ($V_{CM} = 5.1\text{V}$)									
Input Offset Voltage		●		2	5		2	10	mV
Input Bias Current		●		1	3		1	10	μA
Input Offset Current		●			0.5			1	μA
DC Open Loop Gain	$R_L \geq 10\text{M}\Omega$	●	70	80		60	75		dB
Gain Bandwidth Product	$A_V = 0\text{dB}, T_J = 25^\circ\text{C}$ (Note 5)		1	2		1	2		MHz
Output Low Level		●		0.2	0.5		0.2	0.5	V
Output High Level		●	3.8	5.6		3.8	5.6		V
Common Mode Rejection	$V_{CM} = 1.5\text{V to } 5.2\text{V}$	●	75	90		60	75		dB
Supply Voltage Rejection	$V_{IN} = 8\text{V to } 35\text{V}$	●	75	90		50	60		dB
PWM COMPARATOR									
Minimum Duty Cycle		●			0			0	%
Maximum Duty Cycle		●	45	49		45	49		%
Input Threshold	Zero Duty Cycle (Note 6)	●	0.6	0.9		0.6	0.9		V
Input Threshold	Max Duty Cycle (Note 6)	●	3.3	3.6		3.3	3.6		V
Input Bias Current		●	0.05	1.0		0.05	1.0		μA
SOFT-START SECTION									
Soft-Start Current	$V_{SHUTDOWN} = 0\text{V}$	●	25	50	80	25	50	80	μA
Soft-Start Voltage	$V_{SHUTDOWN} = 2\text{V}$	●	0.4	0.6		0.4	0.6		V
Shutdown Input Current	$V_{SHUTDOWN} = 2.5\text{V}$	●	0.4	1.0		0.4	1.0		mA

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	LT3525A LT3527A			SG3525A SG3527A			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX		
OUTPUT DRIVERS (Each Output) ($V_C = 20V$)									
Undervoltage Lockout Hysteresis			0.2	0.6		0.2	0.6	V	
Output Low Level	$I_{SINK} = 20mA$	●		0.2	0.4		0.2	0.4	V
	$I_{SINK} = 100mA$	●		1.0	2.0		1.0	2.0	V
Output High Level	$I_{SOURCE} = 20mA$	●	18	19		18	19	V	
	$I_{SOURCE} = 100mA$	●	17	18		17	18	V	
Undervoltage Lockout	V_{COMP} and $V_{SS} = High$	●	6	7	8	6	7	8	V
Collector Leakage	$V_C = 35V$ (Note 7)	●			200			200	μA
Rise Time	$C_L = 1nF$, $T_J = 25^\circ C$ (Note 5)			100	600		100	600	ns
Fall Time	$C_L = 1nF$, $T_J = 25^\circ C$ (Note 5)			50	300		50	300	ns
Shutdown Delay	$V_{SD} = 3V$, $C_S = 0$, $T_J = 25^\circ C$ (Note 5)			0.2	0.5		0.2	0.5	μs
TOTAL STANDBY CURRENT									
Supply Current	$V_{IN} = 35V$	●		14	20		14	20	mA

The ● denotes the specifications which apply of the full operating temperature range.

Note 1: Values beyond which damage may occur.

Note 2: Derate at 10mW/°C for ambient temperatures above +50°C.

Note 3: Derate at 16mW/°C for case temperatures above +25°C.

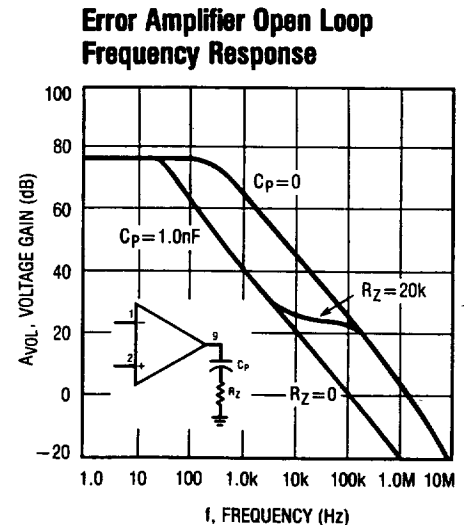
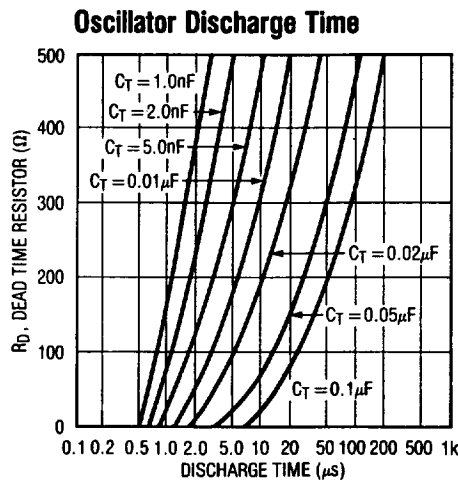
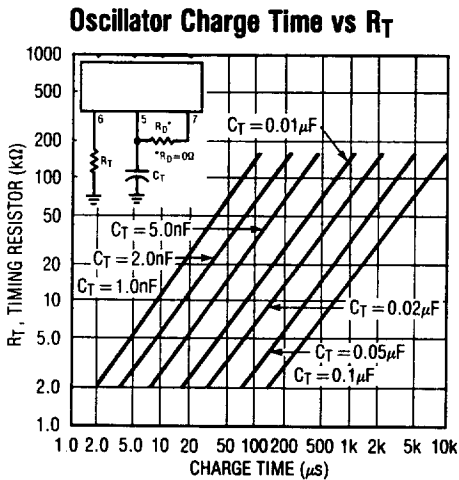
Note 4: Range over which the device is functional and parameter limits are guaranteed.

Note 5: These parameters, although guaranteed over the recommended operating conditions, are not 100% tested in production.

Note 6: Tested at $f_{OSC} = 40kHz$ ($R_T = 3.6k\Omega$, $C_T = 0.01\mu F$, $R_D = 0\Omega$).

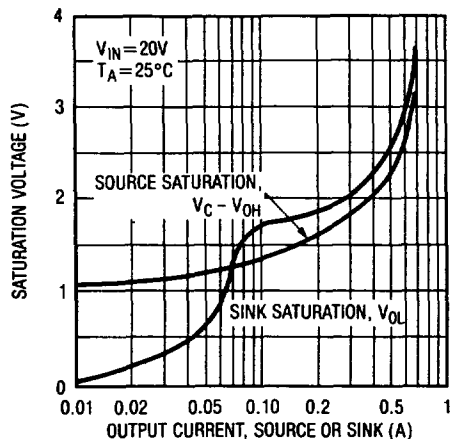
Note 7: Applies to 1525A/3525A only, due to polarity of output pulses.

TYPICAL PERFORMANCE CHARACTERISTICS

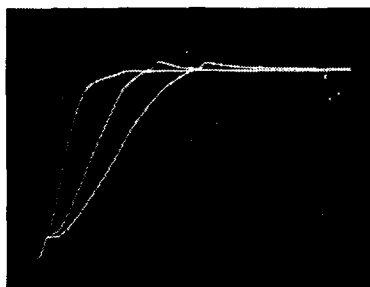
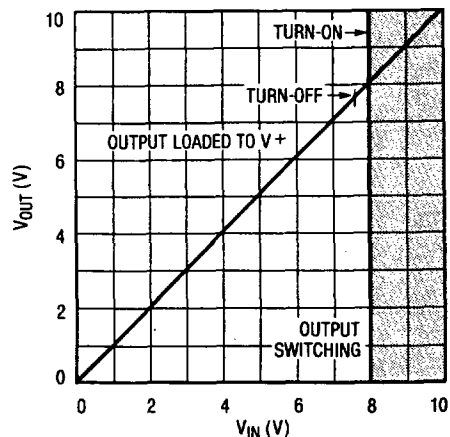


TYPICAL PERFORMANCE CHARACTERISTICS

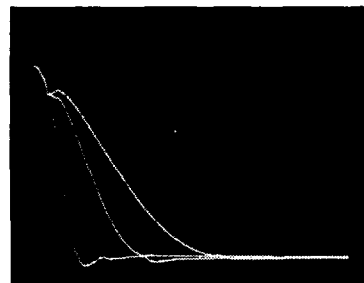
1525A Output Saturation Characteristics



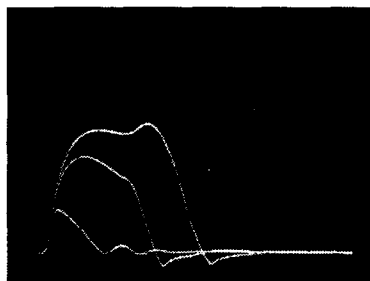
LT1527A Start-Up



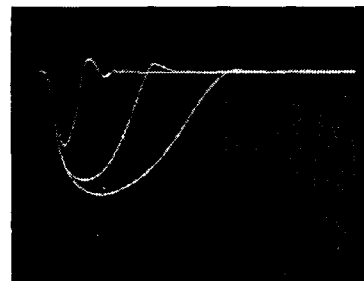
1525A/1527A
 $C_L = 1\text{kF}$,
 $= 5\text{kF}$,
 $= 10\text{kF}$
 $V = 2.5V/DIV$
 $H = 100\text{ns}/DIV$



1525A/1527A
 $C_L = 1\text{kF}$,
 $= 5\text{kF}$,
 $= 10\text{kF}$
 $V = 2.5V/DIV$
 $H = 100\text{ns}/DIV$



OUTPUT CURRENT
 $100\text{mA}/DIV$
 $100\text{ns}/DIV$



OUTPUT CURRENT
 $100\text{mA}/DIV$
 $100\text{ns}/DIV$

APPLICATIONS INFORMATION

Shutdown Options

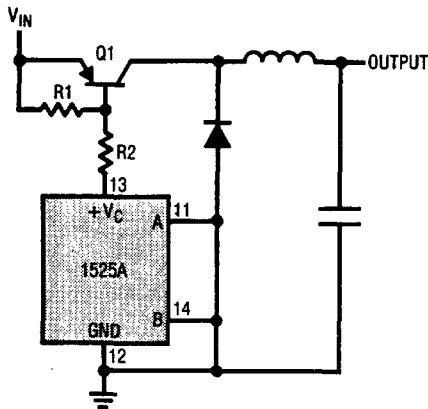
1. An external open collector comparator or transistor can be used to pull down the compensation pin (9). This will set the PWM latch and turn off both outputs. Pulse-by-pulse protection can be accomplished if the shutdown signal is momentary, since the PWM latch will be reset with each clock pulse.
2. Shutdown can also be accomplished by pulling down on the soft-start pin (8). When using this approach, shutdown will not affect the amplifier compensation network; however, if a soft-start capacitor is used, it must be discharged, possibly slowing shutdown response.

APPLICATIONS INFORMATION

- Applying a positive-going signal to the shutdown pin (10) will provide the most rapid shutdown of the outputs if a soft-start capacitor is not used at pin 8. An external soft-start capacitor at pin 8 will slow shutdown response due to the discharge time of the soft-start capacitor. Discharge current is approximately twice the charging current.
- The shutdown terminal can be used to set the PWM latch on a pulse-by-pulse basis if there is no external capacitance on pin 8. Soft-start characteristics may still be achieved by applying an external capacitor, blocking diode and charging resistor to the compensation pin (9).

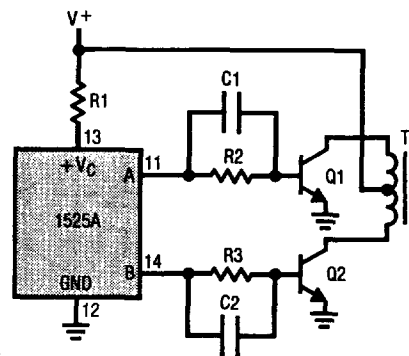
TYPICAL APPLICATIONS

Single Ended Supply



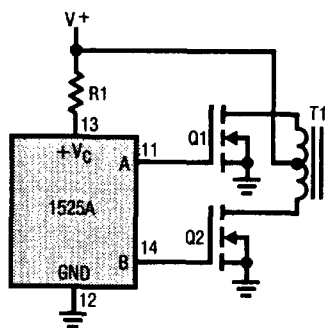
FOR SINGLE ENDED SUPPLIES, THE DRIVER OUTPUTS ARE GROUNDED. THE +V_C TERMINAL IS SWITCHED TO GROUND BY THE TOTEM-POLE SOURCE TRANSISTORS ON EVERY OSCILLATOR CYCLE.

Bipolar Push-Pull Supply



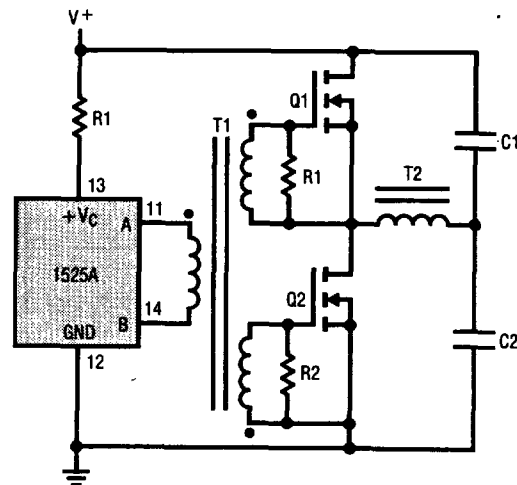
IN CONVENTIONAL PUSH-PULL BIPOLAR DESIGNS, FORWARD BASE DRIVE IS CONTROLLED BY R1-R3. RAPID TURN-OFF TIMES FOR THE POWER DEVICES ARE ACHIEVED WITH SPEED-UP CAPACITORS C1 AND C2.

Power FETs Push-Pull Supply



THE LOW SOURCE IMPEDANCE OF THE OUTPUT DRIVERS PROVIDES RAPID CHARGING OF POWER FET INPUT CAPACITANCE, WHILE MINIMIZING EXTERNAL COMPONENTS.

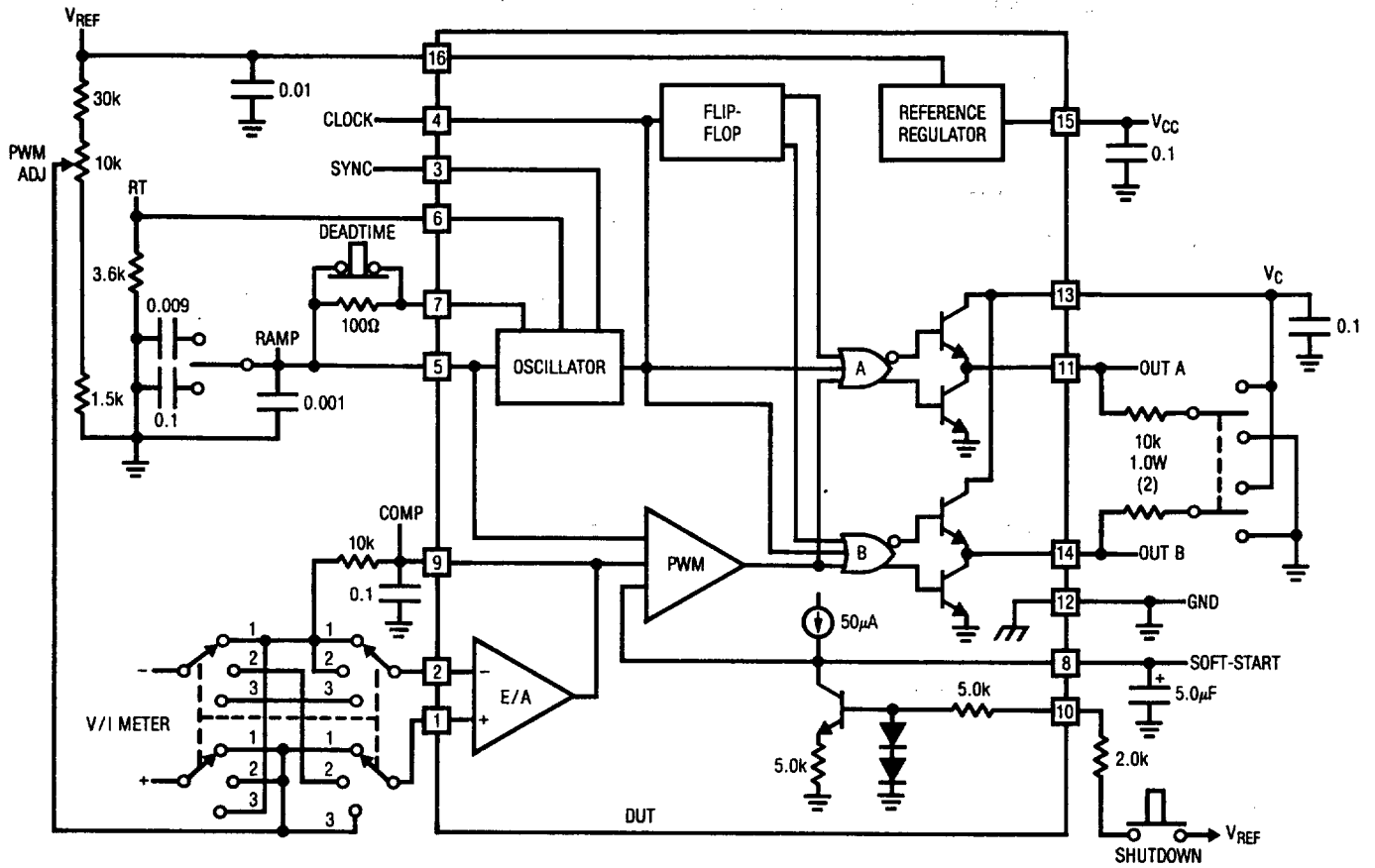
Driving Transformers Directly



LOW POWER TRANSFORMERS CAN BE DRIVEN DIRECTLY BY THE 1525A. AUTOMATIC RESET OCCURS DURING DEADTIME, WHEN BOTH ENDS OF THE PRIMARY WINDING ARE SWITCHED TO GROUND.

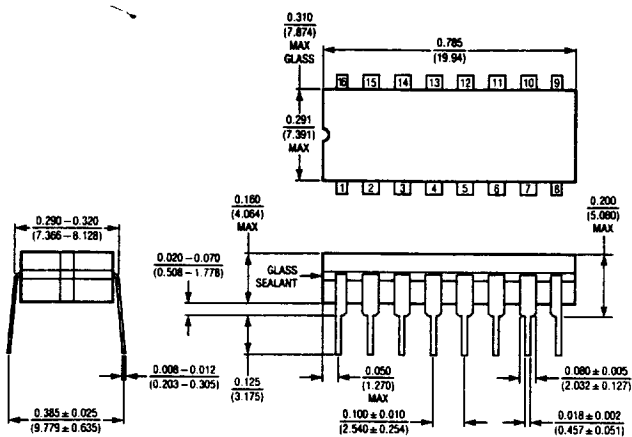
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TEST CIRCUIT



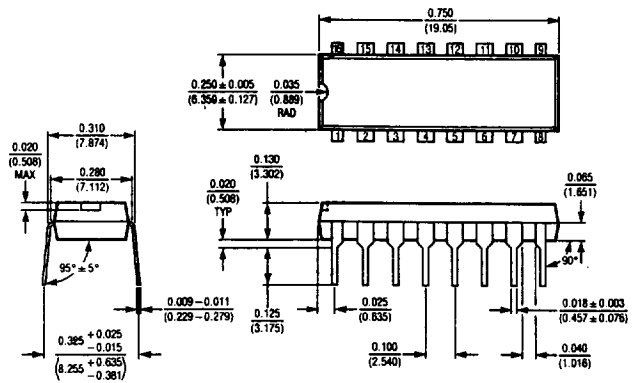
PACKAGE DESCRIPTION

16 Pin Cavity DIP (J)



	T _{jmax}	Θ _{JA}	Θ _{JC}
LT/SG1525AJ LT/SG1527AJ	150°C	100°C/W	60°C/W
LT/SG3525AJ LT/SG3527AJ	150°C	100°C/W	60°C/W

16 Pin Molded DIP (N)



	T _{jmax}	Θ _{JA}	Θ _{JC}
LT/SG3525AN LT/SG3527AN	105°C	100°C/W	60°C/W