PCB Translators User’s Guide

HyperLynx

December, 1999

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Installation

To install a translator:

1. Place the HyperLynx CD-ROM in a CD-ROM drive.
2. If the Windows CD-ROM “AutoPlay” feature is enabled (“normal installation”):

   A. After a short period, the HyperLynx Install program will start automatically.

   -OR-

   If the Windows CD-ROM “AutoPlay” feature is disabled (“manual installation”):

   B. Using the Windows Explorer, double-click the Setup application (SETUP.EXE) on the CD-ROM; the HyperLynx Install program will start.
3. From the menu, click the Install PCB Translators button. The Install HyperLynx Translators dialog box opens.
4. Select the translator that you want to install and click the button. A dialog box opens and asks for confirmation; click Yes.
5. **The installation program prompts for a password. This password is found on your CD-ROM envelope or jewel-case (it is case-sensitive).**
6. Click OK.
7. Follow the on-screen instructions until the installation is complete. The translator must be installed in the same directory as BoardSim.

Accel-EDA Translator

Introduction

This describes how to create a HyperLynx .HYP file from an Accel EDA (Sequoia) board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

Important! *The Accel EDA translator is compatible with Accel P-CAD PCB, and Accel Tango PCB (the "Sequoia" technology). It is not compatible with older, pre-Sequoia versions of P-CAD or most old versions of Tango. If you are using a "pre-Sequoia" version of P-CAD or Tango, you need a separate translator that works for the older systems. Contact HyperLynx or your local re-seller for details.*

Creating a .HYP File from an Accel EDA Board

To create a .HYP file from your Accel EDA board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Create an ASCII Version of your Board File

The Accel EDA translator runs on an *ASCII* version of your board file (.PCB). The translator cannot read a binary .PCB file.

To create an ASCII version of your board file in Accel EDA:

1. Choose File/Save As.
2. In the file type list box, choose ASCII.
3. Click OK.

Run the Translator

To run the Accel EDA translator:

1. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the Accel EDA button.
2. Change to the directory your ASCII .PCB file is in, and select **boardname.PCB**, where **boardname** is the name of your board. Then click OK.

A DOS box opens and the translator runs in it, displaying messages about its progress.

When the translation is complete, the DOS box will close automatically (unless you force it to stay open; see below). The translator has created the HyperLynx signal-integrity file **boardname.HYP**.

The translator reports status messages to a log file (.LOG), and errors or warnings to a .ERR file. You can view the log file after translation by clicking View .LOG File in the Import PCB File to BoardSim dialog box. You can view the .ERR file by clicking View .ERR File.

You can keep the DOS box open after translation is complete (for example, to see on-screen messages).

To keep the DOS box open after translation:

1. Before running the translator, in the DOS Features area, click on the Keep Translator's DOS Box Open check box. Then choose the translator and run it.

To close the DOS box:

1. Click the Windows system closing control in the box's upper right-or left-hand corner.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.
2. From BoardSim's File menu, choose Open BoardSim File.
3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

About Component Values and IC Names

The translator takes passive-component values (values for resistors, capacitors, inductors) and IC names from the Accel EDA "Value" attribute. This attribute can be set in Accel EDA as follows:

To set the component "Value" attribute in Accel EDA:

1. From the Edit menu, choose Components.
2. In the Components list box, highlight the component whose value you wish to set.
3. Click the Properties button.
4. On the Pattern tab, in the upper left corner, type the desired value in the Value data box.

For passive components (Rs, C, Ls), BoardSim will properly convert the value if it is expressed in the form <number><suffix>, where <number> is the numeric value and <suffix> is an optional scaling suffix.

Following is a summary of the rules for constructing passive-component values that BoardSim will properly convert:

- Numeric values can be followed by an exponent of the form
  exxx or Exxx
  where xxx is any integer value, positive or negative.

- All numeric values can be followed by alphabetic scaling factors:
  M = mega (1,000,000x)
  K or k = kilo (1,000x)
  m = milli (0.001x)
  u or U = micro (1e-6x)
  n or N = nano (1e-9x)
  p or P = pico (1e-12x)

- Scaling-factor suffixes may be followed by other alphanumeric characters, e.g., uH or pF.

ACCEL P-CAD Master Designer Translator

Introduction

This describes how to create a HyperLynx .HYP file from a P-CAD board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

The P-CAD translator is supplied to HyperLynx by Router Solutions, Inc. It runs in a DOS box after being launched from BoardSim's user interface.

The translator reads PDIF files. It supports all versions of PDIF from 2 to 8.

Important! *This translator is designed to run with older versions of P-CAD that output PDIF files for inter-tool connectivity. If you have Accel P-CAD PCB (the new Sequoia version), there is a different translator that reads an ASCII .PCB file (instead of a .PDF file). Contact HyperLynx or your local re-seller for details.*

Creating a .HYP File from a P-CAD Board

To create a .HYP file from your P-CAD board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Create PDIF File

To create a PDIF file representing your board:

1. From the DOS prompt, type the following command line:

   pdifout -I filename.pcb

   where **filename.pcb** is the name of your board file. The P-CAD **pdifout** utility creates the file **filename.PDF**.

Specify Drill Sizes in a File (Optional)

The PDIF format does not support drill-hole sizes.

To include drill sizes in the .HYP file, you can either:

- Specify them in an ASCII "technology" file, before translating
  OR
- Specify them during translation when queried for

To specify drill sizes in a technology file:

1. Open the file PDIF.TEC with a text editor. (The file is installed in the same directory as the P-CAD translator.)

2. Add lines of the form

   .DRILL padstack_name drill_diameter

   to specify the drill-holes sizes for the padstacks on your boards. drill_diameter must be in inches.

For example,

```
; Drill diameter set
; .DRILL Padname Drilldia in inches
; Pad0 is always the via
.DRILL V50R28C 0.028
.DRILL N60S40C 0.040
.DRILL C60S40C 0.040
.DRILL N60R40C 0.040
.DRILL C60R40C 0.040
.DRILL H110 0.110
.DRILL N240R120 0.120
.DRILL C240R120 0.120
```

Do not delete any of the information already present in PDIF.TEC when you first open it. This default information is required for the translator to run properly. You should only add .DRILL lines to represent the padstack names and drill-hole sizes unique to your boards.

Note that you will typically only have to edit PDIF.TEC the first time you run the translator, and then occasionally thereafter, as long as you re-use the same names for padstacks from board to board.

Router Solutions advises that the syntax checking for the file is very limited, so make modifications carefully. You should save the PDIF.TEC file to another filename before editing, in case you create errors.

Run the Translator

To run the P-CAD translator:

1. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the P-CAD button.

2. Change to the directory your PDIF output file is in, and select **boardname.PDF**, where **boardname** is the name of your board. Then click OK.

A DOS box opens and the translator runs in it, displaying messages about its progress.

If you have specified the drill-hole sizes for all padstacks on your board in PDIF.TEC (see above for details), the translator will run without querying you. If you did not specify the drill sizes, the translator will ask you for them; type the appropriate diameter value in inches each time you are queried.

When the translation is complete, the DOS box will close automatically (unless you force it to stay open; see below). The translator has created the HyperLynx signal-integrity file **boardname.HYP**.

The translator reports status messages to a log file (.LOG), and errors or warnings to a .ERR file. You can view the log file after translation by clicking View .LOG File in the Import PCB File to BoardSim dialog box. You can view the .ERR file by clicking View .ERR File.

You can keep the DOS box open after translation is complete (for example, to see on-screen messages).

To keep the DOS box open after translation:

1. Before running the translator, in the RSI Features area, click on the Keep Translator's DOS Box Open check box. Then choose the translator and run it.

To close the DOS box:

1. Click the Windows system closing control in the box's upper right-or left-hand corner.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.

2. From BoardSim's File menu, choose Open BoardSim File.

3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Additional Information

- Before BoardSim runs the P-CAD translator, it copies the .PDF file into the local BoardSim directory; then translates; then copies the resulting .HYP file back into the original directory and deletes the temporary files. This is done to avoid running the translation over a network, since the translator can be up to 10 times slower if the input and output files are on a network drive than if they are local. Note that this scheme assumes

that BoardSim itself is located on a local drive; if not, the network-drive performance decrease is unavoidable.

- The translator does not support flash rotation in pad stacks.
- Shape types for flashes are translated to round, except rectangle, which is translated, to rectangle.
- Local padstack overwrite (IPT command) is not supported.
- The translator works from LIBRARY definition, but pad forms can be locally defined.
- DIMENSION entities are not supported.
- P-CAD allows duplicate pin names (e.g. two pin 6's). This is not supported by the translator. To resolve this problem, modify the .PINNAMENUMBER command in the PDIF.TEC file to "y".

ACCEL Tango Translator

Introduction

This describes how to create a HyperLynx .HYP file from a Tango board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

The Tango translator is supplied to HyperLynx by Router Solutions, Inc. It runs in a DOS box after being launched from BoardSim's user interface.

Important! *This translator is designed to run with older versions of Tango that cannot create ASCII .PCB files. If you have a recent version of Tango Pro or Accel Tango PCB, there is a different translator that you probably should use instead. Contact HyperLynx or your local re-seller for details.*

Creating a .HYP File from a Tango Board

To create a .HYP file from your Tango board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Create ASCII Version of Board

Simply do a normal ASCII save of your board from the Tango software.

Run the Translator

To run the Tango translator:

1. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the Tango button.

2. Change to the directory your Tango ASCII file is in, and select **boardname.PCB**, where **boardname** is the name of your board. Then click OK.

A DOS box opens and the translator runs in it, displaying messages about its progress.

When the translation is complete, the DOS box will close automatically (unless you force it to stay open; see below). The translator has created the HyperLynx signal-integrity file **boardname.HYP**.

The translator reports status messages to a log file (.LOG), and errors or warnings to a .ERR file. You can view the log file after translation by clicking View .LOG

File in the Import PCB File to BoardSim dialog box. You can view the .ERR file by clicking View .ERR File.

You can keep the DOS box open after translation is complete (for example, to see on-screen messages).

To keep the DOS box open after translation:

1. Before running the translator, in the RSI Features area, click on the Keep Translator's DOS Box Open check box. Then choose the translator and run it.

To close the DOS box:

1. Click the Windows system closing control in the box's upper right-or left-hand corner.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.

2. From BoardSim's File menu, choose Open BoardSim File.

3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Additional Information

- Be sure that a netlist is loaded into the Tango database before the ASCII file is saved.

- Tango allows component definition with duplicate or no pin names. (This is not allowed in most other CAD systems.) The translator will create a local component definition for every component with system-generated pin names.

- Components are placed by Tango PCB without a placement side indication in the database. The translator detects the placement side (mirror side) of a component by evaluating the layer of the reference designator. If the reference designator is placed in the "T SILK" (top silkscreen side), then the component is assumed to be not mirrored. If the component is placed on the "B SILK" side (bottom silk screen side), the component is assumed to be mirrored. If the component has a reference designator on both sides of the board then the component is placed on the same side as the last entry.

Cadence Allegro Translator

Introduction

This describes how to create a HyperLynx .HYP file from a Cadence Allegro board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.) The procedure differs slightly depending on whether you're running Allegro on a UNIX workstation or on a Windows PC; see the appropriate sections below for details.

Creating a .HYP File from a Cadence Board

To create a .HYP file from your Cadence Allegro board design and load the .HYP file into BoardSim, follow the steps in the remaining sections. There are small differences in the steps depending on whether you run Allegro on a UNIX workstation or a Windows PC; see the appropriate section below.

If You Run Allegro on a UNIX Workstation

Create ASCII Version of Board

Use the Allegro 'ad_extract' or 'extract' utility (the name differs depending on the version of Allegro you own; the program is the same) to translate the Allegro board file into three files describing the outline, stackup, and connectivity for the circuit board. (This step must be run on the Allegro UNIX workstation, either directly or via a TELNET session from your PC; if you don't have access to the workstation, ask your layout engineer or service bureau to run 'extract' for you.) HyperLynx provides a script file called 'hyp.txt' which specifies the necessary rules for the extraction process.

Note: *HYP.TXT is installed in the same directory as BoardSim, on your PC. Copy it to the UNIX workstation for use with Cadence's 'ad_extract' or 'extract'. HyperLynx provides two script files, HYP.TXT for* ***UNIX machines*** *and HYPD.TXT for the Windows version of Allegro.* ***Be sure to use HYP.TXT.***

To create an ASCII version of your board file:

Type the following command line on the Allegro workstation:

extract fname.brd hyp.txt fname.a_l fname.a_o fname.a_c
OR
ad_extract fname.brd hyp.txt fname.a_l fname.a_o fname.a_c

where:
fname.brd is the name of your Allegro board file;

hyp.txt is the HyperLynx-supplied script file which defines the information to be extracted;
fname.a_l ('**l**' for "**l**ayer") is an intermediate file containing the board's stackup (not 'a_1' or 'a_I');
fname.a_o ('**o**' for "**o**utline") is an intermediate file containing the board's outline; and
fname.a_c ('**c**' for "**c**onnectivity/**c**omponent") is an intermediate file containing the board's connectivity and component information

Allegro creates the three ASCII output files. Be sure you name them *exactly* as described above, because the HyperLynx translator will look for exactly those names. Again, whether you run 'ad_extract' or 'extract' depends on which version of Allegro you have (same program, different names).

Move ASCII Files to PC

Move the three intermediate files created by the extraction process to the PC that has BoardSim installed. (Over the network is the easiest way, especially since the file **fname.a_c** can be very large for some designs.)

If You Run Allegro on a Windows PC

Create ASCII Version of Board

Use the Allegro 'ad_extract' or 'extract' utility (the name differs depending on the version of Allegro you own; the program is the same) to translate the Allegro board file into three files describing the outline, stackup, and connectivity for the circuit board. HyperLynx provides a script file called 'hypd.txt' which specifies the necessary rules for the extraction process.

Note: *HYPD.TXT is installed in the same directory as BoardSim, on your PC. Copy it to another directory, if needed, for use with Cadence's 'ad_extract' or 'extract'. HyperLynx provides two script files, HYPD.TXT for* ***Windows machines*** *and HYP.TXT for the UNIX version of Allegro.* ***Be sure to use HYPD.TXT.***

To create an ASCII version of your board file:

Type the following command line for Allegro's 'extract' utility:

extract fname.brd hypd.txt fname.a_l fname.a_o fname.a_c
OR
ad_extract fname.brd hyp.txt fname.a_l fname.a_o fname.a_c

where:
fname.brd is the name of your Allegro board file;
hyp.txt is the HyperLynx-supplied script file which defines the information to be extracted;
fname.a_l ('**l**' for "**l**ayer") is an intermediate file containing the board's stackup (not 'a_1' or 'a_I');
fname.a_o ('**o**' for "**o**utline") is an intermediate file containing the board's outline; and

fname.a_c (‘**c**’ for “**c**onnectivity/**c**omponent”) is an intermediate file containing the board's connectivity and component information

Allegro creates the three ASCII output files. Again, whether you run ‘ad_extract’ or ‘extract’ depends on which version of Allegro you have (same program, different names).

Run the Translator

To run the Cadence translator:

1. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the Cadence Allegro button.

2. Change to the directory your ASCII board files are in, and select **filename.a_c**, where **filename** is the name you specified when you ran ‘ad_extract’ or ‘extract’. Then click OK.

The translator runs, displaying messages about its progress. When it finishes, it has created the HyperLynx signal-integrity file **boardname.HYP**.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.

2. From BoardSim's File menu, choose Open BoardSim File.

3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Cadnetix Translator

Introduction

This describes how to create a HyperLynx .HYP file from a Cadnetix board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

The Cadnetix translator is supplied to HyperLynx by Router Solutions, Inc. It runs in a DOS box after being launched from BoardSim's user interface.

Creating a .HYP File from a Cadnetix Board

To create a .HYP file from your Cadnetix board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Create Cadnetix Output File

(This step must be run on a UNIX workstation, either directly or via a TELNET session from your PC; if you don't have access to a workstation, ask your layout engineer or service bureau to run this for you.)

Create a .EDF (EDIF) output file from Cadnetix by running the following command:

edif2outpcb -s -e <error_file> -o <output_file> "input_file"

where "input_file" must be enclosed by quotes (") and the path must begin at the folder level, e.g., "/rpct.fld/pcu.spc"

Move Output File to PC

Move the .EDF output file to your PC. (Over the network is the easiest way, especially since the file may be large for big designs.)

Run the Translator

To run the Cadnetix translator:

1. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the Cadnetix button.

2. Change to the directory your Cadnetix output file is in, and select **filename.EDF**, where **filename** is the name of your board. Then click OK.

A DOS box opens and the translator runs in it, displaying messages about its progress.

When the translation is complete, the DOS box will close automatically (unless you force it to stay open; see below). The translator has created the HyperLynx signal-integrity file **filename.HYP.**

The translator reports status messages to a log file (.LOG), and errors or warnings to a .ERR file. You can view the log file after translation by clicking View .LOG File in the Import PCB File to BoardSim dialog box. You can view the .ERR file by clicking View .ERR File. (See the note under "Additional Information" regarding warnings in the .ERR file.)

You can keep the DOS box open after translation is complete (for example, to see on-screen messages).

To keep the DOS box open after translation:

1. Before running the translator, in the RSI Features area, click on the Keep Translator's DOS Box Open check box. Then choose the translator and run it.

To close the DOS box:

1. Click the Windows system closing control in the box's upper right-or left-hand corner.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.
2. From BoardSim's File menu, choose Open BoardSim File.
3. Select **filename.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Additional Information

- Via size is determined by the ".TEC" file which is installed in the same directory as the Cadnetix translator (the BoardSim root directory). You can change via sizes by editing the .TEC file with a text editor.
- Board outline is PSEUDO REAL.
- The translator is LIBRARY driven.
- Cadnetix's EDIF file cannot handle signal layers higher than "bottom layer". To change "bottom layer", on the UNIX workstation enter the

following:

mv **trc**<*old_layer*>**Z6gr trc**<*new_layer*>**Z6gr**

Then edit window Z6gr bottom layer entity to the correct layer.

- Copper areas are drawn with thousands of multiple line segments, which may lead to very large output files for boards with large copper areas.

EAGLE Translator

Introduction

This describes how to create a HyperLynx .HYP file from an ***EAGLE*** board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help. For details on ***EAGLE***'s .ULP files, see the Eagle Reference Manual or the Eagle on line Help.)

Creating a .HYP File from an *EAGLE* Board

To create a .HYP file from your ***EAGLE*** board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Run the Translator

To create the .HYP output file from *EAGLE*:

1. Load your board into ***EAGLE***.
2. From the File menu, choose Run. (Or click on the 

button.)
A **Run** dialog box opens.
3. Use the mouse to choose "**HyprLynx.ulp**".
4. Click OK. (Or double-click the "HyprLynx..ulp" name.)

While the translator is running, ***EAGLE*** displays a tick-tock message in the status line. When it finishes, it has created the HyperLynx signal-integrity file **boardname.HYP** located in the same directory as your **boardname.BRD** file.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.
2. From BoardSim's File menu, choose Open BoardSim File.
3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Features and Limitations Of The Translator

The following features, limitations, and compromises are imposed upon the translator. Some features or options can be controlled. To learn how, see the next section on **Changing Options In The Translator**.

1. ***EAGLE***'s User Language Program (ULP) feature is used to implement the translator. This has the advantage of allowing minor changes to the translator, however, on the other hand, it can take a few minutes to run on large boards, especially when the option "GeneratePinDirection" is enabled (yes). When using this option, you may find more than one driver for the net. Change the driver information in BoardSim.

2. The Translator can output the .HYP file. Normally, this option is always left on (yes).

3. The Translator can output the .REF file, however, only components with reference names beginning with U or IC and who's values begin with "74" or "40" are translated. The translation may not be the desired result, so check values in BoardSim and change them if necessary. Note that this option can be turned off (no).

4. The Translator outputs board perimeter information including wires and arcs on the dimension layer, and holes as 360 degree arcs. Components with wires and arcs on the dimension layer and holes are included in the board perimeter section.

5. The Translator can output the Stack Up parameters. This option can be turned off (no).

6. All unrelated copper objects that are not a part of a net, are all put into the single net name of "N$ComNet". (Do not use this net name in your board/schematic.) These include: arcs, circles, rectangles, and wires.

7. All component pins that are not a part of a net, are put into their own net name called "HYP$n.p" where 'n' represents the reference designator (U1, R1, etc) and 'p' represents the pin number/name such as '1', '2', or 'K' or 'A'. (Do not use this net name in your board/schematic.).

8. Polygons are not filled. They are output as wire segments of its perimeter information only. Polygons are part of a net.

9. Rectangles are not filled. They are output as wire segments of its perimeter information only.

10. An attempt is made to look at ***EAGLE*** package internal wires that are connected to pins. Normally, packages do not have internal copper wires, but, if you do use them, you'll have to make sure that they have translated properly.

11. ***EAGLE*** has no dialog box feature to allow WYSIWYG editing of the options available in the translator. See the next section on editing the translator options.

Changing Options In The Translator

This translator has a few options that can be changed by using an editor such as **Notepad**. Although ***EAGLE*** has an editor, it does not have large enough buffer to hold the translator. Therefore, use **Notepad** to make changes.

If you must edit the translator, make a copy of it. It's location is in:
C:\Program Files\EAGLE\ulp
You should always keep backups of your files. Do this **NOW**.

In the following descriptions, the **bold underlined** parameters may be changed and indicate the default value. Do not change any other characters.

Output File Control.

Generate Files Options:

Generate the Reference File *.REF ('yes'/'no'):
char GenerateReferenceFile = **yes**;

Generate the Hyperlynx File *.HYP ('yes'/'no'):
char GenerateHyperlynxFile = **yes**;

Component Types, Pins, and Values Control.

Generate Component Types Options:

Devices U, IC, C, D, L, R, BD, etc. ('yes'/'no')
char UseComponentTypes = **yes**;

Generate Component Pin Direction Options:

Generate the pin direction information within the .HYP file. ('yes'/'no'):
char GeneratePinDirection = **no**; If 'yes', slows down many times.

Component Value Change Options:

Truncate. Example: ".1uf 50v" to ".1uf". ('yes'/'no')
char TruncateComponentValues = **no**;

Convert Capacitor Values. i.e. change ".1" to ".1u". ('yes'/'no')
char ConvertCapValues = **yes**;

Values less than 1 are labeled as this unit:
string ConvertLT1to = "**uF**";

Values greater than or equal to 1 are labeled as this unit:
string ConvertGE1to = "**uF**";

Board Stack Up Control.

Stack Up Option:

Use board thickness data. ('yes'/'no')
char UseBoardStackUp = **yes**;

Board Thickness Option:

Board Thickness, if 0: use fixed layer sizes else calculate layer thickness'
real board_thickness = **0.0625**;

Copper Weight to Thickness Conversion Value Options:

Zero Copper thickness:
real zerooz = **0.0000**;

Half Ounce 0.5 oz Copper Thickness
real halfoz = **0.0007**;

One Ounce 1.0 oz Copper Thickness
real oneoz = **0.0014**;

Two Ounce 2.0 oz Copper Thickness
real twooz = **0.0028**;

Table of Copper Thickness' for Each Layer of Copper:
real copper_thickness[] = {0.0,
halfoz,halfoz,halfoz,halfoz,halfoz,halfoz,
halfoz,halfoz,halfoz,halfoz,halfoz,halfoz,
halfoz,halfoz,halfoz,halfoz};
Note: 1st number is not used (no layer 0)

Table of Plating Thickness' for Each Layer of Copper:
Note: Top and Bottom are used most often.
real copper_plating[] = {0.0,
halfoz,**zerooz**, **zerooz**, **zerooz**, **zerooz**, **zerooz**,
zerooz, **zerooz**, **zerooz**, **zerooz**, **zerooz**, **zerooz**,
zerooz, **zerooz**, **zerooz**, **halfoz** };
Note: 1st number is not used (no layer 0)

Dielectric Value Options:

Default Dielectric Constant
real dicons = **4.8**;

Dielectric Thickness for 1 sided board
real dit1ly = **0.0611**;

Dielectric Thickness for 2 sided board
real dit2ly = **0.0597**;

Dielectric Thickness for Multi-layered boards
real ditmly = **0.0200**;

Table of Dielectric Constants for Different Numbers of Layers:
real dielectric_constant[] = {
dicons,dicons,dicons,dicons,dicons,dicons,dicons,dicons,dicons};

Table of Dielectric Thickness' for Different Numbers of Layers:
real dielectric_thickness[] = {
dit1ly,dit2ly,ditmly,ditmly,ditmly,ditmly,ditmly,ditmly,ditmly};

Special Controls.

Special Wire Width Options:

Rectangle outline wire width in inches
real RectOutlineWireWidth = **0.001**;

Holes outline wire width in inches
real HoleOutlineWireWidth = **0.001**;

Precision of board components to accurately draw and locate:

(***Note***: Number of digits after the decimal '.' point.
Example: if precision is set for 3, an output value will be given as X.XXX,
whereas a precision of say 5, gives an output value of X.XXXXX,
noting that rounding occurs in the last digit.
Keep these values between 3 and 6. Unexpected results will occur otherwise.)

Board perimeter dimension precision
int precision_of_perimeter = **4**;

Layer thickness precision
int precision_of_layers = **5**;

Pad/Smd size precision
int precision_of_pads = **3**;

Pin/Via/Segment/Width precision
int precision_of_nets = **4**;

Mentor BoardStation Translator

Introduction

This describes how to create a HyperLynx .HYP file from a Mentor BoardStation board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

The Mentor translator is supplied to HyperLynx by Router Solutions, Inc. It runs in a DOS box after being launched from BoardSim's user interface.

The translator supports Mentor BoardStation release 8. If you are running release 7 rather than 8, contact HyperLynx about a special version of the translator executable.

Creating a .HYP File from a Mentor Board

To create a .HYP file from your Mentor board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Create Mentor Output Files

(This step must be run on a UNIX workstation, either directly or via a TELNET session from your PC; if you don't have access to a workstation, ask your layout engineer or service bureau to run this for you.)

First, create a .PRT file:

1. In Mentor's LIBRARIAN functions, select the following
   LOAD PART FILE

2. Then select
   SAVE GEOMETRY ASCII

This creates the .PRT file.

Another method of using the LIBRARIAN is to select the MGC button, then the Design Management function. Do a “COPY OBJECT”, then select ASCII_GEOM as source file and enter <boardname.PRT> as the output.

Note: *Some versions of BoardStation may not have the LIBRARIAN function. If your version does not, use instead the “Select PCB Diagram” option in the LAYOUT portion of the program.*

Then locate three other, standard Mentor files:

- boardname.WIR (may also be named TRACES.TRACES)
- boardname.CMP (may also be named COMP_FILE)
- boardname.NET (may also be named NETS_FILE)

where **boardname** is the name of your board.

Note: *Unix soft links may useful in associating the original file names with the files required by the translator.*

Move Mentor Output Files to PC

Move the four Mentor output files to your PC. (Over the network is the easiest way, especially since some of the files may be large for big designs.)

Run the Translator

To run the Mentor translator:

1. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the Mentor button.

2. Change to the directory your Mentor output files are in, and select **boardname.PRT**, where **boardname** is the name of your board. Then click OK.

A DOS box opens and the translator runs in it, displaying messages about its progress.

When the translation is complete, the DOS box will close automatically (unless you force it to stay open; see below). The translator has created the HyperLynx signal-integrity file **boardname.HYP**.

The translator reports status messages to a log file (.LOG), and errors or warnings to a .ERR file. You can view the log file after translation by clicking View Log File in the Import PCB File to BoardSim dialog box. You can view the .ERR file by clicking the View .ERR File button.

You can keep the DOS box open after translation is complete (for example, to see on-screen messages).

To keep the DOS box open after translation:

1. Before running the translator, in the RSI Features area, click on the Keep Translator's DOS Box Open check box. Then choose the translator and run it.

To close the DOS box:

1. Click the Windows system closing control in the box's upper right-or left-hand corner.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.

2. From BoardSim's File menu, choose Open BoardSim File.

3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Additional Information

- Mentor names (e.g., Padstacks, Parts, etc.) are not handled as case sensitive by the translator.
- All vias must be part of a net.
- No $$ADD commands are supported, except in create_board mode.
- Only one VIEW per translation is supported.
- The WIRE/TRACE file can contain AREAs, which are filled polygons. These polygons can have overlapping sides. (Overlapping sides are polylines that lie on top of existing polylines and therefore do not form a "good" polygon.)
- The "Solder Layer" must be known by the translator for proper operation. The "Solder Layer" is derived by the translator as follows:

    1. .SOLDERSIDE layer name (SIGNAL _xx) from the Mentor .TEC file is used.
    2. XRF: the highest signal number from the wire reference table is used.
    3. Routing_Layer attribute, i.e. the layer SIGNAL_number_of_routing_layers

- Unplaced components are positioned at location 0,0.
- Attribute "DRILL_DEFINITION_UNPLATED" is not implemented (i.e., free standing drill holes).

Mentor Integra Translator

Introduction

This describes how to create a HyperLynx .HYP file from a Mentor Integra board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

Creating a .HYP File from an Integra Board

To create a .HYP file from your Mentor Integra board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Run the Translator

To run the Integra translator:

1. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the Mentor Integra button.

2. Change to the directory your Layout board file is in, and select **boardname.txf**, where **boardname** is the name of your board. Then click OK.

The translator runs, displaying messages about its progress. When it finishes, it has created the HyperLynx signal-integrity file **boardname.HYP.**

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.

2. From BoardSim's File menu, choose Open BoardSim File.

3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

OrCAD Layout Translator

Introduction

This describes how to create a HyperLynx .HYP file from an OrCAD Layout board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

Creating a .HYP File from an OrCAD Layout Board

To create a .HYP file from your OrCAD Layout board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Run the Translator

To run the OrCAD Layout translator:

3. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the OrCAD Layout button.

4. Change to the directory your Layout board file is in, and select **boardname.MAX**, where **boardname** is the name of your board. Then click OK.

The translator runs, displaying messages about its progress. When it finishes, it has created the HyperLynx signal-integrity file **boardname.HYP.**

Loading Your Board into BoardSim

To load your board into BoardSim:

4. From the Windows Start Menu or in the Program Manager, open BoardSim.

5. From BoardSim's File menu, choose Open BoardSim File.

6. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

OrCAD PCB386+ Translator

Introduction

This describes how to create a HyperLynx .HYP file from an OrCAD PCB386+ board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

Creating a .HYP File from an OrCAD PCB386+ Board

Running the Translator

To run the OrCAD PCB386+ translator:

1. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the OrCAD PCB386+ button.

2. Change to the directory your board file is in, and select **boardname.BD1**, where **boardname** is the name of your board. Then click OK.

The translator runs, displaying messages about its progress. When it finishes, it has created the HyperLynx signal-integrity file **boardname.HYP.**

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.

2. From BoardSim's File menu, choose Open BoardSim File.

3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

PADS PowerPCB

Introduction

This describes how to create a HyperLynx .HYP file from a PADS board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

How you transfer a board design from PADS into BoardSim depends on which version of PADS you are using:

- **PowerPCB** writes HyperLynx-format files (.HYP files) directly from its Tool/BoardSim menu; no intermediate translator is required
- For **Perform (and other pre-PowerPCB version of PADS),** you first write an ASCII file, then run a HyperLynx translator to create the .HYP file

This chapter describes how to create .HYP files from PowerPCB. If you are using Perform instead, see section "PADS Perform Translator."

Creating a .HYP File from a PowerPCB Board

No External Translator Required

Because PowerPCB can write HyperLynx-format .HYP files directly, there is no separate or external translator required.

Generating the .HYP File

With your board loaded in PowerPCB:

1. Choose BoardSim from the Tools menu. The BoardSim dialog box opens.
2. Change settings, if desired, in the dialog box. (See "Settings in PowerPCB's BoardSim Dialog Box" below details.) Then click OK.

PowerPCB's built-in HyperLynx translator runs. When it finishes, it has created the HyperLynx signal-integrity file **boardname.HYP.**

Settings in PowerPCB's BoardSim Dialog Box

Mode

Create Files Only

If you choose Create Files Only, clicking the OK button will cause PowerPCB to run its built-in HyperLynx translator. After the .HYP file is created, you can manually run BoardSim and load the .HYP file for analysis. If you have the proper attributes set in your design and enable the option, a .REF file will be created also (see "Creating a .REF 'IC AutoMapping' File from PowerPCB" below for details).

Create Files and Launch BoardSim

If you choose Create Files and Launch BoardSim, clicking the OK button will first run PowerPCB's built-in HyperLynx translator, then when translation is complete, automatically launch BoardSim with the .HYP file loaded.

Output Unrouted and Unroutes Options

If you check the Unrouted box in the Output area, PowerPCB will generate HyperLynx output for not only the routed traces on your board, but also for unrouted traces. **This is a powerful capability that allows you to perform signal-integrity and EMC analysis at a very early stage in the board-design process — even before routing.** For example, using this feature, you can perform analysis:

- immediately after placement and before routing even begins
- after only some critical nets have been routed, but while the remainder of the board is still unrouted
- on nets that are only partially routed (e.g., a net whose routing to several critical components has been hand-routed, but the remainder of which is unrouted)

How Unrouted Nets are Modeled

To model unrouted nets, PowerPCB intelligently routes pseudo-connections between the pins on an unrouted net. These are output in the .HYP file (and displayed in BoardSim) as point-to-point connections. However, the length of each connection is set to the Manhattan length of the actual connection for realistic simulation.

You can control the "pessimism" of the Manhattan distances and specify the stackup layer on which unrouted segments are assumed to exist. See the following sections for details.

Note: *"Manhattan" length refers to the length of the shortest connection that can be established between two points on a board, using traces on the board's X-Y grid (i.e., no diagonal routing). Real connections are usually at least somewhat longer than the ideal, Manhattan length.*

Assumed Layer

Pull down the Assumed Layer combo box to choose the layer on which unrouted segments will be assumed to exist. The layer choice affects the width of the unrouted trace (the default routing width for the chosen layer is used for the unrouted segment), and its impedance.

Percent Excess Over Manhattan Length

Type a value in the Percent Excess Over Manhattan Length box to specify what percentage beyond Manhattan length unrouted traces should be. For example, if you type "50," all unrouted traces will be output with lengths of 1.5 times their Manhattan lengths (i.e., 50% longer than Manhattan).

The recommended value is "20", meaning 20% longer than Manhattan.

.HYP File Name

Type the name and path of the .HYP file you want created for your board. If you prefer to browse for a directory, click the Browse button.

Other Settings in the Dialog Box

Two of the other setting in the BoardSim dialog are for future use and should not be enabled for current designs:

- Attributes for Nets and Net Classes
- Attributes for Power and Ground Nets

For details on the ".REF IC AutoMapping File" setting, see "Creating a .REF 'IC AutoMapping' File from PowerPCB" below.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.
2. From BoardSim's File menu, choose Open BoardSim File.
3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

About Unrouted Nets in the Board Viewer

If you enabled modeling for unrouted nets (see "Output Unrouted and Unroutes Options" above for details), any such nets will be displayed in the board viewer as narrow, point-to-point connections, rather than "normal" routed traces with realistic widths. However, BoardSim uses the default trace width of the unrouted nets' "Assumed Layer" when it calculates the impedances of the nets' segments (see "Assumed Layer" above for details).

Analyzing Boards Before Routing

With PowerPCB and BoardSim, you can analyze your PCBs at the very earliest stages of design, including immediately after placement and before any routing has occurred. This is a powerful capability unique to PowerPCB.

For details on outputting data from an unrouted or partially routed board, see "Output Unrouted and Unroutes Options" above.

Setting Resistor and Capacitor Values for BoardSim

PowerPCB can pass resistor and capacitor values directly into the .HYP file, ready for use in BoardSim. The method for setting values differs depending on whether you're using version 3.0 or later, or an earlier version.

Setting Values in PowerPCB V3.0 or Later

To specify a resistor or capacitor value, set the component's Value attribute to the desired number. You can set this attribute either directly in PowerPCB, or in your schematic (PowerLogic or Viewdraw). You can scale the number (for example, to specify picoFarads or Megohms) using any of the following scaling suffixes:

M=mega (1,000,000x)

K or k =kilo (1,000x)

m=milli (0.001x)

u or U=micro (1e-6x)

n or N=nano (1e-9x)

p or P=pico (1e-12x)

Scaling-factor suffixes may be followed by other alphanumeric characters, e.g., uH or pF; these additional characters are ignored.

A scaling factor is not required, since the Value can be expressed in scientific notation:

exxx or Exxx

where xxx is any integer value, positive or negative.

Setting Values in a Version of PowerPCB Earlier than 3.0

Prior to version 3.0, PowerPCB did not support component attributes. However, you can set an attribute in your schematic (PowerLogic or Viewdraw). To specify a resistor or capacitor value, use the component's Part Type attribute. Modify the Part Type as follows:

```
<other_Part_Type_information>,<R_or_C_value>[<scaling_factor>][<units>]
```

I.e., follow the other information in the Part Type attribute with a comma, then the resistor's or capacitor's value. The value can optionally be followed by a scaling factor and/or a units designator.

The following scaling factors are allowed:

M=mega (1,000,000x)

K or k =kilo (1,000x)

u or U=micro (1e-6x)

n or N=nano (1e-9x)

p or P=pico (1e-12x)

Note: *PowerPCB pre-V3.0 does not allow the use "m" (for "milli," i.e., 0.001x) as a scaling factor. Use an explicit fraction instead, e.g., 0.001 or 1.0e-3.*

A scaling factor is not required, since the <R_or_C_value> can be expressed in scientific notation:

exxx or Exxx

where xxx is any integer value, positive or negative.

For units, you can use "ohm" or "farad" or "F". If no scaling factor is used, these units are "safe" because the first letter of each ("o" in ohm and "f" in farad) will not be confused with a scaling factor.

Examples:

In the examples below, `<other_Part_Type_information>` *means whatever additional, non-value information you would normally have in the Part Type attribute.*

```
<other_Part_Type_information>,100

<other_Part_Type_information>,33.0e-12

<other_Part_Type_information>,33.0p

<other_Part_Type_information>,33pF

<other_Part_Type_information>,33pFarads

<other_Part_Type_information>,10k

<other_Part_Type_information>,100Kohm
```

Creating a .REF "IC AutoMapping" File from PowerPCB

PowerPCB V3.0 and later supports the automatic creation of a .REF file, which maps IC reference designators on your board to signal-integrity buffer models (of type IBIS, or HyperLynx .MOD or .PML).

To specify the IC model for a particular IC on your board, and have the model appear automatically in the .REF file, set the following two of the IC's attributes (either in PowerPCB or in your schematic):

HyperLynx.Model File	Set value to the file name of the library containing the IC model. The library can be of type .IBS, .MOD, or .PML.
HyperLynx.Model	*If the library is of type .IBS or .PML,* set the value to the name of the model's component in the library. *If the library is of type .MOD,* set the value to the name of the model in the library.

If one or more of these attributes is set, then in PowerPCB's Tools/BoardSim dialog box, in the Output area, the .REF IC AutoMapping File option becomes ungrayed. Click on the check box to enable it. Then when you generate the .HYP file, a corresponding .REF file will also be created.

When a .REF file is created, it has name **boardname.REF**, where **boardname** is the name of your PCB design and .HYP file. The .REF file is created in the same directory as the .HYP file.

For more information about .REF files, see the BoardSim User's Guide.

PADS Perform Translator

Introduction

This describes how to create a HyperLynx .HYP file from a PADS board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

How you transfer a board design from PADS into BoardSim depends on which version of PADS you are using:

- **PowerPCB** writes HyperLynx-format files (.HYP files) directly from its Tool/BoardSim menu; no intermediate translator is required

For **Perform (and other pre-PowerPCB version of PADS),** you first write an ASCII file, then run a HyperLynx translator to create the .HYP file

Refer to the appropriate section, depending on which version of PADS you're running.

Creating a .HYP File from a PADS Perform Board

To create a .HYP file from your PADS Perform (or other pre-PowerPCB version) board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Create ASCII Version of Board

To create the PADS ASCII output file:

1. Load your board into PADS.
2. From the main menu, choose ASCII Out.
3. In the ASCII OUTPUT OPTIONS dialog box, set the following options:
   - for "Sections to Output", select the "All" check box
   - select the "Include Part Attributes from Library" check box
   - verify that the "Output Format" is set to "Basic Units"
   - specify the "Output File Name" as <board_name>.ASC, where <board_name> is the name of your board
4. Click the OK button.

PADS creates the ASCII file **boardname.ASC.**

Run the Translator

To run the translator:

1. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the PADS button.

2. Change to the directory your ASCII output file is in, and select **boardname.ASC**, where **boardname** is the name of your board. Then click OK.

The translator runs, displaying messages about its progress. When it finishes, it has created the HyperLynx signal-integrity file **boardname.HYP.**

Note: *If you do not select the "Convert Mitres to Route Segments" check box when you create the ASCII file from PADS, the PADS2HYP translator will report an error when you attempt to create the .HYP file. If this occurs, re-generate the ASCII file from PADS with the check box selected. The resulting output will replace mitered corners with route segments; this will have a negligible effect on simulation results.*

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.

2. From BoardSim's File menu, choose Open BoardSim File.

3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Protel Translator

Introduction

This describes how to translate a Protel board design into a HyperLynx .HYP file. (For details on .HYP files, see the BoardSim User's Guide.)

The Protel-to-.HYP-file translator is built-in to Protel's Advanced PCB software and installed automatically with Advanced PCB.

Protel's Built-In Translator to HyperLynx

In Advanced PCB 98

The translator in Advanced PCB 98 works correctly, with no known bugs or problems. The following sections discuss certain limitations in the translator built-in to earlier, pre-98 versions of Advanced PCB.

In Advanced PCB Version 2.8

The translator in version 2.8 of Advanced PCB works correctly, *with the following minor exceptions:*

- Traces containing arc segments (i.e., curves) may not be translated correctly. When this happens, the arc portion of the trace is omitted and the trace's connectivity is broken, so that BoardSim cannot correctly simulate. The workaround is to first modify the trace in Advanced PCB to change the arc(s) into straight segments before running File/Export/HyperLynx.

- Board outlines containing arc segments may not be translated correctly. This is cosmetic problem only, i.e., the board outline is displayed in BoardSim's PCB viewer but has no effect on simulation. BoardSim attempts to determine if an outline is incorrect, and if it is, BoardSim displays the outline as a rectangle large enough to hold all of the components on the board.

Protel has promised that these problems will be fixed in Advanced PCB 3.0!

In Earlier Versions of Advanced PCB

HyperLynx strongly encourages you to use the most-current version of Advanced PCB to avoid translator problems that were present in earlier versions. However, if you must use an older version, the following paragraphs provide some details on what problems to expect.

Versions 2.6 and 2.7

The translator provided with versions 2.6 and 2.7 of Advanced PCB has the following problems (in addition to those described for version 2.8):

- SMD pads have one incorrect dimension: rectangles are made into squares and ovals into circles. This may occasionally cause adjacent component pins on the same net to electrically short.
- Vias for through-hole pins are missing from the .HYP file. BoardSim attempts to compensate for this, but occasionally a net's connectivity will be "broken," resulting in incorrect simulation.
- Vias that join trace segments are missing pad information. If the ends of the segments do not have coordinates that match exactly, the net's connectivity will be broken, resulting in incorrect simulation. *This is the most serious bug.*
- Drill-hole information for vias is not output. This is a cosmetic problem only.

Version 2.5

V2.5 of the translator was not functional. *Do not attempt to load into BoardSim .HYP files created by V2.5; they will not simulate.*

Creating a .HYP File from a Protel Board

To create a .HYP file from your Protel board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Run the Translator

- Load your board into Protel's Advanced PCB.
- From Advanced PCB's File menu, choose Export, then choose HyperLynx. Click OK.
- Advanced PCB will run for some time, creating a .HYP file of name **boardname.HYP**, where **boardname** is the name of your board file.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.
2. From BoardSim's File menu, choose Open BoardSim File.
3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Additional Information

The “HyperLynx” topic in the Advanced PCB Help system describes how to use the component comment field to force device records into the .HYP file. HyperLynx recommends that you *not* use this feature; instead, allow BoardSim to automatically map components to component types. If some mappings are incorrect, change BoardSim’s reference-designator mappings as needed to fix them. (See the BoardSim User’s Guide or on-line Help for details.)

Ultiboard Translator

Introduction

This describes how to create a HyperLynx .HYP file from an Ultiboard board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

The Ultiboard translator is supplied to HyperLynx by Router Solutions, Inc. It runs in a DOS box after being launched from BoardSim's user interface.

Creating a .HYP File from an Ultiboard Board

To create a .HYP file from your Ultiboard board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Create Ultiboard Output File

In the Ultiboard system, create a file for your board in "external data file" format (.EDF).

Note: *The .EDF file's format must be V1.2 or later.*

Run the Translator

To run the Ultiboard translator:

1. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the Ultiboard button.

2. Change to the directory your .EDF file is in, and select **boardname.EDF**, where **boardname** is the name of your board. Then click OK.

A DOS box opens and the translator runs in it, displaying messages about its progress.

When the translation is complete, the DOS box will close automatically (unless you force it to stay open; see below). The translator has created the HyperLynx signal-integrity file **boardname.HYP**.

The translator reports status messages to a log file (.LOG), and errors or warnings to a .ERR file. You can view the log file after translation by clicking View .LOG File in the Import PCB File to BoardSim dialog box. You can view the .ERR file by clicking View .ERR File.

You can keep the DOS box open after translation is complete (for example, to see on-screen messages).

To keep the DOS box open after translation:

1. Before running the translator, in the RSI Features area, click on the Keep Translator's DOS Box Open check box. Then choose the translator and run it.

To close the DOS box:

1. Click the Windows system closing control in the box's upper right-or left-hand corner.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.
2. From BoardSim's File menu, choose Open BoardSim File.
3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Additional Information

- Board outline is PSEUDO.
- LIBRARY definition needed.
- Void areas are not optimally translated. Set default switch off in the file ULT.TEC (located in the same directory as the translator executable).

Veribest Translator

Introduction

This describes how to translate a Veribest board design into a HyperLynx .HYP file. (For details on .HYP files, see the BoardSim User's Guide.)

The Veribest-to-.HYP-file translator is shipped with Veribest's PCB software, version VB97.0 and later.

Creating a .HYP File from a Veribest Board

To create a .HYP file from your Veribest board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Create an MS Access Database Using the Veribest Report Writer

The translator runs from a Microsoft Access database file created by the Veribest Report Writer.

To create the database file:

1. With your board loaded in the Veribest system, run the Veribest Report Writer.
2. Using the Writer, create a Microsoft Access database file (.MDC) for your board.

Run the Translator (HLYNX.EXE)

The .HYP-file translator is shipped as an example executable with the Report Writer. After creating the MS Access database file, you can run the translator standalone from Windows, or launch it from inside the Report Writer.

To run the translator standalone:

1. From the Windows Start menu or Program Manager's File menu, choose Run.
2. Click the Browse button.
3. Change directories to the Veribest Report Writer examples directory; then change to VBAPPS\HLYNX.
4. Double-click on the HLYNX executable.

5. The translator asks on which database file to run; choose the file you created above.

When the translator finishes running, it has created a .HYP file, ready to load into BoardSim.

To run the translator from inside the Veribest Report Writer:

1. Follow the instructions in your Veribest documentation to add the translator executable HLYNX.EXE to the Report Writer's tool launcher. The executable is located below the Report Writer's example directory, in the VBAPPS\HLYNX subdirectory.

2. Run the translator from the tool launcher.

When the translator finishes running, it has created a .HYP file, ready to load into BoardSim.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.

2. From BoardSim's File menu, choose Open BoardSim File.

3. Select the .HYP file you created in the steps above, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Encore/Scicards Translator

Introduction

This describes how to create a HyperLynx .HYP file from an Encore/Scicards board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

The Encore/Scicards translator is supplied to HyperLynx by Router Solutions, Inc. It runs in a DOS box after being launched from BoardSim's user interface.

The translator supports Encore/Scicards versions 23 through 28 (CII 2 -8).

Creating a .HYP File from an Encore/Scicards Board

To create a .HYP file from your Encore/Scicards board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Create Encore/Scicards Output File

(This step must be run on a UNIX workstation, either directly or via a TELNET session from your PC; if you don't have access to a workstation, ask your layout engineer or service bureau to run this for you.)

Create a .DAT (CII) output file from Encore/Scicards by running the following command:

EXPORT -> READABLE (REA00x) -> ALL OPTIONS ON

Note: *The .DAT file is in CII format. If you have a CII file with extension .CII, rename it to have a .DAT extension before running the translator.*

Move Output File to PC

Move the .DAT output file to your PC. (Over the network is the easiest way, especially since the file may be large for big designs.)

Run the Translator

To run the Encore/Scicards translator:

1. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the Scicards button.

2. Change to the directory your Encore/Scicards output file is in, and select **boardname.DAT**, where **boardname** is the name of your board. Then click OK.

A DOS box opens and the translator runs in it, displaying messages about its progress.

When the translation is complete, the DOS box will close automatically (unless you force it to stay open; see below). The translator has created the HyperLynx signal-integrity file **boardname.HYP**.

The translator reports status messages to a log file (.LOG), and errors or warnings to a .ERR file. You can view the log file after translation by clicking View .LOG File in the Import PCB File to BoardSim dialog box. You can view the .ERR file by clicking View .ERR File. (See the note under "Additional Information" regarding warnings in the .ERR file.)

You can keep the DOS box open after translation is complete (for example, to see on-screen messages).

To keep the DOS box open after translation:

1. Before running the translator, in the RSI Features area, click on the Keep Translator's DOS Box Open check box. Then choose the translator and run it.

To close the DOS box:

1. Click the Windows system closing control in the box's upper right-or left-hand corner.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.

2. From BoardSim's File menu, choose Open BoardSim File.

3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Additional Information

- If your board has vias inside surface-mount pads, you may see a large number of warnings in the .ERR file that say "Pad is on different location than pin." These can usually be safely ignored.

- The translator is LOCAL COMPONENT driven.

- Can define local padstacks per component, which may be different from the Library definition.
- Filled Outline Areas (record 666 in version 8) are not implemented.

CADStar/MaxiPC Translator

Introduction

This describes how to create a HyperLynx .HYP file from a CADStar or MaxiPC board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

The CADStar/MaxiPC translator is supplied to HyperLynx by Router Solutions, Inc. It runs in a DOS box after being launched from BoardSim's user interface.

Important! *This translator is designed to run with older versions of CADStar that output .CDI files for inter-tool connectivity. If you have a newer Windows version of CADStar that outputs the CADF format (.PAF files), there is a different translator that you probably should use instead. Contact HyperLynx or your local re-seller for details.*

Creating a .HYP File from a CADStar Board

To create a .HYP file from your CADStar board design and load the .HYP file into BoardSim, follow the steps in the remaining sections. (For more information about .HYP files, see the BoardSim on-line Help.)

Run the Translator

To run the CADStar translator:

1. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the CADStar/MaxiPC button.

2. Change to the directory your CADStar or MaxiPC board file is in, and select **boardname.CDI**, where **boardname** is the name of your board. Then click OK.

A DOS box opens and the translator runs in it, displaying messages about its progress.

When the translation is complete, the DOS box will close automatically (unless you force it to stay open; see below). The translator has created the HyperLynx signal-integrity file **boardname.HYP**.

The translator reports status messages to a log file (.LOG), and errors or warnings to a .ERR file. You can view the log file after translation by clicking View Log File in the Import PCB File to BoardSim dialog box. You can view the .ERR file by clicking the View .ERR File button.

You can keep the DOS box open after translation is complete (for example, to see on-screen messages).

To keep the DOS box open after translation:

1. Before running the translator, in the RSI Features area, click on the Keep Translator's DOS Box Open check box. Then choose the translator and run it.

To close the DOS box:

1. Click the Windows system closing control in the box's upper right-or left-hand corner.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.
2. From BoardSim's File menu, choose Open BoardSim File.
3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Additional Information

- Bullet pads are approximated as oblong pads.
- Self-intersecting filled polygons are not supported.
- The CDI file uses an unusual method of defining the layering for a pin. The translator only supports "natural" component definitions, i.e., all aspects of the component must be created as viewed from the component side of the PCB, then the entire part may be mirrored for the solder side.
- The first board outline present in the file is expected to be closed.

Zuken CR-3000 Translator

Introduction

This describes how to create a HyperLynx .HYP file from a Zuken CR-3000 board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

The CR-3000 translator is supplied to HyperLynx by Router Solutions, Inc. It runs in a DOS box after being launched from BoardSim's user interface.

Important! *This version of the translator supports only the CR-3000 product, not CR-5000. If you are using the CR-5000 product, contact HyperLynx about translator availability.*

Creating a .HYP File from a CR-3000 Board

To create a .HYP file from your CR-3000 board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Create CR-3000 ASCII Files for Your PCB

HyperLynx provides a UNIX shell script called **READZUKN** which calls a series of CR-3000 utility programs to create an ASCII representation of your board design. **READZUKN** is initially installed in the same directory as BoardSim, on your PC. Copy it to a workstation for use with the CR-3000 utility programs.

To create an ASCII version of your board file:

1. On a UNIX workstation with access to the CR-3000 utility programs, run the shell script **READZUKN**. The script will call several CR-3000 utilities and generate a series of ASCII files representing your PCB.

Specifically, ASCII files with the following extensions will be created: BSF, UDF, MDF, WDF, WSF, CCF, PMA.

Note: The script file **READZUKN** is a UNIX shell script; therefore, it can only be executed on a UNIX workstation (not on your Windows PC).
If you attempt to run the script and it fails because it cannot find the appropriate CR-3000 utility programs, contact your CAD manager or network administrator for assistance. **READZUKN** must be able to call the CR-3000 utility programs in order to run successfully.

Running in a Non-English-Language Environment

The **READZUKN** script was designed to run in an English-language environment. If you are running instead in a Japanese or other non-English environment, you must add the following two lines to the beginning of the script file:

```
setenv ZLANG english

setenv ZNLSLANG english
```

Move ASCII Files to Your PC

Move the intermediate ASCII files (.BSF, .UDF, .MDF, .WDF, .WSF, .CCF, and .PMA) created by the **READZUKN** script to the PC that has BoardSim installed. Then continue with the translation process on your PC as described in the next section.

On Your PC, Run HyperLynx Translator on ASCII Files

Finish the translation by running the HyperLynx CR-3000 translator on your PC.

To run the HyperLynx CR-3000 translator:

1. On your PC, from BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the Zuken CR-3000 button.

2. Change to the directory your ASCII board files are in, and select **filename.bsf**, where **filename** is the name of your board file. Then click OK.

A DOS box opens and the translator runs in it, displaying messages about its progress.

When the translation is complete, the DOS box will close automatically (unless you force it to stay open; see below). The translator has created the HyperLynx signal-integrity file **boardname.HYP**.

The translator reports status messages to a log file (.LOG), and errors or warnings to a .ERR file. You can view the log file after translation by clicking View .LOG File in the Import PCB File to BoardSim dialog box. You can view the .ERR file by clicking View .ERR File.

You can keep the DOS box open after translation is complete (for example, to see on-screen messages).

To keep the DOS box open after translation:

1. Before running the translator, in the RSI Features area, click on the Keep Translator's DOS Box Open check box. Then choose the translator and run it.

To close the DOS box:

1. Click the Windows system closing control in the box's upper right-or left-hand corner.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.

2. From BoardSim's File menu, choose Open BoardSim File.

3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Visula/CADStar for Windows Translator

Introduction

This describes how to create a HyperLynx .HYP file from a Visula or CADStar for Windows board design, and load the .HYP file into BoardSim. (For details on .HYP files, see the BoardSim User's Guide or the BoardSim on-line Help.)

The translator is supplied to HyperLynx by Router Solutions, Inc. It runs in a DOS box after being launched from BoardSim's user interface.

Creating a .HYP File from a Visula or CADStar for Windows Board

To create a .HYP file from your Visula or CADStar for Windows board design and load the .HYP file into BoardSim, follow the steps in the remaining sections.

Create CADIF Output File

The translator reads CADIF-format "neutral-database" files, which normally have a file extension of ".PAF". From Visula or CADStar for Windows, create a .PAF file with the same file name as for your board.

(For Visula, this step must be run on a UNIX workstation, either directly or via a TELNET session from your PC; if you don't have access to a workstation, ask your layout engineer or service bureau to run this for you.)

Move Output File to PC *(Visula Only)*

Move the .PAF output file to your PC. (Over the network is the easiest way, especially since the file may be large for big designs.)

Run the Translator

To run the Visula/CADSTAR for Windows translator:

1. From BoardSim, open the translator by choosing Translate PCB to .HYP File from the File menu, then clicking on the Visula/CADStar Windows button.

2. Change to the directory your .PAF output file is in, and select **boardname.PAF**, where **boardname** is the name of your board. Then click OK.

A DOS box opens and the translator runs in it, displaying messages about its progress.

When the translation is complete, the DOS box will close automatically (unless you force it to stay open; see below). The translator has created the HyperLynx signal-integrity file **boardname.HYP**.

The translator reports status messages to a log file (.LOG), and errors or warnings to a .ERR file. You can view the log file after translation by clicking View .LOG File in the Import PCB File to BoardSim dialog box. You can view the .ERR file by clicking View .ERR File.

You can keep the DOS box open after translation is complete (for example, to see on-screen messages).

To keep the DOS box open after translation:

1. Before running the translator, in the RSI Features area, click on the Keep Translator's DOS Box Open check box. Then choose the translator and run it.

To close the DOS box:

1. Click the Windows system closing control in the box's upper right-or left-hand corner.

Loading Your Board into BoardSim

To load your board into BoardSim:

1. From the Windows Start Menu or in the Program Manager, open BoardSim.

2. From BoardSim's File menu, choose Open BoardSim File.

3. Select **boardname.HYP**, and click OK.

BoardSim loads your board and brings it up in the board viewer, ready to simulate.

Additional Information

- Padforms are derived from the PADASSIGN section (not from the padstack section). Therefore PADFORMS are the same, regardless of the placement side of the shape.

- All pins are converted to the original defined pin numbers (not the optional pin names).

- Only 90-degree pad rotation is allowed.
- Diamond padforms are treated as round.
- Bullet padforms are treated as “finger.”
- Dimension entities are ignored.
- Taper line ends and pads are ignored.
- Copper areas and voids are not completely supported.
- Closed polylines containing arcs will not be filled.