# SPICE Writer User's Guide

**HyperLynx**

July 1999



HyperLynx
17641 N.E. 67th Court
Redmond, WA 98052
support@hyperlynx.com

# HyperLynx SPICE Writer

## What is the SPICE Writer?

The HyperLynx SPICE Writer is an optional module that can be added to LineSim or BoardSim (or both). It allows you to generate SPICE netlists of any schematic or selected net that you have loaded in LineSim or BoardSim.

### Why the Writer is Needed to Model Interconnect in SPICE

Normally, as a HyperLynx user, you'll perform your signal-integrity, crosstalk, and EMC simulations in LineSim or BoardSim. However, there may be certain situations in which you want to move interconnect simulation out of HyperLynx and into SPICE.

For example, HyperLynx does not supply models for analog ICs. If you have a mixed-mode design, HyperLynx can simulate the digital portions, but not the analog. SPICE, of course, handles analog simulation well.

However the difficulty with modeling interconnect in SPICE is getting the detailed transmission-line information into a SPICE netlist. For example, on a typical PCB, the clock net may involve literally hundreds of individual metal segments, each of which, for an accurate simulation, must be modeled as an individual transmission line with a certain delay and characteristic impedance. Translating this information from the PCB layout into SPICE manually is virtually an impossible task.

Worse yet, consider trying to model several complex, real-world PCB traces that are coupled to each other, using a SPICE netlist. SPICE itself may be able to perform the simulation if you can produce the netlist, but the netlist creation is probably impossible at the required level of detail. (To model coupling, you need to translate not only the "raw" physical layout

information, but also to run a field solver to find the coupling C and L matrices.)

## Let HyperLynx Do All of the Interconnect Modeling *Automatically*

The beauty of the SPICE writer is that it allows HyperLynx to perform for you the task the makes interconnect modeling in SPICE so difficult: the SPICE writer automatically extracts all of the detailed physical information from your PCB layout (or LineSim schematic), converts it to electrical data (including coupling), and writes it into a Spice netlist. Then you can add SPICE IC models as needed, and simulate.

## What the SPICE Writer Generates

The SPICE writer generates two files for every net or schematic on which you run it:

- a SPICE sub-circuit, containing:
  - all of the interconnect for the net(s) (modeled as SPICE transmission lines)
  - any passive components (resistors, capacitors, inductors) attached to the interconnect
  - external nodes for the points on the net(s) at which IC pins are to be connected (normally, SPICE IC models)
- a top-level SPICE “test bench,” the use of which is optional; it contains:
  - an instantiation of the sub-circuit
  - simple voltage-ramp + resistor “stand-in” models for the ICs attached to the sub-circuit; the voltage ramp switches in a time equal to the IC’s slew time, and the resistance equals the IC’s driving impedance
  - other control statements that allow the sub-circuit to be simulated, including probing of all of the sub-circuit’s external nodes

- if a coupled netlist (containing Hspice “W” elements) is generated, a series of .RLC files containing the electrical cross-section information for each W element in the netlist

## Two Types of Netlist Output, Uncoupled and Coupled

The files generated by the HyperLynx SPICE writer come in two “flavors”, depending on whether or not crosstalk is enabled in BoardSim/LineSim when you generate the netlist:

- uncoupled, in which no coupling is modeled, and all transmission lines are modeled with the standard SPICE lossless “T” element
- coupled, in which coupling is included and all coupled transmission lines are modeled with the Hspice coupled, lossy “W” element

Specifically, the choice between uncoupled and coupled output is made automatically by the SPICE Writer, as follows:

- if you are running BoardSim, and you have crosstalk enabled, coupled output is generated; if crosstalk is disabled, uncoupled output is generated
- if you are running LineSim, and you have coupling anywhere in your schematic, coupled output is generated; if there is no coupling in your schematic, uncoupled output is generated

## Coupled Netlists and the HyperLynx Field Solver

If you generate a coupled netlist, it includes Hspice-compatible “W” elements (see above). These require field solutions which result in capacitance and inductance matrices that characterize each element’s coupling. The solutions are generated automatically by HyperLynx’s field solver, and output in a series of files with extension “.RLC.”

You can correlate each W element to its .RLC file by looking in the netlist at the “RLGCfile=” field in the W element line.

Resistance matrices are also output into the .RLC file. Only “diagonal” DC resistances are included.

### Compatibility with SPICE Programs

The SPICE Writer’s *uncoupled* output uses only the standard “T” element, and should therefore be compatible with most programs derived from Berkeley SPICE. The output has been tested with a Berkeley version of SPICE.

The SPICE Writer’s *coupled* output uses the Hspice “W” element, and is only known to be compatible with Hspice. If you are running a different version of SPICE (not Hspice), you probably cannot use the coupled flavor of the Writer’s output.

## Running the SPICE Writer

### Load a Net or Draw a Schematic

In order to generate a SPICE netlist (actually, the two files described in section “What the SPICE Writer Generates” above), you must first decide which circuit you want modeled.

If you’re running BoardSim, select a net for simulation. If crosstalk is enabled, you should also adjust BoardSim Crosstalk’s threshold so that the desired number of aggressor nets are included in the board viewer. The SPICE Writer will netlist the selected net, its associated nets, and (if crosstalk is enabled) all aggressor nets.

If you’re running LineSim, draw the schematic you want netlisted. The SPICE writer will include in its netlist all of the elements (transmission lines, resistors, capacitors, etc.) in the schematic.

### Generate the Netlist

Once you have the desired net selected or schematic drawn, creating the netlist is easy.

**To generate the SPICE Writer's netlist output:**

1. From the File menu, choose Create Spice File. A dialog box opens.

2. In the dialog box, if you want parasitic package leads modeled in the netlist, click on the Include Lead Parasitics box. (See "About Lead Parasitics" below for a few more details about parasitics.)

3. By default, the Spice node numbers used in the sub-circuit output will start at "100." If you want them to start at a different value, type it into the Spice Node Numbering edit box.

4. Click Save As. A dialog box prompts you for the name to use for the sub-circuit (appended automatically with extension ".SP"). Click Save. The netlist files are generated.

### Names of the Output Files

The sub-circuit file is named <your_name>.SP, where <your_name> is the name you chose in step #4 above. The top-level test-bench file is named <your_name>_TEST.SP.

### About Lead Parasitics

Lead parasitics are modeled in the SPICE netlist as continuous transmission lines in the sub-circuit file. (The parasitic "L" and "C" values are "blended together" to form a continuous transmission line.)

For ICs, if you plan to model them with SPICE models that already include package effects, you should disable the SPICE Writer's output of lead parasitics. Otherwise, you will double-account for the package effects: once in the sub-circuit netlist file, and again in your SPICE IC model.