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Parallel Connection of Power Electronic Devices

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Introduction

There are several reasons for connecting multiple power semiconductor devices in parallel, such as cost, performance, and physical layout. Cost often takes precedence over other considerations such as performance and manufacturability. The total component cost for paralleled discrete devices is usually less than for a single power module that could do the job.

A power module usually provides better performance than multiple discrete devices in terms of stray inductances, circuit complexity, and total thermal resistance. So how would multiple devices perform better than a single power module? Power modules tend to have high heat density. In some cases where heat dissipation is limited, such as in enclosed areas with limited airflow, multiple devices spread heat dissipation over a larger area, reducing peak temperatures. The small size of discrete devices may also provide flexibility in physical layout, which can be advantageous for mounting in various patterns or around obstacles.

There are drawbacks and potential problems with paralleling. This application note explains some common problems, provides some relevant background on device and circuit characteristics, and outlines some guidelines for successfully paralleling IGBTs, power MOSFETs, and diodes.

Risks of Paralleling Devices

The risks with any power electronic application are failures due to overheating and exceeding safe operating conditions. An additional risk when paralleling is parasitic oscillation of power MOSFETs and IGBTs.

Overheating can be the result of excessive current imbalance between devices, both while conducting as well as during switching. The chances of exceeding safe operating conditions and the susceptibility for parasitic oscillation can be slightly increased due to variation between devices but more significantly by problems in the gate drive and power circuits.

If one device fails, oftentimes all the others get destroyed as well. A number of mechanisms can cause this 'domino' failure effect. Failure of one device could result in excessive current through others, causing their subsequent failure. A failure can cause an excessively large or fast transient in the power circuit, leading to other failures due to over-voltage, excessive dv/dt, or rupturing the gate oxide. Finally, if gate drive circuitry experiences a high voltage transient, it may rupture the gate oxide of each device driven by that gate drive circuitry.

Multiple failure mechanisms may make finding the root cause challenging, since failures could be induced by factors that have nothing to do with paralleling. An example would be inadequate capacitance (possibly due to normal capacitor degradation over time) resulting in excessive ripple current and consequent over-voltage transients.

Number of Devices

There is basically no limit to the number of devices that can be paralleled, again providing that no device

overheats, and safe operating conditions are maintained. Some DC motor drives use more than 30 devices in parallel. Of course cost is the reason behind so many paralleled devices, and performance could probably be improved by using a power module instead.

The real question is how many devices should be paralleled. The amount of current that each device is capable of conducting must be greater than what each device is required to conduct in the application. In other words, current derating is required. So the number of devices is equal to the total current divided by derated device current. For example, suppose the total current is 90 Amps, each device can safely handle 30 Amps (over the range of operating conditions), and the device current is derated by 30%. The minimum number of devices is

$\frac{90\text{A}}{30\text{A}\cdot(1-30\%)} = 4.3$, which must be rounded up. So the minimum number is 5, whereas with no derating, 3 devices would just be enough.

Temperature Coefficient

A negative temperature coefficient (negative tempco) means that at a given current through the device, as the device heats up, the voltage drop across its current-carrying terminals decreases. Conversely, for a given voltage across the device, the current increases with increasing temperature. A positive tempco is just the opposite: the current decreases as the temperature increases for a given voltage across the device.

A positive tempco causes decreasing current through a device as its temperature increases above that of other paralleled devices. Therefore, a positive tempco is desirable for paralleling since it avoids a potential thermal runaway condition where a hotter device hogs current, resulting in ever increasing current and heating until destruction. However, a positive tempco neither ensures that each device conducts equal current, nor that the temperature of each device is the same.

Even with the potential risk of thermal runaway, it is a common misconception that negative tempco devices cannot be paralleled. There are two balancing mechanisms that enable paralleling, even of negative tempco devices. These mechanisms are:

- Heat sharing
- Increasing tempco with increasing current (meaning the tempco increases in numerical value and not necessarily in magnitude since it could be a negative number)

Heat sharing through the heat sink reduces the difference between device junction temperatures, which is what really matters. Heat sharing is especially important for negative tempco devices. However, even for positive tempco devices, heat sharing does not significantly force current sharing [2], [3]. Negative tempco devices must share a common heat sink. If possible, positive tempco devices should be mounted on a common heat sink as well. If multiple heat sinks must be used, their heat dissipation capacities should be matched (same type of heat sink, same coolant flow, same coolant temperatures, etc.) In other words, the thermal impedance from die to ambient for each device should be about the same.

Diodes and IGBTs that have higher voltage drop at a given current and temperature have higher switching speed than devices with less voltage drop. A generalization can be made that the tempco increases (in value) with decreasing device speed. However, this is only noticeable between technologies, such as between PT and NPT IGBTs. There is no significant correlation between tempco value and device speed for like devices. Thus variation in tempco is a negligible factor, unless you parallel devices with different part numbers or devices from different manufacturers. Of course this should be avoided.

On-State Current Sharing

When paralleled devices are all conducting, the steady-state voltage across each parallel device is forced to be the same. Therefore, excessive imbalance in current and/or heat dissipation can cause overheating in one or more devices. Some causes of on-state current imbalance are:

- variation in gate drive voltage for IGBTs and MOSFETs
- variation in R_{dson} for MOSFETs
- variation in current between devices at a given $V_{CE(on)}$ for IGBTs or forward voltage for diodes
- variation in heat dissipation

Note that it is not necessary for each device to conduct exactly the same amount of current or to operate at the same temperature. In fact they typically don't. What is necessary is to avoid overheating any device, or exceeding safe operating area conditions.

It is also not necessary for all devices to be driven by the same gate driver or buffer. However, the gate drive voltage and gate drive current capacity should be the same for each device. Equal gate drive voltage is especially important for IGBTs and low voltage power MOSFETs due to their high transconductance, which persists even at high gate voltage [1].

Diodes

Figure 1 shows forward current versus forward voltage curves for a Fast Recovery Epitaxial Diode (FRED). For any given forward voltage, the current increases with increasing temperature. This clearly shows a negative forward voltage tempco characteristic.

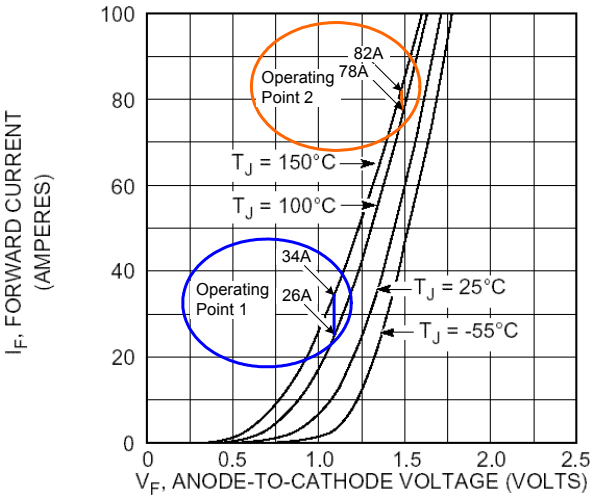

Figure 1 FRED V_F versus Current

Careful examination of Figure 1 shows that the temperature coefficient, while still negative, increases with increasing current. This is evidenced by the space between the curves (the difference in forward voltage for a given difference in temperature) decreasing with increasing current.

Consider the two operating points highlighted in Figure 1. Suppose two identical diodes operating in parallel share a total of 30 Amps, and that the junction of one diode is at 100 ºC and the other is at 150 ºC. According to the curves in Figure 1, one diode will conduct about 26 Amps while the hotter diode will conduct about 34 Amps, a difference of 8 Amps. Now suppose the same two diodes share 80 Amps, again at 100 ºC and 150 ºC junction temperatures. Now the currents are about 78 and 82 Amps through the cooler and hotter diodes respectively, a difference of only 4 Amps even though the total current is higher. The negative tempco of diodes increases with increasing current, which reduces the imbalance in current. This balancing mechanism combined with heat sharing through the heat sink enables paralleling of diodes.

If the current were increased enough, the constant temperature lines in Figure 1 would actually cross over each other. We'll call this the crossover point. This diode crossover point can be seen in the graph of reverse drain current versus forward voltage for the body diode of a MOSFET, as shown in Figure 2.

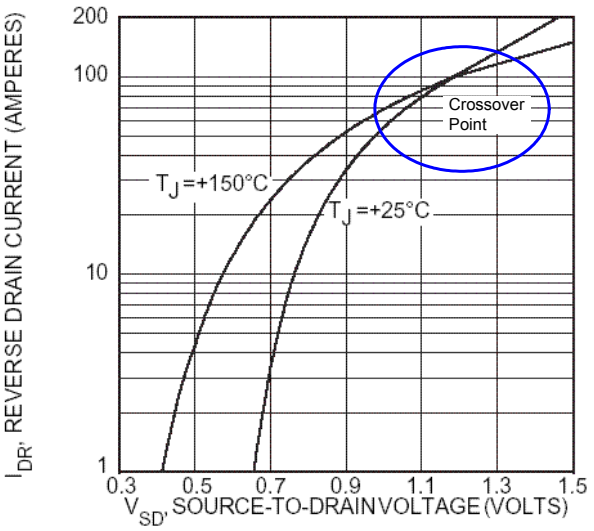

Figure 2 MOSFET Body Diode Forward Voltage

Before the crossover point, the diode exhibits a negative tempco characteristic; at current above the crossover point, it has a positive tempco. The crossover point is caused by the resistance of silicon, which goes up with increasing temperature.

Power MOSFETs and IGBTs

Power MOSFET R_{dson} always has a positive temperature coefficient regardless of current because of the resistance of silicon, and the fact that there is no conductivity modulation (MOSFETs are majority carrier only devices). R_{dson} also increases with current.

Figure 3 shows on-state voltage versus current curves for a PT IGBT, and the crossover point is plain to see.

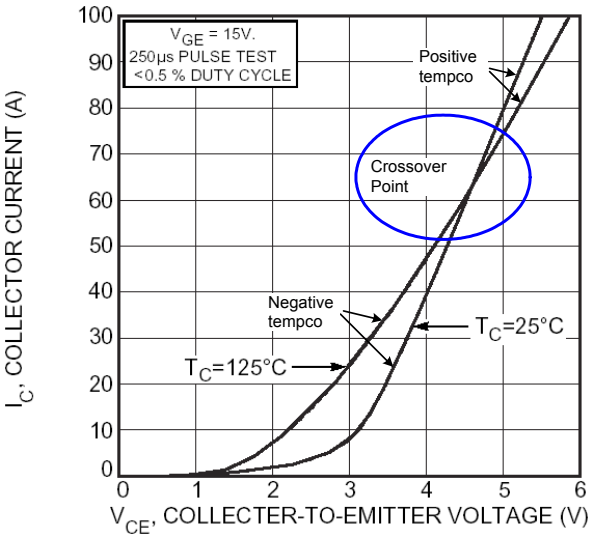

Figure 3 PT IGBT V_{CE} versus Current

NPT IGBTs also have a crossover point. The IGBT crossover point is due to the effective combination of a negative tempco diode in series with a positive tempco MOSFET [1]. For all practical purposes, most NPT IGBTs can be considered as having a positive V_{CE} tempco since the crossover point occurs at relatively low current. As Figure 3 illustrates however, PT IGBTs can exhibit a negative V_{CE} tempco until the device conducts rather high current.

Figure 4 illustrates similar information as Figure 3 but in a different format. Figure 4 is convenient for seeing the magnitude of the temperature coefficient because it is simply the slope of the curves. As in Figure 3, the tempco increases with increasing current.

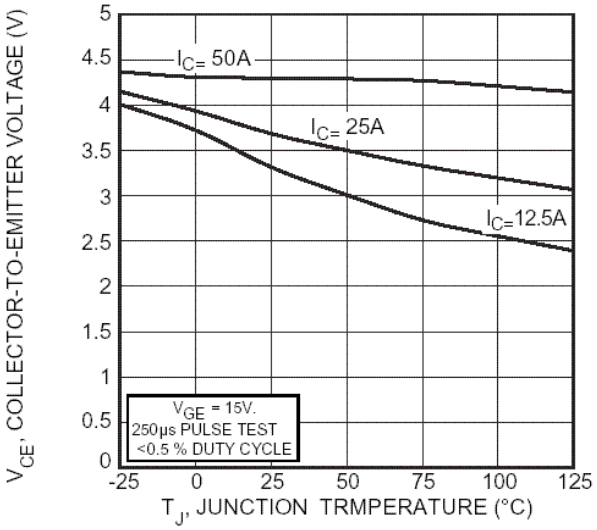

Figure 4 PT IGBT V_{CE} vs. Junction Temperature

As with diodes, the increase in tempco with increasing current and heat sharing are the balancing mechanisms that enable paralleling negative tempco IGBTs.

For all types of devices but especially negative tempco devices, heat sharing is critical. Current derating is also required, even for positive tempco devices, since variation in device speed and heat dissipation leads to variation in current and junction temperatures between paralleled devices.

Current Sharing During Switching

Some causes of current imbalance during switching are:

- variation in gate drive voltage
- variation in gate drive impedance, including stray inductances
- variation in gate drive timing
- variation in power circuit impedances, especially stray inductances
- variation in device speed
- variation in threshold voltage
- variation in heat dissipation

Some of these causes are the same as for on-state current imbalance, and the same guidelines apply. To reiterate:

- Multiple gate drivers/buffers are OK, but gate drive voltage and gate drive current capacity should be the same for each device.
- Mount devices on a common heat sink.

Diodes

For transient analysis, parallel diodes have been modeled as a ladder network in [4] and [5] as shown in Figure 5. Although the work in [4] and [5] was for high current line rectifiers with higher current and larger geometries, the concepts still apply to switch mode converters because current slew rates are very high. Even with diodes of identical forward drop characteristics and perfectly matched inductances and resistances, the ladder effect can cause variation in diode currents due to mutual inductance.

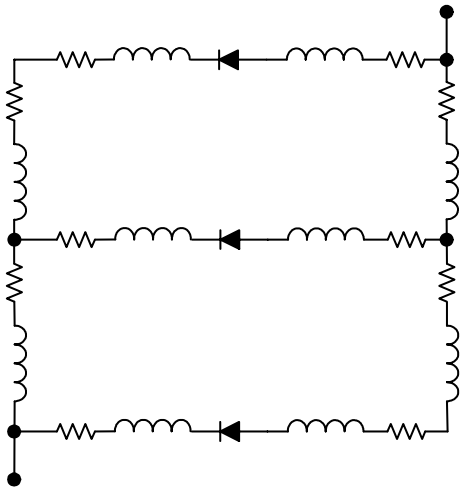

Figure 5 Diode Ladder Network

Variation in stray inductances can cause variation in induced voltages that dwarf the spread in forward voltage at rated current. The effect is greater during turn-on due to the relatively low voltage across the diode to suppress imbalanced transients. Bus layout should be symmetrical.

Higher resistance in the diode path than in the bus path helps reduce current imbalance, so the bus impedances should be minimized. Keep the busses as close together as possible and diode current paths as short as

possible to reduce the magnitude of stray inductances. If there are fewer diodes than IGBTs (or MOSFETs), place the IGBTs (or MOSFETs) close together, and space the diodes evenly apart. This reduces mutual inductance, but more importantly minimizes bus impedances and results in a symmetrical layout.

Power MOSFETs and IGBTs

The comments concerning the ladder effect for diodes applies equally well to all types of power semiconductor devices. This discussion focuses on IGBTs, however it applies as well to power MOSFETs. Simply substitute drain for collector and source for emitter.

Figure 6 shows a pair of parallel IGBTs, although there could be any number of them in parallel. Stray inductances are shown. L_c and L_e are the inductances of the power busses (rails). L_{c1}, L_{c2}, L_{e1}, and L_{e2} are the inductances created by the connections between the IGBTs and the power busses. In a nutshell, stray collector inductance causes overshoots and ringing; stray emitter inductance slows down switching. Actually, collector and emitter inductances both effect voltage and current during switching. However, emitter inductance has a strong influence on switching speed and consequently on current between devices because of its impact on the effective gate-emitter voltage.

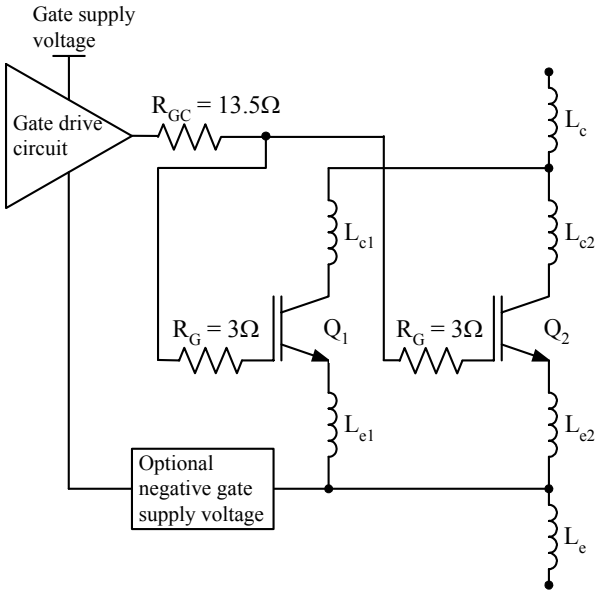

Figure 6 Parallel IGBT Stray Inductances

An inductance resists changes in current by generating an opposing voltage. This opposing voltage across stray emitter inductance raises the potential of the emitter during turn-on and lowers it during turn-off, shrinking the voltage available to drive the gate. Thus the effect of stray emitter inductance is very analogous to a ferrite bead on the gate. It is very important that the stray emitter inductances L_{e1} and L_{e2} be matched, and that all emitter inductances (L_{e1}, L_{e2}, and L_e) be minimized. Gate drive loop areas should be minimized. Connect the gate drive circuit's supply return as close as possible to the emitter pins. Devices and their bus connections should be arranged symmetrically. Gate drive circuitry should also be arranged as symmetrically as possible.

It is normal for MOS gated devices to exhibit variation in threshold voltage and capacitances. At high switching frequency, the variation in threshold voltage should be accommodated for by sorting, since lower threshold devices will turn on before and off after the others, potentially causing excessive current imbalance during switching. Threshold voltage should be sorted to within 150 to 200 millivolts for high frequency applications.

Current imbalance due to variation in capacitances must be accommodated for by separate gate resistors, one per device [6]. The separate gate resistors also absorb the energy of currents that can shoot through parasitic device capacitances, suppressing oscillation with parasitic inductances of parallel devices. The individual gate resistance should be as small as possible for balancing switching current yet large enough to preclude parasitic oscillation. Also, the total gate resistance value should not be larger than necessary to set voltage overshoot and ringing within desired limits. Otherwise, the switching losses would increase unnecessarily.

Reference [6] recommends that R_G/N be set at about 10% of the total gate resistance R_T, where N is the number of paralleled IGBTs (or MOSFETs).

$$R_T = R_{GC} + \frac{R_G}{N} \quad (1)$$

$$\frac{R_G}{N} = 0.1 \cdot R_T \Rightarrow R_G = 0.1 \cdot R_T \cdot N \quad (2)$$

Substituting (2) into (1), $R_{GC} = 0.9 \cdot R_T$. For an example corresponding to Figure 6, if the desired total gate resistance is 15 Ohms, and the number of paralleled devices is 2, then $R_G = 0.1 \cdot 15 \cdot 2 = 3\Omega$, and $R_{GC} = 0.9 \cdot 15 = 13.5\Omega$.

The resistance values in Figure 6 are for example only and not necessarily recommended values. In fact, the gate resistors in Figure 6 are conceptual really, since sometimes ferrite beads are added to control

oscillations [3], [7], and sometimes Schottky diodes and separate resistors are used to tune turn-off speed independently of turn-on speed. Turn-on is typically affected by diode reverse recovery current, so turn-on speed is set to minimize turn-on loss and noise [8]. Turn-off speed is set to control voltage overshoot and/or suppress dv/dt induced turn-on in bridge topologies.

The most important point is that the gates of the parallel devices should not be simply directly connected to each other. Also, to help reduce current imbalance during switching, the tolerance for individual gate resistors should be tight, 5% or less.

The total charge required to switch all parallel devices is the sum of what is required to switch each device. A low output impedance gate driver circuit should be used. If many devices are paralleled, it may be necessary to use multiple gate driver ICs, or to use a low output impedance buffer stage, or both. An example of a gate drive buffer circuit is shown in Figure 7.

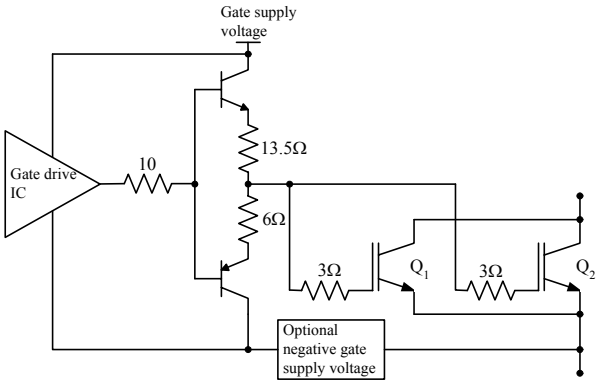

Figure 7 Gate Drive Buffer Stage

Note that MOSFETs could be used in the buffer stage in Figure 7 instead of the matched NPN, PNP transistor pair.

If separate gate drive ICs are used, make sure the maximum difference in propagation delay between them is low, about 25ns or less. Do not use multiple optically isolated gate drive ICs since they typically have too much variation in propagation delay.

Resistance added in series with each emitter helps force current balance and damps out oscillations, if any. However, it also adds stray inductance, slows switching, and dissipates power. Therefore, adding series emitter resistance should be avoided for high power switch mode applications. For power MOSFETs operated in the linear region, APT offers a series of Linear MOSFETs specifically tailored to linear mode operation, and references [3] and [9] discuss adding source resistance for parallel operation.

Derating and Sorting

Paralleling IGBTs and diodes with matched voltage drop (switching speed) is ideal both for current balancing as well as for synchronizing switching transients. However, sorting devices based on switching speed is not necessarily required, especially for positive tempco devices and for operation at low to medium switching frequencies. Sorting MOSFETs based on R_{dson} or gain is also unnecessary. Current derating on the other hand, for both positive and negative tempco devices, is always required. For high frequency applications, MOSFETs and IGBTs should be sorted for threshold voltage within a window of 150 to 200 millivolts. Sorting devices allows less derating for the same level of reliability.

Device speed, heat sharing, tempco, and dynamic effects (stray inductances and ladder effect) determine the balancing of current and consequently the amount of current derating required. There is not a simple closed form solution for current derating. If you know the distribution of on voltage for IGBTs or diodes, or R_{dson} for MOSFETs (by measuring several parts), you can estimate the on-state current imbalance and can derate the current accordingly. For IGBTs and diodes, you can use datasheet graphs to estimate the current imbalance. Die temperatures won't all be the same, so add additional guard band for that. If you don't know the distribution, you can use typical and maximum ratings from the datasheet to determine the spread in device speed. Beware that datasheet maximums represent the edge of the distribution, and may result in somewhat conservative derating. If typical values for R_{dson} are not listed, use at least a 25% spread.

Derating for dynamic effects is not so straightforward. However, switching current imbalance for unmatched devices is relatively small [3]. The effect of unmatched stray inductances is much greater. Because of dynamic effects, in general, the more devices in parallel, the more current derating must be increased.

Summary

Paralleling discrete semiconductor devices is often done as a lower cost alternative to power modules. Even negative temperature coefficient devices can be paralleled. Power modules in fact usually reach their power handling capability by paralleling multiple dice. Of course it is easier for a module manufacturer to parallel devices since the dice are easily matched by

manufacturing lot and connections are made as "tight" as can possibly be done, both electrically and thermally. Thus manufacturers of power modules follow best paralleling practices for you, resulting in better performance than is possible with paralleled discrete devices in terms of stray inductance, heat sharing, heat dissipation, parameter matching, compact size, and ease of manufacturing. When component cost, heat density, or unique layout requirements mandate the parallel connection of discrete devices, the following the guidelines outlined in this application note will help ensure success. These guidelines are summarized here.

- Mount the devices on the same heat sink. This is mandatory for negative tempco devices but is also important for positive tempco devices.
- If multiple heat sinks must be used, the thermal impedance from die to ambient for each device should be matched (same type of heat sink, same coolant flow, same coolant temperatures, etc.).
- Allow for some current derating.
- Arrange devices, connections and busses symmetrically.
- Minimize bus impedances and stray inductances, especially emitter (source) inductances by keeping the busses as close together as possible and device current paths as short as possible.
- Use a separate gate resistor (or resistor network) for each switching device. Do not tie the gates directly together.
- Use a small value for individual gate resistors. Use the $R_G = 0.1 \cdot R_T \cdot N$ rule.
- The tolerance for individual gate resistors should be tight, 5% or less.
- For high frequency applications, sort MOSFETs and IGBTs based on threshold voltage to within 150 to 200 millivolts.
- The gate drive voltage and gate drive current capacity should be the same for each device.
- Use a gate drive circuit with sufficiently low output impedance. Use multiple gate driver ICs and/or buffer stages if necessary.
- Make sure the gate drive pulses are synchronized. Do not use multiple opto-isolated gate drivers.
- Higher resistance in the device path than in the bus path helps reduce current imbalance – minimize bus impedances.
- Add source resistance only for linear applications or if required for control or protection of low power switch mode applications.
- If there are fewer diodes than IGBTs (or MOSFETs), place the IGBTs (or MOSFETs) close together, and space the diodes evenly apart.

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