Digital Scalar Pulse-Width Modulation: A Simple Approach to Introduce Non-Sinusoidal Modulating Waveforms

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***Abstract*—The digital scalar pulse-width modulation (DSPWM) gathers the characteristics of simplicity of implementation found in the regular sampling with the flexibility of manipulation of the switching patterns in the space vector modulation (SVPWM). This paper establishes a correlation between the SVPWM and DSPWM techniques. It also shows how to make the DSPWM strategy equivalent to the SVPWM technique without loosing its simplicity of implementation. By using such equivalence concept a microprocessor-based scheme, which uses standard timer circuits and a simple software algorithm, is proposed to implement the DSPWM technique. The introduction of the "distribution ratio" in this technique, allows the development of a systematic approach for implementing of either conventional or any modified vector strategies without changing the modulator scheme. This corresponds to generate any attractive nonsinusoidal modulating signals (NSMS) in the carrier-based modulation techniques. Furthermore, the simple digital blocks can be easily implemented as an specialized integrated circuit. Simulated and experimental results demonstrate the validity of the proposed methods.**

***Index Terms*—Pulse-width modulation, three-phase inverter.**

I. Introduction

THE classical sine-triangle modulation, or natural sampling modulation (NSPWM), compares a high frequency triangular carrier with three reference signals, known as modulating signals, to create gating pulses for the switches of the power converter [1]. This technique is basically an analog domain technique and its digital version led to the technique named as regular-sampled PWM (RSPWM) [2]. In the RSPWM technique, the modulating signal is sampled at each period (symmetric regular sampling) or at every peak (asymmetric regular sampling) of the triangular signal to produce a sampled-hold modulating wave. Its digital comparison to a triangular signal, generated by up-down counters, define the switching instants. In other words, the corresponding time intervals are computed in real time from the respective sampled value [3]. Differently from the previous methods, the space vector pulse-width modulation (SVPWM) technique [4], [5] does not consider each of the three phases as a separate entity. The three-phase voltages are simultaneously performed within a two-dimensional reference frame (dq plane), the complex reference voltage vector being processed as a whole. Because its flexibility of manipulation, the SVPWM technique is widely employed, nowadays [3].

It is well-known that the addition of proper zero-sequence components to the modulating signals generates nonsinusoidal modulating signals (NSMS). Several different waveform profiles can be used as modulating signals [3], [6]. These NSMS improve the performance of both NSPWM and RSPWM [7], [8]. On the other hand, the same effect obtained by the use of NSMS in carrier-based techniques, is achieved with both conventional SVPWM and modified SVPWM techniques. It should be noted that the modified SVPWM strategy is known in the literature under names such as "two-phase modulation" [9], "bus-clamping modulation" [10], or "discontinuous modulation" [11].

Several authors have discussed the correlation among the NSPWM, RSPWM, and SVPWM techniques, under different focuses. With that purpose, the concept of "ordering of the reference voltages" has been used to establish the analogy among the sectors defined by the active vectors and the segments of 60°, existing in a period of the references. Also, the concept of "distribution ratio" [12], named as "apportioning factor" in [8] and defined as the relation between the time of application of one of the two null vectors and the total null-vector time, has been employed. In fact, properly choosing the distribution factor determines both the distribution of the zero voltage vectors inside the sampling period and its correspondence to the modified SVPWM [8], [12]–[14].

The alternative "digital scalar pulse-width modulation" (DSPWM) technique imposes, to the pole voltage of an inverter leg, an average value that corresponds to each reference phase within the sampling interval [15]. Such strategy is of simpler implementation than the SVPWM technique, reducing the effort of calculation [16]. The technique introduced in [17] has a similar treatment by using the concept of reallocation of the "effective time." This "effective time" is in fact the sum of the times of application of the active vectors. The pulse-widths are ordered and the sum of times is appropriately moved within the sampling period.

Different methods have been employed to implement the resultant modulators of these recent studies. In [17], an algorithm is provided and implemented with a DSP TMS320C31. However, because of the correspondence between of the carrier-

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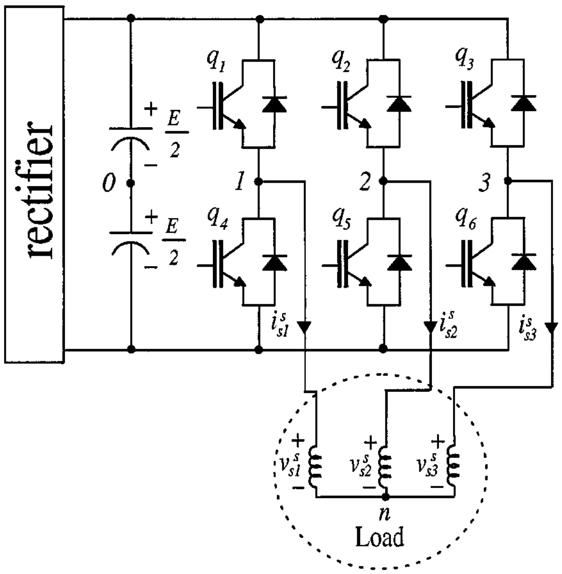

Fig. 1. Voltage source inverter feeding a three-phase load.

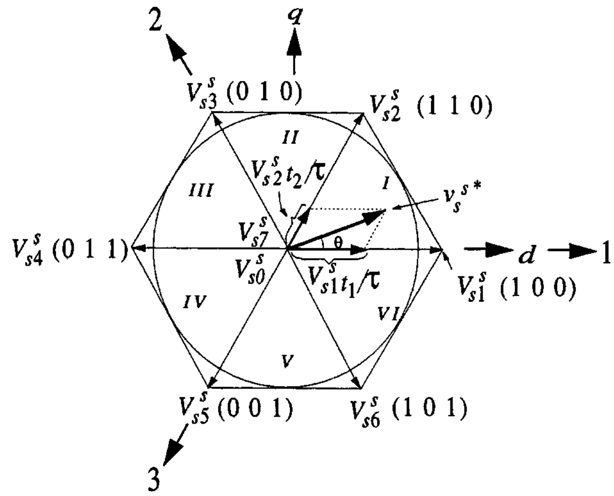

Fig. 2. Space vector dq plane.

based and the conventional and modified vector modulation, an analog implementation can also be done [13], [14]. In this case, three-phase rectifier bridges are employed to accomplish the ordering of the reference voltages. Another approach is the use of digital circuits to control electronic switches (CMOS) that order the references [12]. Such an alternative avoids the obligatory compensation of the diode voltage drop in the previous solution.

This paper establishes a correlation among the SVPWM and DSPWM techniques. It also shows how to make the DSPWM strategy equivalent to the SVPWM technique without loosing its simplicity of implementation. By using such equivalence concept a microprocessor-based scheme, which uses standard timer circuits and a simple software algorithm, is proposed to implement the DSPWM technique. The introduction of the "distribution ratio" in this technique, allows the development of a systematic approach for implementation of either conventional or any modified vector strategies without changing the modulator scheme. This corresponds to generate any attractive NSMS in the carrier-based modulation techniques. The simple digital blocks can be also easily implemented as an application specific integrated circuit (ASIC). Simulated and experimental results demonstrate the validity of the proposed methods.

II. Space Vector Modulation

Consider a three-phase inverter feeding a three-phase Y connected load and with neutral N non interconnected like illustrated in Fig. 1.

The states of the switches of the inverter can be represented by binary values q_1, q_2, q_3, q_4, q_5, and q_6, that is $q_k = 0$ for a turned-off switch and $q_k = 1$ for a turned-on switch. The pairs q_1q_4, q_2q_5 and q_3q_6 are complementary, therefore $q_4 = 1 - q_1$, $q_5 = 1 - q_2$ and $q_6 = 1 - q_3$. Using the conservative three-phase to two-phase transformation, it can be shown that the stator voltages v_{sd}^s and v_{sq}^s in the stator reference frame can be expressed as functions of q_1, q_2, and q_3, that is

$$\begin{bmatrix} v_{sd}^s \\ v_{sq}^s \end{bmatrix} = E\sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} q_1 \\ q_2 \\ q_3 \end{bmatrix}. \tag{1}$$

There are eight possible combinations of q_1, q_2, and q_3, which originate two null voltage vectors $V_{s0}^s = V_{s7}^s = 0$ and six active voltage vectors of amplitude $\sqrt{2/3}E$, spatially displaced 60° apart. These active vectors define Sectors *I, II, III, IV, V,* and *VI* as depicted in Fig. 2.

SVPWM involves vectorial equating volt-second integrals between a desired reference voltage vector, and the output vector realizable by two adjacent vectors, as defined by Van der Broeck *et al.* [5]. Assuming that the reference vector represented by $v_s^{s*} = v_{sd}^{s*} + jv_{sq}^{s*}$ is constant in the sampling interval τ, and that the two adjacent vectors are $V_{sk}^s = V_{sdk}^s + jV_{sqk}^s$ and $V_{sl}^s = V_{sdl}^s + jV_{sql}^s$ ($k = 1, \ldots, 6$; $l = k + 1$ if $k \leq 5$ and $l = 1$ if $k = 6$), one can obtain

$$v_s^{s*} = \frac{t_k}{\tau} V_{sk}^s + \frac{t_l}{\tau} V_{sl}^s \tag{2}$$

where t_k and t_l are the time intervals during which the adjacent vectors V_{sk}^s and V_{sl}^s are applied, respectively. Rewriting this vector equation in terms of dq components yields

$$t_k = \frac{(V_{sql}^s v_{sd}^{s*} - V_{sdl}^s v_{sq}^{s*})\tau}{V_{sdk}^s V_{sql}^s - V_{sdl}^s V_{sqk}^s} \tag{3}$$

$$t_l = \frac{(V_{sdk}^s v_{sq}^{s*} - V_{sqk}^s v_{sd}^{s*})\tau}{V_{sdk}^s V_{sql}^s - V_{sdl}^s V_{sqk}^s}. \tag{4}$$

A constant frequency operation of the inverter defined by a constant sampling interval τ is achieved if the null vectors are applied for the rest of the sampling interval, t_o, that is

$$t_o = t_{oi} + t_{of} = \tau - t_k - t_l. \tag{5}$$

In this expression, the time interval t_o, can be split and distributed at the beginning, t_{oi}, and at the end, t_{of}, of the sampling

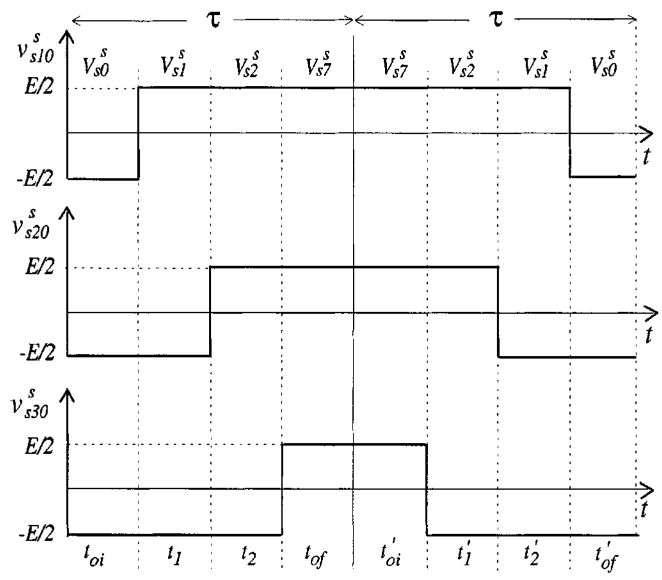

Fig. 3. Three-phase voltage generated with SVPWM.

interval τ as shown in Fig. 3. In general when the SVPWM technique is used, the time interval of application of null vectors, i.e., V_{s0}^s and V_{s7}^s, is equally distributed, that is $t_{oi} = t_{of} = t_o/2$.

Considering a normalized sampling interval equation (5) becomes

$$t_{oi}/\tau + t_{of}/\tau = 1 - t_k/\tau + t_l/\tau. \tag{6}$$

Equation (6) shows that the relation between t_{oi} and t_{of} for a given τ is a straight line with the slope equal to -1. That means that when t_{oi} increases t_{of} decreases at the same proportion, and vice-versa, for a given t_o. Therefore

$$(1-\mu)t_{oi} = \mu t_{of}, \qquad 0 \le \mu \le 1 \tag{7}$$

where $\mu = t_{oi}/(t_{oi}+t_{of})$ and $(1-\mu) = t_{of}/(t_{oi}+t_{of})$ are the distribution ratios of weights t_{oi} and t_{of}, respectively. A change in μ changes the commutation rhythm of the inverter producing modified PWM techniques [12], [18], [19].

It is of interest to reverse the sequence of the two non null vectors at the beginning of each sampling interval τ to reduce the switching losses and minimize the harmonic distortion of the load current waveform. Fig. 3 depicts the case in which vectors V_{s1}^s, V_{s2}^s and V_{s0}^s or V_{s7}^s are applied during two consecutive sampling intervals.

III. Digital Scalar Modulation

It is possible to impose, to each leg voltage pole of the inverter, an average voltage corresponding to its reference phase voltage during the sampling interval. Modified voltage references $v_{s1}^{*\prime}$, $v_{s2}^{*\prime}$ and $v_{s3}^{*\prime}$ can be defined from the three-phase sinusoidal reference voltages v_{s1}^{*}, v_{s2}^{*} and v_{s3}^{*} as follows:

$$v_{sj}^{s*\prime} = v_{sj}^{s*} + v_h, \qquad j = 1, 2, 3 \tag{8}$$

where v_h is a zero-sequence component. In the analysis that follows, voltages $v_{s1}^{s*\prime}$, $v_{s2}^{s*\prime}$ and $v_{s3}^{s*\prime}$ are considered as constants in the interval τ. As a first step lets make the average values

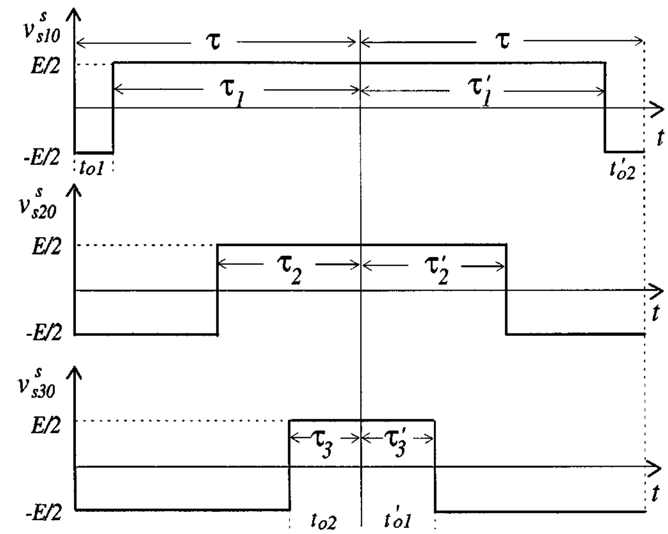

Fig. 4. Three-phase voltage generated with DSPWM.

of these voltages equal to the average values of the midpoint voltages v_{s10}, v_{s20} and v_{s30}. (See Figs. 1 and 4). This leads to

$$\frac{1}{\tau}\int_0^\tau v_{sj}^{s*\prime}(t)\,dt = \frac{1}{\tau}\int_0^\tau v_{sj0}^{s}(t)\,dt \tag{9}$$

and consequently to

$$v_{sj}^{s*\prime} = \left[\frac{E}{2}\tau_j - \frac{E}{2}(\tau - \tau_j)\right]\frac{1}{\tau} \tag{10}$$

since $v_{sj}^{s*\prime}$ are assumed to be constant over τ. From expression (10) it is possible to calculate the time intervals, that is

$$\tau_j = \left(\frac{v_{sj}^{s*\prime}}{E} + \frac{1}{2}\right)\tau. \tag{11}$$

In (11), τ_1, τ_2 and τ_3 are the time intervals in which switches q_1, q_2 and q_3 are closed, respectively, as defined in Fig. 4.

Fig. 5 establishes the correlation between this approach and that of the RSPWM for one sampling interval. It also shows that the application time t_1 and t_2 of the active vectors, do not change inside the interval if a zero-sequence component, v_h, is added to all reference samples, v_{sj}^{s*}. The crossing instants of $v_{sj}^{s*\prime}$ with the downward triangle slope, $p(t)$, determine the same values for τ_j as in (11).

Although the average voltages obtained by this approach refer to the point 0, (See Fig. 1), it can be shown that the average phase voltages $\overline{v}_{s1}^{s}$, $\overline{v}_{s2}^{s}$ and $\overline{v}_{s3}^{s}$ equal the reference voltages v_{s1}^{s*}, v_{s2}^{s*} and v_{s3}^{s*}, respectively, for symmetrical loads. Using the conservative three-phase to two-phase transformation, the equation (11) can be expressed in terms of dq components as

$$\tau_1 = \left(\sqrt{\frac{2}{3}}\,\frac{v_{sd}^{s*}}{E} + \frac{v_h}{E} + \frac{1}{2}\right)\tau \tag{12}$$

$$\tau_2 = \left(-\frac{1}{\sqrt{6}}\,\frac{v_{sd}^{s*} - \sqrt{3}v_{sq}^{s*}}{E} + \frac{v_h}{E} + \frac{1}{2}\right)\tau \tag{13}$$

$$\tau_3 = \left(-\frac{1}{\sqrt{6}}\,\frac{v_{sd}^{s*} + \sqrt{3}v_{sq}^{s*}}{E} + \frac{v_h}{E} + \frac{1}{2}\right)\tau. \tag{14}$$

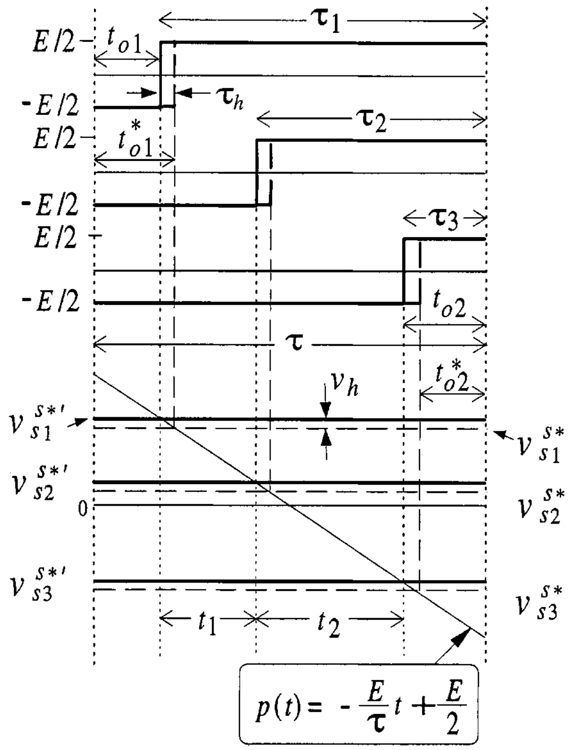

Fig. 5. Crossing instants, t_n, of the nth voltage reference sample with the downward triangle slope.

The comparison of Figs. 3 and 4 shows that the time intervals t_1 and t_2 corresponding to the vectors V^s_{s1} and V^s_{s2} (Sector *I*, $k = 1$, $l = 2$), respectively, are given by

$$t_1 = \tau_1 - \tau_2 \tag{15}$$

$$t_2 = \tau_2 - \tau_3. \tag{16}$$

From expressions (3) and (4), these time intervals can be calculated, for $k = 1$ and $l = 2$, as

$$t_1 = \frac{1}{\sqrt{2}} \frac{\tau}{E} \left(\sqrt{3} v^{s*}_{sd} - v^{s*}_{sq}\right) \tag{17}$$

$$t_2 = \sqrt{2} \frac{\tau}{E} v^{s*}_{sq}. \tag{18}$$

A similar result is obtained when t_1 and t_2 are calculated from (15) and (16), with τ_1 and τ_2 given by (12)–(14). This fact demonstrates that the inverter controlled by either SVPWM or DSPWM methods provides the same average voltage as applied to the load.

The expressions in (15) and (16) may be generalized by ordering the values computed using equations (12)–(14), i.e., by introducing the concept of maximum, τ_M, minimum, τ_m, and intermediate, τ_i, pulse-widths values [20], [21]. In the case of Fig. 4, the ordering is $\tau_M = \tau_1$, $\tau_m = \tau_3$ and $\tau_i = \tau_2$. From this, it can determined that

$$t_k = \tau_M - \tau_i \tag{19}$$

$$t_l = \tau_i - \tau_m. \tag{20}$$

TABLE I
TESTS TO ASSOCIATE VECTOR AND SCALAR APPROACHES

Modulation	
Vector	Scalar
Sector I - $(V^s_1 - V^s_2)$	$\tau_1 > \tau_2 > \tau_3$
Sector II - $(V^s_2 - V^s_3)$	$\tau_2 > \tau_1 > \tau_3$
Sector III - $(V^s_3 - V^s_4)$	$\tau_2 > \tau_3 > \tau_1$
Sector IV - $(V^s_4 - V^s_5)$	$\tau_3 > \tau_2 > \tau_1$
Sector V - $(V^s_5 - V^s_6)$	$\tau_3 > \tau_1 > \tau_2$
Sector VI - $(V^s_6 - V^s_1)$	$\tau_1 > \tau_3 > \tau_2$

From (19), (20), and (5), one can also obtain the following expression for the free-wheeling time interval

$$t_o = \tau - \tau_M + \tau_m. \tag{21}$$

Tests that associate vector and scalar approaches are synthesized in Table I.

Considering the first cycle of Fig. 4 there are two free-wheeling time intervals $t_{o1} = \tau - \tau_1$ and $t_{o2} = \tau_3$, at the beginning and at the end of the interval τ, respectively. The free-wheeling time intervals of the DSPWM are always determined by

$$t_{o1} = \tau - \tau_M \quad 22)$$

$$t_{o2} = \tau_m. \tag{23}$$

In general, these free-wheeling time intervals are different. A complete equivalence between SVPWM and DSPWM is achieved only if $t_{o1} = t_{oi}$ and $t_{o2} = t_{of}$. To achieve such condition, a time interval τ_h is added to each of τ_1, τ_2 and τ_3. This action is equivalent to compute (12)–(14) with

$$v_h = \tau_h E / \tau. \tag{24}$$

Fig. 5 shows that the term τ_M is modified to be $\tau'_M = \tau_M + \tau_h$, when v_h is added to the reference voltages. By using (22), one can obtain τ_h as given by

$$\tau_h = \tau - t_{o1} - \tau_M. \tag{25}$$

Similarly τ_m is modified to be $\tau'_m = \tau_m + \tau_h$. By using (23), one can find out that τ_h is

$$\tau_h = t_{o2} - \tau_m. \tag{26}$$

Since the time intervals τ_h computed by (25) and (26) must be equal, it can be written that

$$t_{o1} + t_{o2} = \tau - \tau_M + \tau_m. \tag{27}$$

Taking into account the fact that $t_{o1} + t_{o2} = t_o = t_{oi} + t_{of}$ the equivalence is completely established. The most usual case corresponds to $t_{oi} = t_{of} = t_o/2$ and uses (25) or (26) to calculate τ_h.

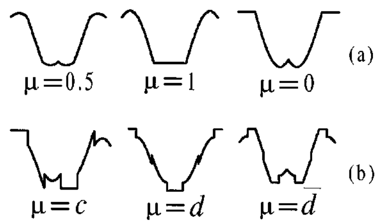

Fig. 6. Non-sinusoidal modulating signals: (a) constant μ and (b) variable μ.

IV. NON-SINUSOIDAL WAVEFORMS

It has been seen from Fig. 5 that t_1 and t_2 do not change if a zero-sequence component, v_h, is added to each reference signal within the sampling interval. In contrast, the values of t_{o1} and t_{o2} change to t^*_{o1} and t^*_{o2}. This change in the distribution of the null-vectors within the sampling interval, which can be represented in terms of the parameter μ as defined in (7).

The total time interval for application of the zero-sequence components, as a function of μ, is given by the solution of the system of equations formed by (6), (7), (19), and (20), i.e.,

$$t_{o1} = \mu(\tau - \tau_M + \tau_m) \tag{28}$$

$$t_{o2} = (1-\mu)(\tau - \tau_M + \tau_m). \tag{29}$$

Therefore, one can say that the distribution of the null-vectors in the DSPWM plays the same role as the nonsinusoidal modulating signals in the carrier based modulation technique, within the same sampling interval. This is beneficial since it is already known that the use of certain NSMS permits to increase the switching frequency of the inverter [14], [7]. The use of NSMS also improves the performance of the modulator in terms of the total harmonic distortion when the modulation depth increases [14], [8].

Different types of NSMS are obtained depending on how the null-vectors are distributed within the sampling interval, that is, as a function of the parameter μ. Fig. 6 shows one cycle of some of the well-known distorted modulating signals for different values of the μ parameter. Fig. 6(a) shows waveform for constant μ and Fig. 6(b) shows waveforms for variable μ. It should be noted that when one of the phases is clamped the number of commutations per cycle of the power switches is reduced.

A. Implementing NSMS

The distribution ratio μ can be defined in terms of logic signals originated from the comparison among the calculated pulse-widths in the DSPWM technique.

Fig. 7(a) presents a period for the three-phase reference signals. The six intervals 1 to 6 define the Ordered Voltage Segments (OVS) which are ordered in terms of their magnitude. It can be noticed that each OVS has a characteristic switching pattern [12]. As shown in that figure, a_1, a_2 and a_3 signals are obtained from the following comparisons: $a_1 = 1$ if $\tau_1 \geq \tau_2$, $a_1 = 0$ if $\tau_1 < \tau_2$; $a_2 = 1$ if $\tau_2 \geq \tau_3$, $a_2 = 0$ if $\tau_2 < \tau_3$ and $a_3 = 1$ if $\tau_3 \geq \tau_1$, $a_3 = 0$ if $\tau_3 < \tau_1$. From these signals one can obtain $c = a_1 \oplus a_2 \oplus a_3$, where $\oplus$ is the "exclusive or" operator. Signals b_j result from comparisons of type $\tau_j \geq \tau/2$, i.e., b_j is the sign of the modulating waveform, v^{s*}_{sj}. From b_j the signal $d = b_1 \oplus b_2 \oplus b_3$ is obtained. In Fig. 6(b) three discontinuous NSMS are presented, of which the logic signals that determine μ are also indicated. For $\mu = c$ the phases that correspond to subscripts M and m are clamped. For $\mu = d$ only phases that correspond to the maximum absolute value are clamped. For $\mu = \bar{d}$ only phases with medium absolute value are clamped.

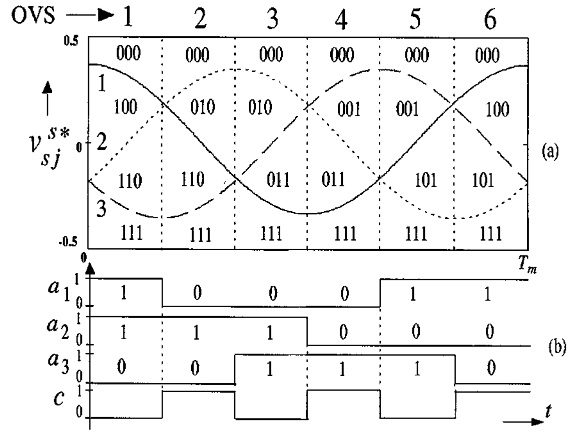

Fig. 7. (a) Three-phase references waveforms 1: v^{s*}_{s1}, 2: v^{s*}_{s2} and 3: v^{s*}_{s3}. (b) Logical signals that identify the OVS.

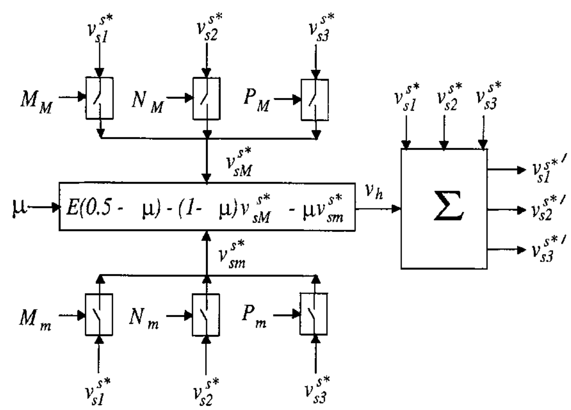

Fig. 8. PWM modulator for synthesizing the modulating signals specified by μ.

The introduction of NSMS in the DSPWM technique is, then, direct: the parameter μ is defined by the nonsinusoidal modulating signals wished and t_{o1} or t_{o2} are calculated by (28) and (29).

V. SOFTWARE IMPLEMENTATION

The procedure to obtain results equivalent to the SVPWM with the DSPWM implementation consists in

a) calculating τ_1, τ_2 and τ_3 from (12)–(14), with $v_h = 0$;
b) ordering by magnitude the calculated time intervals to obtain τ_M and τ_m and determine t_o from (21);
c) selecting the wished μ and calculate t_{o1} or t_{o2} from (28) and (29);
d) calculating the interval τ_h from (25) or (26) for given values of t_{o1} or t_{o2};

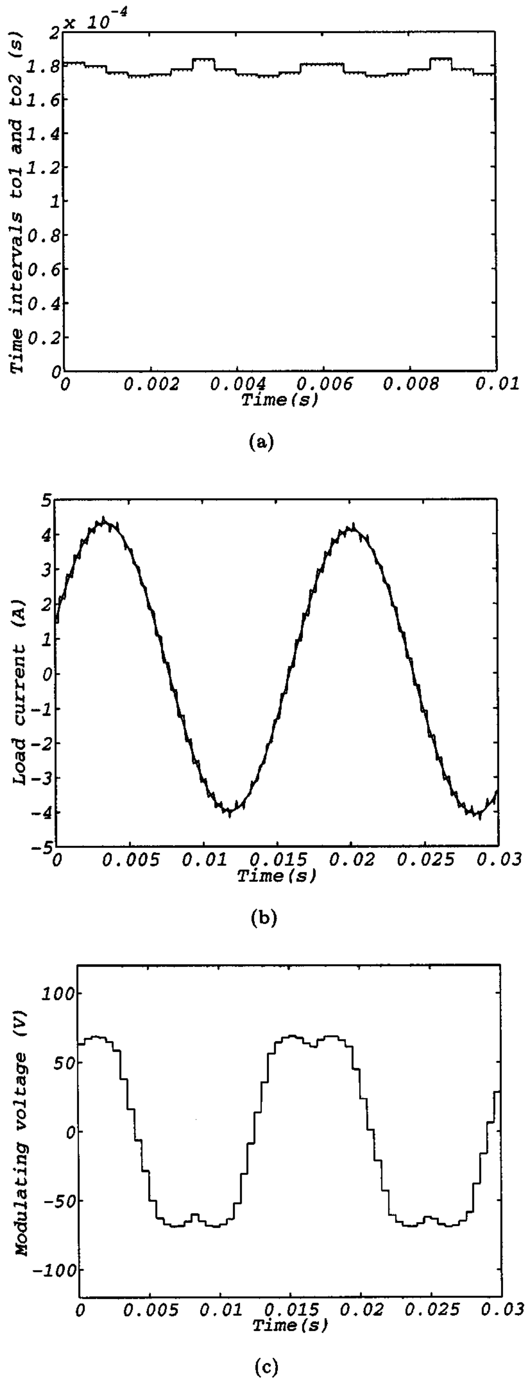

Fig. 9. Simulation results for $\mu = 0.5$. (a) Free-wheeling time intervals. (b) Load current. (c) Voltage $v_{s1}^{s*\prime}$.

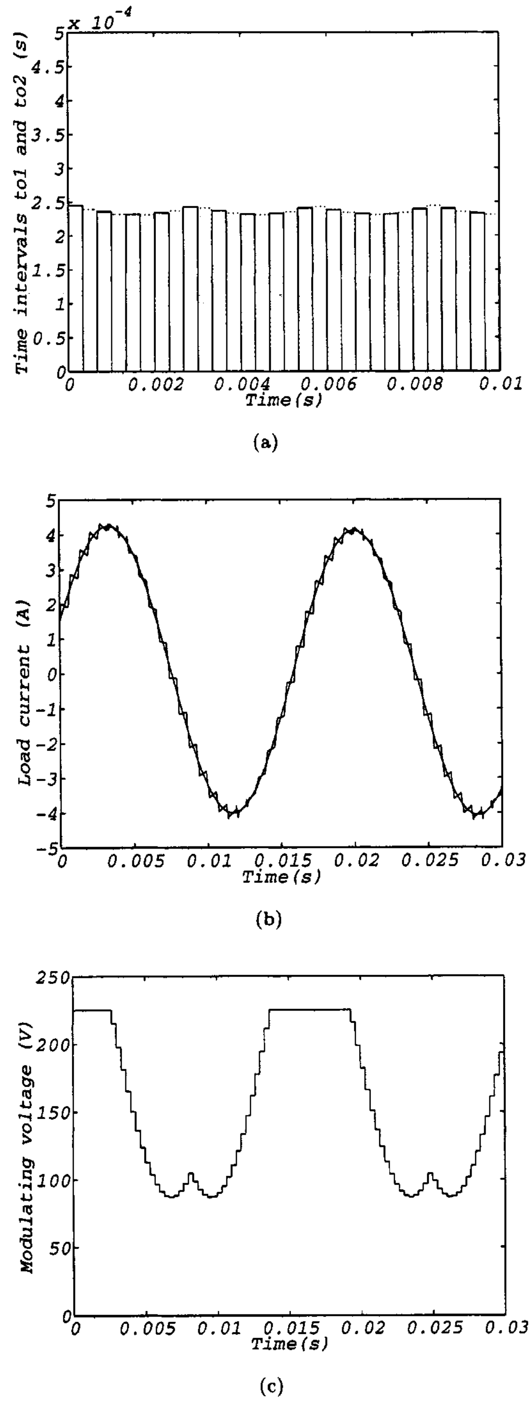

Fig. 10. Simulation results when one phase is clamped for $\mu = 0$. (a) Free-wheeling time intervals. (b) Load current. (c) Voltage $v_{s1}^{s*\prime}$.

e) calculating the modified time intervals $\tau_1' = \tau_1 + \tau_h$, $\tau_2' = \tau_2 + \tau_h$ and $\tau_3' = \tau_3 + \tau_h$;

f) programming the three timers associated with each phase with values τ_1', τ_2' and τ_3'.

It can be noted that the technique of reversing the pattern in the next sampling interval can also be used. In this case the calculated values of t_{o1} and t_{o2} are valid for the first sampling interval. In the second interval, to achieve the reversing, the calculated values of t_{o1}' and t_{o2}' are interchanged as illustrated in Figs. 3 and 4.

VI. Hardware Implementation

The hardware implementation of the idea outlined in Sections III and IV, consists in synthesizing the zero-sequence component, v_h, to be added to the three-phase reference signals. From (24), (25), (28), (29), and (11), it comes

$$v_h = E\left(\tfrac{1}{2} - \mu\right) - (1-\mu)v_{sM}^{s*} - \mu v_{sm}^{s*} \qquad (30)$$

where v_{sM}^{s*} and v_{sm}^{s*} are the maximum and the minimum values, respectively.

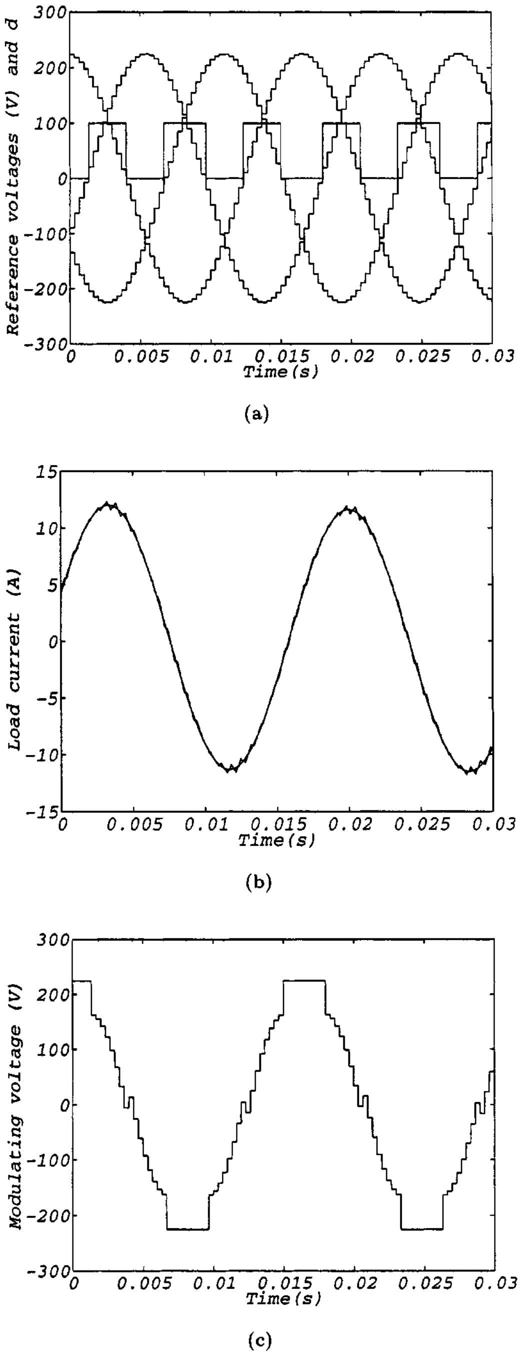

Fig. 11. Simulation results when one phase is clamped for $\mu = d$. (a) Reference voltages and signal $d \times 100$. (b) Load current. (c) Voltage $v_{s1}^{s*\prime}$.

Since v_{sM}^{s*} and v_{sm}^{s*} are directly related to τ_M and τ_m, respectively, those values can be determined by the logic signals a_1, a_2 and a_3 that identify the OVS. Therefore, in either hardware or digital version of the modulator, it is established that: $a_1 = 1$ if $v_{s1}^{s*} \geq v_{s2}^{s*}$, $a_1 = 0$ if $v_{s1}^{s*} < v_{s2}^{s*}$; $a_2 = 1$ if $v_{s2}^{s*} \geq v_{s3}^{s*}$, $a_2 = 0$ if $v_{s2}^{s*} < v_{s3}^{s*}$; and $a_3 = 1$ if $v_{s3}^{s*} \geq v_{s1}^{s*}$, $a_3 = 0$ if $v_{s3}^{s*} < v_{s1}^{s*}$.

Fig. 8 illustrates the hardware structure of the proposed modulator. The analog switches used to determine v_{sM}^{s*} and v_{sm}^{s*} from the three-phase references, are controlled by boolean expressions of logic signals a_1, a_2 and a_3. For example, $P_m = 1$ in OVS(1) and OVS(2) where v_{sm}^{s*} has the smallest value among the references [see Fig. 7(b)].

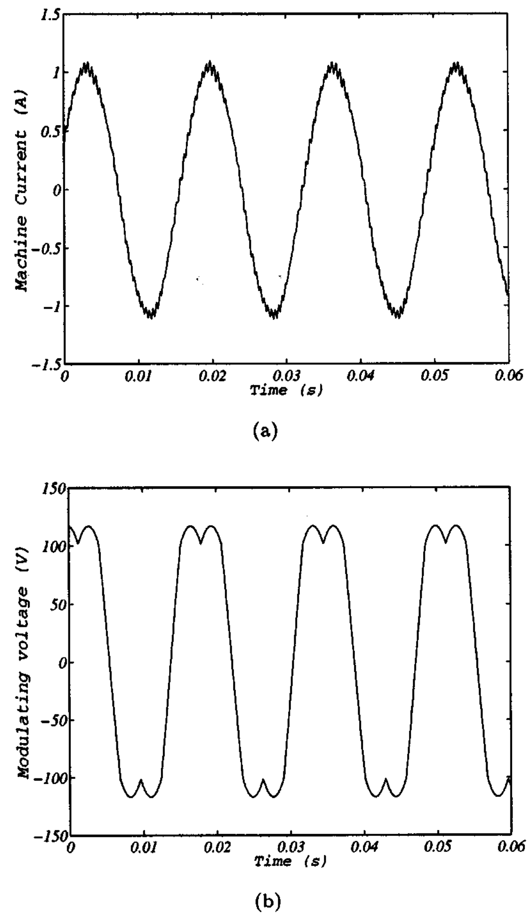

Fig. 12. Experimental results for $\mu = 0.5$. (a) Machine current. (b) Voltage $v_{s1}^{s*\prime}$.

The boolean expressions used to control the analog switches of Fig. 7 are given by

$$M_M = a_1\overline{a_3}, \quad N_M = \overline{a_1}a_2, \quad P_M = \overline{a_2}a_3$$

and

$$M_m = \overline{a_1}a_3, \quad N_m = a_1\overline{a_2}, \quad P_m = a_2\overline{a_3}.$$

The structure with analog switches in Fig. 8, replaces the sorting bridge in the modulators presented in [13] and [14]. These simple digital blocks can be easily implemented as an specialized integrated circuit.

VII. Simulation Results

The DSPWM algorithm was validated by simulation tests for a three-phase RL load ($R = 1\ \Omega$ and $L = 10$ mH). Figs. 9 and 10 show the free-wheeling time intervals t_{o1} and t_{o2}, the stator current, i_{s1}^s, and the modulating voltage, $v_{s1}^{s*\prime}$, obtained by simulation with the algorithm of the DSPWM. Fig. 9 corresponds to the case where $\mu = 0.5$ ($t_{o1} = t_{o2} = t_o/2$). Fig. 10 corresponds to the case in which one phase is clamped with $\mu = 0$. Fig. 11 shows the stator current, the modulating voltage and the reference voltages (v_{s1}^{s*}, v_{s2}^{s*}, v_{s3}^{s*}) and logic signal d ($\times 100$). In the test for Fig. 9 $\tau = 500\ \mu$s and in the test for Figs. 10 and 11 $\tau = 333\ \mu$s. For the results presented in Figs. 9 and 10, the modulation depth was $\pi\sqrt{2}/16$ [3]. For Fig. 11, the modulation

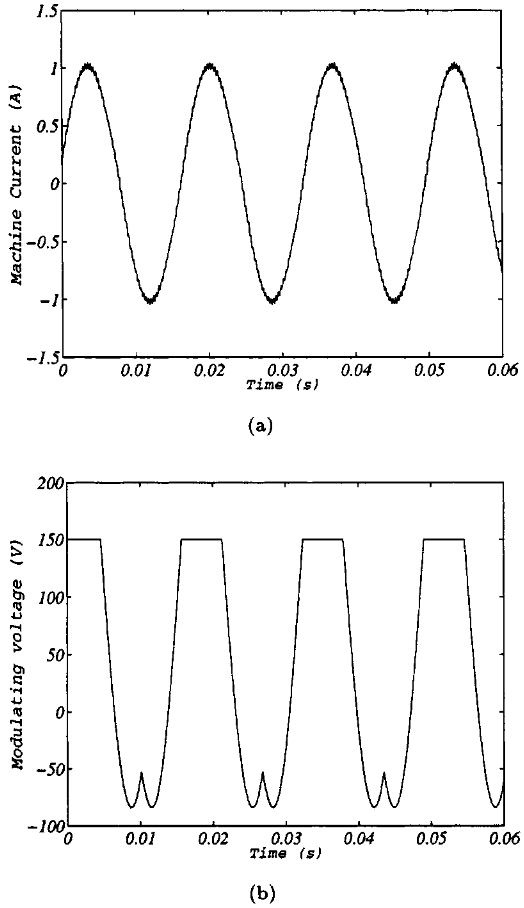

Fig. 13. Experimental results when one phase is clamped for $\mu = 0$. (a) Machine current. (b) Voltage $v_{s1}^{s*\prime}$.

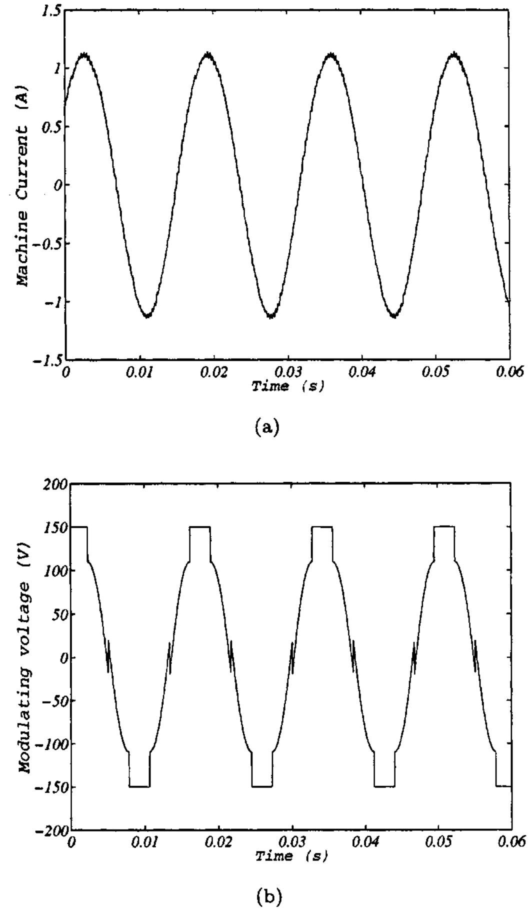

Fig. 14. Experimental results when one phase is clamped for $\mu = d$. (a) Machine current. (b) Voltage $v_{s1}^{s*\prime}$.

depth was $\pi/4$. In the case of Figs. 10 and 11 the switching frequency was increased by $3/2$ to make the power devices switch as fast as in the case of Fig. 9. For comparison purposes, the load current presented in these figures are superimposed to the ideal current waveforms (inner curve). The ideal waveforms were obtained by assuming the machine as supplied by a sinusoidal three-phase source. Note that the DSPWM imposes correctly the desired free-wheeling time intervals. One can observe by comparing the results of Figs. 9 and 10 that the current ripple has a minimum for $\mu = 0.5$, as expected for such modulation depth.

VIII. Experimental Results

Fig. 12 presents the machine voltage waveform obtained experimentally when an AC drive is used. The ac drive consists of a *Pentium* microcomputer equipped with a plug-in board, a three-phase six-switch (IGBT) inverter and a three-phase induction motor ($1/3CV$, $R_s = 26.8\ \Omega$, $R_r' = 26.8\ \Omega$, $L_{\sigma s} = 23$ mH, $L_{\sigma r}' = 23$ mH and $L_m = 0.5$ H). A programmable timer unit in the plug-in board generate the command signal to switch on and off the power switches.

Figs. 12–14 show $v_{s1}^{s*\prime}$ and i_{s1}^{s} with the real-time implementation of the DSPWM algorithm. Fig. 12 corresponds to the case where $\mu = 0.5$ and $\tau = 500\ \mu$s. Fig. 13 corresponds to the case when one phase is clamped for $\mu = 0$ and $\tau = 333\ \mu$s. For the results presented in Figs. 12 and 13, the modulation depth was $0.9\pi/4$. For Fig. 14, the modulation depth was $\pi/4$. One can also observe by comparing the experimental results of Figs. 12 and 13 that the current ripple has a minimum for $\mu = 0$, as expected for such modulation depth.

IX. Conclusions

This paper shows that it is possible to obtain the same results as those obtained with the space vector modulation by using a digital scalar modulation approach. Such equivalence was employed to propose a simple software algorithm to generate the space vector modulation from the scalar implementation. A simple hardware version of the proposed scheme was also presented. The proposed scheme provides a direct method to deal with nonsinusoidal modulating waveforms. The proposed scheme was evaluated mathematically and tested via computer simulations and experimental tests.

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