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Application Note

AN-Driver-TDA21102 / TDA21106

TDA21102 / TDA21106

TDA21102 / TDA21106 - Application Information

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Power Management & Supply

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Contents:

1 Short Description

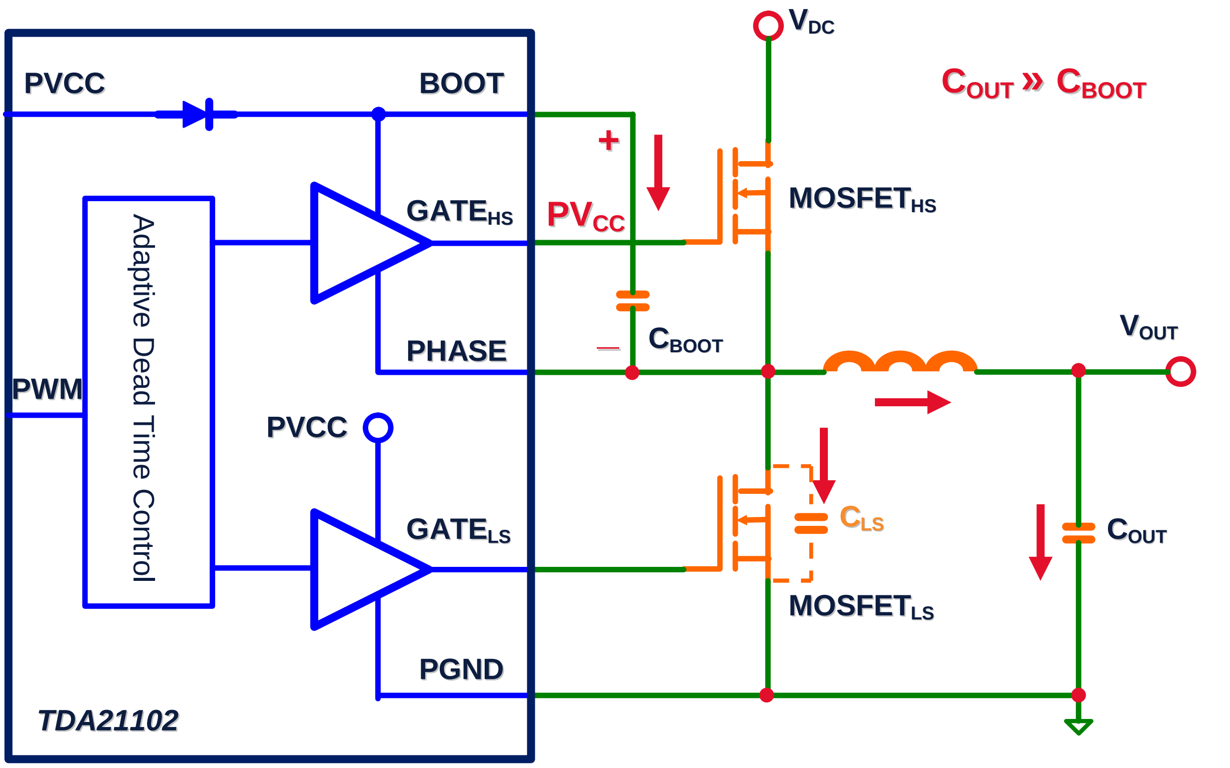
The dual phase high speed driver **TDA21102** is designed to drive a wide range of N-Channel low side and N-Channel high side MOSFETs with varying gate charges and it's counterpart is **TDA21106** which is the single phase MOSFET driver . It has less propagation delay from input to output, shorter rise and fall times and the same pin configuration as the HIP6602B. (TDA21106 is pin compatible with HIP6601B.) A circuit designer can fully take advantage of the driver´s capabilities in high-efficiency, high-density synchronous DC/DC converters that operate at high switching frequencies, e.g. in multi-phase converters for CPU supplies on motherboards and VRM´s but also in motor drive and class-D amplifier type applications.

The high breakdown voltage makes it suitable for Notebook applications as well.

2 Useful Application Information:

High-Side Driver

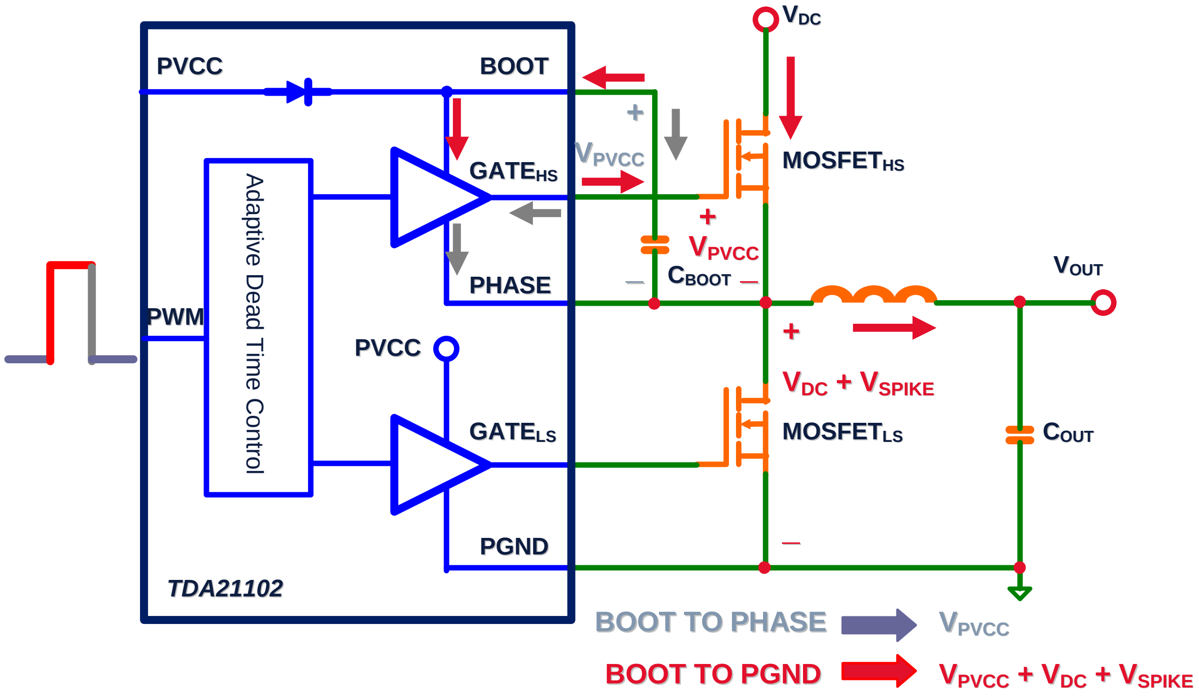
The high-side driver is designed to drive a floating low gate charge N-channel MOSFET. The gate voltage for the high-side driver is established by an external bootstrap supply circuit, which is a bootstrap capacitor connected between the **BOOT** and **PHASE** pins. The bootstrap diode is integrated in the chip itself. When the **TDA21102** is initiated, the bootstrap capacitor, $\mathbf{C_{BOOT}}$ will be charged up to $\mathbf{V_{PVCC}}$ through the integrated bootstrap diode because of $C_{BOOT} \ll C_{OUT}$.



$$V_{BOOT} = V_{PVCC} \times \frac{(C_{LS} + C_{OUT})}{C_{BOOT} // (C_{LS} + C_{OUT})}, \quad \because C_{OUT} >> C_{LS} \quad \therefore V_{BOOT} = V_{PVCC} \times \frac{C_{OUT}}{C_{BOOT} + C_{OUT}}$$

$$\because C_{OUT} >> C_{BOOT}, \quad \therefore V_{BOOT} \cong V_{PVCC} \times \frac{C_{OUT}}{C_{OUT}} = V_{PVCC}$$

When the **PWM** input goes high, the high-side driver will begin to turn on the high-side MOSFET, **MOSFET$_{HS}$**, by injecting the charges of **C$_{BOOT}$** into its Ciss. The voltage at the **PHASE** pin will begin to rise up to **V$_{DC}$** once the V_{GS} of **MOSFET$_{HS}$** reaches its threshold voltage and the voltage at the **BOOT** pin shall be pulled up to **V$_{DC}$ + V$_{PVCC}$**, which is enough V_{GS} to hold **MOSFET$_{HS}$** with low Rds(on). When the **PWM** goes low to complete the cycle, **MOSFET$_{HS}$** is switched off by pulling the gate down to the voltage at the **PHASE** pin. After **MOSFET$_{HS}$** is completely off, the voltage across the inductor is reversed due to the Lenz's Law. Then the inductor current is flowing through **C$_{OUT}$** and the body diode of **MOSFET$_{LS}$**. When the low-side MOSFET, **MOSFET$_{LS}$**, turns on, the **PHASE** pin is pulled to ground. This allows the **C$_{BOOT}$** to be charged up to **V$_{PVCC}$** again. The **GATE$_{HS}$** is in phase with the **PWM**. When the driver is disabled, the **GATE$_{HS}$** is held low. For **PVCC** of the **TDA21102**, a local bypass capacitor is recommended and it should be kept as close as possible to the **TDA21102.**Low ESR MLCC capacitor offers the best combination of ESR and size.



Bootstrap

The bootstrap diode has been integrated in the driver, so the designer just simply places an external bootstrap capacitor, **C$_{BOOT}$** across the **BOOT** pin and **PHASE** pin for the charge storage.
Selection of **C$_{BOOT}$** can be done after the high-side MOSFET has been chosen. The selected bootstrap capacitor must have a voltage rating that is able to handle the supply voltage, **V$_{PVCC}$**. The capacitance is determined using the following equation.

$$C_{BOOT} \geq Q_{MOSFETHS} \div \Delta V_{GS}$$

, where ***Q$_{MOSFETHS}$*** is the total gate charge of the high-side MOSFET required, and D**V$_{BOOT}$** is the voltage droop allowed on the bootstrap capacitor or let's say on the gate of high side MOSFET. For example, an IPD13N03LA has a total gate charge of about 20 nC at 12V V_{GS}. For an allowed droop of 200 mV, the required bootstrap capacitance is 100 nF. A good quality ceramic capacitor should be used.

Low-Side Driver

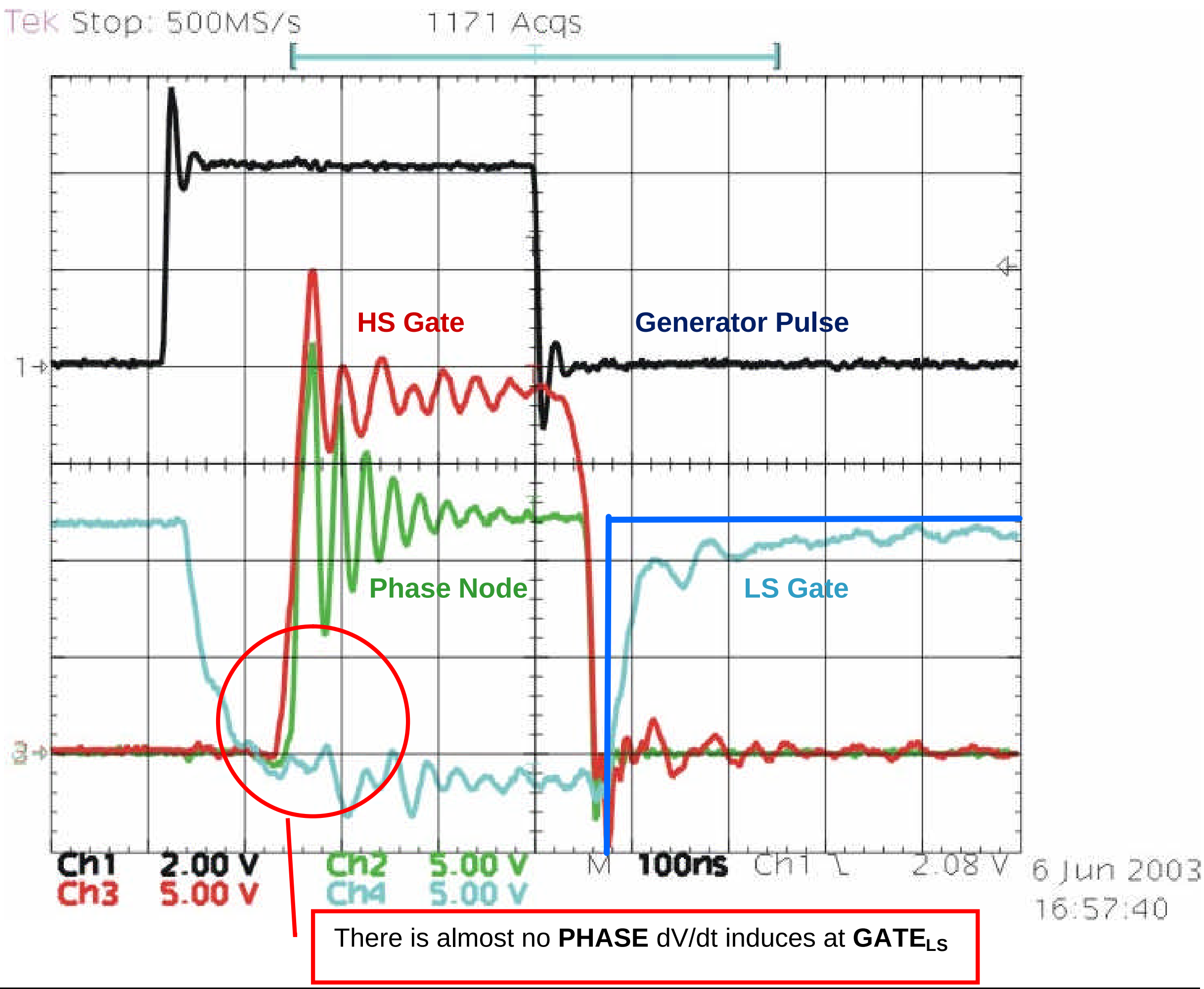
The low-side driver is designed to drive a very low RDS(ON) N-channel MOSFET which is referenced to ground. The driving voltage is internally connected to the **PVCC** supply which is normally +12V. (For TDA21106 it is connected to **VCC** which is normally +12V as well.)

dV/dt Noise Immunity

Under the higher input voltages, $\mathbf{V_{DC}}$, with a fast turn-on high-side MOSFET could momentarily turn on the low-side MOSFET due to the high dV/dt appearing at **PHASE**. This very high dV/dt shall induce a voltage at the VGS of low side MOSFET through a current flowing into the Miller capacitance, C_{GD} or Crss and the C_{GS} capacitance of the low-side MOSFET. Improper selection of the low-side MOSFET that has a higher ratio of Qgd/Qgs_1 makes the problem worst.

Test Condition : Vin = 12V, Vout = 1,3V, Iout = 20A / phase,

Driver : TDA21106, HS : BSC038N03L x 1, LS : BSC022N03 x 2,



To avoid this problem, there are several things necessary to be cared as listing below,

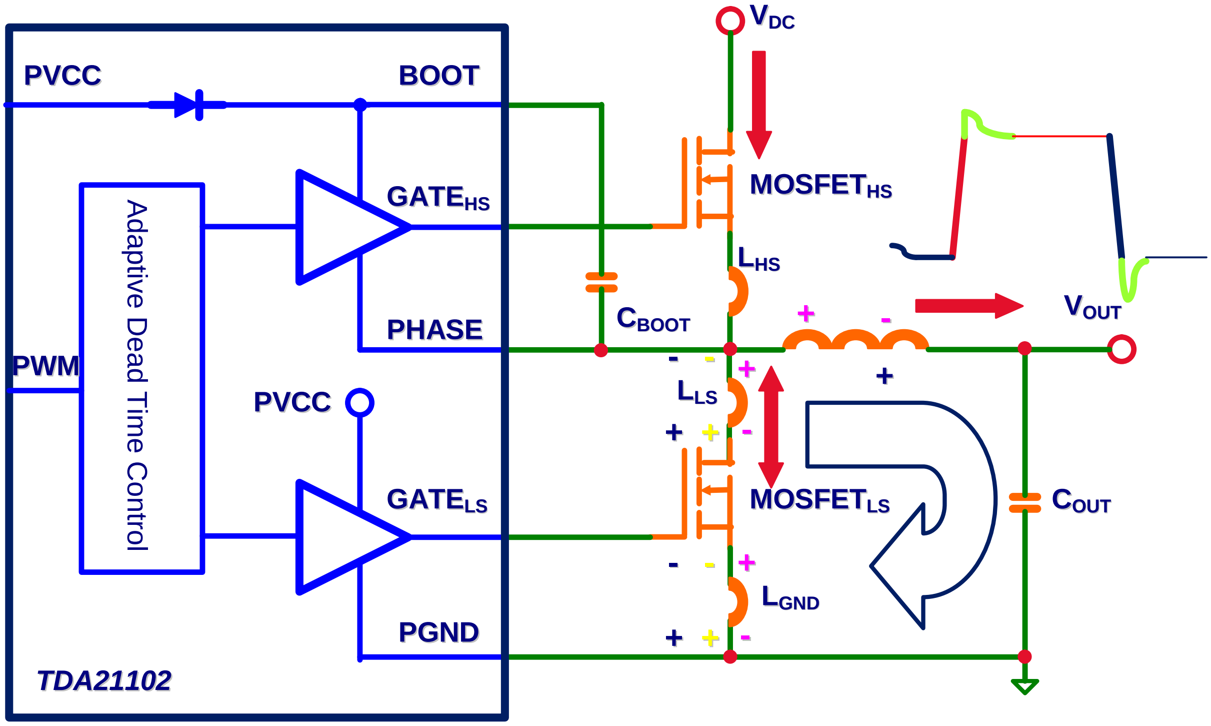
- Paying special attention on the ratio of Qgd/Qgs_1 while selecting the low-side MOSFET.
- Proper routing of the trace of $\mathbf{GATE_{LS}}$ can not worsen the situation. It is necessary to keep his trace wide and short with lower impedance.
- Normally the MOS IC process at the output driver stage shall be helpful compared to bipolar process in this case since there is certain voltage drop on the V_{CE} of bipolar transistor.
- Adding a capacitor at the gate to the source of the high-side MOSFET has the same effect.
- Adding a resistor between the $\mathbf{GATE_{HS}}$ and the gate of high side MOSFET can slow down the dV/dt slew rate at the **PHASE**. Additional reverse diode can be added for speeding the turn-off of the high side MOSFET.

However, the last two methods are increasing the switching losses.

PHASE

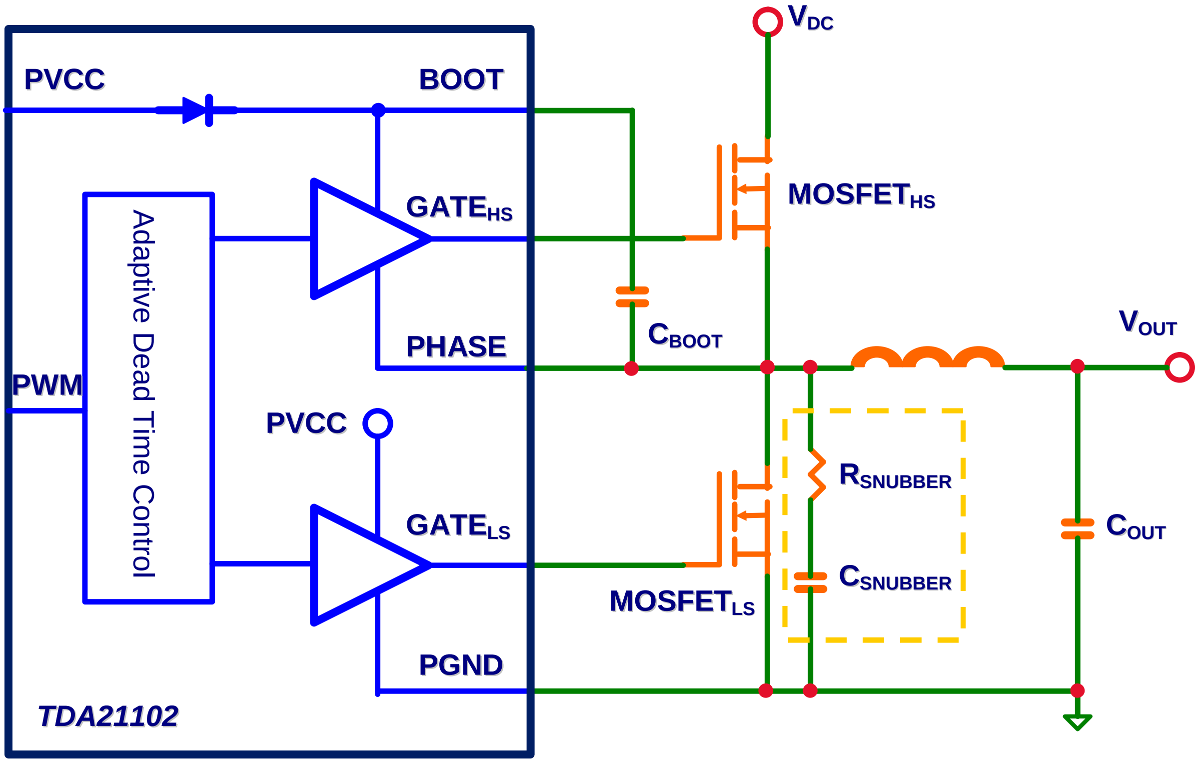
.

This pin is the conjunction of the source pin of high side MOSFET, drain pin of the low side MOSFET and the output inductor. The parasitic inductances due to the PCB routing traces and the package of the power devices shall generate the voltage spike ringing during high side MOSFET turn-on and the negative spike ringing at the trailing edge of the **PHASE**. Both of the voltage spikes should be taken care in a proper way to make sure that the voltage spike is not over the specification of both the driver IC and MOSFETs.



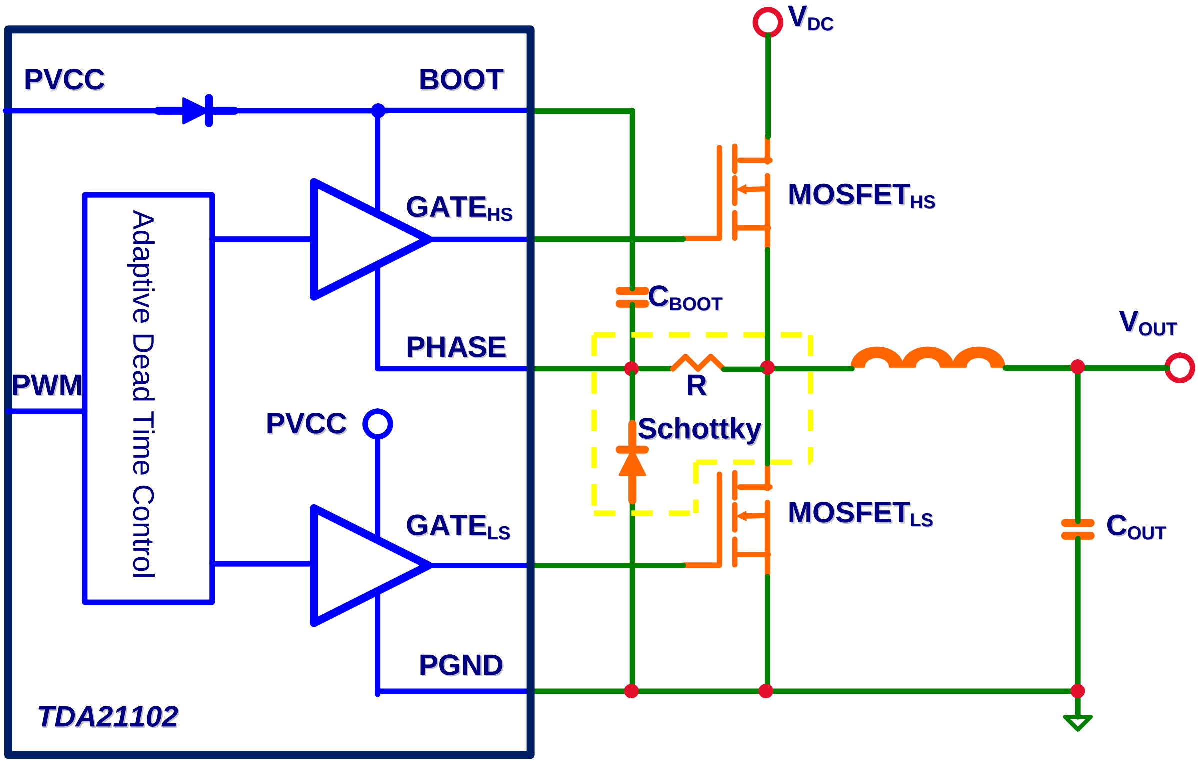
The Positive Voltage Spike at PHASE

This voltage spike shall stress the voltage at drain to source of the low side MOSFET and at both of **PHASE** and **BOOT** of the driver IC. Usually a RC snubber circuit is placed at the **PHASE** to **PGND** to absorb the energy of the spike. A zener diode or TVS (Transient Voltage Supressor) can be used for limiting the spike here but the are more costly.



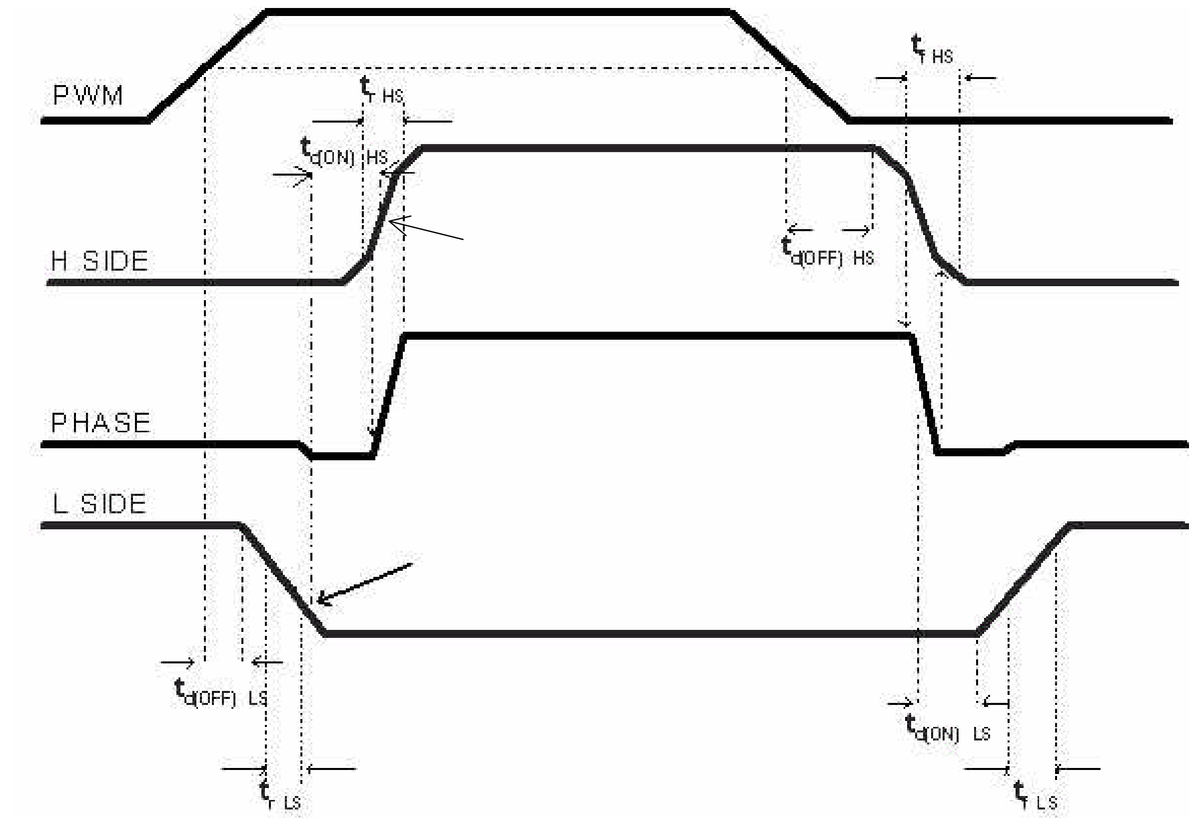
The Negative Voltage Spike at PHASE

The negative spike voltage shall force the **BOOT** to **PHASE** voltage increasing. This should be specially taken care if the higher bootstrap voltage is in use. The internal ESD diode at the **PHASE** shall clamp this negative voltage with dissipating certain amount of power on this diode. Proper layout and the reduction of package inductance in the MOSFETs can minimize the ringing. Usually a resistor and a schottky diode placed at the conjunction of MOSFETs and output inductor to **PGND** for further clamping this negative voltage spike. The Schottky diode recommended should be placed as close to **PHASE** and **PGND** of driver IC as possible.

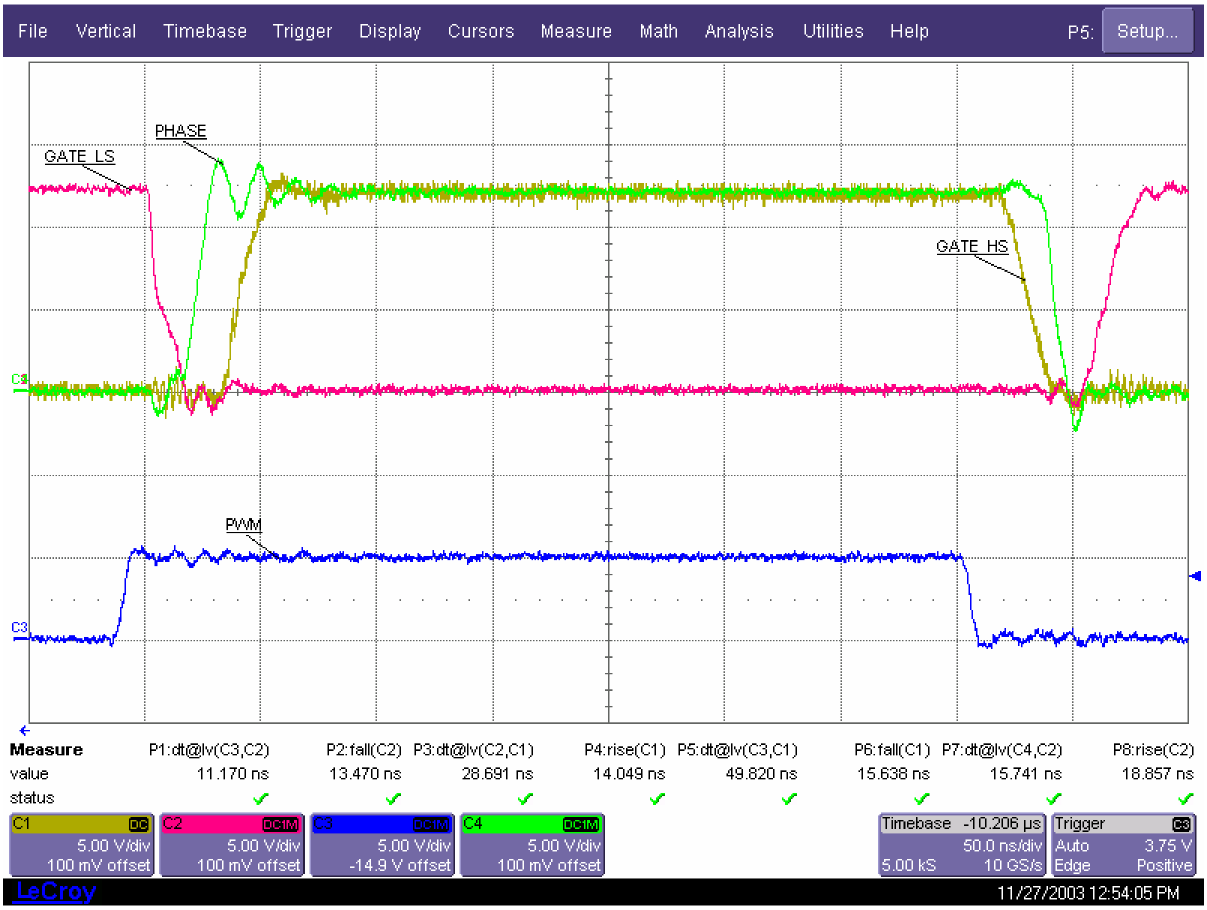


Operation Timing Diagram

At rising edge of **PWM** signal it initiates the turn-off of the low side MOSFET. After a short propagation delay time, $\mathbf{t_{d(off)\ LS}}$, the lower gate starts to fall. Typical fall time, $\mathbf{t_{f\ LS}}$ is specified in the Electrical Specifications. Adaptive shoot-through circuitry monitors the **Gate** $_{\mathbf{LS}}$ voltage and determines the starting point of the upper gate delay time, $\mathbf{t_{d(on)\ HS}}$ based on how fast the **Gate** $_{\mathbf{LS}}$ voltage drops below 1V. This prevents both the lower and upper MOSFETs from cross conducting or shoot-through. At the end of the delay time, the upper gate drive **Gate** $_{\mathbf{HS}}$ begins to rise and the upper MOSFET turns on when the voltage is above its threshold voltage. The rise time of high side MOSFET, $\mathbf{t_{r\ HS}}$ is specified in the Electrical Specifications. The falling edge of PWM initiates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay $\mathbf{t_{d(off)\ HS}}$ is encountered before the upper gate starts to fall $\mathbf{t_{f\ HS}}$. Again, the adaptive shoot-through circuitry determines the lower gate delay time, $\mathbf{t_{d(on)\ LS}}$. The **PHASE** voltage is monitored and the **Gate** $_{\mathbf{LS}}$ is allowed to rise only when the **PHASE** voltage drops below 2V typically. The **Gate** $_{\mathbf{LS}}$ rises and starts to turn the low side MOSFET on when the **Gate** $_{\mathbf{LS}}$ reaches the threshold voltage of low side MOSFET. The rise time of low side MOSFET, $\mathbf{t_{r\ LS}}$ is specified in the Electrical Specifications.



The following scope shoot is the real board measurement with IPD09N03LA as high side switch and IPD06N03LA as the low side switch.



Adaptive Shoot-Through Protection

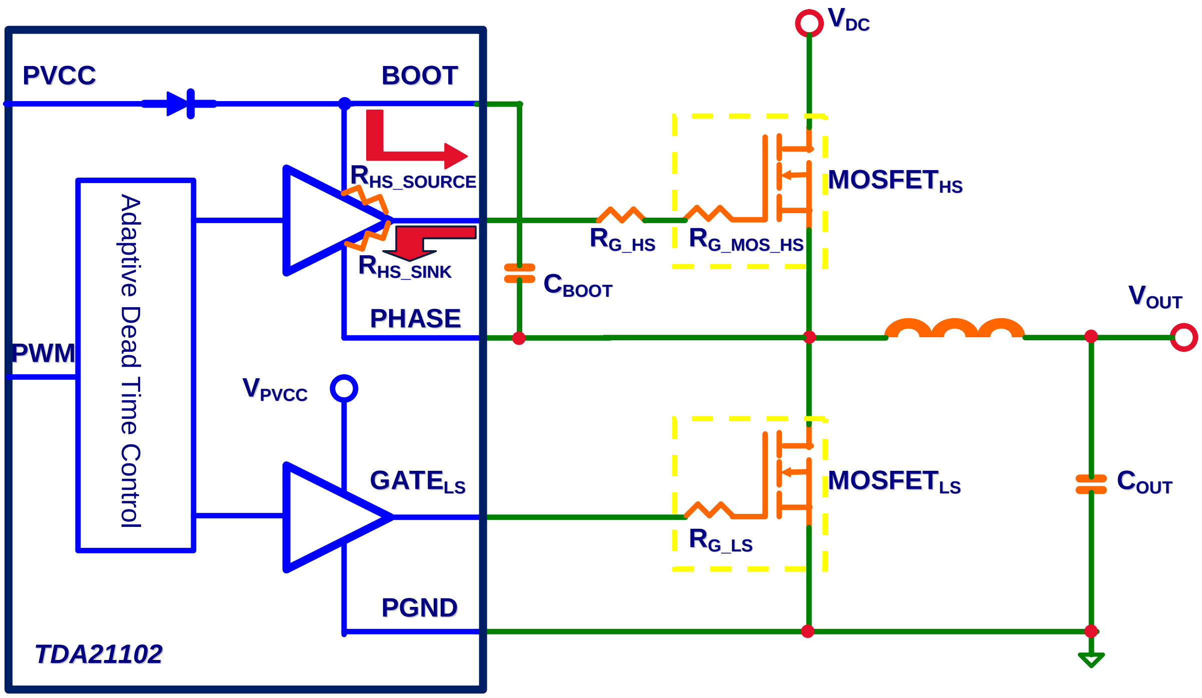
Both high side and low side drivers incorporate adaptive shoot-through protection to **MOSFET$_{HS}$** and **MOSFET$_{LS}$** from on at the same time and shorting the **V$_{DC}$** to ground. This is achieved by ensuring the either **GATE$_{HS}$** or **GATE$_{LS}$** has been in the low state before the other is allowed to rise. During turn-off of the **MOSFET$_{LS}$**, the **GATE$_{LS}$** is monitored until it is below 2V typically. After a certain delay time, td(on) $_{HS}$, the **GATE$_{HS}$** is begin to rise. Adaptive shoot-through circuit monitors the **PHASE** voltage during **GATE$_{HS}$** turn-off. Once **PHASE** voltage has dropped below 2V typically, the **GATE$_{LS}$** is allowed to rise.

Tri-State PWM Input

TDA-21102 offers a shutdown window to the **PWM**. If the **PWM** signal enters and remains within the shutdown window which is normally 1.45V ~ 3.6V for a set hold-off time, 230nS typically, the output drivers shall be disabled and both MOSFET gates, **GATE$_{HS}$** and **GATE$_{LS}$**, are held low. The shutdown state is removed when the **PWM** signal moves out of the shutdown window. Otherwise, the **PWM** rising and falling thresholds specified in the ELECTRICAL SPECIFICATIONS determine when the **GATE$_{HS}$** and **GATE$_{LS}$** are enabled.

There is an additional feature at **PWM** input. The high side gate is not going to be on if the **PWM** pulse width is less than 40 nS. The following scope shoots shall show this behavior.

Power Dissipation and thermal consideration :



$$P * T = 0.5 * Q_G * V_{GS} \Rightarrow P = 0.5 * Q_G * V_{GS} * f_{SW}$$

High Side Driver Losses :

$$P_{HS\_DRIVER\_SOURCE} = 0.5 * Q_{G\_MOSFET\_HS} * f_{SW} * V_{PVCC} * (R_{HS\_SOURCE} / (R_{HS\_SOURCE} + R_{G\_HS} + R_{G\_MOS\_HS}))$$

$$P_{HS\_DRIVER\_SINK} = 0.5 * Q_{G\_MOSFET\_HS} * f_{SW} * V_{PVCC} * (R_{HS\_SINK} / (R_{HS\_SINK} + R_{G\_HS} + R_{G\_MOS\_HS}))$$

Low Side Driver Losses :

$$P_{LS\_DRIVER\_SOURCE} = 0.5 * Q_{G\_MOSFET\_LS} * f_{SW} * V_{PVCC} * (R_{LS\_SOURCE} / (R_{LS\_SOURCE} + R_{G\_LS} + R_{G\_MOS\_LS}))$$

$$P_{LS\_DRIVER\_SINK} = 0.5 * Q_{G\_MOSFET\_LS} * f_{SW} * V_{PVCC} * (R_{LS\_SINK} / (R_{LS\_SINK} + R_{G\_LS} + R_{G\_MOS\_LS}))$$

Logic Circuit Losses :

$$P_{VCC} = V_{VCC} * I_{VCC}$$

Total Driver Losses :

$$P_{DRIVER} = 2 * (P_{HS\_DRIVER\_SOURCE} + P_{HS\_DRIVER\_SINK} + P_{LS\_DRIVER\_SOURCE} + P_{LS\_DRIVER\_SINK}) + P_{VCC}$$

Junction Temperature Calculation :

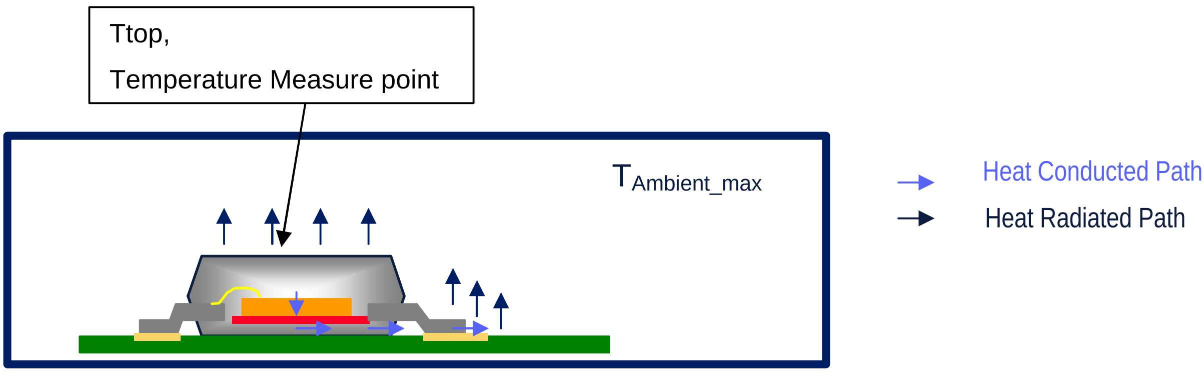
$$T_j = T_{Ambient} + P_{DRIVER} * \theta_{jc}$$

T_j : Calculated working junction temperature. It can not be higher than the maximum allowed working junction temperature given in the datasheet

$T_{Ambient}$: Ambient temperature measured

θ_{jc} : Given IC junction to case thermal resistance

P_{DRIVER} : Calculated driver IC losses



Quick Device Temperature Measurement and Junction Temperature Calculation

If the temperature is measured on the top of the package which is the most easier way to measure the temperature of the device, the junction temperature can be calculated by the following formula.

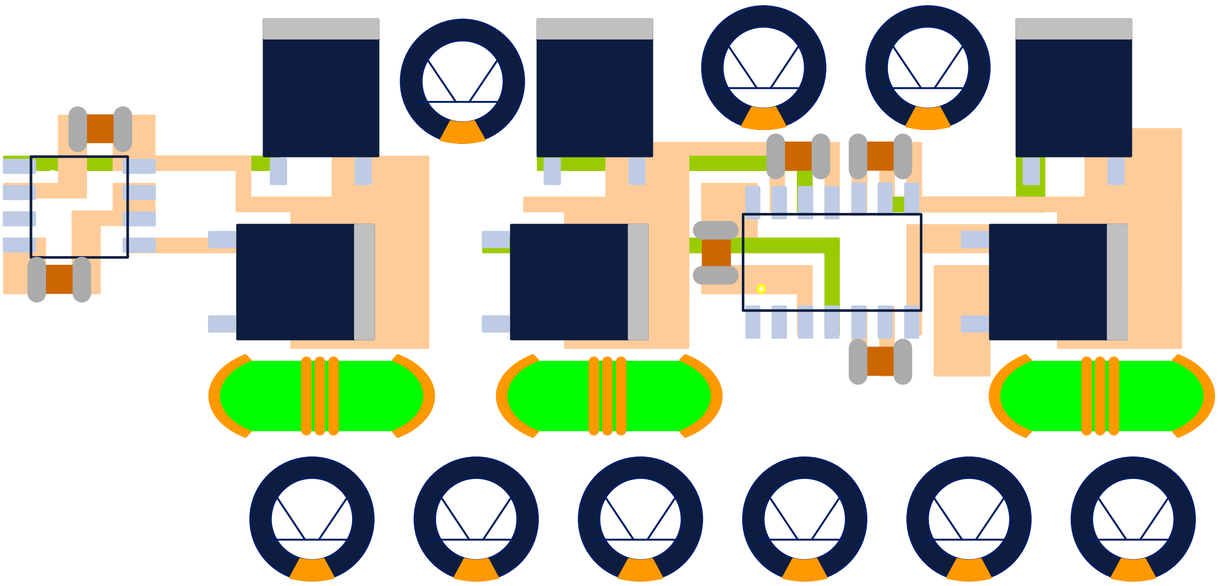
$$\Upsilon_{JT} = (T_{junction} - T_{top}) / P_{DRIVER}$$

Attention: Ψ_{JT}: is 4,3 K/W for TDA21102 in P-DSO-14-3 package but it is not a thermal resistance !

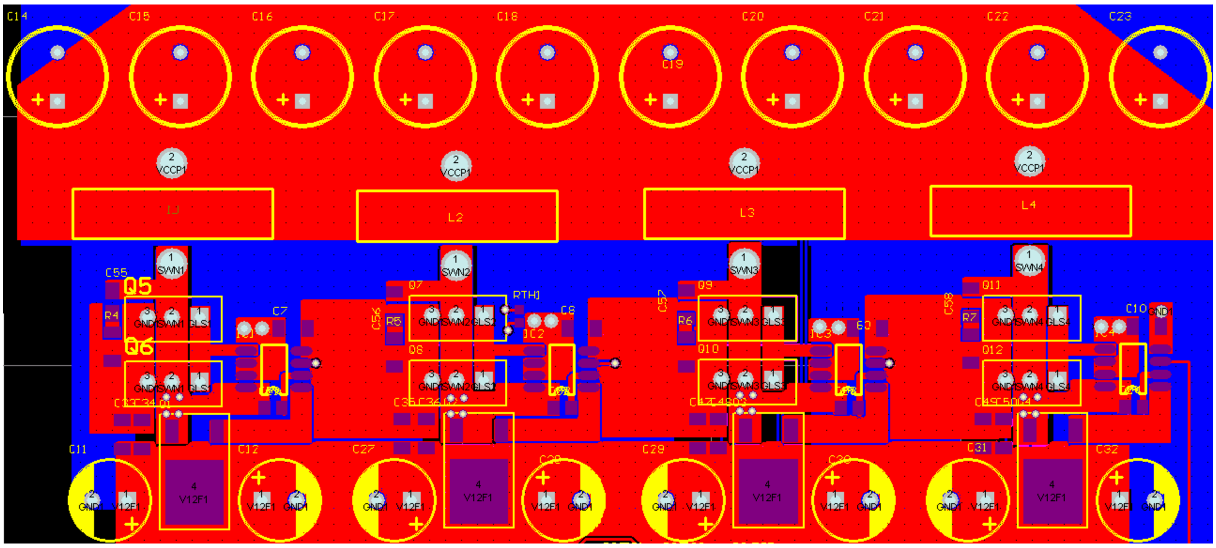
Component Placement and Layout suggestion :

- Both of the decoupling capacitors for VCC and PVCC should be placed as close to the driver IC as possible.
- The bootstrap capacitor should be placed close to the **BOOT** pin.
- The traces of **GATE**$_{HS}$ and **PHASE** should be routed in parallel and to keep it short and wide. The width of the trances should be no less than 40mils.
- High current loops from the input capacitor, high side MOSFET, output inductors and output capacitors back to the input capacitor negative terminal should be kept the distance minimized.
- The conjunction of high side MOSFET, low side MOSFET and output inductor should be kept as close as possible.

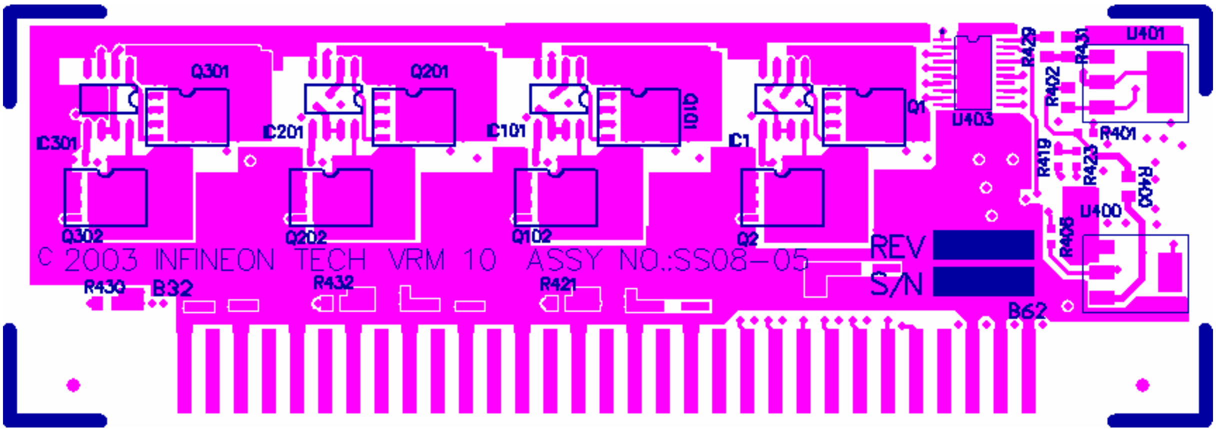
Eexample 1 : TDA21106 x 1 + TDA21102 x 1 (DPAK or D^{2}PAK MOSFET)



Example 2 : TDA21106 x 4 (HS : DPAK x 1 + LS : IPAK x 2)



Example 3 : TDA21106 x 4 (HS : SS08 x 1 + LS : SS08 x 1)



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[1] **Infineon Technologies AG:** TDA21106 – High Speed Driver With Bootstrapping For Dual Power MOSFETs ; Data sheet Rev1,1 ; Infineon Technologies AG; Munich; Germany; 09/03.

[2] **Infineon Technologies AG:** TDA21102 – High Speed Driver With Bootstrapping For Dual Power MOSFETs ; Data sheet Rev1,0 ; Infineon Technologies AG; Munich; Germany; 12/03.

[3] **Intersil Coroperation:** HIP6601B – Synchronous Rectified Buck MOSFET Drivers ; Data Sheet; Intersil Coroperation ; Irvine, CA USA; 04/02.

[4] **Intersil Coroperation:** HIP6602B – Synchronous Rectified Buck MOSFET Drivers ; Data Sheet; Intersil Coroperation ; Irvine, CA USA; 03/02..

[5] **Maxim Integrated Products:** MAX8523 – High Speed Dual Phase Gate Driver for Multi-phase Step-down Converter ; Data Sheet; Intersil Coroperation ; Sunnyvale, CA USA; 04/03..

[6] **Thomas Wu :** CDV/DT INDUCED TURN-ON IN SYNCHRONOUS BUCK REGULATORS ; Technical Paper ; International Rectifier ; El Segundo, CA USA.

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Page of actual Rel.	Page of prev. Rel.	Subjects changed since last release	

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