An Applications Guide for Op Amps

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Introduction

The general utility of the operational amplifier is derived from the fact that it is intended for use in a feedback loop whose feedback properties determine the feed-forward characteristics of the amplifier and loop combination. To suit it for this usage, the ideal operational amplifier would have infinite input impedance, zero output impedance, infinite gain and an open-loop 3 dB point at infinite frequency rolling off at 6 dB per octave. Unfortunately, the unit cost–in quantity–would also be infinite.

Intensive development of the operational amplifier, particularly in integrated form, has yielded circuits which are quite good engineering approximations of the ideal for finite cost. Quantity prices for the best contemporary integrated amplifiers are low compared with transistor prices of five years ago. The low cost and high quality of these amplifiers allows the implementation of equipment and systems functions impractical with discrete components. An example is the low frequency function generator which may use 15 to 20 operational amplifiers in generation, wave shaping, triggering and phase-locking.

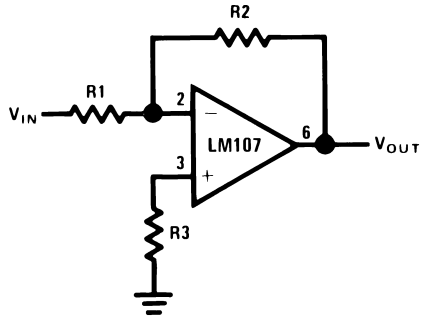
The availability of the low-cost integrated amplifier makes it mandatory that systems and equipments engineers be familiar with operational amplifier applications. This paper will present amplifier usages ranging from the simple unity-gain buffer to relatively complex generator and wave shaping circuits. The general theory of operational amplifiers is not within the scope of this paper and many excellent references are available in the literature.[1,2,3,4] The approach will be shaded toward the practical, amplifier parameters will be discussed as they affect circuit performance, and application restrictions will be outlined.

The applications discussed will be arranged in order of increasing complexity in five categories: simple amplifiers, operational circuits, transducer amplifiers, wave shapers and generators, and power supplies. The integrated amplifiers shown in the figures are for the most part internally compensated so frequency stabilization components are not shown; however, other amplifiers may be used to achieve greater operating speed in many circuits as will be shown in the text. Amplifier parameter definitions are contained in Appendix I.

The Inverting Amplifier

The basic operational amplifier circuit is shown in *Figure 1*. This circuit gives closed-loop gain of R2/R1 when this ratio is small compared with the amplifier open-loop gain and, as the name implies, is an inverting circuit. The input impedance is equal to R1. The closed-loop bandwidth is equal to the unity-gain frequency divided by one plus the closed-loop gain.

The only cautions to be observed are that R3 should be chosen to be equal to the parallel combination of R1 and R2 to minimize the offset voltage error due to bias current and that there will be an offset voltage at the amplifier output equal to closed-loop gain times the offset voltage at the amplifier input.



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$$V_{OUT} = \frac{R2}{R1} V_{IN}$$

$$R3 = R1 \parallel R2$$

For minimum error due to input bias current

FIGURE 1. Inverting Amplifier

Offset voltage at the input of an operational amplifier is comprised of two components, these components are identified in specifying the amplifier as input offset voltage and input bias current. The input offset voltage is fixed for a particular amplifier, however the contribution due to input bias current is dependent on the circuit configuration used. For minimum offset voltage at the amplifier input without circuit adjustment the source resistance for both inputs should be equal. In this case the maximum offset voltage would be the algebraic sum of amplifier offset voltage and the voltage drop across the source resistance due to offset current. Amplifier offset voltage is the predominant error term for low source resistances and offset current causes the main error for high source resistances.

In high source resistance applications, offset voltage at the amplifier output may be adjusted by adjusting the value of R3 and using the variation in voltage drop across it as an input offset voltage trim.

Offset voltage at the amplifier output is not as important in AC coupled applications. Here the only consideration is that any offset voltage at the output reduces the peak to peak linear output swing of the amplifier.

The gain-frequency characteristic of the amplifier and its feedback network must be such that oscillation does not occur. To meet this condition, the phase shift through amplifier and feedback network must never exceed 180° for any frequency where the gain of the amplifier and its feedback network is greater than unity. In practical applications, the phase shift should not approach 180° since this is the situation of conditional stability. Obviously the most critical case occurs when the attenuation of the feedback network is zero.

Amplifiers which are not internally compensated may be used to achieve increased performance in circuits where

The Inverting Amplifier (Continued)

feedback network attenuation is high. As an example, the LM101 may be operated at unity gain in the inverting amplifier circuit with a 15 pF compensating capacitor, since the feedback network has an attenuation of 6 dB, while it requires 30 pF in the non-inverting unity gain connection where the feedback network has zero attenuation. Since amplifier slew rate is dependent on compensation, the LM101 slew rate in the inverting unity gain connection will be twice that for the non-inverting connection and the inverting gain of ten connection will yield eleven times the slew rate of the non-inverting unity gain connection. The compensation trade-off for a particular connection is stability versus bandwidth, larger values of compensation capacitor yield greater stability and lower bandwidth and vice versa.

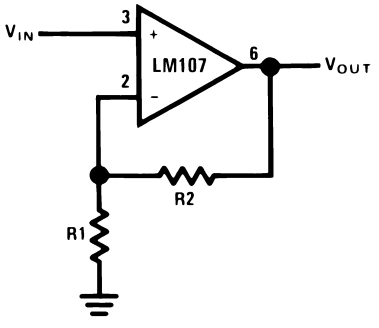
The preceding discussion of offset voltage, bias current and stability is applicable to most amplifier applications and will be referenced in later sections. A more complete treatment is contained in Reference 4.

The Non-Inverting Amplifier

Figure 2 shows a high input impedance non-inverting circuit. This circuit gives a closed-loop gain equal to the ratio of the sum of R1 and R2 to R1 and a closed-loop 3 dB bandwidth equal to the amplifier unity-gain frequency divided by the closed-loop gain.

The primary differences between this connection and the inverting circuit are that the output is not inverted and that the input impedance is very high and is equal to the differential input impedance multiplied by loop gain. (Open loop gain/Closed loop gain.) In DC coupled applications, input impedance is not as important as input current and its voltage drop across the source resistance.

Applications cautions are the same for this amplifier as for the inverting amplifier with one exception. The amplifier output will go into saturation if the input is allowed to float. This may be important if the amplifier must be switched from source to source. The compensation trade off discussed for the inverting amplifier is also valid for this connection.



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$$V_{OUT} = \frac{R1 + R2}{R1} V_{IN}$$

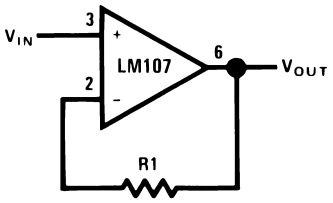
$R1 \parallel R2 = R_{SOURCE}$

For minimum error due to input bias current

FIGURE 2. Non-Inverting Amplifier

The Unity-Gain Buffer

The unity-gain buffer is shown in *Figure 3*. The circuit gives the highest input impedance of any operational amplifier circuit. Input impedance is equal to the differential input impedance multiplied by the open-loop gain, in parallel with common mode input impedance. The gain error of this circuit is equal to the reciprocal of the amplifier open-loop gain or to the common mode rejection, whichever is less.



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$V_{OUT} = V_{IN}$

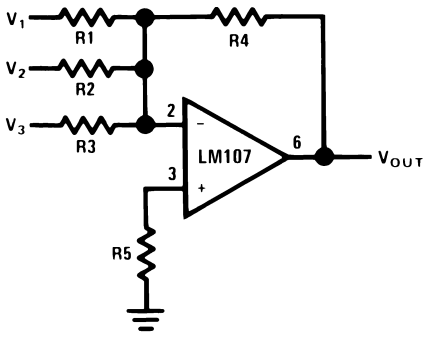
$R1 = R_{SOURCE}$

For minimum error due to input bias current

FIGURE 3. Unity Gain Buffer

Input impedance is a misleading concept in a DC coupled unity-gain buffer. Bias current for the amplifier will be supplied by the source resistance and will cause an error at the amplifier input due to its voltage drop across the source resistance. Since this is the case, a low bias current amplifier such as the LH102[6] should be chosen as a unity-gain buffer when working from high source resistances. Bias current compensation techniques are discussed in Reference 5.

The cautions to be observed in applying this circuit are three: the amplifier must be compensated for unity gain operation, the output swing of the amplifier may be limited by the amplifier common mode range, and some amplifiers exhibit a latch-up mode when the amplifier common mode range is exceeded. The LM107 may be used in this circuit with none of these problems; or, for faster operation, the LM102 may be chosen.



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$$V_{OUT} = -R4\left(\frac{V_1}{R1} + \frac{V_2}{R2} + \frac{V_3}{R3}\right)$$

$R5 = R1 \parallel R2 \parallel R3 \parallel R4$

For minimum offset error due to input bias current

FIGURE 4. Summing Amplifier

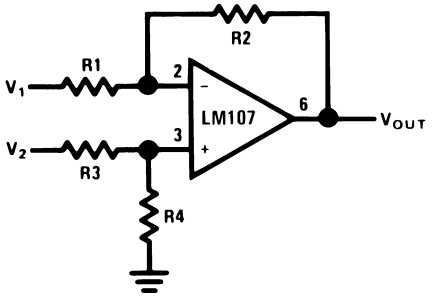
Summing Amplifier

The summing amplifier, a special case of the inverting amplifier, is shown in *Figure 4*. The circuit gives an inverted output which is equal to the weighted algebraic sum of all three inputs. The gain of any input of this circuit is equal to the ratio of the appropriate input resistor to the feedback resistor, R4. Amplifier bandwidth may be calculated as in the inverting amplifier shown in *Figure 1* by assuming the input resistor to be the parallel combination of R1, R2, and R3. Application cautions are the same as for the inverting amplifier. If an uncompensated amplifier is used, compensation is calculated on the basis of this bandwidth as is discussed in the section describing the simple inverting amplifier.

The advantage of this circuit is that there is no interaction between inputs and operations such as summing and weighted averaging are implemented very easily.

The Difference Amplifier

The difference amplifier is the complement of the summing amplifier and allows the subtraction of two voltages or, as a special case, the cancellation of a signal common to the two inputs. This circuit is shown in *Figure 5* and is useful as a computational amplifier, in making a differential to single-ended conversion or in rejecting a common mode signal.



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$$V_{OUT} = \left(\frac{R1 + R2}{R3 + R4}\right)\frac{R4}{R1}V_2 - \frac{R2}{R1}V_1$$

For R1 = R3 and R2 = R4

$$V_{OUT} = \frac{R2}{R1}(V_2 - V_1)$$

R1 || R2 = R3 || R4

For minimum offset error due to input bias current

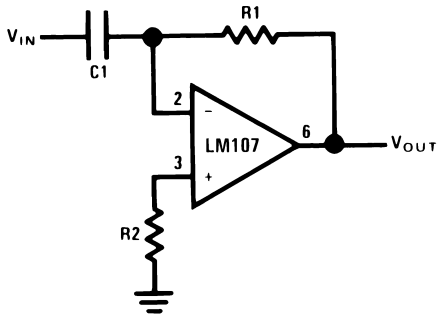
FIGURE 5. Difference Amplifier

Circuit bandwidth may be calculated in the same manner as for the inverting amplifier, but input impedance is somewhat more complicated. Input impedance for the two inputs is not necessarily equal; inverting input impedance is the same as for the inverting amplifier of *Figure 1* and the non-inverting input impedance is the sum of R3 and R4. Gain for either input is the ratio of R1 to R2 for the special case of a differential input single-ended output where R1 = R3 and R2 = R4. The general expression for gain is given in the figure. Compensation should be chosen on the basis of amplifier bandwidth.

Care must be exercised in applying this circuit since input impedances are not equal for minimum bias current error.

Differentiator

The differentiator is shown in *Figure 6* and, as the name implies, is used to perform the mathematical operation of differentiation. The form shown is not the practical form, it is a true differentiator and is extremely susceptible to high frequency noise since AC gain increases at the rate of 6 dB per octave. In addition, the feedback network of the differentiator, R1C1, is an RC low pass filter which contributes 90° phase shift to the loop and may cause stability problems even with an amplifier which is compensated for unity gain.



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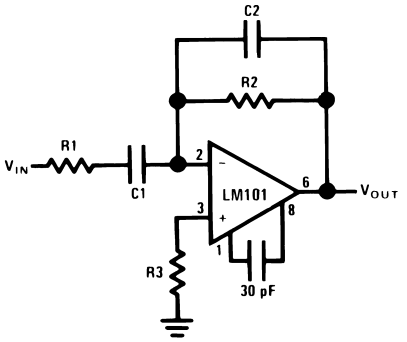
$$V_{OUT} = -R1C1\frac{d}{dt}(V_{IN})$$

R1 = R2

For minimum offset error due to input bias current

FIGURE 6. Differentiator



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$$f_c = \frac{1}{2\pi R2C1}$$

$$f_h = \frac{1}{2\pi R1C1} = \frac{1}{2\pi R2C2}$$

$$f_c \ll f_h \ll f_{unity\ gain}$$

FIGURE 7. Practical Differentiator

A practical differentiator is shown in *Figure 7*. Here both the stability and noise problems are corrected by addition of two additional components, R1 and C2. R2 and C2 form a 6 dB per octave high frequency roll-off in the feedback network and R1C1 form a 6 dB per octave roll-off network in the input network for a total high frequency roll-off of 12 dB per octave to reduce the effect of high frequency input and amplifier noise. In addition R1C1 and R2C2 form lead networks in the

Differentiator (Continued)

feedback loop which, if placed below the amplifier unity gain frequency, provide 90° phase lead to compensate the 90° phase lag of R2C1 and prevent loop instability. A gain frequency plot is shown in *Figure 8* for clarity.

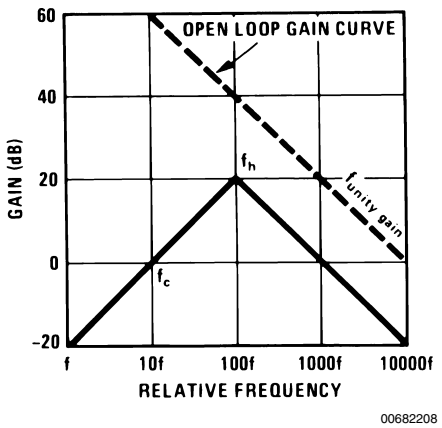
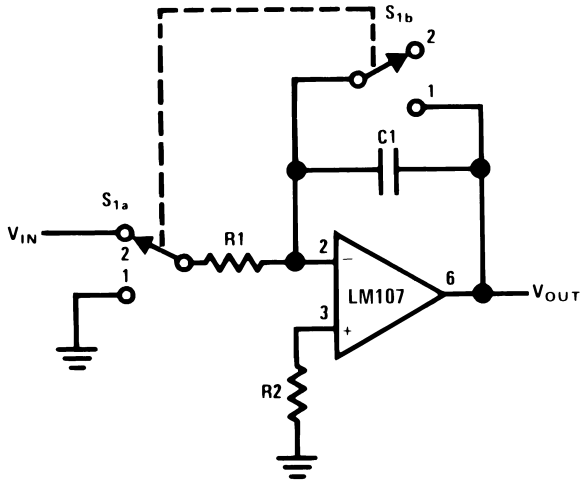


FIGURE 8. Differentiator Frequency Response

Integrator

The integrator is shown in *Figure 9* and performs the mathematical operation of integration. This circuit is essentially a low-pass filter with a frequency response decreasing at 6 dB per octave. An amplitude-frequency plot is shown in *Figure 10*.



$$V_{OUT} = \frac{1}{R1C1}\int_{t_1}^{t_2} V_{IN}\,dt$$

$$f_c = \frac{1}{2\pi R1C1}$$

$R1 = R2$

For minimum offset error due to input bias current

FIGURE 9. Integrator

Integrator (Continued)

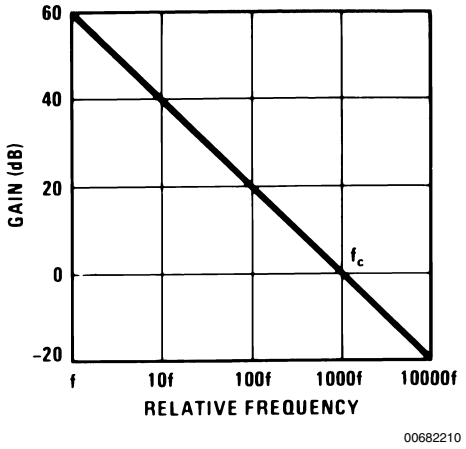


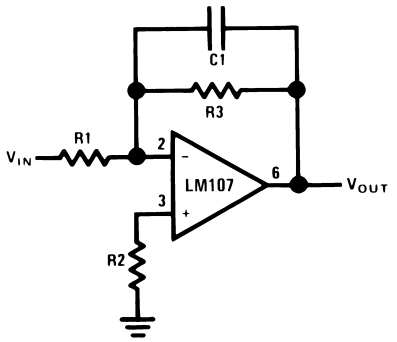
FIGURE 10. Integrator Frequency Response

The circuit must be provided with an external method of establishing initial conditions. This is shown in the figure as S_1. When S_1 is in position 1, the amplifier is connected in unity-gain and capacitor C1 is discharged, setting an initial condition of zero volts. When S_1 is in position 2, the amplifier is connected as an integrator and its output will change in accordance with a constant times the time integral of the input voltage.

The cautions to be observed with this circuit are two: the amplifier used should generally be stabilized for unity-gain operation and R2 must equal R1 for minimum error due to bias current.

Simple Low-pass Filter

The simple low-pass filter is shown in *Figure 11*. This circuit has a 6 dB per octave roll-off after a closed-loop 3 dB point defined by f_c. Gain below this corner frequency is defined by the ratio of R3 to R1. The circuit may be considered as an AC integrator at frequencies well above f_c; however, the time domain response is that of a single RC rather than an integral.



$$f_L = \frac{1}{2\pi R1C1}$$

$$f_c = \frac{1}{2\pi R3C1}$$

$$A_L = \frac{R3}{R1}$$

FIGURE 11. Simple Low Pass Filter

R2 should be chosen equal to the parallel combination of R1 and R3 to minimize errors due to bias current. The amplifier should be compensated for unity-gain or an internally compensated amplifier can be used.

Simple Low-pass Filter (Continued)

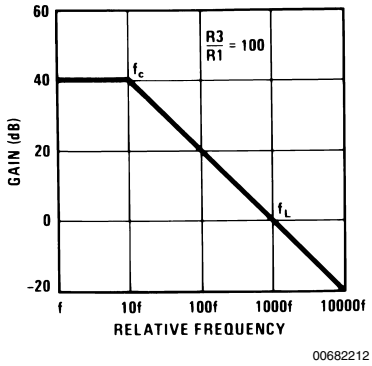


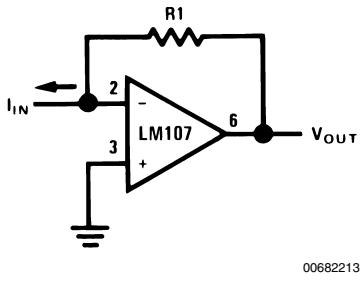
FIGURE 12. Low Pass Filter Response

A gain frequency plot of circuit response is shown in *Figure 12* to illustrate the difference between this circuit and the true integrator.

The Current-to-Voltage Converter

Current may be measured in two ways with an operational amplifier. The current may be converted into a voltage with a resistor and then amplified or the current may be injected directly into a summing node. Converting into voltage is undesirable for two reasons: first, an impedance is inserted into the measuring line causing an error; second, amplifier offset voltage is also amplified with a subsequent loss of accuracy. The use of a current-to-voltage transducer avoids both of these problems.

The current-to-voltage transducer is shown in *Figure 13*. The input current is fed directly into the summing node and the amplifier output voltage changes to extract the same current from the summing node through R1. The scale factor of this circuit is R1 volts per amp. The only conversion error in this circuit is I_{bias} which is summed algebraically with I_{IN}.



$V_{OUT} = I_{IN}\ R1$

FIGURE 13. Current to Voltage Converter

This basic circuit is useful for many applications other than current measurement. It is shown as a photocell amplifier in the following section.

The only design constraints are that scale factors must be chosen to minimize errors due to bias current and since voltage gain and source impedance are often indeterminate (as with photocells) the amplifier must be compensated for unity-gain operation. Valuable techniques for bias current compensation are contained in Reference 5.

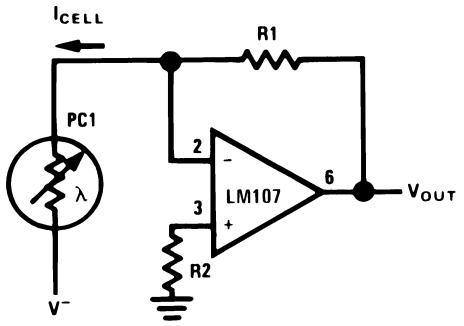
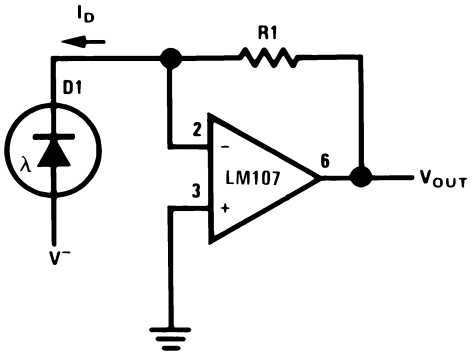


FIGURE 14. Amplifier for Photoconductive Cell

Photocell Amplifiers

Amplifiers for photoconductive, photodiode and photovoltaic cells are shown in *Figures 14, 15, 16* respectively.

All photogenerators display some voltage dependence of both speed and linearity. It is obvious that the current through a photoconductive cell will not display strict proportionality to incident light if the cell terminal voltage is allowed to vary with cell conductance. Somewhat less obvious is the fact that photodiode leakage and photovoltaic cell internal losses are also functions of terminal voltage. The current-to-voltage converter neatly sidesteps gross linearity problems by fixing a constant terminal voltage, zero in the case of photovoltaic cells and a fixed bias voltage in the case of photoconductors or photodiodes.

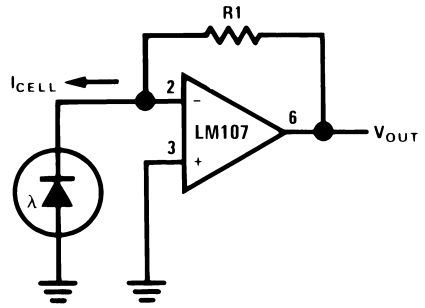


$V_{OUT} = R1\ I_D$

FIGURE 15. Photodiode Amplifier

Photocell Amplifiers (Continued)

Photodetector speed is optimized by operating into a fixed low load impedance. Currently available photovoltaic detectors show response times in the microsecond range at zero load impedance and photoconductors, even though slow, are materially faster at low load resistances.



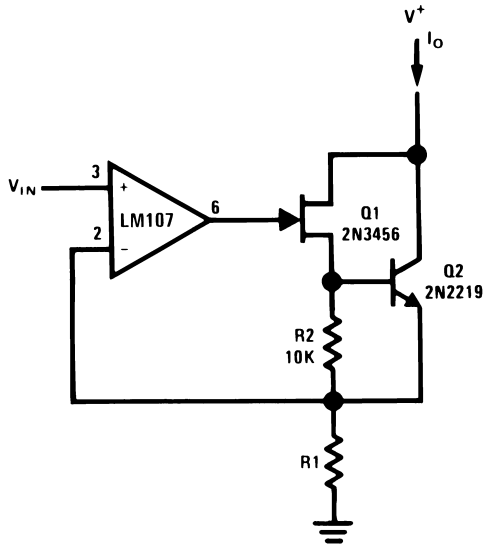
$V_{OUT} = I_{CELL}$ R1

FIGURE 16. Photovoltaic Cell Amplifier

The feedback resistance, R1, is dependent on cell sensitivity and should be chosen for either maximum dynamic range or for a desired scale factor. R2 is elective: in the case of photovoltaic cells or of photodiodes, it is not required in the case of photoconductive cells, it should be chosen to minimize bias current error over the operating range.

Precision Current Source

The precision current source is shown in *Figures 17, 18*. The configurations shown will sink or source conventional current respectively.



$$I_O = \frac{V_{IN}}{R1}$$

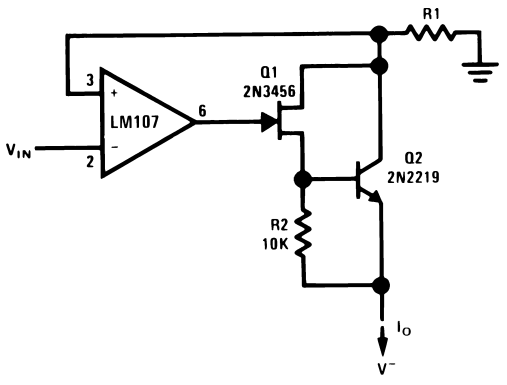
$V_{IN} \geq 0V$

FIGURE 17. Precision Current Sink

Caution must be exercised in applying these circuits. The voltage compliance of the source extends from BV_{CER} of the external transistor to approximately 1 volt more negative than V_{IN}. The compliance of the current sink is the same in the positive direction.

The impedance of these current generators is essentially infinite for small currents and they are accurate so long as V_{IN} is much greater than V_{OS} and I_O is much greater than I_{bias}.

The source and sink illustrated in *Figures 17, 18* use an FET to drive a bipolar output transistor. It is possible to use a Darlington connection in place of the FET-bipolar combination in cases where the output current is high and the base current of the Darlington input would not cause a significant error.



$$I_O = \frac{V_{IN}}{R1}$$

$V_{IN} \leq 0V$

FIGURE 18. Precision Current Source

The amplifiers used must be compensated for unity-gain and additional compensation may be required depending on load reactance and external transistor parameters.

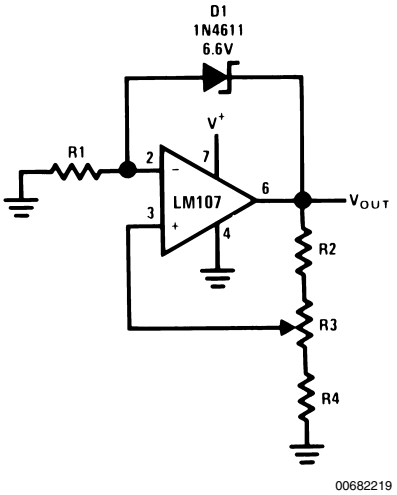


FIGURE 19. Positive Voltage Reference

Adjustable Voltage References

Adjustable voltage reference circuits are shown in *Figures 19, 20, 21, 22*. The two circuits shown have different areas of applicability. The basic difference between the two is that *Figures 19, 20* illustrate a voltage source which provides a voltage greater than the reference diode while *Figures 21, 22* illustrates a voltage source which provides a voltage lower than the reference diode. The figures show both positive and negative voltage sources.

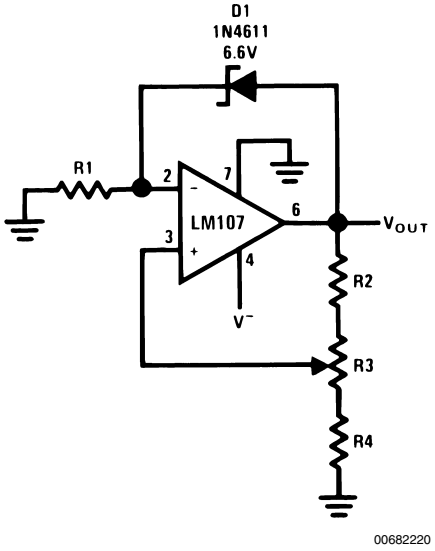


FIGURE 20. Negative Voltage Reference

High precision extended temperature applications of the circuit of *Figures 19, 20* require that the range of adjustment of V_{OUT} be restricted. When this is done, R1 may be chosen to provide optimum zener current for minimum zener T.C. Since I_Z is not a function of V^+, reference T.C. will be independent of V^+.

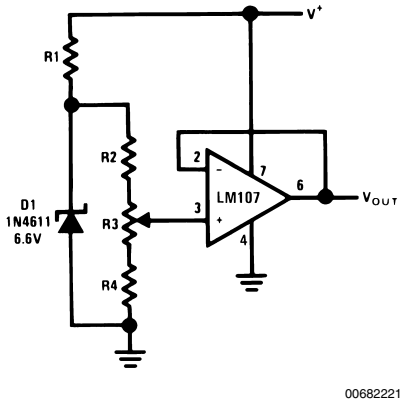


FIGURE 21. Positive Voltage Reference

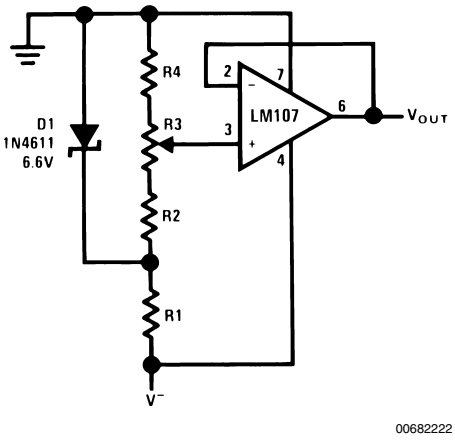


FIGURE 22. Negative Voltage Reference

The circuit of *Figures 21, 22* are suited for high precision extended temperature service if V^+ is reasonably constant since I_Z is dependent on V^+. R1, R2, R3, and R4 are chosen to provide the proper I_Z for minimum T.C. and to minimize errors due to I_{bias}.

The circuits shown should both be compensated for unity-gain operation or, if large capacitive loads are expected, should be overcompensated. Output noise may be reduced in both circuits by bypassing the amplifier input.

The circuits shown employ a single power supply, this requires that common mode range be considered in choosing an amplifier for these applications. If the common mode range requirements are in excess of the capability of the amplifier, two power supplies may be used. The LH101 may be used with a single power supply since the common mode range is from V^+ to within approximately 2 volts of V^-.

The Reset Stabilized Amplifier

The reset stabilized amplifier is a form of chopper-stabilized amplifier and is shown in *Figure 23*. As shown, the amplifier is operated closed-loop with a gain of one.

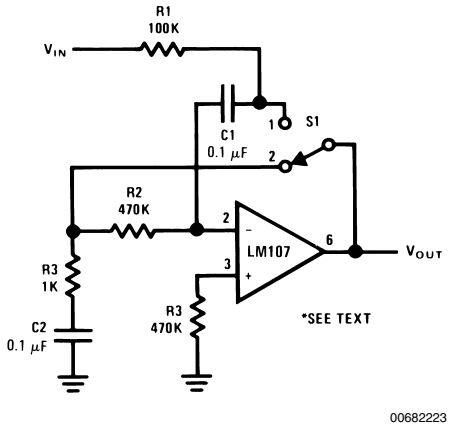
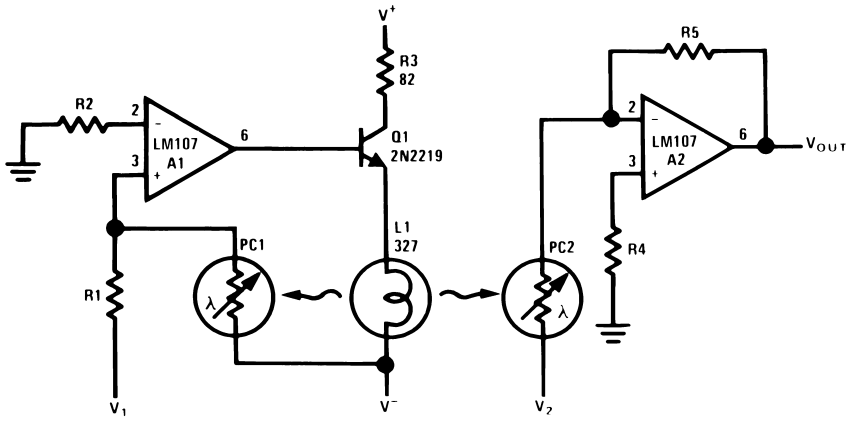


FIGURE 23. Reset Stabilized Amplifier

The connection is useful in eliminating errors due to offset voltage and bias current. The output of this circuit is a pulse whose amplitude is equal to V_{IN}. Operation may be understood by considering the two conditions corresponding to the position of S_1. When S_1 is in position 2, the amplifier is connected in the unity gain connection and the voltage at the output will be equal to the sum of the input offset voltage and the drop across R2 due to input bias current. The voltage at the inverting input will be equal to input offset voltage. Capacitor C1 will charge to the sum of input offset voltage and V_{IN} through R1. When C1 is charged, no current flows through the source resistance and R1 so there is no error due to input resistance. S_1 is then changed to position 1. The voltage stored on C1 is inserted between the output and inverting input of the amplifier and the output of the amplifier changes by V_{IN} to maintain the amplifier input at the input offset voltage. The output then changes from (V_{OS} + I_{bias}R2) to (V_{IN} + I_{bias}R2) as S_1 is changed from position 2 to position 1. Amplifier bias current is supplied through R2 from the output of the amplifier or from C2 when S_1 is in position 2 and position 1 respectively. R3 serves to reduce the offset at the amplifier output if the amplifier must have maximum linear range or if it is desired to DC couple the amplifier.

An additional advantage of this connection is that input resistance approaches infinity as the capacitor C1 approaches full charge, eliminating errors due to loading of the source resistance. The time spent in position 2 should be long with respect to the charging time of C1 for maximum accuracy.

The amplifier used must be compensated for unity gain operation and it may be necessary to overcompensate because of the phase shift across R2 due to C1 and the amplifier input capacity. Since this connection is usually used at very low switching speeds, slew rate is not normally a practical consideration and overcompensation does not reduce accuracy.



$$R5 = R1\left(\frac{V^-}{10}\right)$$

$$V_1 > 0$$

$$V_{OUT} = \frac{V_1 V_2}{10}$$

FIGURE 24. Analog Multiplier

The Analog Multiplier

A simple embodiment of the analog multiplier is shown in *Figure 24*. This circuit circumvents many of the problems associated with the log-antilog circuit and provides three quadrant analog multiplication which is relatively temperature insensitive and which is not subject to the bias current errors which plague most multipliers.

The Analog Multiplier (Continued)

Circuit operation may be understood by considering A2 as a controlled gain amplifier, amplifying V_2, whose gain is dependent on the ratio of the resistance of PC2 to R5 and by considering A1 as a control amplifier which establishes the resistance of PC2 as a function of V_1. In this way it is seen that V_{OUT} is a function of both V_1 and V_2.

A1, the control amplifier, provides drive for the lamp, L1. When an input voltage, V_1, is present, L1 is driven by A1 until the current to the summing junction from the negative supply through PC1 is equal to the current to the summing junction from V_1 through R1. Since the negative supply voltage is fixed, this forces the resistance of PC1 to a value proportional to R1 and to the ratio of V_1 to V^-. L1 also illuminates PC2 and, if the photoconductors are matched, causes PC2 to have a resistance equal to PC1.

A2, the controlled gain amplifier, acts as an inverting amplifier whose gain is equal to the ratio of the resistance of PC2 to R5. If R5 is chosen equal to the product of R1 and V^-, then V_{OUT} becomes simply the product of V_1 and V_2. R5 may be scaled in powers of ten to provide any required output scale factor.

PC1 and PC2 should be matched for best tracking over temperature since the T.C. of resistance is related to resistance match for cells of the same geometry. Small mismatches may be compensated by varying the value of R5 as a scale factor adjustment. The photoconductive cells should receive equal illumination from L1, a convenient method is to mount the cells in holes in an aluminum block and to mount the lamp midway between them. This mounting method provides controlled spacing and also provides a thermal bridge between the two cells to reduce differences in cell temperature. This technique may be extended to the use of FET's or other devices to meet special resistance or environment requirements.

The circuit as shown gives an inverting output whose magnitude is equal to one-tenth the product of the two analog inputs. Input V_1 is restricted to positive values, but V_2 may assume both positive and negative values. This circuit is restricted to low frequency operation by the lamp time constant.

R2 and R4 are chosen to minimize errors due to input offset current as outlined in the section describing the photocell amplifier. R3 is included to reduce in-rush current when first turning on the lamp, L1.

The Full-Wave Rectifier and Averaging Filter

The circuit shown in *Figure 25* is the heart of an average reading, rms calibrated AC voltmeter. As shown, it is a rectifier and averaging filter. Deletion of C2 removes the averaging function and provides a precision full-wave rectifier, and deletion of C1 provides an absolute value generator.

Circuit operation may be understood by following the signal path for negative and then for positive inputs. For negative signals, the output of amplifier A1 is clamped to +0.7V by D1 and disconnected from the summing point of A2 by D2. A2 then functions as a simple unity-gain inverter with input resistor, R1, and feedback resistor, R2, giving a positive going output.

For positive inputs, A1 operates as a normal amplifier connected to the A2 summing point through resistor, R5. Amplifier A1 then acts as a simple unity-gain inverter with input resistor, R3, and feedback resistor, R5. A1 gain accuracy is not affected by D2 since it is inside the feedback loop. Positive current enters the A2 summing point through resistor, R1, and negative current is drawn from the A2 summing point through resistor, R5. Since the voltages across R1 and R5 are equal and opposite, and R5 is one-half the value of R1, the net input current at the A2 summing point is equal to and opposite from the current through R1 and amplifier A2 operates as a summing inverter with unity gain, again giving a positive output.

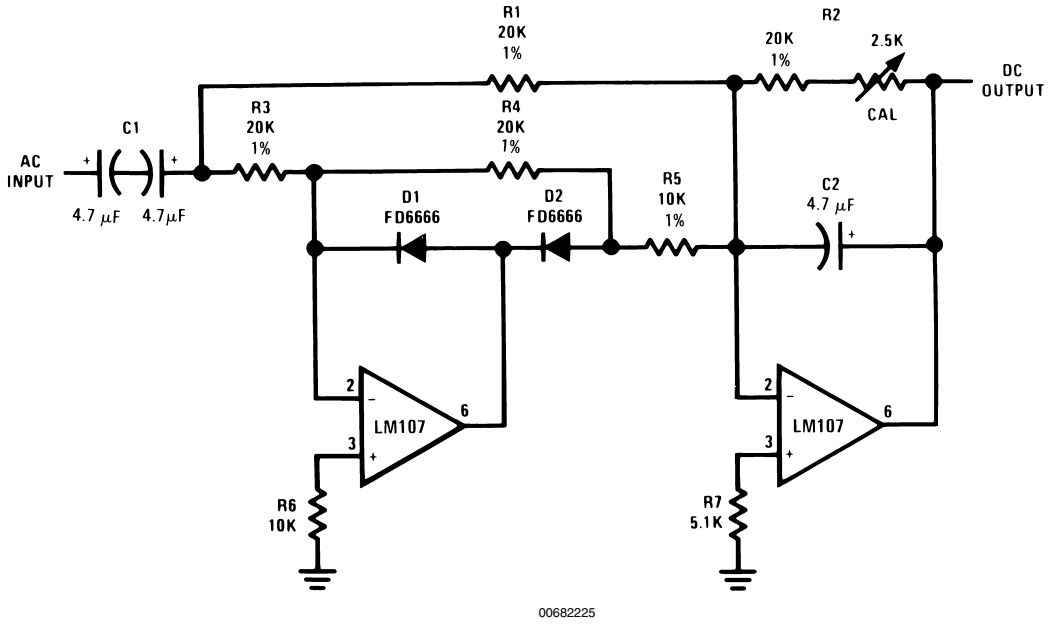


FIGURE 25. Full-Wave Rectifier and Averaging Filter

The Full-Wave Rectifier and Averaging Filter (Continued)

The circuit becomes an averaging filter when C2 is connected across R2. Operation of A2 then is similar to the Simple Low Pass Filter previously described. The time constant R2C2 should be chosen to be much larger than the maximum period of the input voltage which is to be averaged.

Capacitor C1 may be deleted if the circuit is to be used as an absolute value generator. When this is done, the circuit output will be the positive absolute value of the input voltage.

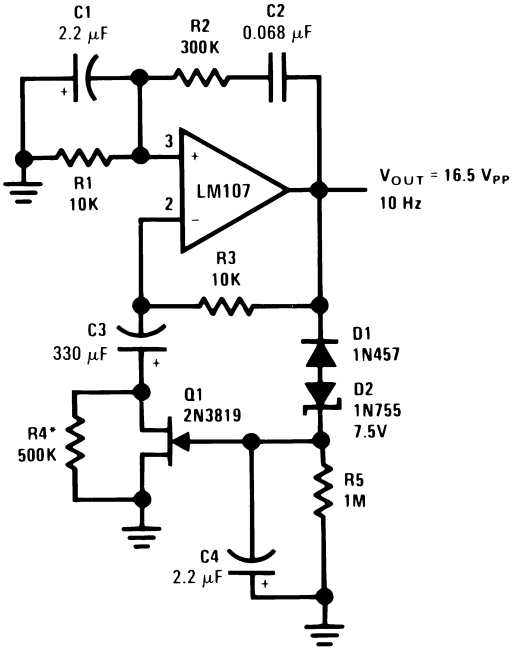
The amplifiers chosen must be compensated for unity-gain operation and R6 and R7 must be chosen to minimize output errors due to input offset current.

Sine Wave Oscillator

An amplitude-stabilized sine-wave oscillator is shown in *Figure 26*. This circuit provides high purity sine-wave output down to low frequencies with minimum circuit complexity. An important advantage of this circuit is that the traditional tungsten filament lamp amplitude regulator is eliminated along with its time constant and linearity problems.

In addition, the reliability problems associated with a lamp are eliminated.

The Wien Bridge oscillator is widely used and takes advantage of the fact that the phase of the voltage across the parallel branch of a series and a parallel RC network connected in series, is the same as the phase of the applied voltage across the two networks at one particular frequency and that the phase lags with increasing frequency and leads with decreasing frequency. When this network—the Wien Bridge—is used as a positive feedback element around an amplifier, oscillation occurs at the frequency at which the phase shift is zero. Additional negative feedback is provided to set loop gain to unity at the oscillation frequency, to stabilize the frequency of oscillation, and to reduce harmonic distortion.



*See Text

FIGURE 26. Wien Bridge Sine Wave Oscillator

The circuit presented here differs from the classic usage only in the form of the negative feedback stabilization scheme. Circuit operation is as follows: negative peaks in excess of −8.25V cause D1 and D2 to conduct, charging C4. The charge stored in C4 provides bias to Q1, which determines amplifier gain. C3 is a low frequency roll-off capacitor in the feedback network and prevents offset voltage and offset current errors from being multiplied by amplifier gain.

Distortion is determined by amplifier open-loop gain and by the response time of the negative feedback loop filter, R5 and C4. A trade-off is necessary in determining amplitude stabilization time constant and oscillator distortion. R4 is chosen to adjust the negative feedback loop so that the FET is operated at a small negative gate bias. The circuit shown provides optimum values for a general purpose oscillator.

Triangle-Wave Generator

A constant amplitude triangular-wave generator is shown in *Figure 27*. This circuit provides a variable frequency triangular wave whose amplitude is independent of frequency.

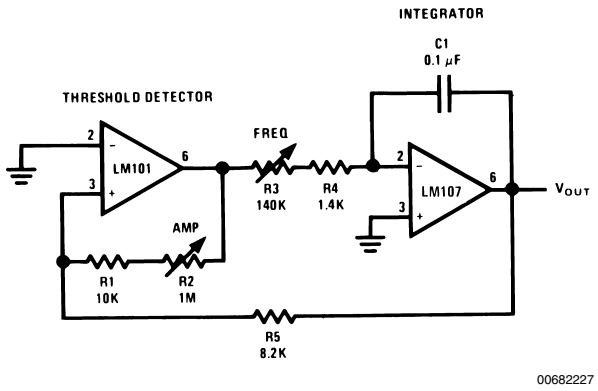


FIGURE 27. Triangular-Wave Generator

The generator embodies an integrator as a ramp generator and a threshold detector with hysterisis as a reset circuit. The integrator has been described in a previous section and requires no further explanation. The threshold detector is similar to a Schmitt Trigger in that it is a latch circuit with a large dead zone. This function is implemented by using positive feedback around an operational amplifier. When the amplifier output is in either the positive or negative saturated state, the positive feedback network provides a voltage at the non-inverting input which is determined by the attenuation of the feedback loop and the saturation voltage of the amplifier. To cause the amplifier to change states, the voltage at the input of the amplifier must be caused to change polarity by an amount in excess of the amplifier input offset voltage. When this is done the amplifier saturates in the opposite direction and remains in that state until the voltage at its input again reverses. The complete circuit operation may be understood by examining the operation with the output of the threshold detector in the positive state. The detector positive saturation voltage is applied to the integrator summing junction through the combination R3 and R4 causing a current I^+ to flow.

The integrator then generates a negative-going ramp with a rate of $I^+/C1$ volts per second until its output equals the negative trip point of the threshold detector. The threshold detector then changes to the negative output state and supplies a negative current, I^-, at the integrator summing point. The integrator now generates a positive-going ramp with a rate of $I^-/C1$ volts per second until its output equals the positive trip point of the threshold detector where the detector again changes output state and the cycle repeats.

Triangular-wave frequency is determined by R3, R4 and C1 and the positive and negative saturation voltages of the amplifier A1. Amplitude is determined by the ratio of R5 to the combination of R1 and R2 and the threshold detector saturation voltages. Positive and negative ramp rates are equal and positive and negative peaks are equal if the detector has equal positive and negative saturation voltages. The output waveform may be offset with respect to ground if the inverting input of the threshold detector, A1, is offset with respect to ground.

The generator may be made independent of temperature and supply voltage if the detector is clamped with matched zener diodes as shown in *Figure 28*.

The integrator should be compensated for unity-gain and the detector may be compensated if power supply impedance causes oscillation during its transition time. The current into the integrator should be large with respect to I_{bias} for maximum symmetry, and offset voltage should be small with respect to V_{OUT} peak.

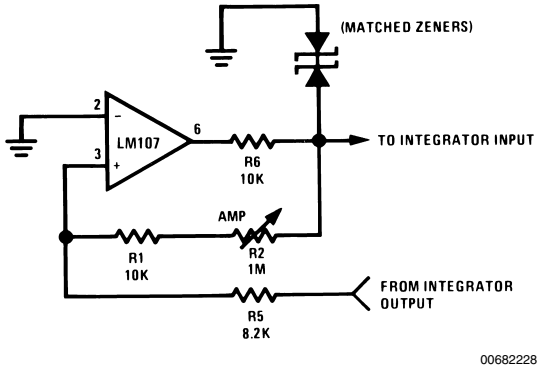
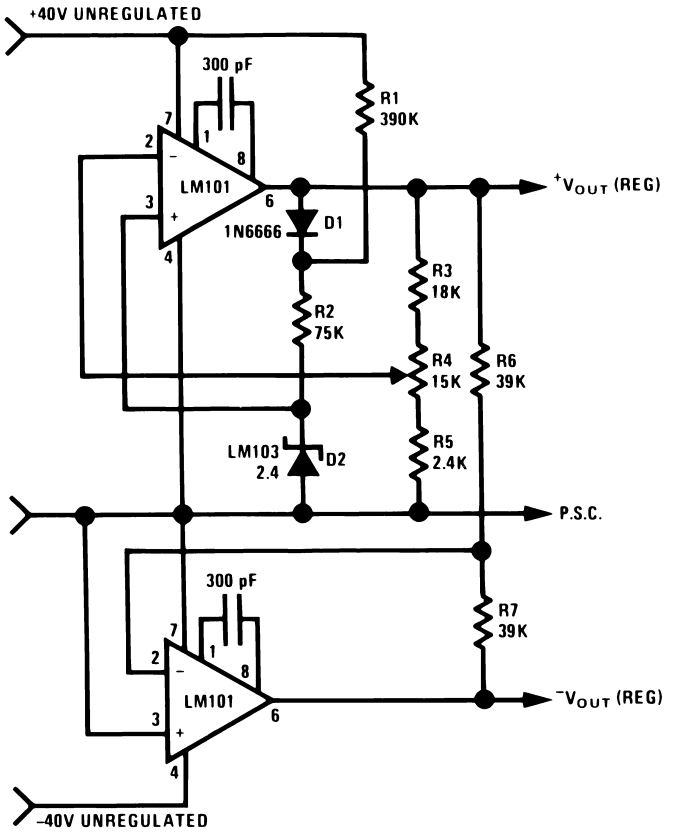


FIGURE 28. Threshold Detector with Regulated Output

Tracking Regulated Power Supply

A tracking regulated power supply is shown in *Figure 29*. This supply is very suitable for powering an operational amplifier system since positive and negative voltages track, eliminating common mode signals originating in the supply voltage. In addition, only one voltage reference and a minimum number of passive components are required.

Tracking Regulated Power Supply (Continued)



Output voltage is variable from ±5V to ±35V.

Negative output tracks positive output to within the ratio of R6 to R7.

FIGURE 29. Tracking Power Supply

Power supply operation may be understood by considering first the positive regulator. The positive regulator compares the voltage at the wiper of R4 to the voltage reference, D2. The difference between these two voltages is the input voltage for the amplifier and since R3, R4, and R5 form a negative feedback loop, the amplifier output voltage changes in such a way as to minimize this difference. The voltage reference current is supplied from the amplifier output to increase power supply line regulation. This allows the regulator to operate from supplies with large ripple voltages. Regulating the reference current in this way requires a separate source of current for supply start-up. Resistor R1 and diode D1 provide this start-up current. D1 decouples the reference string from the amplifier output during start-up and R1 supplies the start-up current from the unregulated positive supply. After start-up, the low amplifier output impedance reduces reference current variations due to the current through R1.

The negative regulator is simply a unity-gain inverter with input resistor, R6, and feedback resistor, R7.

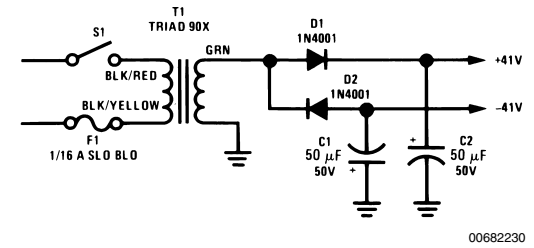
The amplifiers must be compensated for unity-gain operation.

The power supply may be modulated by injecting current into the wiper of R4. In this case, the output voltage variations will be equal and opposite at the positive and negative outputs. The power supply voltage may be controlled by replacing D1, D2, R1 and R2 with a variable voltage reference.

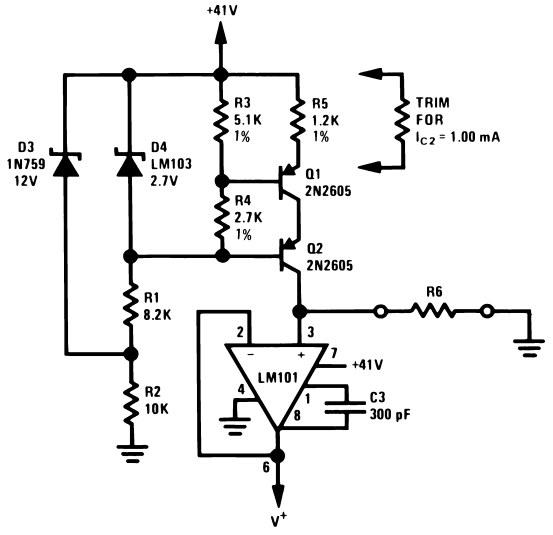
Programmable Bench Power Supply

The complete power supply shown in *Figure 30* is a programmable positive and negative power supply. The regulator section of the supply comprises two voltage followers whose input is provided by the voltage drop across a reference resistor of a precision current source.

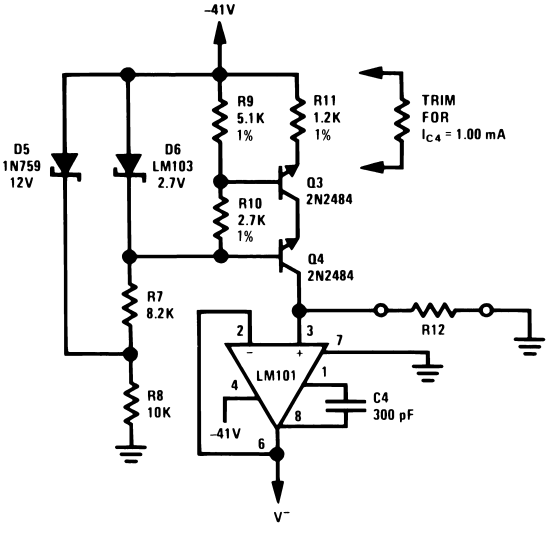
Programmable Bench Power Supply (Continued)



a.



b.



c.

FIGURE 30. Low-Power Supply for Integrated Circuit Testing

Programming sensitivity of the positive and negative supply is 1V/1000Ω of resistors R6 and R12 respectively. The output voltage of the positive regulator may be varied from approximately +2V to +38V with respect to ground and the negative regulator output voltage may be varied from –38V to 0V with respect to ground. Since LM107 amplifiers are

Programmable Bench Power Supply (Continued)

used, the supplies are inherently short circuit proof. This current limiting feature also serves to protect a test circuit if this supply is used in integrated circuit testing.

Internally compensated amplifiers may be used in this application if the expected capacitive loading is small. If large capacitive loads are expected, an externally compensated amplifier should be used and the amplifier should be overcompensated for additional stability. Power supply noise may be reduced by bypassing the amplifier inputs to ground with capacitors in the 0.1 to 1.0 μF range.

Conclusions

The foregoing circuits are illustrative of the versatility of the integrated operational amplifier and provide a guide to a number of useful applications. The cautions noted in each section will show the more common pitfalls encountered in amplifier usage.

Appendix I

Definition of Terms

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Bias Current: The average of the two input currents.

Input Voltage Range: The range of voltages on the input terminals for which the amplifier operates within specifications.

Common Mode Rejection Ratio: The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output at zero.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Power Supply Rejection: The ratio of the change in input offset voltage to change in power supply voltage producing it.

Slew Rate: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

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