An Integrated 200-W Class-D Audio Amplifier

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***Abstract*—An integrated stereo class-D audio power amplifier realized in a silicon-on-insulator (SOI)-based BCD technology is presented. The amplifier is capable of delivering 2×100 W in two 4-Ω loads at a supply voltage of 60 V. A second-order feedback loop is used to supress supply ripple and pulse-shape errors in the switching power stage. The limiting factor in the performance of any class-D amplifiers is the quality of the switching power stage. A high-speed low-current levelshifter and a robust deadtime control arrangement are proposed that enable the realization of a robust high-quality switching power stage. Some practical issues with respect to robustness and electromagnetic compatibility are discussed.**

***Index Terms*—Audio amplifiers, power integrated circuits, pulsewidth modulation, silicon-on-insulator technology.**

I. Introduction

THE operating principles of class-D amplifiers have been known for a long time, but only recently have semiconductor manufacturers been able to produce reliable switching power stages of sufficient quality. The audio performance of modern class-D amplifiers equals or even exceeds that of conventional class-AB amplifiers. The high efficiency of class-D amplifiers can be exploited to reduce heatsink size, increase output power, and/or lengthen battery life. Especially, multichannel DVD receivers appear to be the perfect application for class-D amplifiers.

II. SOI Technology

The amplifier has been realized in A-BCD [1] which is a silicon-on-insulator (SOI)-based single-poly double-metal Bipolar, CMOS, DMOS (BCD) technology. A cross section of a 60-V DMOS transistor in A-BCD is shown in Fig. 1.

The dielectric isolation between the integrated components makes designs in A-BCD inherently free from latchup phenomena. Consequently, the backgate diodes of the DMOS power transistors in the switching power stage can be exploited as freewheel diodes without the need for external Schottky diodes. In conventional bulk technologies, external diodes are often necessary to prevent injection of minority carriers into the substrate which can lead to latchup. A particular advantageous feature of A-BCD is the remarkably small reverse recovery charge associated with the backgate diodes of the DMOS transistors. The reverse recovery charge is almost an order of magnitude smaller than that of a comparable DMOS transistor in bulk technology. The small reverse recovery charge makes A-BCD especially well suited for switching applications, since reverse recovery is one of the major sources of electromagnetic interference (EMI).

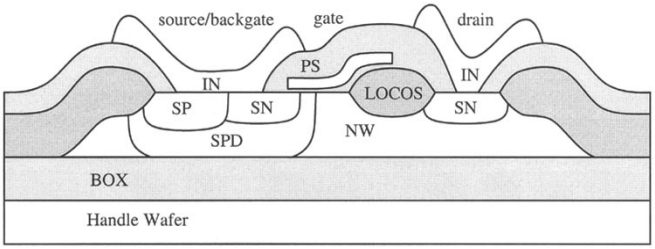

Fig. 1. Cross section of HV-DMOS in A-BCD.

III. Amplifier Topology

A block diagram of the amplifier is shown in Fig. 2. The amplifier consists of two identical audio channels and a common section that contains an oscillator, a mode interface, and a number of references and protection circuits. Each audio channel has a controller in which the audio input signal is converted to a pulsewidth modulated (PWM) signal. The controller drives a switching power stage that boosts the PWM signal to high power levels. The PWM output signal is fed back to the controller. The feedback loop is completely integrated on-chip. External demodulation filters are used to filter the audio content of the PWM signal and suppress the energy at higher frequencies. Usually, a second-order *LC* low-pass filter is sufficient. Both controllers have a differential input stage that makes single-ended (SE) as well as bridge-tied-load (BTL) operation possible.

The protection block includes overcurrent, overtemperature, over/undervoltage, and supply unbalance protections. In SE configuration, the amplifier requires a symmetrical voltage supply $\pm V_p$. The supply unbalance protection is activated if the voltage difference between the positive and negative supply voltage exceeds a predefined value.

The frequency of the low-jitter sawtooth oscillator can be adjusted by an external resistor. Alternatively, it is also possible to synchronize the amplifier to an external clock, which is convenient if more amplifiers are used simultaneously.

The PWM method used in the amplifier is based on double-sided natural sampling [2]. Such a PWM signal can be constructed feedforward by simply comparing the audio input signal $V_{\rm IN}$ with a triangular reference wave V_T as shown in Fig. 3. The fundamental frequency of the reference triangle is called the carrier frequency ω_C. The ratio between the amplitude $V_{\rm IN}$ of the (sinusoidal) audio input signal and the amplitude V_T of the reference triangle is called the modulation depth Δ. The PWM spectrum contains no direct harmonics of the modulating signal, which means it can be considered ideal

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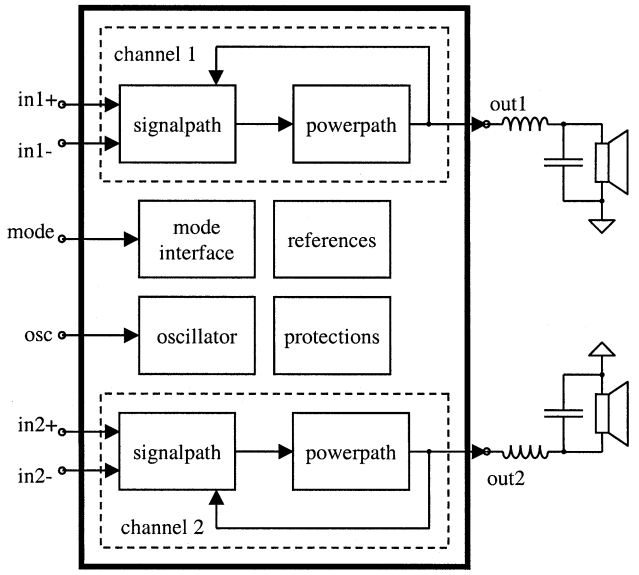

Fig. 2. Amplifier topology.

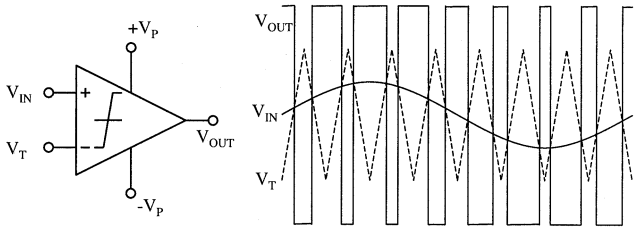

Fig. 3. Feedforward PWM.

in terms of distortion. When only audio signal frequencies are considered the gain of this feedforward PWM is simply the ratio between the amplitude of the reference triangle V_T and the amplitude of the PWM signal V_P:

$$G_{\mathrm{PWM}} = \frac{V_P}{V_T}. \tag{1}$$

A block diagram of one complete audio channel is shown in Fig. 4. A second-order feedback loop is used to suppress supply ripple and pulse-shape errors in the switching power stage [3]. The closed-loop gain for audio frequencies is given by

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = R_1 g_{m1}. \tag{2}$$

The transconductance g_{m1} and feedback resistor R_1 have to be very linear and thermally matched in order to achieve good closed-loop performance.

A transconductance amplifier at the input has several advantages compared to using a simple resistor between input and virtual ground. The input impedance can be chosen independently of the feedback loop which makes ac coupling feasible. BTL operation can be implemented simply by connecting the inputs of two SE channels antiparallel. Further, the amplifier can be muted without influencing the feedback loop. Finally, the noise and offset of the first integrator in the loop are not amplified by the closed-loop gain.

The control loop has two identical integrators which realize a second-order loop transfer. The capacitors of the integrators have the same value, which means that their parasitic capacitances to the substrate also have the same value. Consequently, any disturbance from the substrate appears as common mode at the input of the comparator.

The reference triangle is realized by injecting a square-wave current with amplitude I_C into the virtual ground of the second integrator. The amplitude of the reference triangle V_T is given by

$$V_T = \frac{\pi I_c}{2\omega_c C_2}. \tag{3}$$

An advantage of injecting the carrier signal at this point in the loop is that duty-cycle errors or jitter from the oscillator are now also suppressed by the loop.

For low frequencies ($\omega < 1/R_2C_2$), the loop has a second-order behavior. At higher frequencies, a direct path from the first integrator bypasses the second integrator. This creates an LHP zero in the loop transfer $H(s)$. Assuming sufficiently large values for g_{m2} and g_{m3}, the loop transfer $H(s)$ can be approximated by

$$H(s) = \frac{(sR_1C_1 + 1)}{s^2} \frac{G_{\mathrm{PWM}}}{R_1C_1R_2C_2}. \tag{4}$$

In order to obtain sufficient phase margin and acceptable peaking of the closed-loop transfer, the LHP zero frequency ω_Z should be lower than the unity-gain frequency ω_{UG}. A ratio of $\sqrt{3}$ yields a phase margin of $\pi/3$ and about 2.3-dB peaking.

The unity-gain frequency ω_{UG} in turn should be lower than the fundamental frequency of the reference triangle ω_C. This relation can be quantified by analyzing the internal signals in the loop. During steady state, a triangular wave appears at both input terminals of the loop comparator. At the noninverting input, the integrated sum of the audio input signal and PWM output signal appears. Since the audio input signal has a much lower frequency than the PWM carrier, it can be considered dc in this analysis. First, consider the case where the audio input signal is zero. The PWM output signal than has a 50% duty cycle. Therefore, a current $+I_{\mathrm{FB}}$ or $-I_{\mathrm{FB}}$ is alternatingly injected into the virtual ground. At the output of the first integrator, this results in a triangular wave V_E with amplitude given by

$$V_E = \frac{\pi I_{\mathrm{FB}}}{2\omega_C C_1} = \frac{\pi V_P}{2\omega_C R_1 C_1} \tag{5}$$

where I_{FB} is the current that is fed back from the output to the virtual ground through feedback resistor R_1. This signal is essentially the integrated error signal and will be called the error triangle V_E.

At the inverting input of the comparator, the sum of the reference triangle V_T and the integrated output of the first integrator appear. At the carrier frequency, the contribution of the second term is negligible. Both signals V_T and V_E are shown in Fig. 5(a).

Where the triangles cross each other, the output changes polarity. In order for this process to work correctly, the amplitude of the reference triangle V_T should be larger than the amplitude of the error triangle V_E or, more accurately, the slopes of the

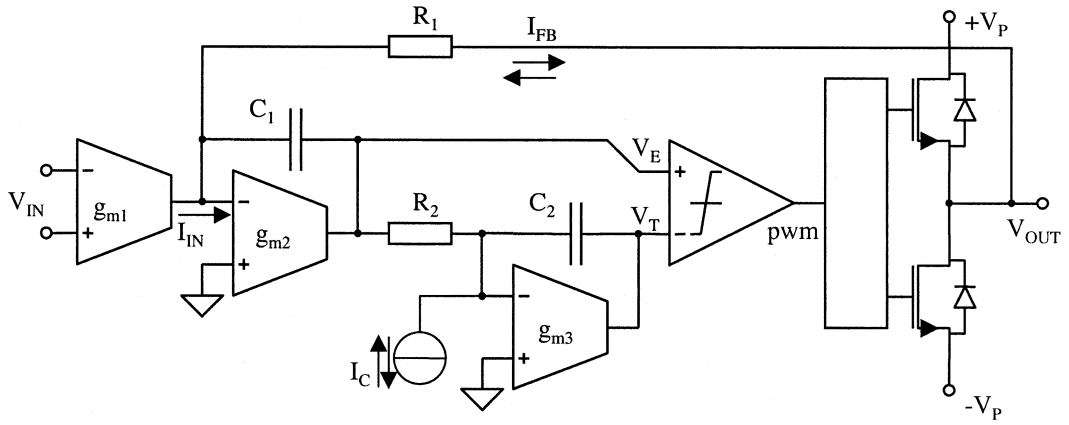

Fig. 4. Second-order PWM control loop.

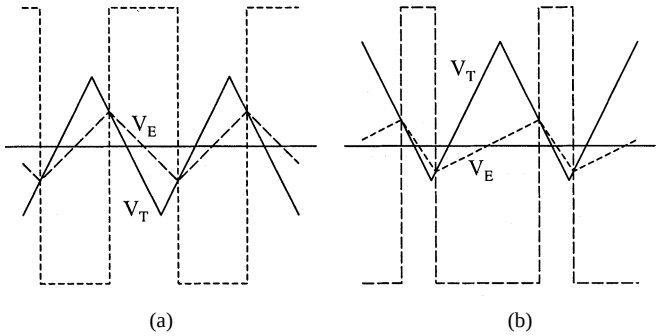

Fig. 5. Internal loop signals. (a) Zero input. (b) Positive input.

reference triangle V_T should be steeper than those of the error triangle V_E. Otherwise, the signals would diverge.

$$\left|\frac{d}{dt}V_E\right| < \left|\frac{d}{dt}V_T\right| \Rightarrow \frac{|I_{\rm FB}|}{C_1} < \frac{|I_C|}{C_2}. \tag{6}$$

Now, consider what happens when a signal current $I_{\rm IN}$ is injected into the loop. As a result, the falling slope of the error triangle V_E becomes steeper while the rising slope becomes less steep. The internal signals inside the loop for this situation are shown in Fig. 5(b). As can be seen, the duty cycle of the output has changed accordingly.

The modulation depth becomes 100% when the signal current $I_{\rm IN}$ equals the feedback current $I_{\rm FB}$. In that case, the slope of the falling edge of the error triangle V_E is almost twice as steep as with no input signal, while the rising edge is almost zero. Consequently, the criterion for convergence and thus stability of the loop becomes

$$\left.\begin{array}{c}\dfrac{2\,|I_{\rm FB}|}{C_1} < \dfrac{|I_C|}{C_2} \\ C_1 = C_2\end{array}\right\} \Rightarrow V_T > 2V_E. \tag{7}$$

This stability criterion can be translated to the frequency domain. The unity-gain frequency $\omega_{\rm UG}$ of the loop transfer $H(s)$ is approximately

$$\omega_{\rm UG} = \frac{G_{\rm PWM}}{R_1 C_1}. \tag{8}$$

With (1), (5), and (7), this yields

$$\omega_{\rm UG} < \frac{\omega_C}{\pi}. \tag{9}$$

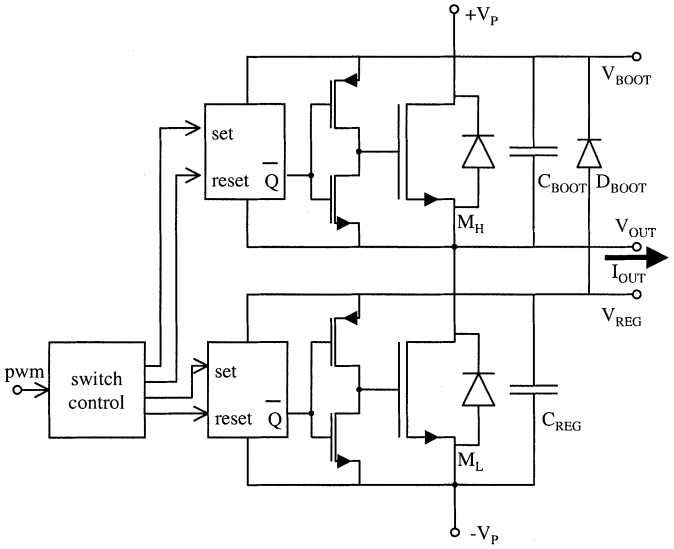

Fig. 6. Half-bridge switching power stage.

Note that this is actually the stability criterion for a first-order feedback loop, which also applies to the second-order loop provided that the LHP zero frequency ω_Z is sufficiently lower than the unity-gain frequency $\omega_{\rm UG}$.

IV. Power Stage Design

The performance of any class-D amplifier is limited by the quality of the switching power stage. The power stage of the amplifier consists of two DMOS power transistors in a totem-pole configuration as shown in Fig. 6.

The power transistors are alternately turned on, switching the output voltage between the supply lines. Cross conduction is avoided by a break-before-make arrangement. This introduces a so-called *deadtime* during each output transition where neither of the power transistors is conducting. The *LC* filter that is usually connected to the output forces a continuous output current. During the deadtime, this continuous output current flows through either of the backgate diodes.

The switching power stage uses a supply voltage of 60 V, whereas the maximum allowable gate–source voltage of the power transistors is 12 V. For the low-side power transistor M_L, the driver circuit uses a 12-V supply voltage $V_{\rm REG}$ that

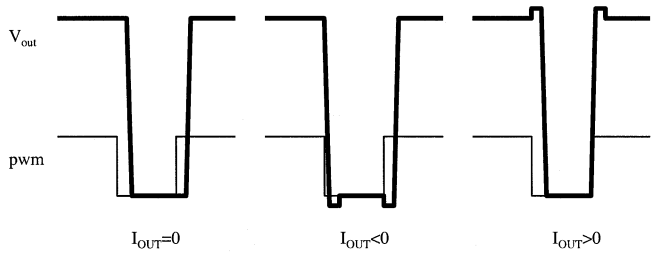

Fig. 7. Deadtime distortion.

is generated by an on-chip voltage regulator with an external decoupling capacitor C_{REG}.

An external bootstrap capacitor C_{BOOT} provides a floating supply voltage V_{BOOT} for the driver of the high-side power transistor M_H. The bootstrap capacitor is recharged each time the output V_{OUT} is low through a diode D_{BOOT} connected to V_{REG}.

In order to guarantee that the gate drive of the high-side transistor is not disturbed by the steep voltage transients at the output, a latch is included in the high-side driver. This latch can be set and reset by a low-side controller. The communication between the controller and the high-side latch requires a robust levelshifter. For simplicity, the low-side driver is made identical to the high-side driver.

V. Distortion

The two main sources of distortion in class-D amplifiers are deadtime and supply-voltage modulation. Both sources of distortion cause pulse-shape errors in the PWM output signal.

Deadtime causes a signal-dependent delay in the switching power stage. Consider the circuit shown in Fig. 6. Suppose the high-side power transistor M_H is conducting and the output current I_{OUT} is flowing toward the load. As soon as transistor M_H switches off, the output voltage changes polarity immediately and the output current continues to flow through the backgate diode of the low-side power transistor M_L. When the current I_{OUT} is flowing in the other direction, the output voltage remains high after transistor M_H switches off, while the output current flows through the backgate diode of transistor M_H. Only after transistor M_L is switched on does the output change polarity. These two situations are illustrated in Fig. 7. As can be seen, the width of the output signal V_{OUT} changes depending on the direction of the output current I_{OUT}. The deadtime can be recognized by the small rectangular distortions on the output signal, which are caused by the forward bias voltage of the backgate diodes. In Fig. 8, the relation between the duty cycle of the PWM signal at the input and at the output of a class-D stage is shown. Two so-called dead-bands [4] exist that correspond to the moment where the output signal current exceeds the ripple current. The deadtime should preferably be made as short as possible.

The other source of distortion in class-D amplifiers is modulation of the supply voltage. Variations in the supply voltage cause amplitude errors in the PWM signal. The current that a

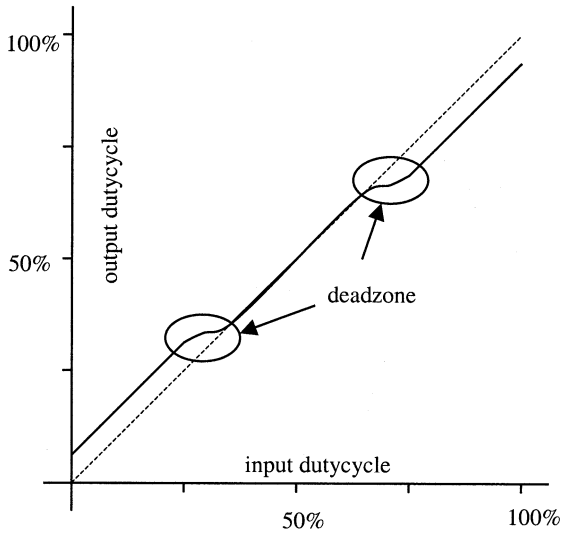

Fig. 8. Relation between input and output duty cycle.

PWM class-D amplifier draws from the supply is on average equal to

$$I_P = \frac{V_p}{2R_L}\left(\Delta + \Delta^2\right) \tag{10}$$

where V_P is the supply voltage, R_L is the load resistance, and Δ is the modulation depth of the PWM output signal. A finite supply impedance causes the supply voltage to vary nonlinearly with the load current. Since a feedforward class-D output stage has only 6-dB supply rejection, supply-voltage modulation adds distortion to the output signal. Note that the expression for the average supply current I_P has a negative minimum value for $\Delta = -0.5$. For this modulation depth, the current is flowing toward the supply. Since most power supplies are unable to sink current, the supply voltage starts increasing at a rate that depends on the value of the supply decoupling capacitors. In order to prevent the amplifier from destroying itself by increasing the supply voltage to an unsafe value, an overvoltage as well as a supply unbalance protection are included.

Distortion caused by deadtime as well as supply voltage modulation are effectively suppressed by the feedback loop of the amplifier. Distortion is in a way related to electromagnetic compatibility (EMC) performance. Good distortion figures are hardly possible when the EMC performance is poor. This can be understood by realizing that severe ringing of the output of the amplifier translates directly in pulse-shape errors.

VI. Carrousel Handshake

In order to be robust against process and temperature variations it is undesirable to let the switch timing be determined by on-chip time constants. Therefore, a handshake is used to control the timing in the switching power stage. A sense circuit has been added to both the high-side and low-side switch that generates a *ready* signal if the corresponding switch is off. The state of the switch can easily be detected by comparing the gate–source voltage of the DMOS power transistor to the threshold voltage. In practice, the exact decision level is not very critical since the voltage transients of the gate source voltage are quite steep.

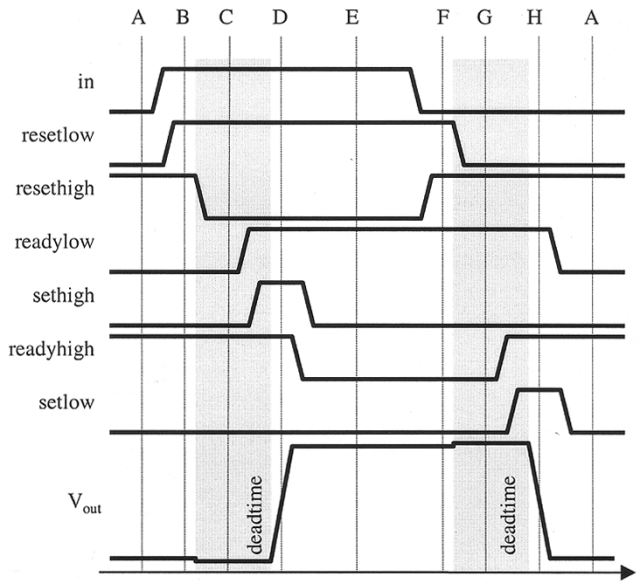

Fig. 9. Handshake signal timing.

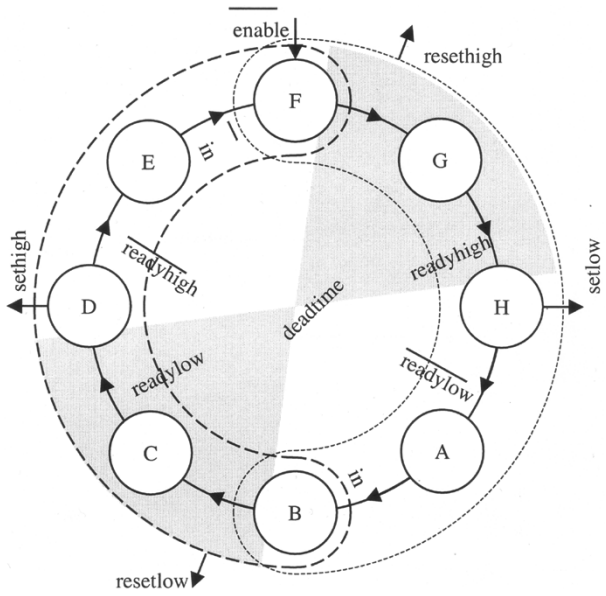

Fig. 10. Carrousel handshake logic.

The handshake procedure forces a cyclic sequence in which the *set* and *reset* signals for the high-side and low-side latches are generated. Deadtime is guaranteed by overlap of the *resethigh* and *resetlow* signal. Further, the *set* and *reset* signals of the same latch should be nonoverlapping. The signal timing during one cycle is shown in Fig. 9. In the initial situation in Fig. 9, the output of the switching power stage is assumed low. In this case, the low-side power transistor M_L is on, the high-side power transistor M_H is off, *resethigh* and *readyhigh* are high and all other signals are low (A). Then after the input signal *in* goes high the following sequence of events take place. First *resetlow* goes high (B) and, following immediately, *resethigh* goes low (C). As a result of *resetlow*, the low-side power transistor M_L is switched off and *readylow* goes high. At this time, both power transistors are off (deadtime). Now it is safe to turn on M_H so *sethigh* goes high (D). As soon as M_H is on, *readyhigh* goes low. Since the latch in the high-side driver is now set, the *sethigh* signal can go low again (E). At this moment, the output of the switching power stage is high. For the transition back to low, the same sequence of events occurs with high and low interchanged (F,G,H,A). This completes one cycle and returns the system to the initial situation.

The *set* and *reset* signals are generated by an asynchronous state machine called carrousel [5] that follows a cyclic pattern of eight states as shown in Fig. 10. The transitions between these states are synchronized by the *in* and *ready* signals.

The carrousel has an *enable* input which can be used to force it into state F in which both *reset* signals are high and both power transistors are consequently switched off.

The eight states of the carrousel are encoded using a 3-bit gray code in order to avoid glitches. The carrousel is a Moore machine, i.e., the output signals are decoded from the state bits. There is no direct connection between input and output signals. This makes the carrousel very robust against disturbances that occur during voltage transients at the output of the switching power stage.

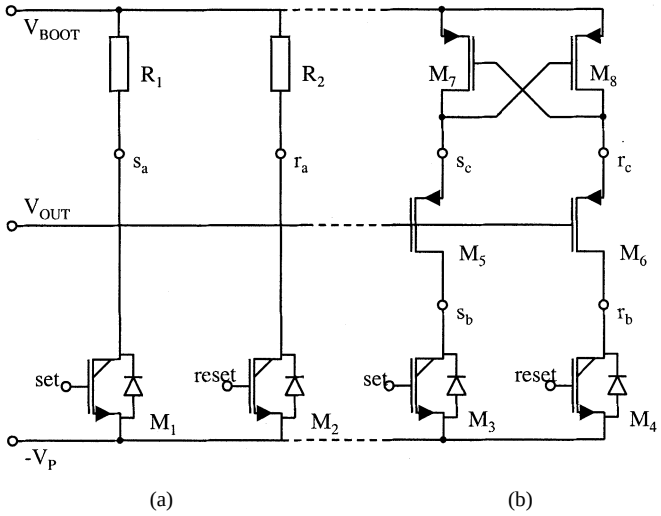

Fig. 11. Levelshifters.

VII. Fourstroke Levelshifter

A fast and robust levelshift is necessary to transfer the *set* and *reset* signals to the latch in the high-side driver. A simple but current-hungry implementation is shown in Fig. 11(a). The pull-down transistors $M_{1,2}$ have to be dimensioned such that their drain currents cause the appropriate voltage drop across the pull-up resistors $R_{1,2}$. For low current consumption the resistors need to be high ohmic, which conflicts with the speed requirement.

A more current-efficient solution is shown in Fig. 11(b). The latch formed by transistors $M_{7,8}$ can be toggled by pull-down transistors $M_{3,4}$. Transistors $M_{5,6}$ serve to limit the voltage on the nodes s_b and r_b. Suppose the *reset* signal is high and the *set* signal is low. In this case, node r_c is pulled down through M_6 to a level that is one threshold voltage higher than V_{out}, while node r_b is pulled down to $-V_P$. On the other side, node s_c is pulled up to V_{BOOT} by M_7 and s_b is pulled up to s_c through M_5. In

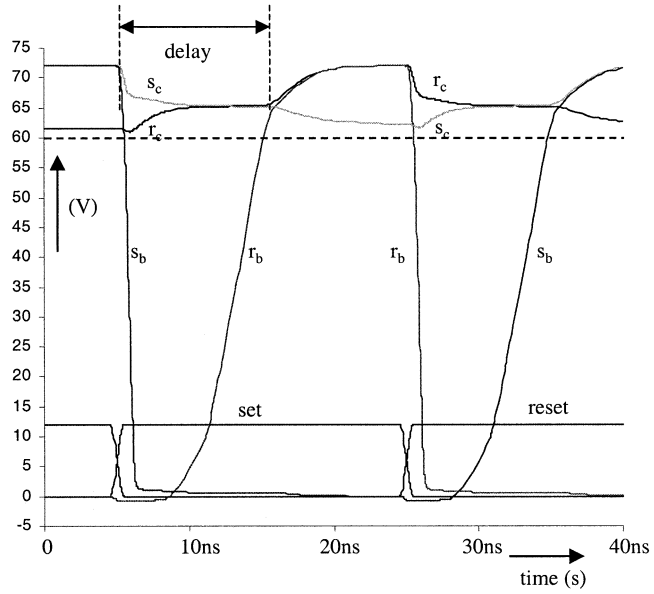

Fig. 12. Voltage transients in levelshifter.

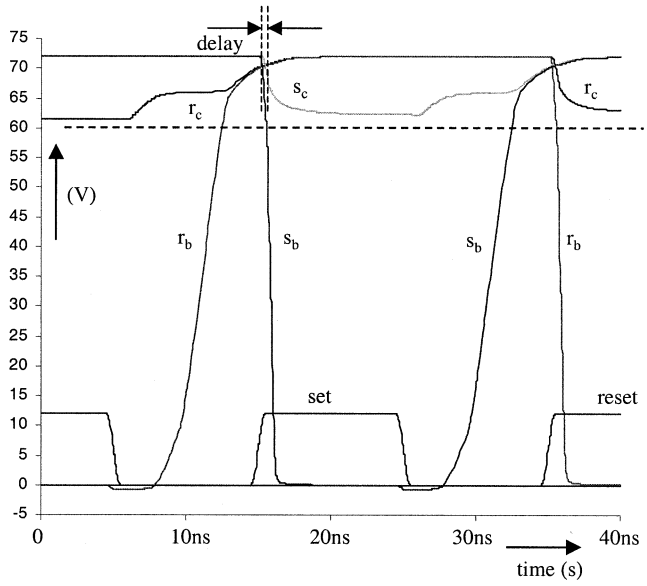

Fig. 14. Voltage transients in fourstroke levelshifter.

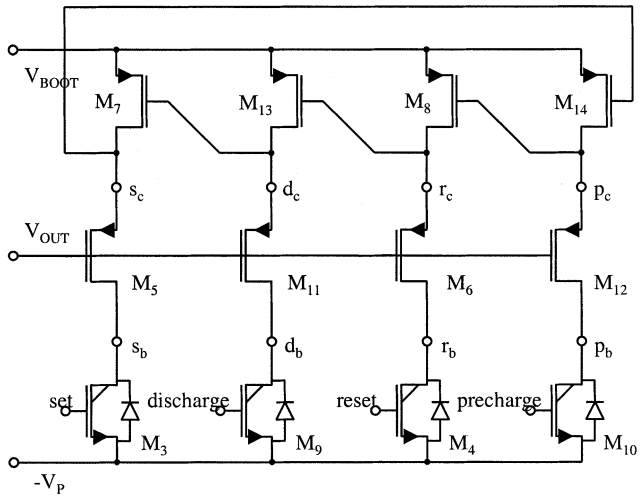

Fig. 13. Fourstroke levelshifter.

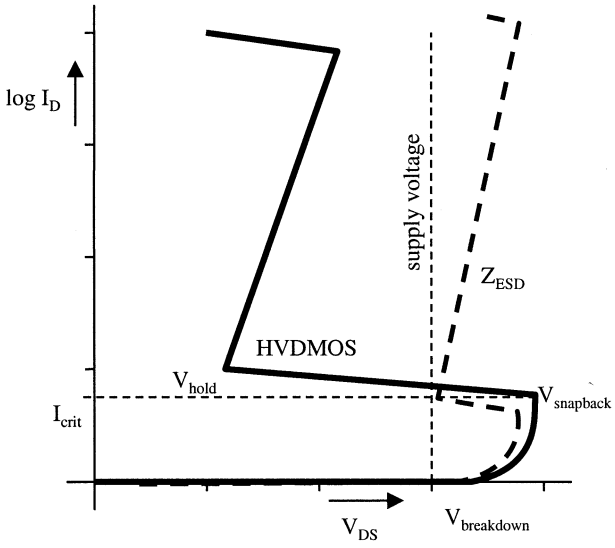

Fig. 15. Snapback curve of HV-DMOS transistor.

this situation, no current flows. As *reset* goes low, the voltages remain the same, but now nodes r_b and r_c have become floating.

As *set* goes high, nodes s_b and s_c are pulled down instantly. However, since M_7 is still switched on, node s_c is not pulled down completely, but stalls at a level determined by the dimensions of M_5 and M_7. In this situation, a substantial current flows through the branch M_3, M_5, M_7. On the other side, M_8 is switched on partially and pulls up node r_c and r_b. If the dimensions of $M_{6,8}$ and $M_{5,7}$ are the same, node r_c stalls at the same level as s_c. This situation continues until node r_b is pulled up to the level of r_c. Then r_b and r_c are pulled up to V_{BOOT}, M_7 shuts down and s_c is pulled down to one threshold above V_{OUT}.

The voltage transients are shown in Fig. 12. As can be seen, this mechanism results in a significant delay in the signal transfer that depends on the voltage level that needs to be shifted. This delay occurs because M_7 and M_3 are conducting at the same time and counteract each other. The same delay occurs when the latch is reset again.

A significant speedup can be achieved if M_7 is switched off before M_3 is switched on. This is realized by the circuit shown in Fig. 13. Two signals *precharge* and *discharge* are inserted between the *set* and *reset* signals. The four signals are subsequently high one at a time in a fixed cyclic sequence. Suppose the *reset* signal is high and the others are low. In that case, nodes r_b and r_c are at $-V_P$ and one threshold above V_{OUT}, respectively, and all other nodes are at V_{BOOT}. In this case, only nodes d_b and d_c are pulled up actively by M_{13}, while the others are floating. As *reset* goes low, *precharge* goes high. Now nodes p_b and p_c are pulled down unhindered since M_{14} is off. Consequently, M_8 is switched on fully and nodes r_b and r_c are pulled up fast.

Next, *precharge* goes low and *set* goes high, and the events are repeated with the corresponding components and nodes. In this manner, it is avoided that pull-up and pull-down transistors counteract each other. This arrangement is called the fourstroke

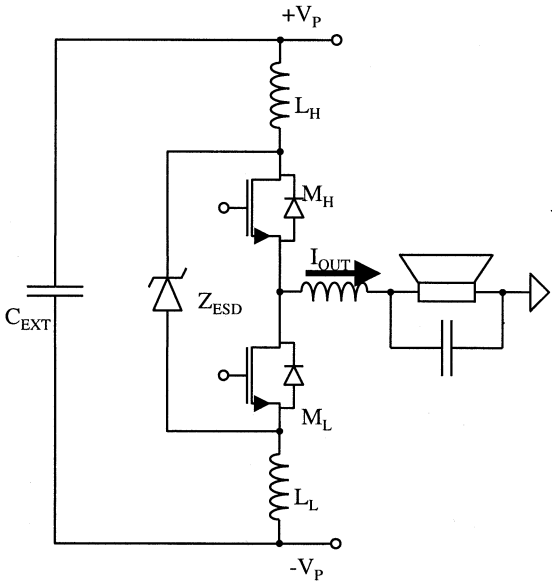

Fig. 16. Switching power stage.

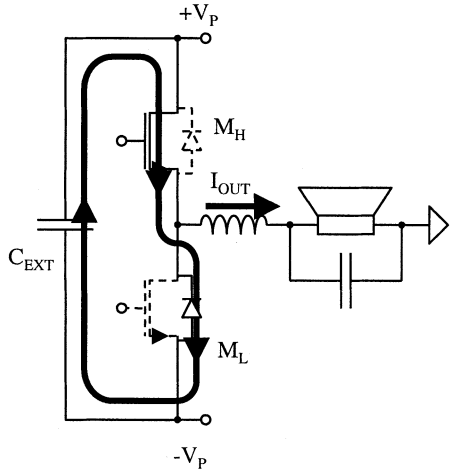

Fig. 17. Reverse recovery current.

levelshifter [6]. The corresponding voltage transients are shown in Fig. 14. As can be seen, the resulting transfer delay is extremely small and almost independent of the voltage level that needs to be shifted. The signals *precharge* and *discharge* can readily be generated by the carrousel handshake logic by decoding them from states C and E, respectively.

VIII. Robustness

A major problem in the design of the switching power stage is robustness. This has to do with the breakdown behavior of the power transistors. DMOS transistors have a bipolar parasite that causes the transistor to snapback when the breakdown current exceeds a critical level, as shown in Fig. 15. The snapback voltage usually lies well below the supply voltage, which leads to destruction of the transistor.

In Fig. 16, a half-bridge switching power stage is shown consisting of two DMOS power transistors. Also shown are the parasitic inductances $L_{H,L}$ associated with the bonding wires and lead fingers and an external decoupling capacitor $C_{\rm EXT}$. In a well-designed application, this decoupling capacitor should be as close as possible to the pins of the amplifier in order to minimize the loop area. Suppose the high-side power transistor M_H is conducting a current $I_{\rm OUT}$, which, consequently, also flows through the parasitic inductance L_H. As soon as the high-side power transistor switches off, the voltage at the output node decreases rapidly toward the low side, while the voltage at the drain of transistor M_H increases due to the steep dI/dt of the current through the parasitic inductor L_H. As a result the voltage across transistor M_H can exceed the breakdown voltage and snap back. In order to prevent this from happening, an electrostatic discharge (ESD) protection $Z_{\rm ESD}$ is placed in parallel, which clamps the voltage across the half-bridge to a safe value. The design of this protection is itself quite challenging since it should trigger before the power transistors break down but should have a hold voltage that is higher than the supply voltage. Of course, this arrangement should also protect the power transistors against ESD events. Evidently, the same mechanism applies to the low-side power transistor M_L.

IX. Electromagnetic Compatibility

The major source of EMI in most class-D amplifiers is the reverse recovery current associated with the backgate diodes. Consider the half-bridge switching power stage shown in Fig. 17. Now suppose the high-side power transistor is conducting a current $I_{\rm OUT}$. As soon as the high-side power transistor M_H is switched off, the output changes polarity and the current continues to flow through the backgate diode of the low-side power transistor M_L. After the deadtime has passed, transistor M_L is switched on and bypasses the backgate diode. No problems so far. After a certain amount of time transistor M_L is switched off again and the output current has to flow through the backgate diode of transistor M_L again. Then, after the deadtime has passed transistor M_H is switched on again, which pulls the output node toward $+V_P$ and reverses the polarity of the voltage across the backgate diode. The minority charge stored in the diode now causes a fast, high short-circuit current between the supplies as illustrated in Fig. 17.

The shape and size of the recovery current can to some extent be influenced by appropriate design of the driver circuits of the power transistors. In order to provide a short return path for the reverse recovery current, an external decoupling capacitor $C_{\rm EXT}$ has to be placed as near to the pins of the amplifier as possible. As mentioned before, the reverse recovery charge of the backgate diodes in the A-BCD process are remarkably small which results in good EMI performance.

Recovery currents excite resonances in the loops that are formed by the bondwire inductances and the parasitic capacitances of the power transistors. In order to dampen these resonances, external snubber networks across the power transistors and across the supplies are necessary. Across the power supplies, an electrolytic capacitor can be used as snubber.

The switching of the output current causes another EMI problem. The (continuous) output current $I_{\rm OUT}$ is alternately rerouted through the positive and negative power supply as illustrated in Fig. 18. Consequently, the supply currents are switched on and off repetitively. In order to provide a short

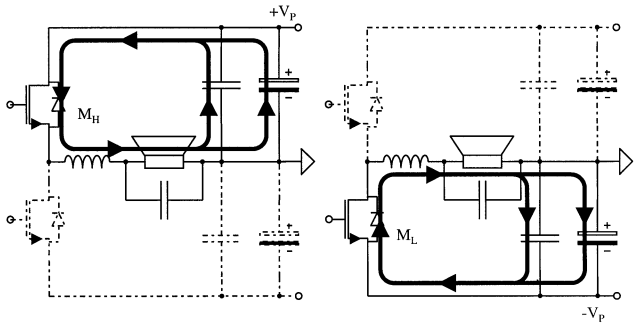

Fig. 18. Current loop switching.

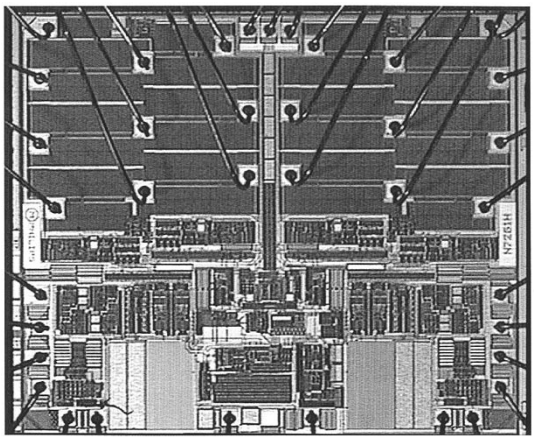

Fig. 19. Chip photograph.

return path for the current good high-frequency and low-frequency decoupling of the supply lines to a low-impedance groundplane is essential.

Ferrite beads in series with the supply lines are required to contain the discontinuous currents in the designed loops and prevent them from leaving the printed circuit board (PCB). In the PCB, the physical layout of the current loops should overlap such that the induced magnetic fields of both loops coincide.

The amplifier is encapsulated in a 24-lead small outline power SMD package. This package allows for very compact application of the amplifier, which is probably the biggest advantage of integrated class-D when compared to discrete solutions. A compact application is essential for good EMC performance. The pinning is such that all input and control pins are grouped on one side and all power outputs on the other. Separate supplies are used for analog, digital and power circuits. The thermal resistance from junction to case is typically 1.0 K/W. Under most practical conditions, only a very small external heatsink is required.

X. Results

The amplifier can be used in SE stereo or BTL mono configuration. At a supply voltage of ± 30 V the amplifier can deliver 2×100 W into two 4-Ω loads in SE or 1×200 W into one 8 Ω load in BTL. A chip photograph is shown in Fig. 19. Some key characteristics are summarized in Table I.

In the current implementation the deadtime of the switching power stage is about 70 ns. Further research is done to reduce the deadtime. In Fig. 20, the total harmonic distortion (THD) + N versus output power is shown for signal frequencies of 100 Hz, 1 kHz, and 10 kHz. The measurements have been done with Audio Precision System Two using a 22-Hz–22-kHz filter. Both channels of the amplifier are loaded with 4-Ω loads and driven simultaneously. The carrier frequency is at 350 kHz and

TABLE I
Performance Characteristics

Vp=+/-30V, R_{LOAD}=2x4Ω, f=1kHz, F_{OSC}=350kHz		
Parameter	**Condition**	**Typical Value**
Output Power	THD=1%	2x85W
Output Power	THD=10%	>2x100W
Quiescent Current	no load connected	55mA
Output Noise	inputs shorted	200μV
THD+Noise	P_{OUT}=1W	0.017%
Dynamic Range		103dB
Deadtime		70ns
R_{ON} DMOSTs		200mΩ
Efficiency	P_{OUT}=100W	>90%
Die Size	$22mm^2$	
Package	24-lead power SMD	

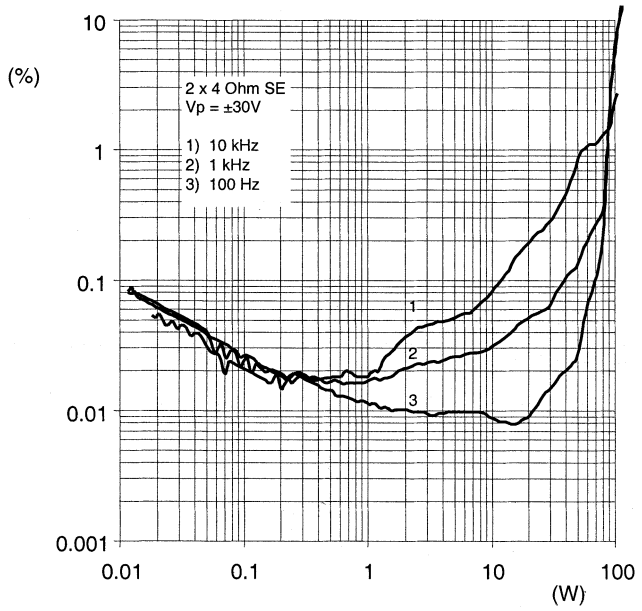

Fig. 20. THD+N versus output power.

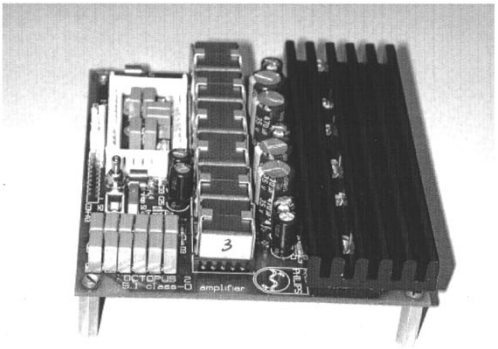

Fig. 21. 6×100-W application for 5.1 systems.

a symmetrical supply voltage of ± 30 V has been used. For moderate output power which corresponds to average listening levels, the distortion is well below 0.05% for all audio frequencies. Because the loopgain decreases with frequency, the distortion increases with frequency.

An application example of the class-D amplifier is the compact six-channel amplifier module for DVD receivers shown in Fig. 21. The application contains three integrated stereo class-D amplifiers, which are located underneath the heatsink. The dimensions of the two-layer PCB are 9.0 cm $\times$ 10.0 cm and it is about 2 cm high. Several measures have been taken to improve EMC performance. All connectors are placed close together and shielded coils have been used. The bottom layer of the PCB is almost completely used as groundplane. A master clock is used that can be switched to two carrier frequencies to avoid problems with AM reception. In this form, the PCB complies with legal EMC limits. However, achieving tuner compatibility remains and probably will remain a matter of careful system design.

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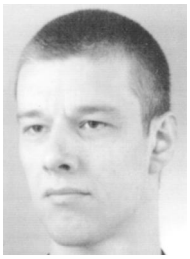

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