

## IR2136/IR21362/ IR21363/IR21365 (J&S)

### Features

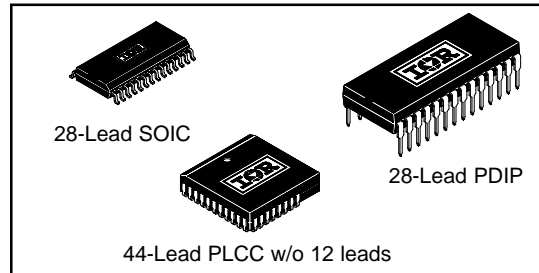
- Floating channel designed for bootstrap operation  
Fully operational to +600V  
Tolerant to negative transient voltage  
dV/dt immune
- Gate drive supply range from 10 to 20V (IR2136),  
11.5 to 20V (IR21362) or 12 to 20V (IR21363/IR21365)
- Undervoltage lockout for all channels
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Lowside outputs out of phase with inputs. High  
side outputs out of phase (IR2136/IR21363/IR21365)  
or in phase (IR21362) with inputs.
- Cross-conduction prevention logic
- 3.3V logic compatible
- Lower di/dt gate driver for better noise immunity
- Externally programmable delay for automatic fault clear

### Description

The IR2136/IR21362/IR21363/IR21365(J&S) are high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with CMOS or LSTTL outputs, down to 3.3V logic. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. An open-drain FAULT signal is provided to indicate that an overcurrent or undervoltage shutdown has occurred. Overcurrent fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the

### 3-PHASE BRIDGE DRIVER

#### Packages



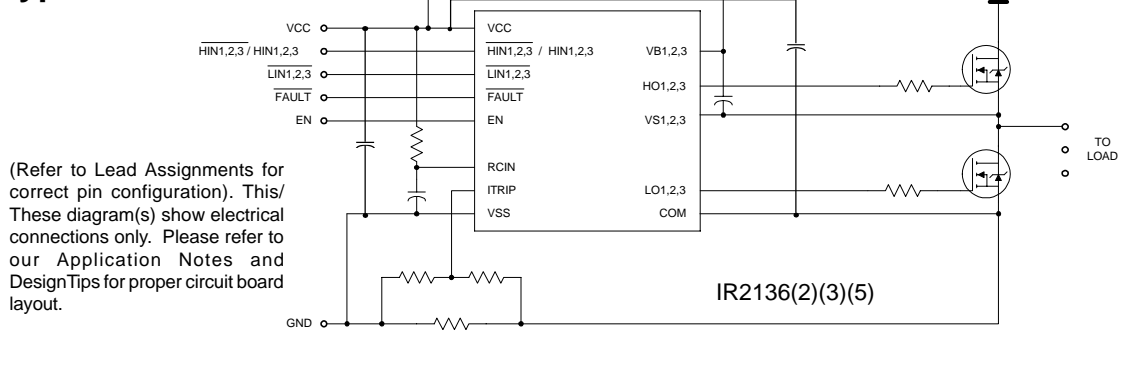
#### Feature Comparison

##### 2136/21362/21363/21365

Part	Input logic	Under voltage Lockout (VCC, VBS)	Itrip Threshold
2136	$\overline{\text{HIN}}/\overline{\text{LIN}}$	10V	0.46V
21362	HIN/LIN	11.5V	0.46V
21363	$\overline{\text{HIN}}/\overline{\text{LIN}}$	12V	0.46V
21365	$\overline{\text{HIN}}/\overline{\text{LIN}}$	12V	4.30V

RCIN input. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive N-channel power MOSFETs or IGBTs in the high side configuration which operates up to 600 volts.

### Typical Connection



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V <sub>S</sub>	High side offset voltage	V <sub>B1,2,3</sub> - 25	V <sub>B1,2,3</sub> + 0.3	V	
V <sub>BS</sub>	High side floating supply voltage	-0.3	625		
V <sub>HO</sub>	High side floating output voltage	V <sub>S1,2,3</sub> - 0.3	V <sub>B1,2,3</sub> + 0.3		
V <sub>CC</sub>	Low side and logic fixed supply voltage	-0.3	25		
V <sub>SS</sub>	Logic ground	V <sub>CC</sub> - 25	V <sub>CC</sub> + 0.3		
V <sub>LO1,2,3</sub>	Low side output voltage	-0.3	V <sub>CC</sub> + 0.3		
V <sub>IN</sub>	Input voltage LIN,HIN,ITRIP, EN, RCIN	V <sub>SS</sub> - 0.3	lower of (V <sub>SS</sub> + 15) or (V <sub>CC</sub> + 0.3)		
V <sub>FLT</sub>	FAULT output voltage	V <sub>SS</sub> - 0.3	V <sub>CC</sub> + 0.3		
dV/dt	Allowable offset voltage slew rate	—	50		
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25°C	(28 lead PDIP)	—	1.5	W
		(28 lead SOIC)	—	1.6	
		(44leadPLCC)	—	2.0	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	(28 lead PDIP)	—	83	°C/W
		(28 lead SOIC)	—	78	
		(44 lead PLCC)	—	63	
T <sub>J</sub>	Junction temperature	—	150	°C	
T <sub>S</sub>	Storage temperature	-55	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The V<sub>S</sub> offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units	
V <sub>B1,2,3</sub>	High side floating supply voltage	IR2136	V <sub>S1,2,3</sub> +10	V <sub>S1,2,3</sub> +20	V
		IR21362	V <sub>S1,2,3</sub> +11.5	V <sub>S1,2,3</sub> +20	
		IR21363/IR21365	V <sub>S1,2,3</sub> +12	V <sub>S1,2,3</sub> +20	
V <sub>S1,2,3</sub>	High side floating supply offset voltage	Note 1	600		
V <sub>HO1,2,3</sub>	High side output voltage	V <sub>S1,2,3</sub>	V <sub>B1,2,3</sub>		
V <sub>LO1,2,3</sub>	Low side output voltage	0	V <sub>CC</sub>		
V <sub>CC</sub>	Low side and logic fixed supply voltage	IR2136	10	20	
		IR21362	11.5	20	
		IR21363/IR21365	12	20	
V <sub>SS</sub>	Logic ground	-5	5		
V <sub>FLT</sub>	FAULT output voltage	V <sub>SS</sub>	V <sub>CC</sub>		
V <sub>RCIN</sub>	RCIN input voltage	V <sub>SS</sub>	V <sub>CC</sub>		

Note 1: Logic operational for V<sub>S</sub> of COM -5V to COM +600V. Logic state held for V<sub>S</sub> of COM -5V to COM -V<sub>BS</sub>. (Please refer to the Design Tip DT97-3 for more details).

Note 2: All input pins and the ITRIP pin are internally clamped with a 5.2V zener diode.

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in figure 1. For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute referenced to COM. The  $V_S$  offset rating is tested with all supplies biased at 15V differential.

Symbol	Definition	Min.	Max.	Units
$V_{ITRIP}$	ITRIP input voltage	$V_{SS}$	$V_{SS} + 5$	V
$V_{IN}$	Logic input voltage $\overline{LIN}$ , HIN (IR2136), HIN(IR21362), EN	$V_{SS}$	$V_{SS} + 5$	
$T_A$	Ambient temperature	-40	125	°C

Note 2: All input pins and the ITRIP pin are internally clamped with a 5.2V zener diode.

## Static Electrical Characteristics

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS1,2,3}$ ) = 15V unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all six channels ( $H_{S1,2,3}$  and  $L_{S1,2,3}$ ). The  $V_O$  and  $I_O$  parameters are referenced to COM and  $V_{S1,2,3}$  and are applicable to the respective output leads:  $H_{O1,2,3}$  and  $L_{O1,2,3}$ .

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions	
$V_{IH}$	Logic "0" input voltage $\overline{LIN1,2,3}$ , HIN1,2,3 Logic "1" input voltage HIN1,2,3	3	—	—	V		
$V_{IL}$	Logic "1" input voltage $\overline{LIN1,2,3}$ , HIN1,2,3 Logic "0" input voltage HIN1,2,3	—	—	0.8			
$V_{EN,TH+}$	EN positive going threshold	—	—	3			
$V_{EN,TH-}$	EN negative going threshold	0.8	—	—			
$V_{IT,TH+}$	ITRIP positive going threshold	IR21361/IR21362/IR21363	0.37	0.46		0.55	
		IR21365	3.85	4.30		4.75	
$V_{IT,HYS}$	ITRIP input hysteresis	IR21361/IR21362/IR21363	—	0.07		—	
		IR21365	—	.15		—	
$V_{RCIN,TH+}$	RCIN positive going threshold	—	8	—			
$V_{RCIN,HYS}$	RCIN input hysteresis	—	3	—			
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	0.9	1.4			$I_O = 20\text{ mA}$
$V_{OL}$	Low level output voltage, $V_O$	—	0.4	0.6			$I_O = 20\text{ mA}$
$V_{CCUV+}$ $V_{BSUV+}$	$V_{CC}$ and $V_{BS}$ supply undervoltage positive going threshold	IR2136	8.0	8.9	9.8		
		IR21362	9.6	10.4	11.2		
		IR21363/IR21365	10.6	11.1	11.6		
$V_{CCUV-}$ $V_{BSUV-}$	$V_{CC}$ and $V_{BS}$ supply undervoltage negative going threshold	IR2136	7.4	8.2	9.0		
		IR21362	8.6	9.4	10.2		
		IR21363/IR21365	10.4	10.9	11.4		
$V_{CCUVH}$ $V_{BSUVH}$	$V_{CC}$ and $V_{BS}$ supply undervoltage lockout hysteresis	IR2136	0.3	0.7	—	$\mu\text{A}$	
		IR21362	0.5	1.0	—		
		IR21363/IR21365	—	0.2	—		
$I_{LK}$	Offset supply leakage current	—	—	50	mA	$V_{B1,2,3}=V_{S1,2,3}=600\text{V}$	
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	70	120			
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	1.6	2.3		$V_{IN} = 0\text{V or } 5\text{V}$	
$V_{IN, CLAMP}$	Input clamp voltage (HIN, LIN, ITRIP and EN)	4.9	5.2	5.5	V	$I_{IN} = 100\mu\text{A}$	
$I_{LIN+}$	Input bias current (LOUT = HI)	—	200	300	$\mu\text{A}$	$V_{LIN} = 0\text{V}$	

# IR2136/IR21362/IR21363/IR21365(J&S)

International  
IR Rectifier

## Static Electrical Characteristics cont.

$V_{BIAS}$  ( $V_{CC}$ ,  $V_{BS1,2,3}$ ) = 15V unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$  and  $I_{IN}$  parameters are referenced to  $V_{SS}$  and are applicable to all six channels ( $H_{S1,2,3}$  and  $L_{S1,2,3}$ ). The  $V_O$  and  $I_O$  parameters are referenced to COM and  $V_{S1,2,3}$  and are applicable to the respective output leads:  $H_{O1,2,3}$  and  $L_{O1,2,3}$ .

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions	
$I_{LIN-}$	Input bias current (LOUT = LO)	—	100	220	μA	$V_{LIN} = 5V$	
$I_{HIN+}$	Input bias current (HOOUT = HI)	IR2136(3)(5)	—	200		300	$V_{HIN} = 0V$
		IR21362	—	30		100	$V_{HIN} = 5V$
$I_{HIN-}$	Input bias current (HOOUT = LO)	IR2136(3)(5)	—	100		220	$V_{HIN} = 5V$
		IR21362	—	0		1	$V_{HIN} = 0V$
$I_{ITRIP+}$	“high” ITRIP input bias current	—	30	100		$V_{ITRIP} = 5V$	
$I_{ITRIP-}$	“low” ITRIP input bias current	—	0	1		$V_{ITRIP} = 0V$	
$I_{EN+}$	“high” ENABLE input bias current	—	30	100		$V_{ENABLE} = 5V$	
$I_{EN-}$	“low” ENABLE input bias current	—	0	1		$V_{ENABLE} = 0V$	
$I_{RCIN}$	RCIN input bias current	—	0	1		$V_{RCIN} = 0V$ or 15V	
$I_{O+}$	Output high short circuit pulsed current	120	200	—	mA	$V_O = 0V$ , $PW \leq 10 \mu s$	
$I_{O-}$	Output low short circuit pulsed current	250	350	—		$V_O = 15V$ , $PW \leq 10 \mu s$	
$R_{ON,RCIN}$	RCIN low on resistance	—	50	100	Ω		
$R_{ON,FLT}$	FAULT low on resistance	—	50	100			

## Dynamic Electrical Characteristics

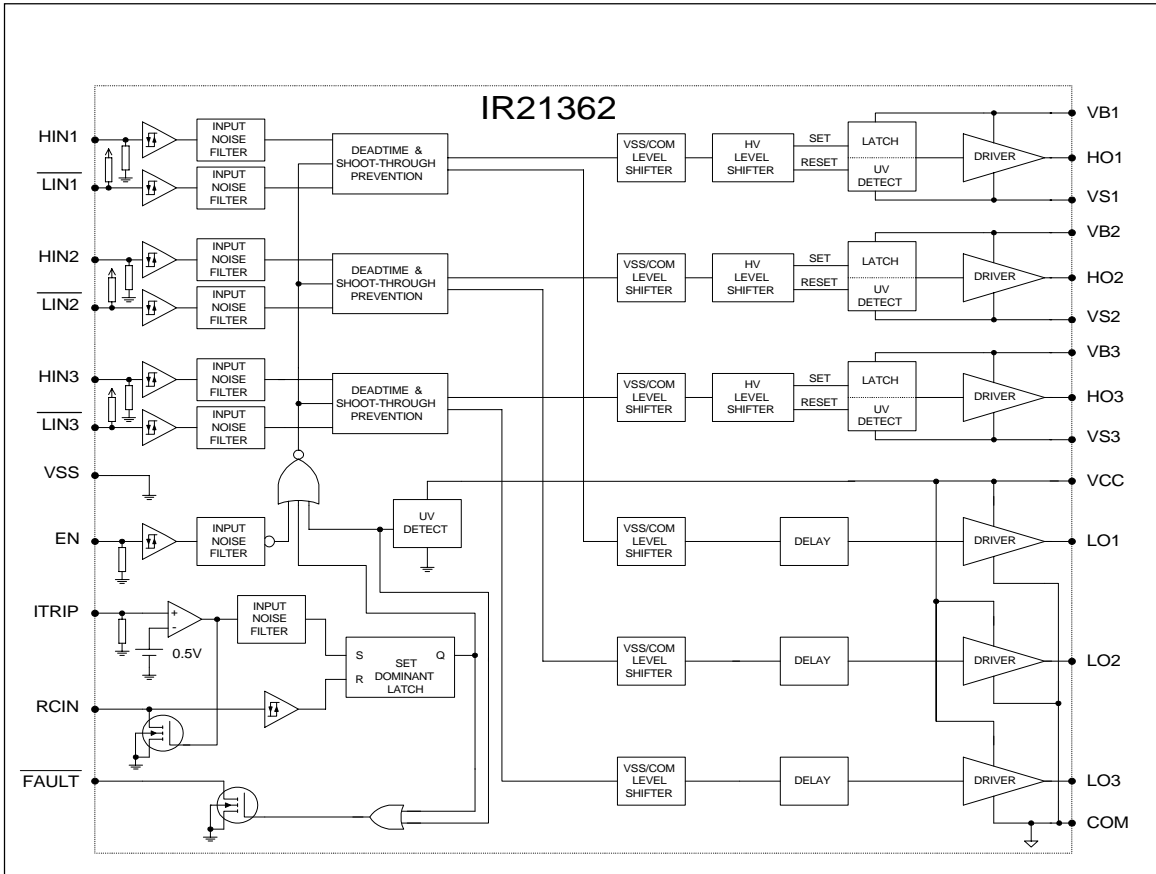
$V_{CC} = V_{BS} = V_{BIAS} = 15V$ ,  $V_{S1,2,3} = V_{SS} = COM$ ,  $T_A = 25^\circ C$  and  $C_L = 1000$  pF unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	300	425	550	nS	$V_{IN} = 0$ & 5V $V_{S1,2,3} = 0$ to 600V
$t_{off}$	Turn-off propagation delay	250	400	550		
$t_r$	Turn-on rise time	—	125	190		
$t_f$	Turn-off fall time	—	50	75		
$t_{EN}$	ENABLE low to output shutdown propagation delay	300	450	600		$V_{IN}, V_{EN} = 0V$ or 5V
$t_{ITRIP}$	ITRIP to output shutdown propagation delay	500	750	1000		$V_{ITRIP} = 5V$
$t_{bl}$	ITRIP blanking time	100	150	—		$V_{IN} = 0V$ or 5V $V_{ITRIP} = 5V$
$t_{FLT}$	ITRIP to FAULT propagation delay	400	600	800		$V_{IN} = 0V$ or 5V $V_{ITRIP} = 5V$
$t_{FILIN}$	Input filter time (HIN, LIN, EN)	100	200	—		$V_{IN} = 0$ & 5V
$t_{FLTCLR}$	FAULT clear time RCIN: R=2meg, C=1nF	1.3	1.65	2		mS
DT	Deadtime	220	290	360	nS	External dead time >400nsec
MT	Matching delay ON and OFF	—	40	75		
MDT	Matching delay, max ( $t_{on}, t_{off}$ ) - min ( $t_{on}, t_{off}$ ), ( $t_{on}, t_{off}$ are applicable to all 3 channels)	—	25	70		
PM	Output pulse width matching, $PW_{in} - PW_{out}$ (fig.2)	—	40	75		

NOTE: For high side PWM, HIN pulse width must be  $\geq 1 \mu sec$



Functional Block Diagram

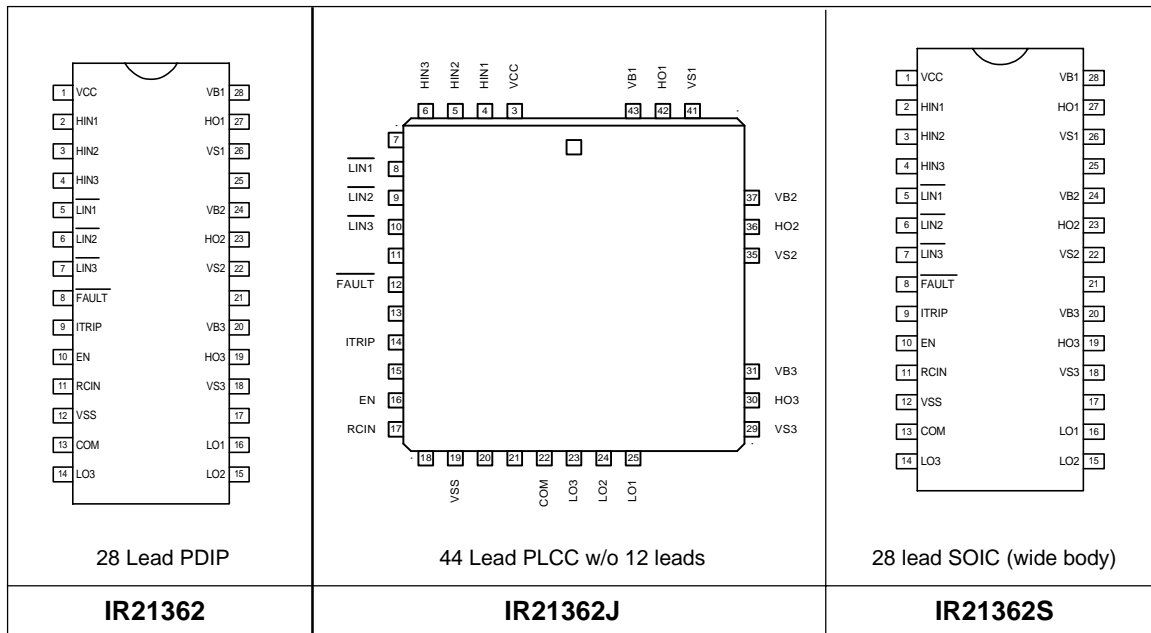
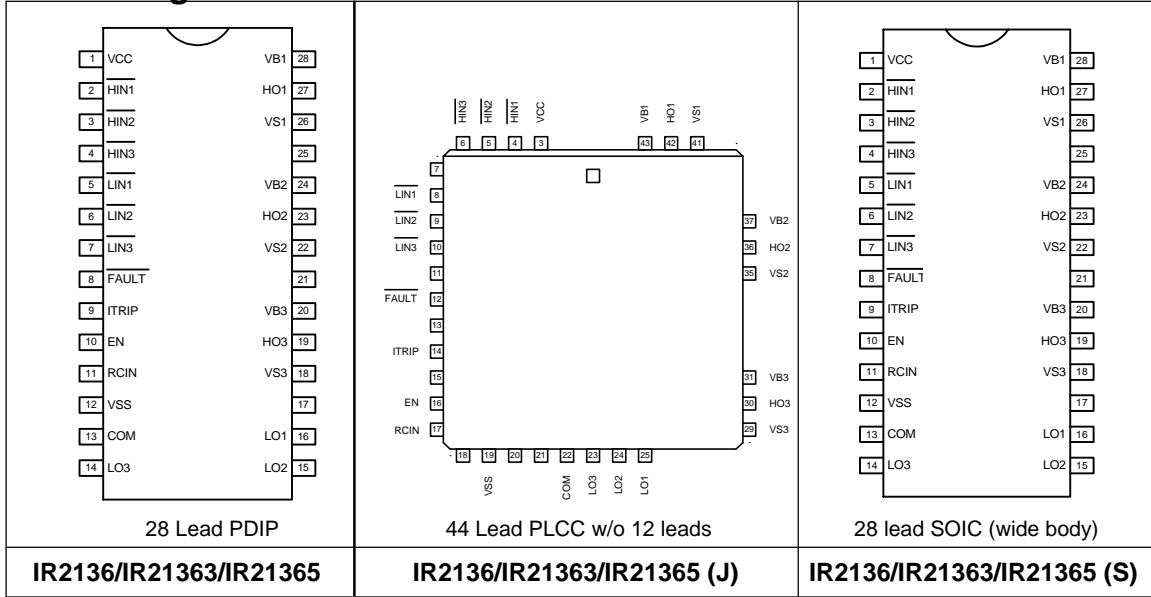


**Lead Definitions**

<b>Symbol</b>	<b>Description</b>
V <sub>CC</sub>	Low side and logic fixed supply
V <sub>SS</sub>	Logic Ground
HIN <sub>1,2,3</sub>	Logic inputs for high side gate driver outputs (HO <sub>1,2,3</sub> ), out of phase (IR2136/IR21363/IR21365)
HIN <sub>1,2,3</sub>	Logic inputs for high side gate driver outputs (HO <sub>1,2,3</sub> ), in phase (IR21362)
LIN <sub>1,2,3</sub>	Logic inputs for low side gate driver outputs (LO <sub>1,2,3</sub> ), out of phase
FAULT	Indicates over-current (ITRIP) or low-side undervoltage lockout has occurred. Negative logic, open-drain output
EN	Logic input to enable I/O functionality. Positive logic, i.e. I/O logic functions when ENABLE is high. No effect on FAULT and not latched
ITRIP	Analog input for overcurrent shutdown. When active, ITRIP shuts down outputs and activates FAULT and RCIN low. When ITRIP becomes inactive, FAULT stays active low for an externally set time T <sub>FLTCLR</sub> , then automatically becomes inactive (open-drain high impedance).
RCIN	External RC network input used to define FAULT CLEAR delay, T <sub>FLTCLR</sub> , approximately equal to R*C. When RCIN>8V, the FAULT pin goes back into open-drain high-impedance
COM	Low side gate driver return
V <sub>B1,2,3</sub>	High side floating supply
HO <sub>1,2,3</sub>	High side gate driver outputs
V <sub>S1,2,3</sub>	High voltage floating supply returns
LO <sub>1,2,3</sub>	Low side gate driver output

# IR2136/IR21362/IR21363/IR21365(J&S)

## Lead Assignments





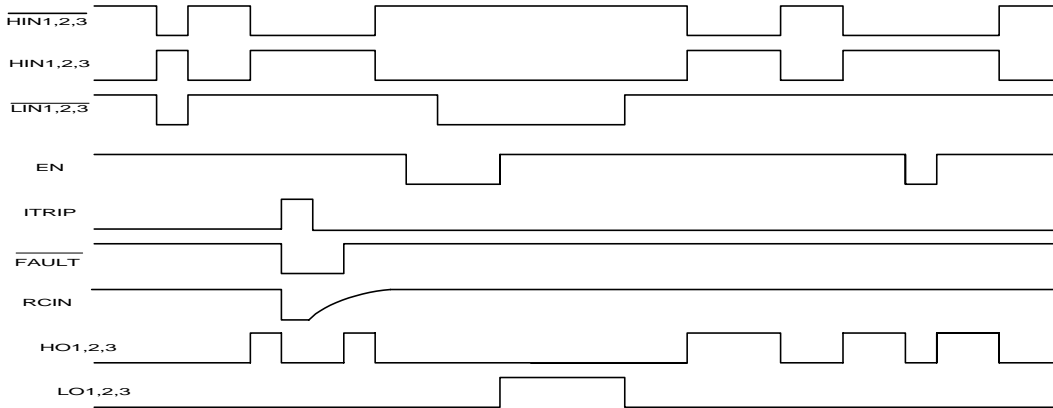


Figure 1. Input/Output Timing Diagram

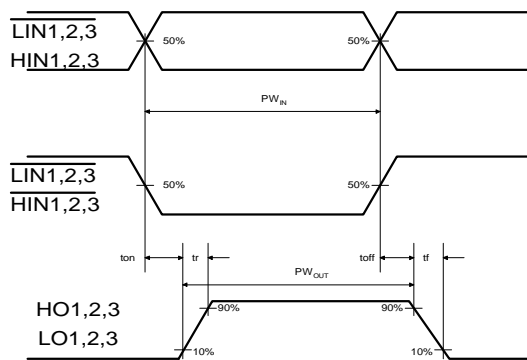


Figure 2. Switching Time Waveforms

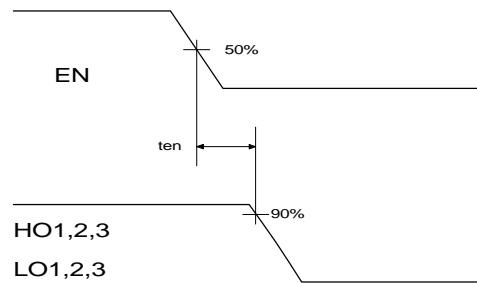
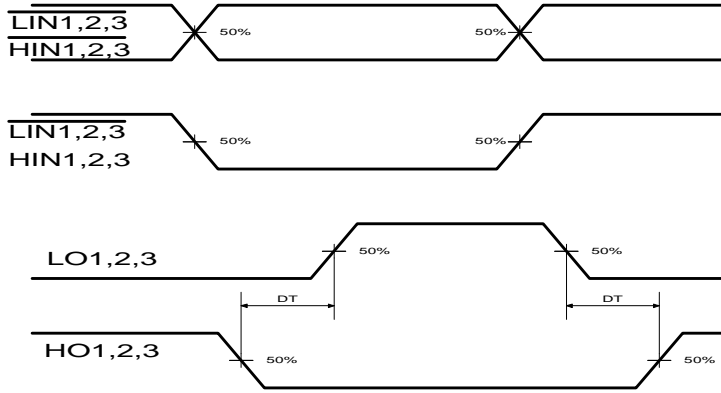
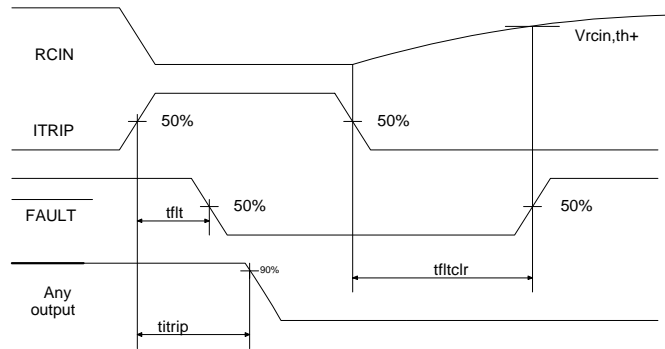


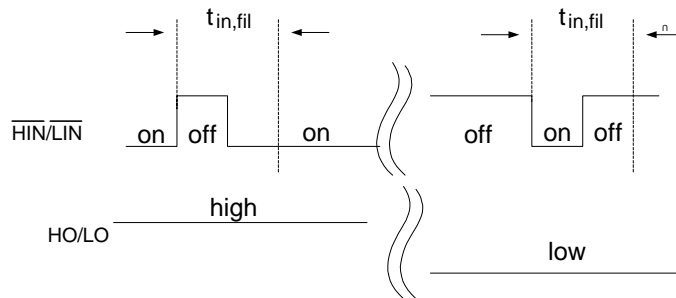
Figure 3. Output Enable Timing Waveform



**Figure 4. Internal Deadtime Timing Waveforms**



**Figure 5. ITRIP/RCIN Timing Waveforms**



**Figure 5.5 Input Filter Function**

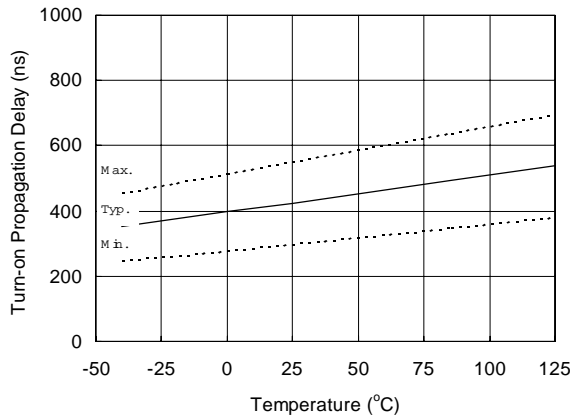


Figure 6A. Turn-on Propagation Delay vs. Temperature

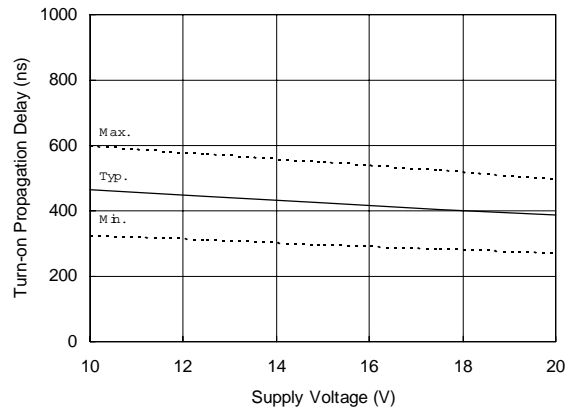


Figure 6B. Turn-on Propagation Delay vs. Supply Voltage

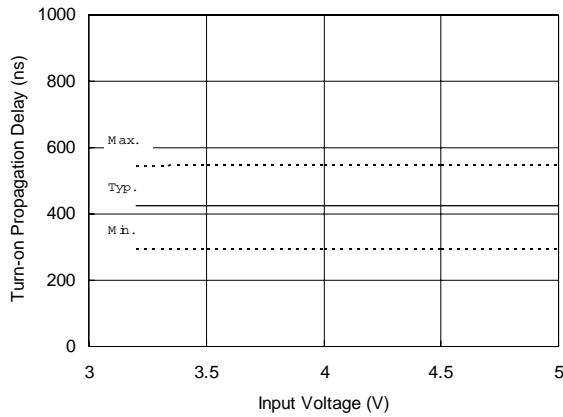


Figure 6C. Turn-on Propagation Delay vs. Input Voltage

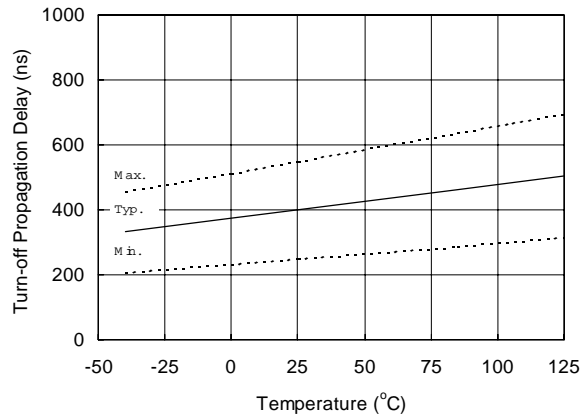


Figure 7A. Turn-off Propagation Delay vs. Temperature

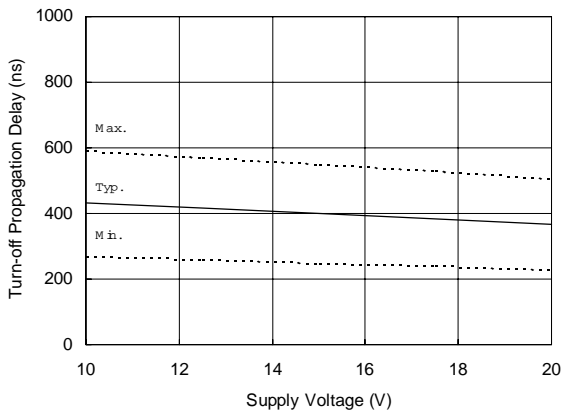


Figure 7B. Turn-off Propagation Delay vs. Supply Voltage

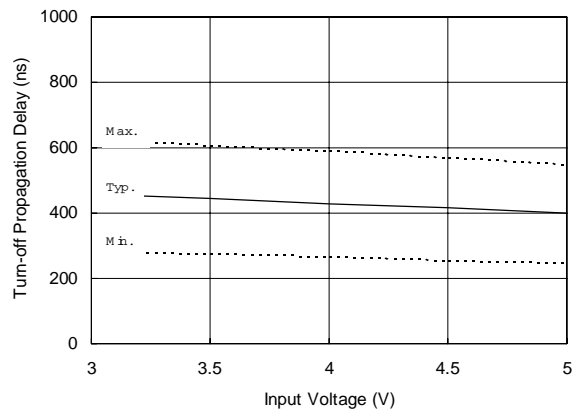


Figure 7C. Turn-off Propagation Delay vs. Input Voltage

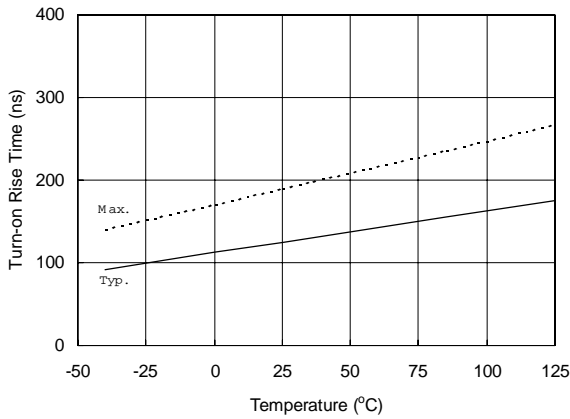


Figure 8A. Turn-on Rise Time vs. Temperature

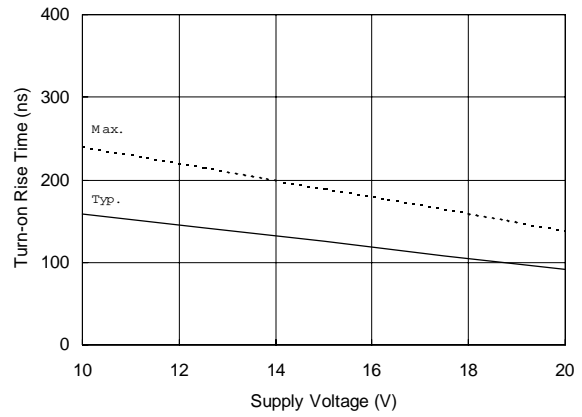
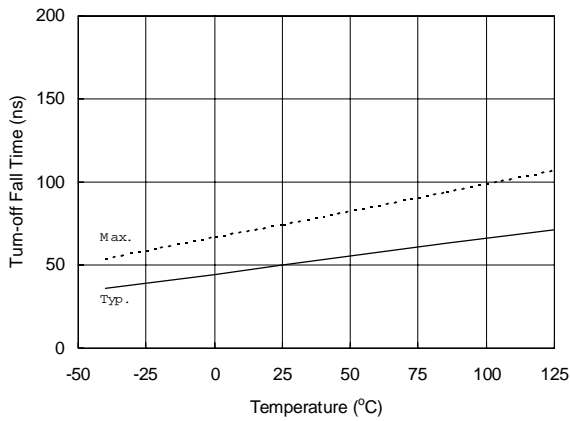
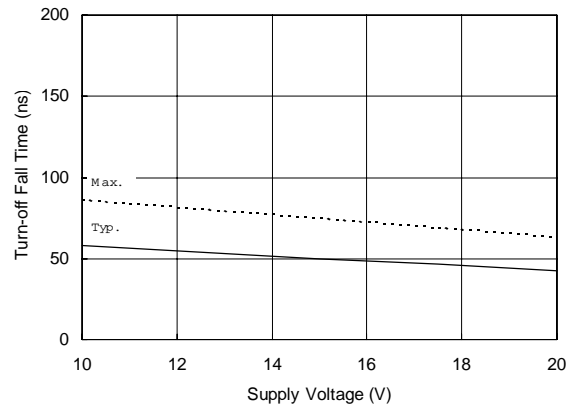


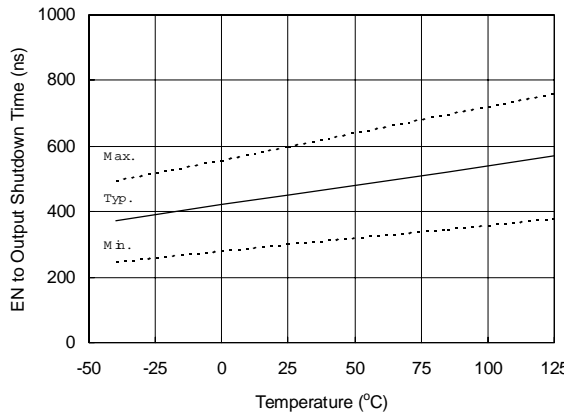
Figure 8B. Turn-on Rise Time vs. Supply Voltage



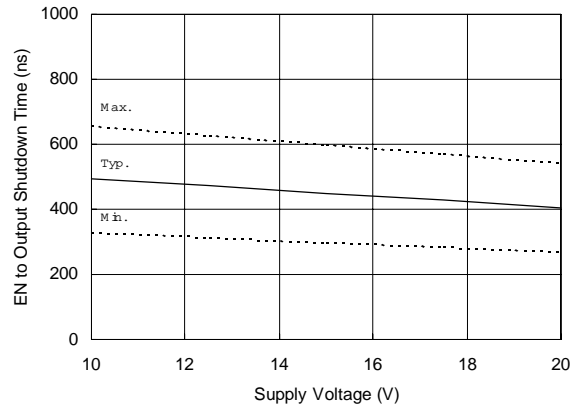
**Figure 9A. Turn-off Fall Time vs. Temperature**



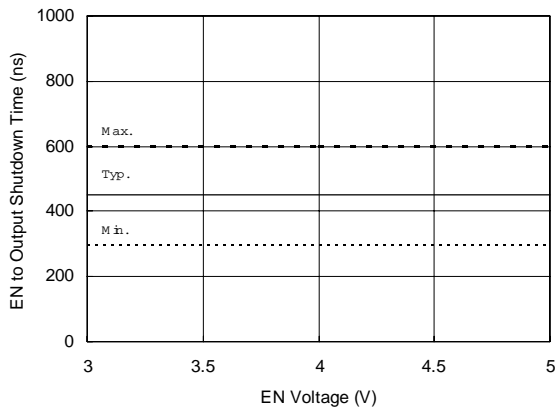
**Figure 9B. Turn-off Fall Time vs. Supply Voltage**



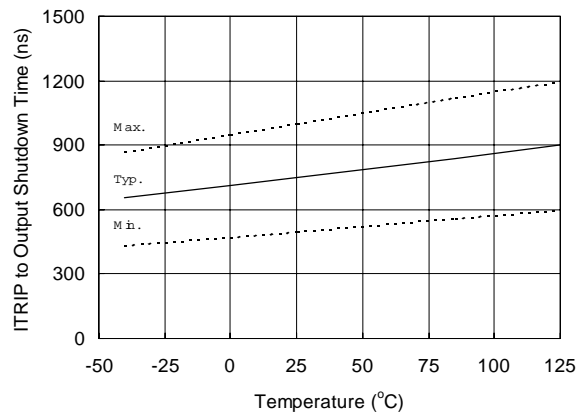
**Figure 10A. EN to Output Shutdown Time vs. Temperature**



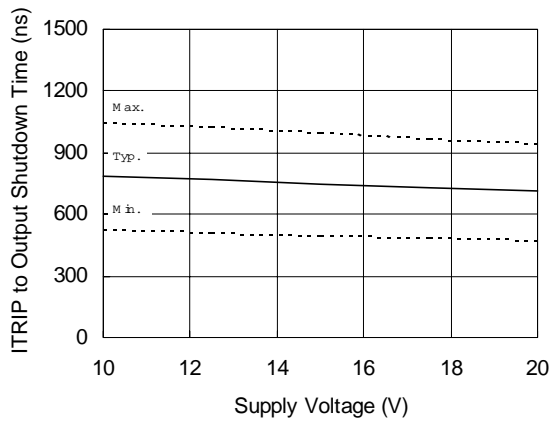
**Figure 10B. EN to Output Shutdown Time vs. Supply Voltage**



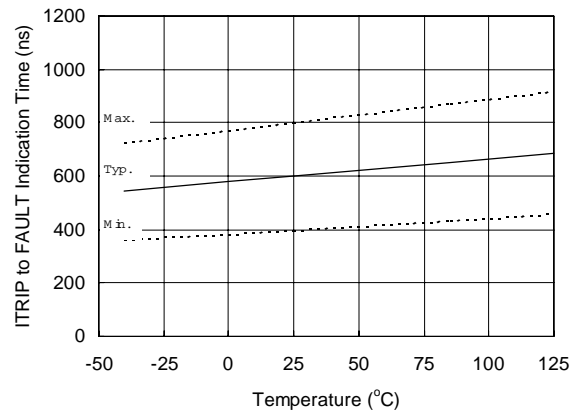
**Figure 10C. EN to Output Shutdown Time vs. EN Voltage**



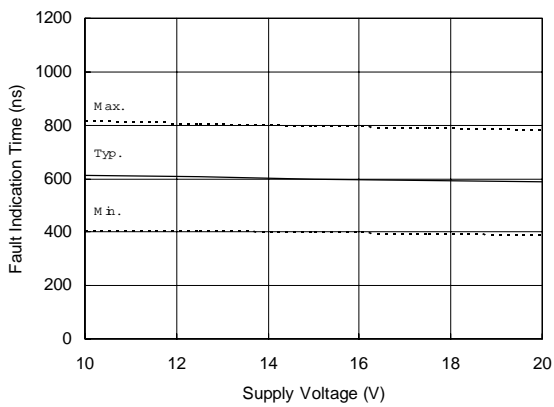
**Figure 11A. ITRIP to Output Shutdown Time vs. Temperature**



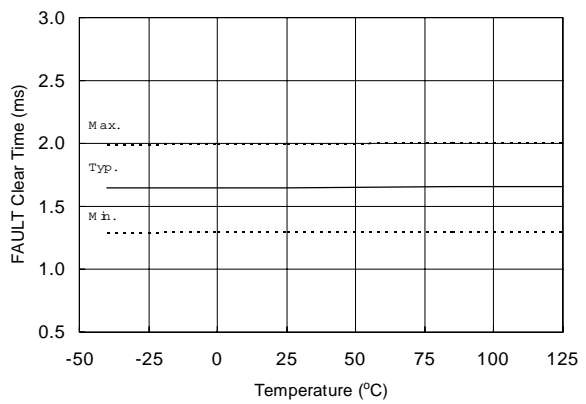
**Figure 11B. ITRIP to Output Shutdown Time vs. Supply Voltage**



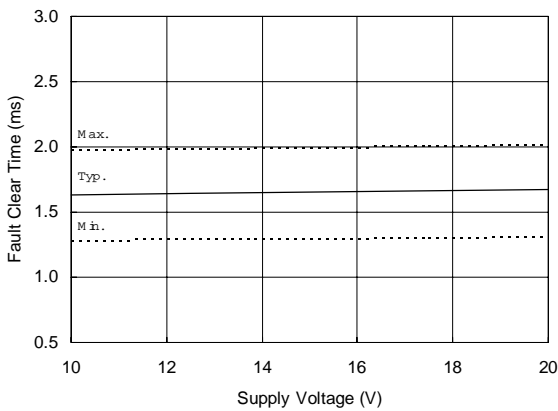
**Figure 12A. ITRIP to FAULT Indication Time vs. Temperature**



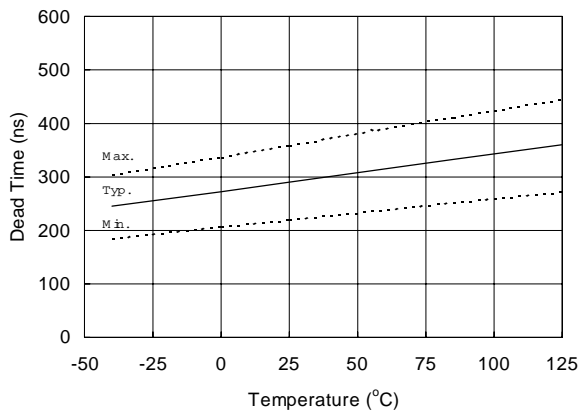
**Figure 12B. ITRIP to FAULT Indication Time vs. Supply Voltage**



**Fig13A. FAULT Clear Time vs. Temperature**



**Figure 13B. FAULT Clear Time vs. Supply Voltage**



**Figure 14A. Dead Time vs. Temperature**

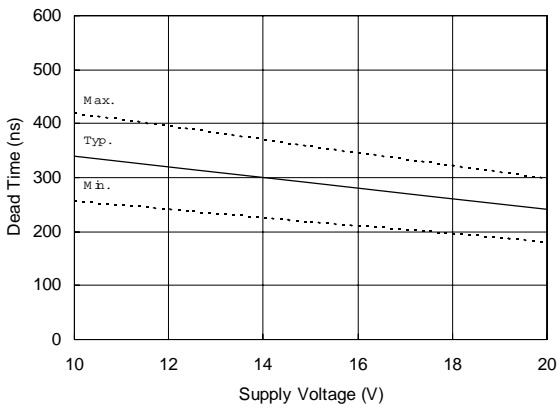


Figure 14B. Dead Time Time vs. Supply Voltage

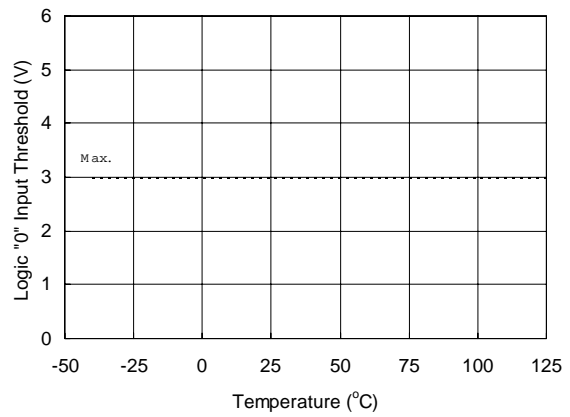


Figure 15A. Logic "0" Input Threshold vs. Temperature

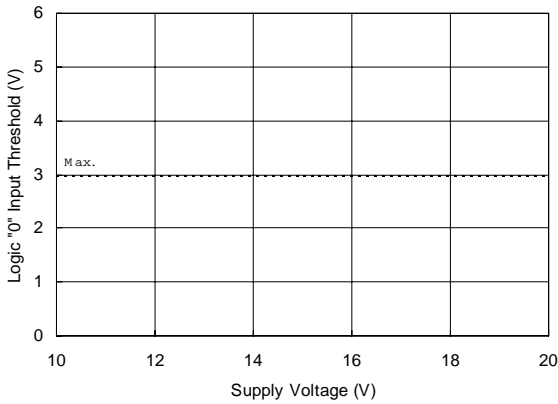


Figure 15B. Logic "0" Input Threshold vs. Supply Voltage

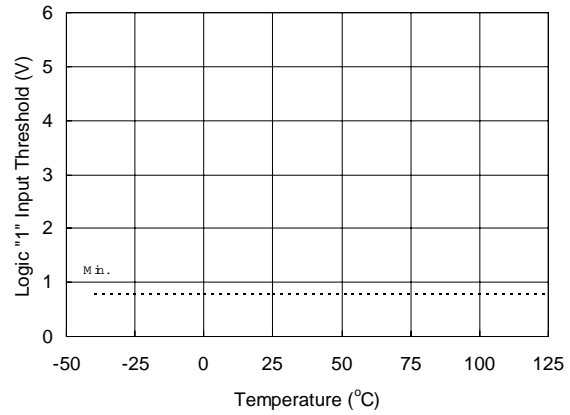
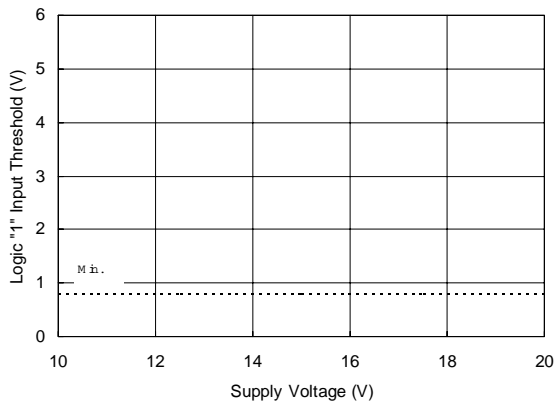
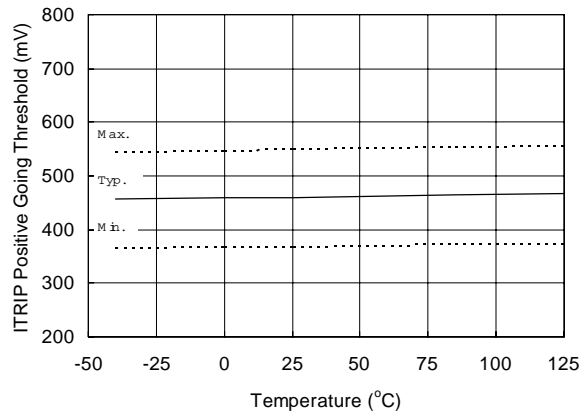


Figure 16A. Logic "1" Input Threshold vs. Temperature

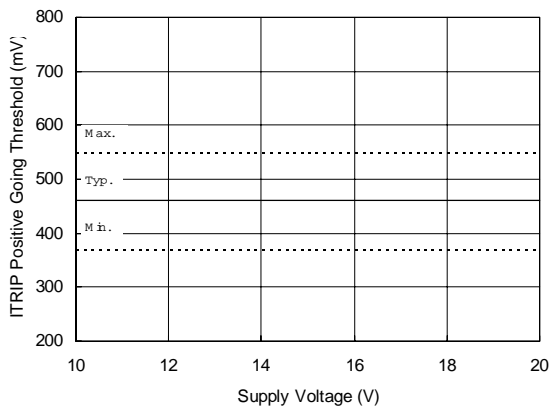




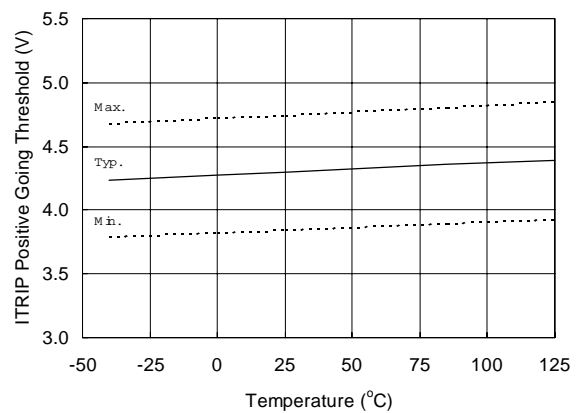
**Figure 16B. Logic "1" Input Threshold vs. Supply Voltage**



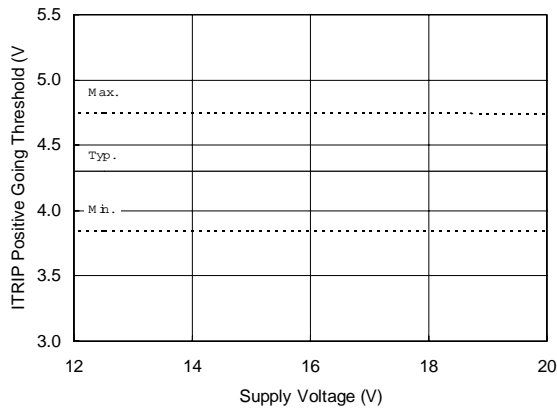
**Figure 17A. ITRIP Positive Going Threshold vs. Temperature (IR2136/21362/21363 Only)**



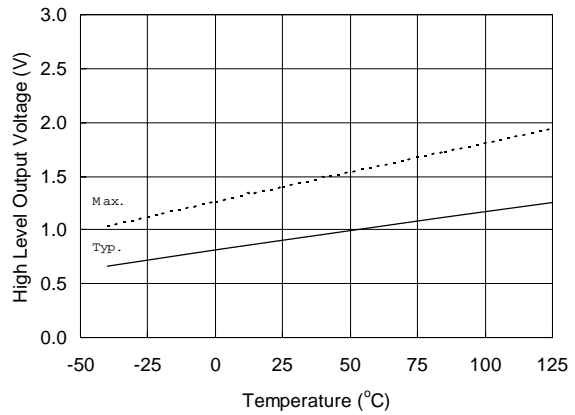
**Figure 17B. ITRIP Positive Going Threshold vs. Supply Voltage (IR2136/21362/21363 Only)**



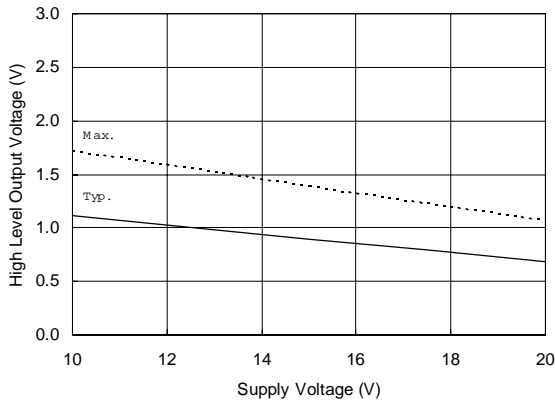
**Figure 17C. ITRIP Positive Going Threshold vs. Temperature (IR21365 Only)**



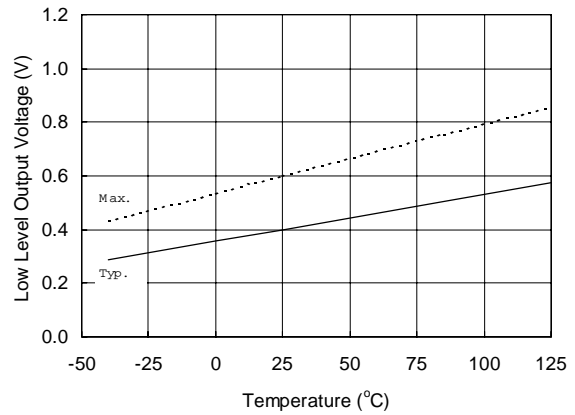
**Figure 17D. ITRIP Positive Going Threshold vs. Supply Voltage (IR21365 Only)**



**Figure 18A. High Level Output vs. Temperature**



**Figure 18B. High Level Output vs. Supply Voltage**



**Figure 19A. Low Level Output vs. Temperature**

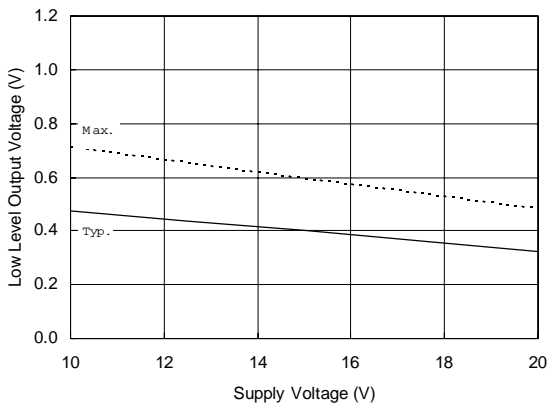


Figure 19B. Low Level Output vs. Supply Voltage

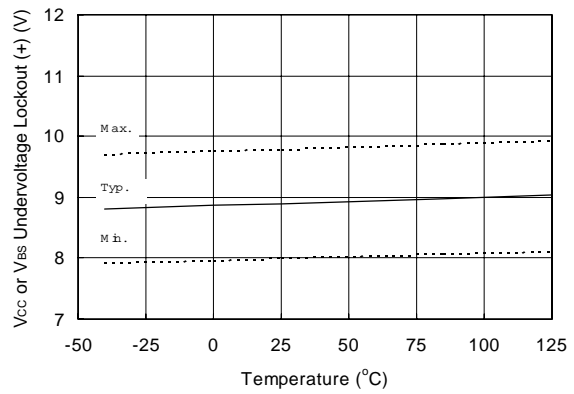


Figure 20.  $V_{CC}$  or  $V_{BS}$  Undervoltage (+) vs. Temperature (IR2136 Only)

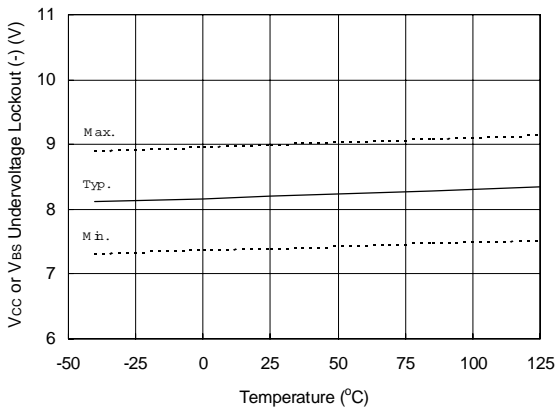


Figure 21.  $V_{CC}$  or  $V_{BS}$  Undervoltage (-) vs. Temperature (IR2136 Only)

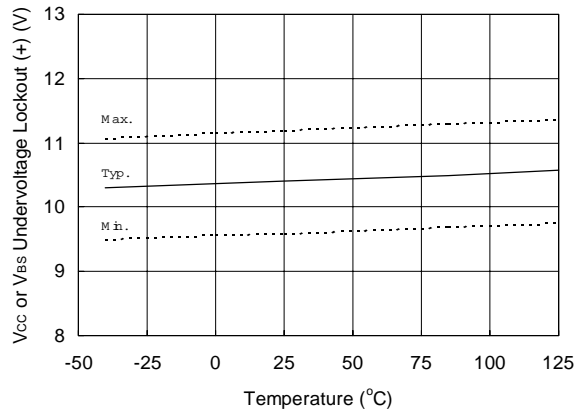
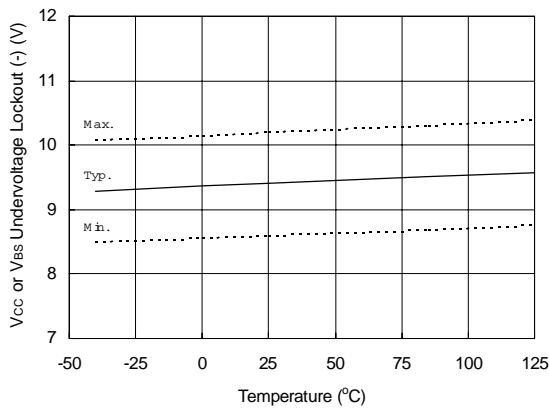
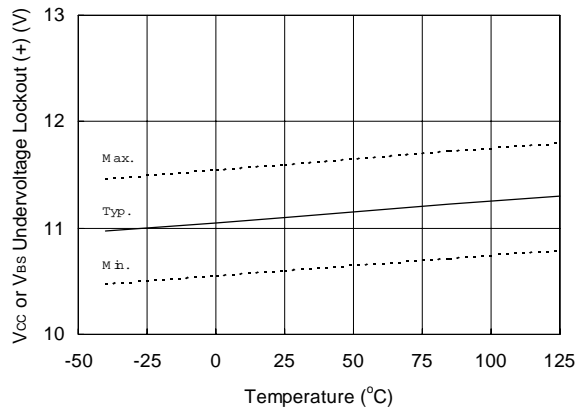


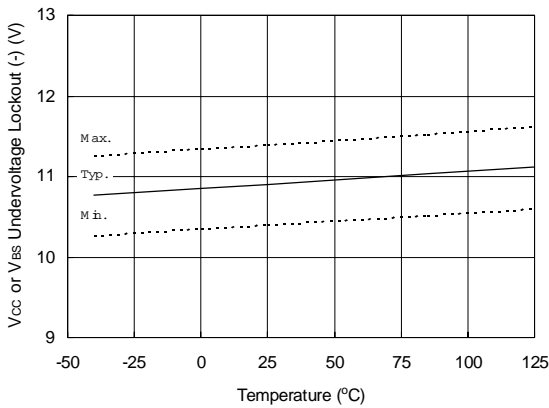
Figure 22.  $V_{CC}$  or  $V_{BS}$  Undervoltage (+) vs. Temperature (IR21362 Only)



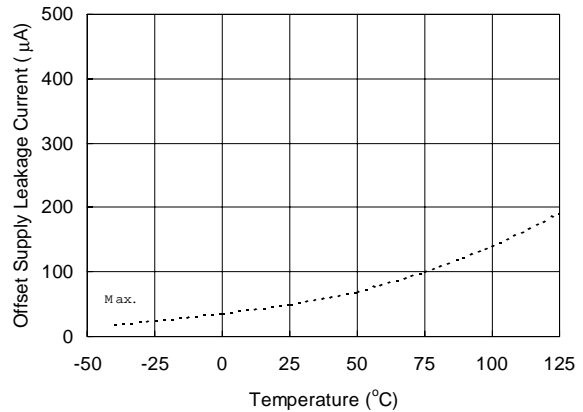
**Figure 23.  $V_{CC}$  or  $V_{BS}$  Undervoltage (-) vs. Temperature (IR21362 Only)**



**Figure 24.  $V_{CC}$  or  $V_{BS}$  Undervoltage (+) vs. Temperature (IR21363/21365 Only)**



**Figure 25.  $V_{CC}$  or  $V_{BS}$  Undervoltage (-) vs. Temperature (IR21363/21365 Only)**



**Figure 26A. Offset Supply Leakage Current vs. Temperature**

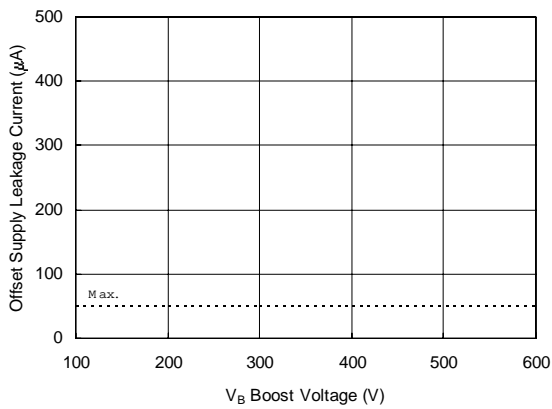


Figure 26B. Offset Supply Leakage Current vs. V<sub>B</sub> Boost Voltage

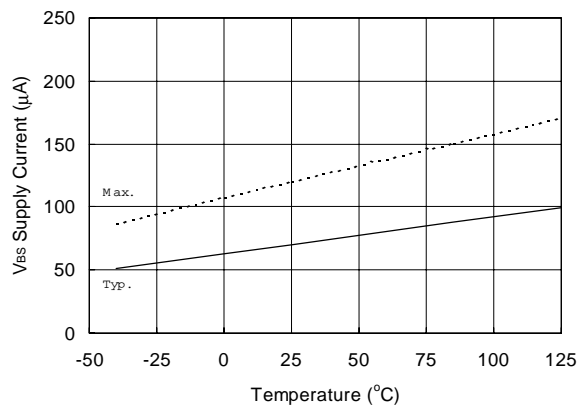


Figure 27A. V<sub>BS</sub> Supply Current vs. Temperature

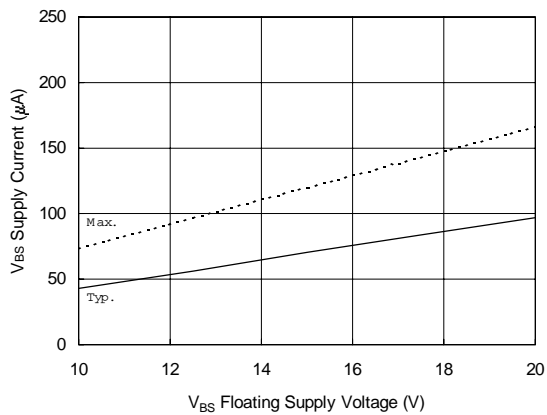


Figure 27B. V<sub>BS</sub> Supply Current vs. V<sub>BS</sub> Floating Supply Voltage

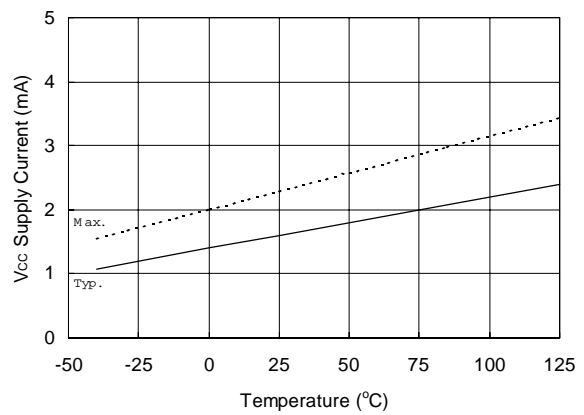
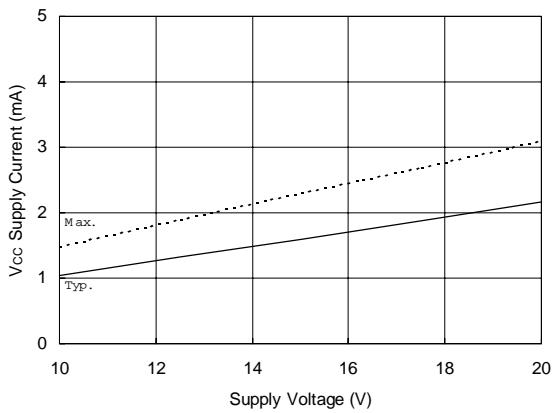
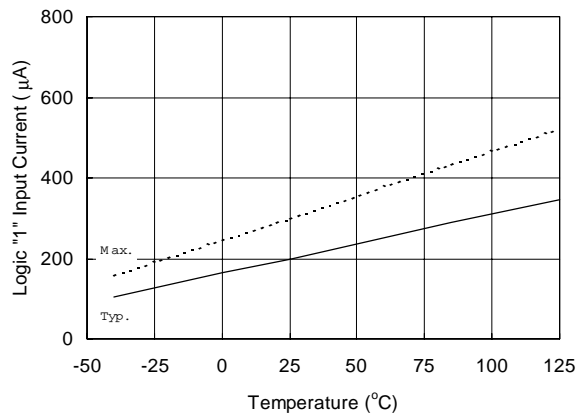


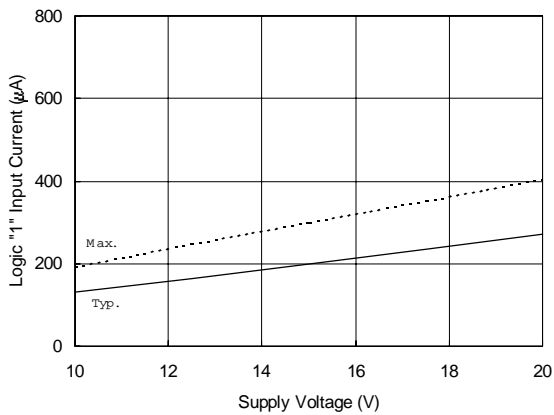
Figure 28A. V<sub>CC</sub> Supply Current vs. Temperature



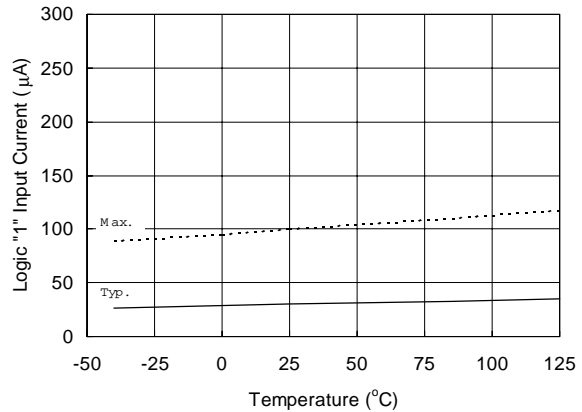
**Figure 28B. V<sub>CC</sub> Supply Current vs. V<sub>CC</sub> Supply Voltage**



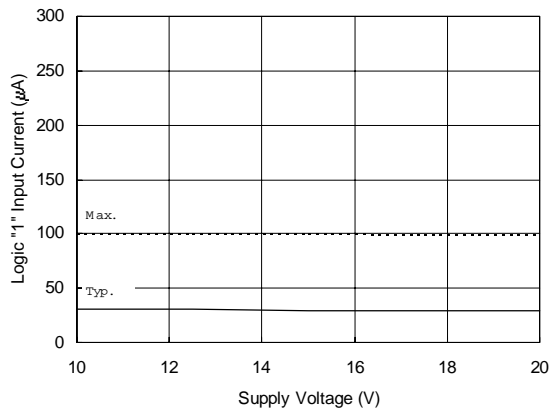
**Figure 29A. Logic "1" Input Current vs. Temperature (IR2136/21363/21365 and IR21362 Low Side Only)**



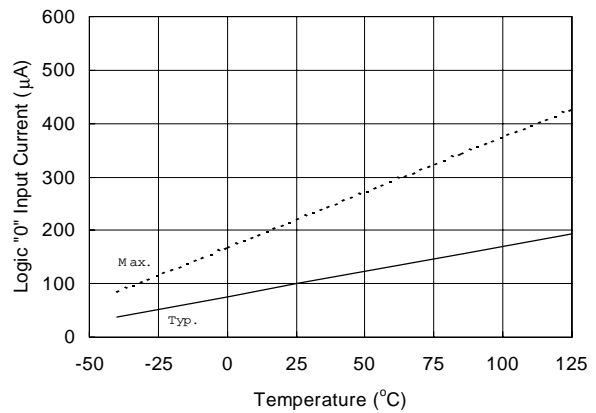
**Figure 29B. Logic "1" Input Current vs. Supply Voltage (IR2136/21363/21365 and IR21362 Low Side Only)**



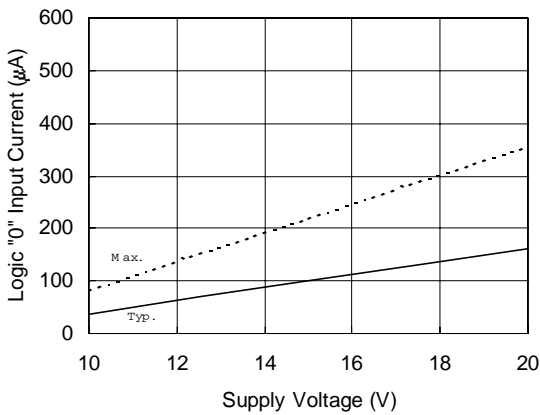
**Figure 29C. Logic "1" Input Current vs. Temperature (IR21362 High Side Only)**



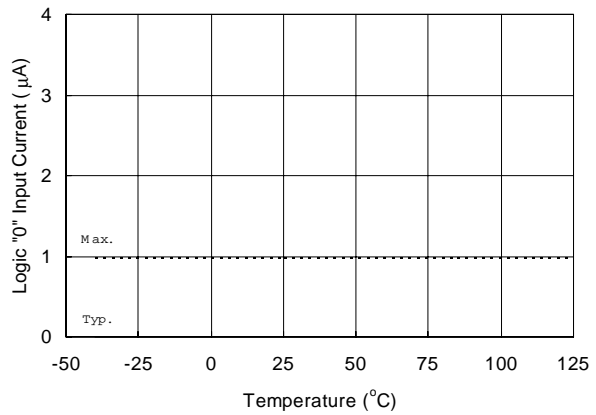
**Figure 29D. Logic "1" Input Current vs. Supply Voltage (IR21362 High Side Only)**



**Figure 30A. Logic "0" Input Current vs. Temperature (IR2136/21363/21365 and IR21362 Low Side Only)**



**Figure 30B. Logic "0" Input Current vs. Supply Voltage (IR2136/21363/21365 and IR21362 Low Side Only)**



**Figure 30C. Logic "0" Input Current vs. Temperature (IR21362 High Side Only)**

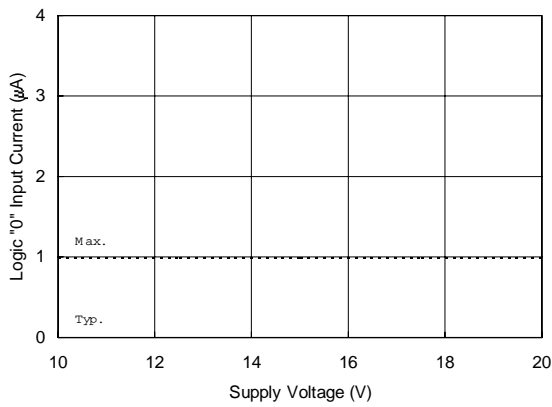


Figure 30D. Logic "0" Input Current vs. Supply Voltage (IR21362 High Side Only)

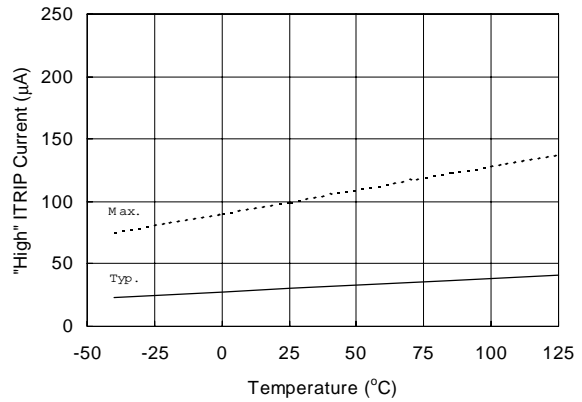


Figure 31A. "High" ITRIP Current vs. Temperature

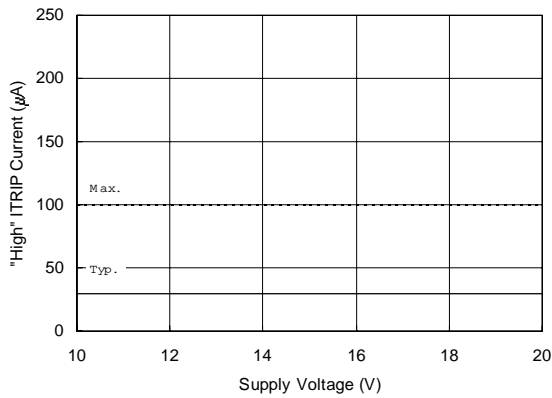


Figure 31B. "High" ITRIP Current vs. Supply Voltage

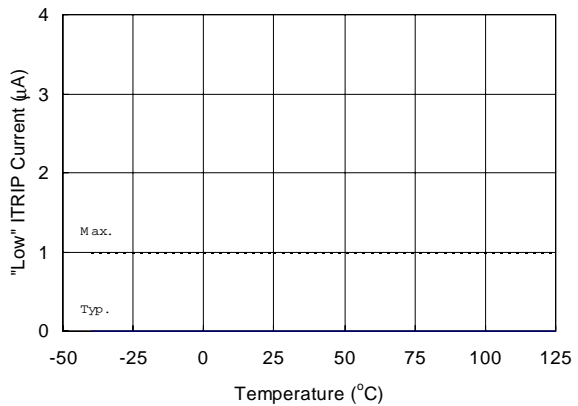
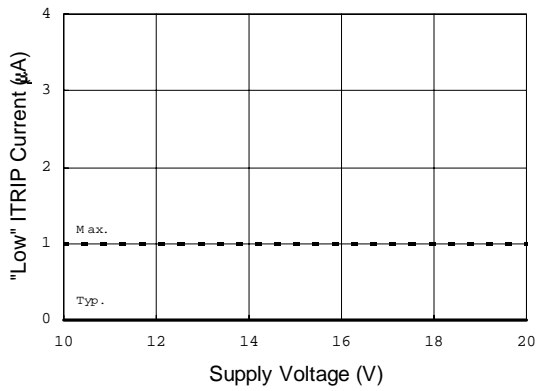
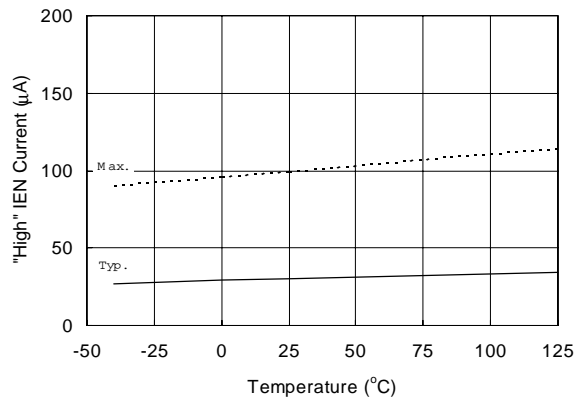


Figure 32A. "Low" ITRIP Current vs. Temperature

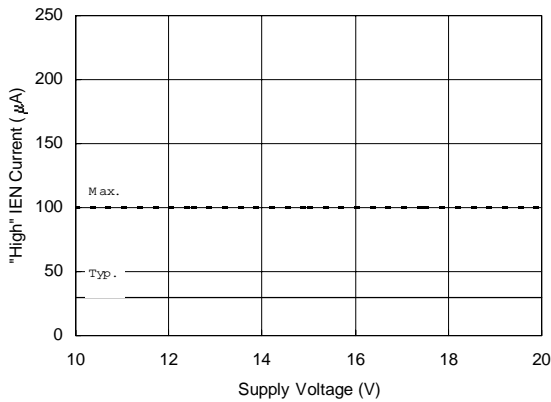




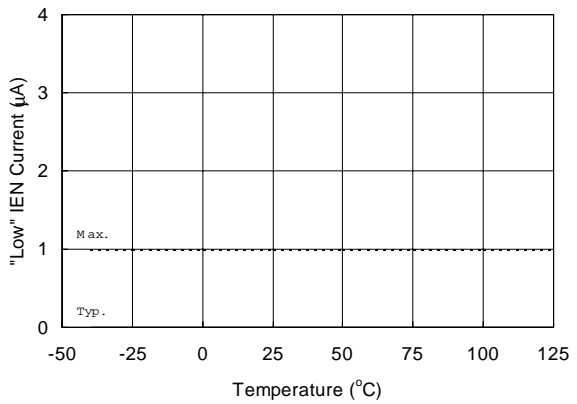
**Figure 32B. "Low" ITRIP Current vs. Supply Voltage**



**Figure 33A. "High" IEN Current vs. Temperature**



**Figure 33B. "High" IEN Current vs. Supply Voltage**



**Figure 34A. "Low" IEN Current vs. Temperature**

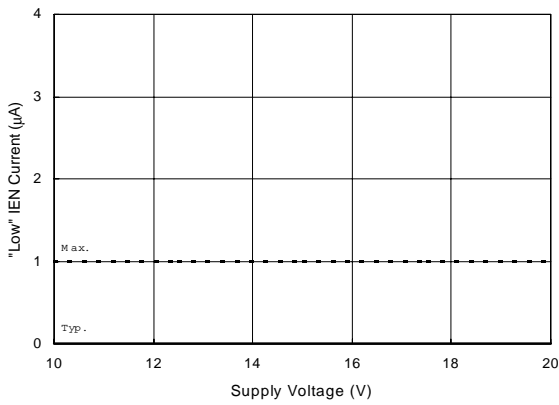


Figure 34B. "Low" IEN Current vs. Supply Voltage

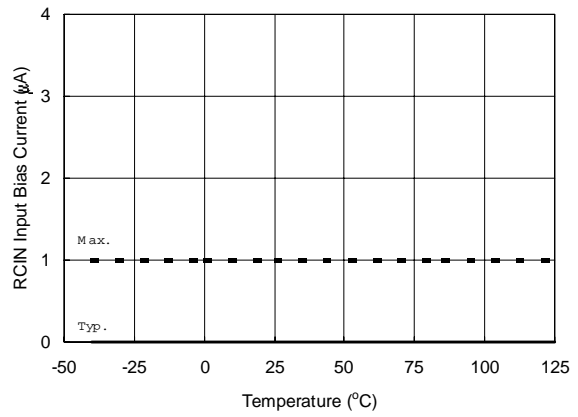


Figure 35A. RCIN Input Bias Current vs. Temperature

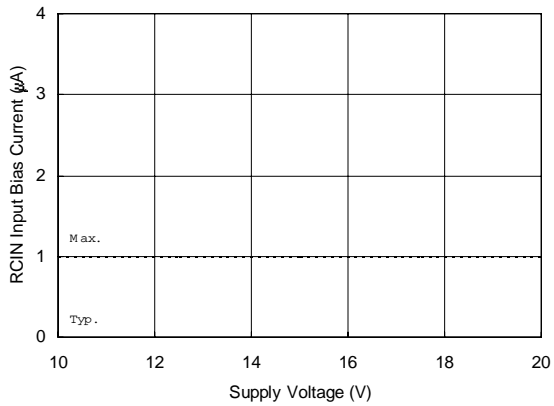


Figure 35B. RCIN Input Bias Current vs. Supply Voltage

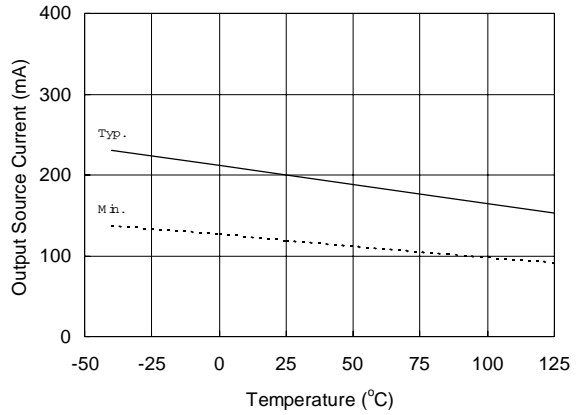
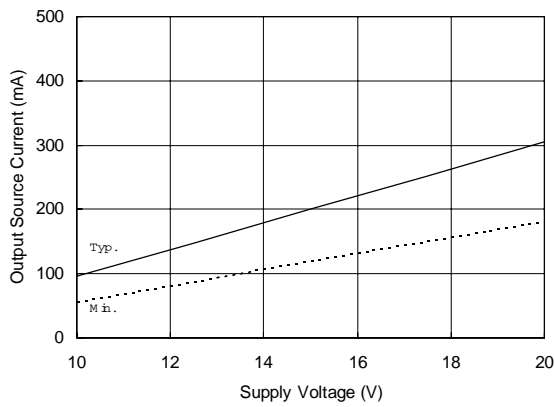
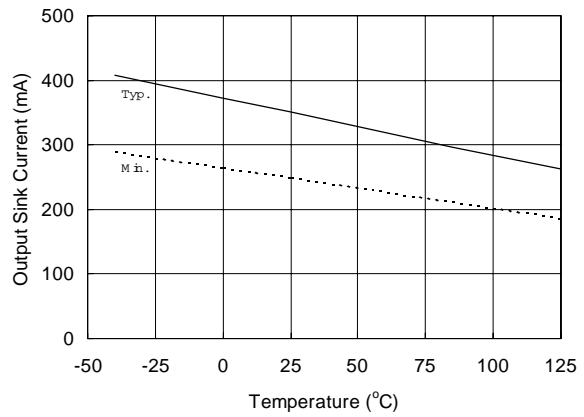


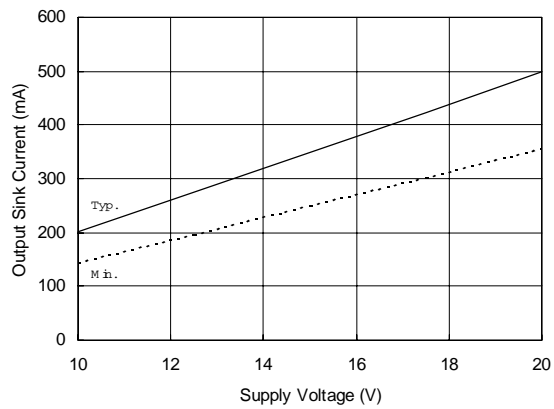
Figure 36A. Output Source Current vs. Temperature



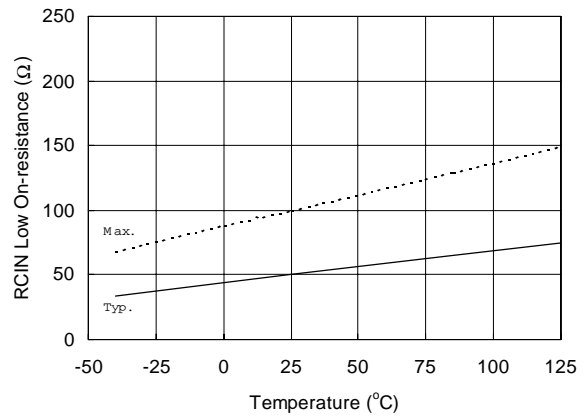
**Figure 36B. Output Source Current vs. Supply Voltage**



**Figure 37A. Output Sink Current vs. Temperature**



**Figure 37B. Output Sink Current vs. Supply Voltage**



**Figure 38A. RCIN Low On-resistance vs. Temperature**

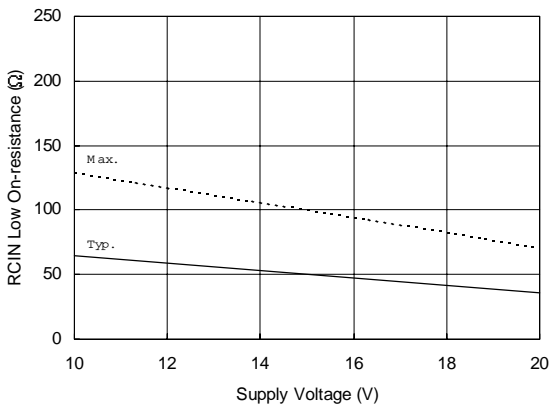


Figure 38B. RCIN Low On-resistance vs. Supply Voltage

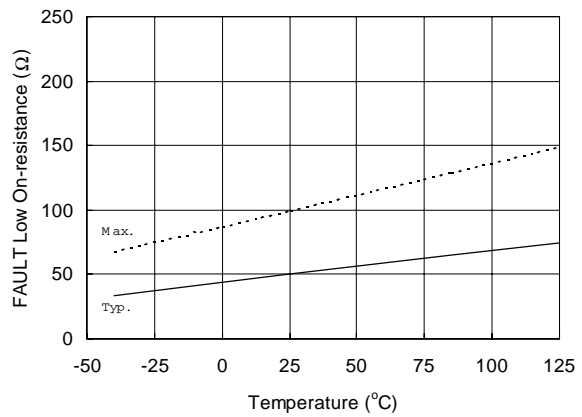


Figure 39A. FAULT Low On-resistance vs. Temperature

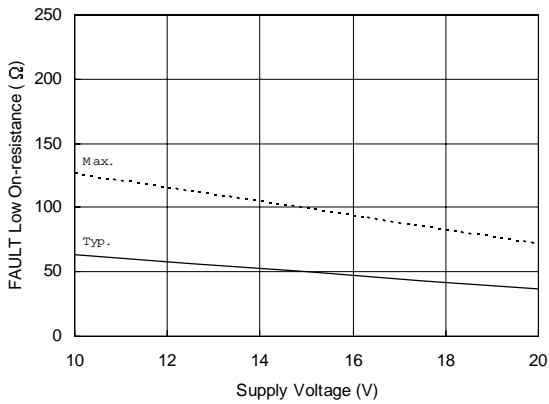


Figure 39B. FAULT Low On-resistance vs. Supply Voltage

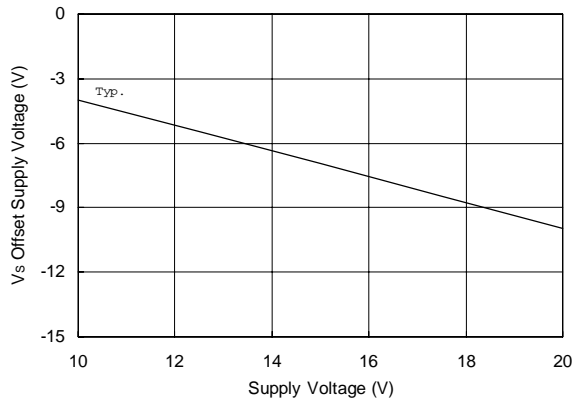
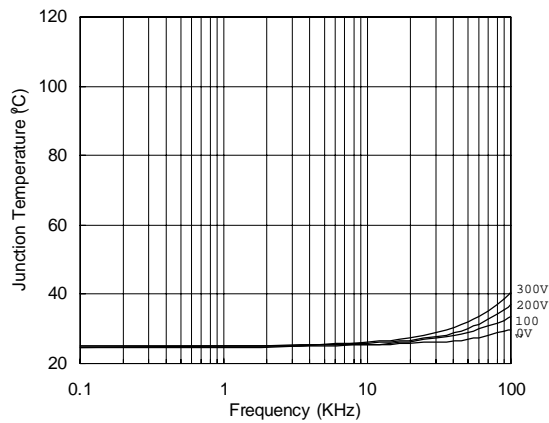
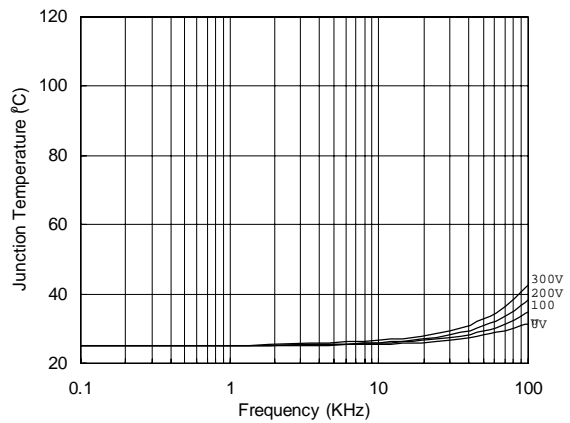


Figure 40. Maximum  $V_S$  Negative Offset vs.  $V_{BS}$  Supply Voltage

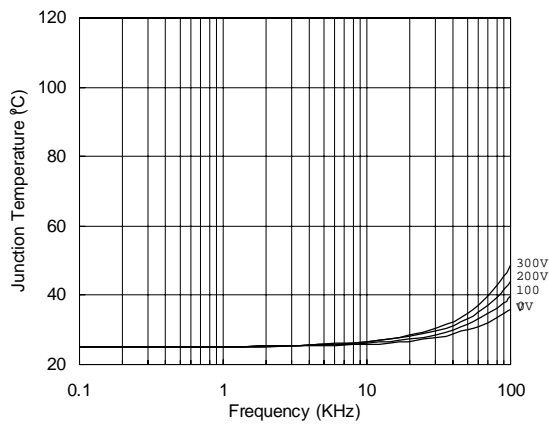
# IR2136/IR21362/IR21363/IR21365(J&S)



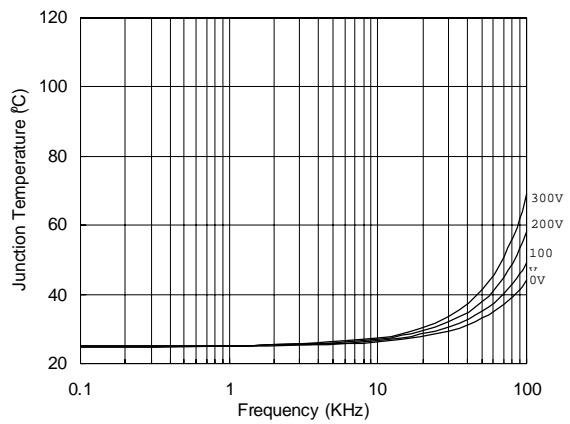
**Figure 41. IR2136/IR21362/IR21363/IR21365 vs. Frequency (IRG4BC20W),  $R_{gate}=33\Omega$ ,  $V_{CC}=15V$**



**Figure 42. IR2136/IR21362/IR21363/IR21365 vs. Frequency (IRG4BC30W),  $R_{gate}=15\Omega$ ,  $V_{CC}=15V$**

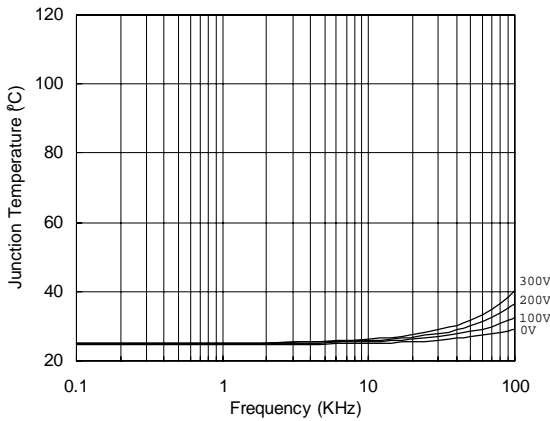


**Figure 43. IR2136/IR21362/IR21363/IR21365 vs. Frequency (IRG4BC40W),  $R_{gate}=10\Omega$ ,  $V_{CC}=15V$**

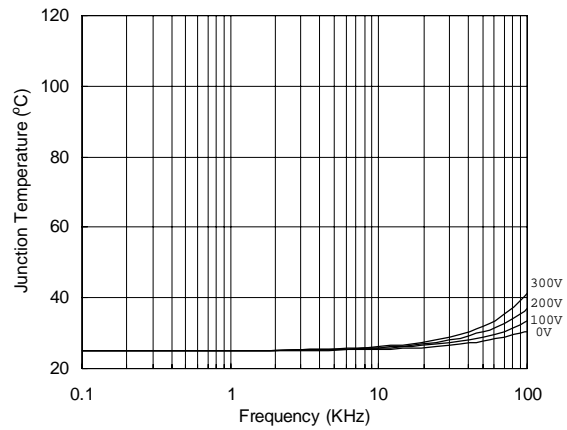


**Figure 44. IR2136/IR21362/IR21363/IR21365 vs. Frequency (IRG4PC50W),  $R_{gate}=5\Omega$ ,  $V_{CC}=15V$**

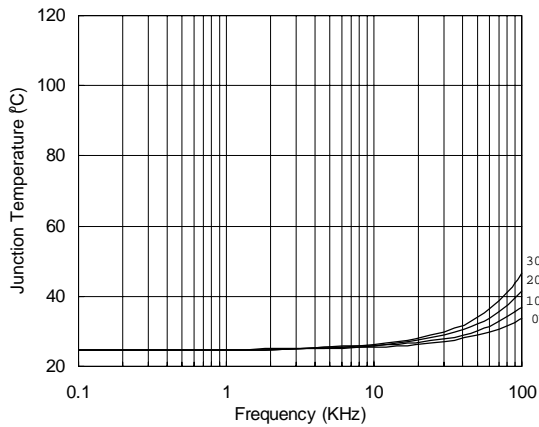
# IR2136/IR21362/IR21363/IR21365(J&S)



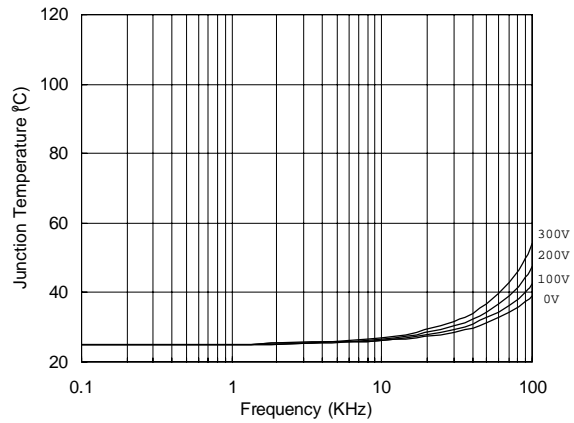
**Figure 45. IR2136J/IR21362J/IR21363J/IR21365J vs. Frequency (IRG4BC20W), R<sub>gate</sub>=33Ω, V<sub>CC</sub>=15V**



**Figure 46. IR2136J/IR21362J/IR21363J/IR21365J vs. Frequency (IRG4BC30W), R<sub>gate</sub>=15Ω, V<sub>CC</sub>=15V**

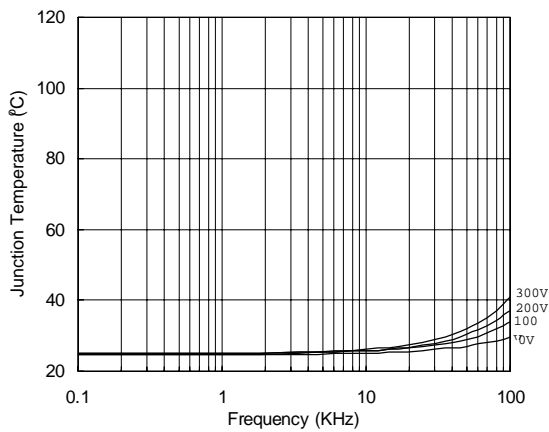


**Figure 47. IR2136J/IR21362J/IR21363J/IR21365J vs. Frequency (IRG4BC40W), R<sub>gate</sub>=10Ω, V<sub>CC</sub>=15V**

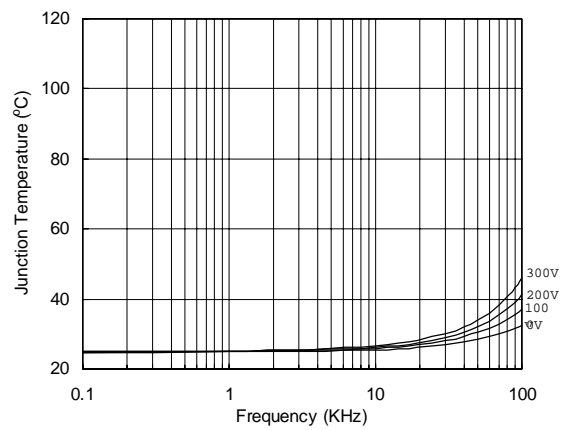


**Figure 48. IR2136J/IR21362J/IR21363J/IR21365J vs. Frequency (IRG4PC50W), R<sub>gate</sub>=5Ω, V<sub>CC</sub>=15V**

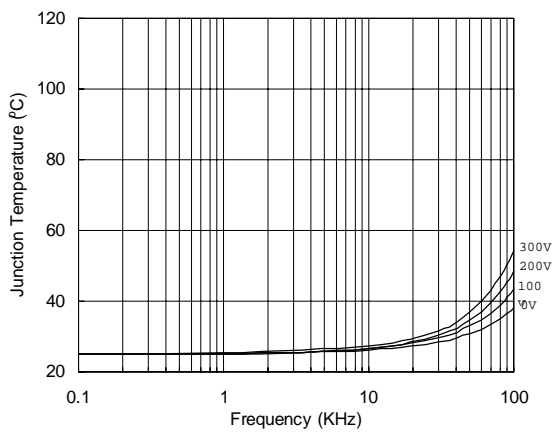
# IR2136/IR21362/IR21363/IR21365(J&S)



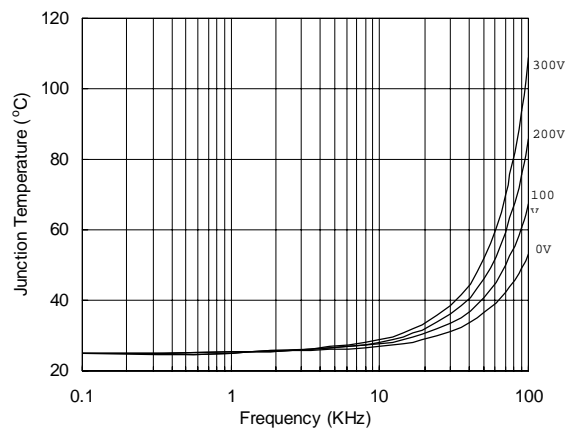
**Figure 49. IR2136S/IR21362S/IR21363S/IR21365S vs. Frequency (IRG4BC20W),  $R_{gate}=33\Omega$ ,  $V_{CC}=15V$**



**Figure 50. IR2136S/IR21362S/IR21363S/IR21365S vs. Frequency (IRG4BC30W),  $R_{gate}=15\Omega$ ,  $V_{CC}=15V$**

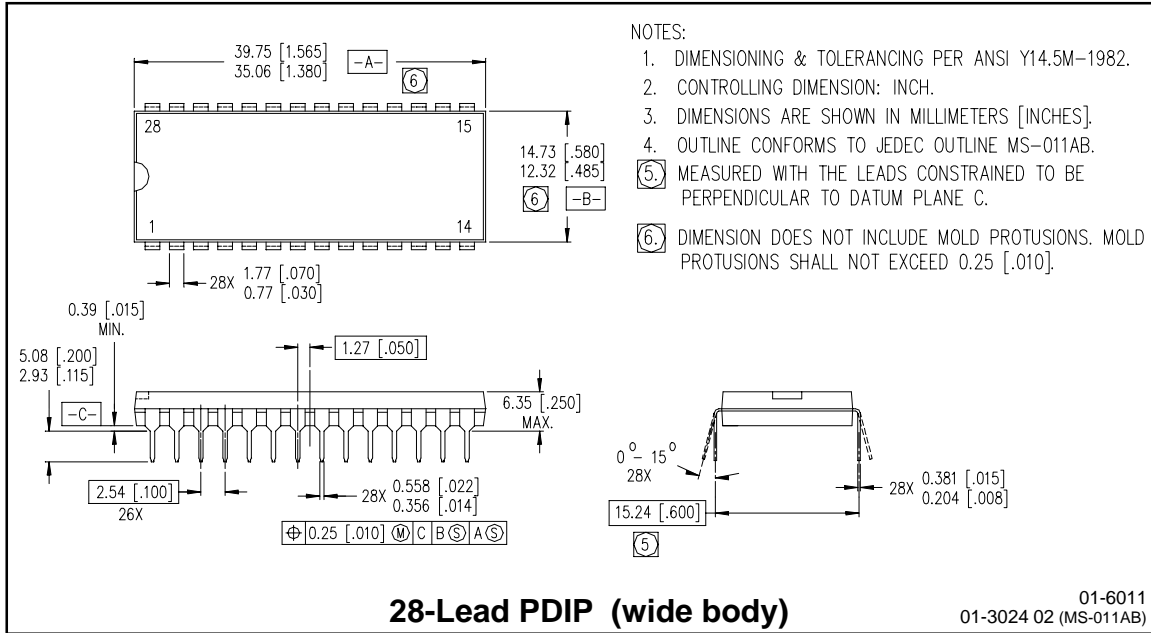


**Figure 51. IR2136S/IR21362S/IR21363S/IR21365S vs. Frequency (IRG4BC40W),  $R_{gate}=10\Omega$ ,  $V_{CC}=15V$**



**Figure 52. IR2136S/IR21362S/IR21363S/IR21365S vs. Frequency (IRG4PC50W),  $R_{gate}=5\Omega$ ,  $V_{CC}=15V$**

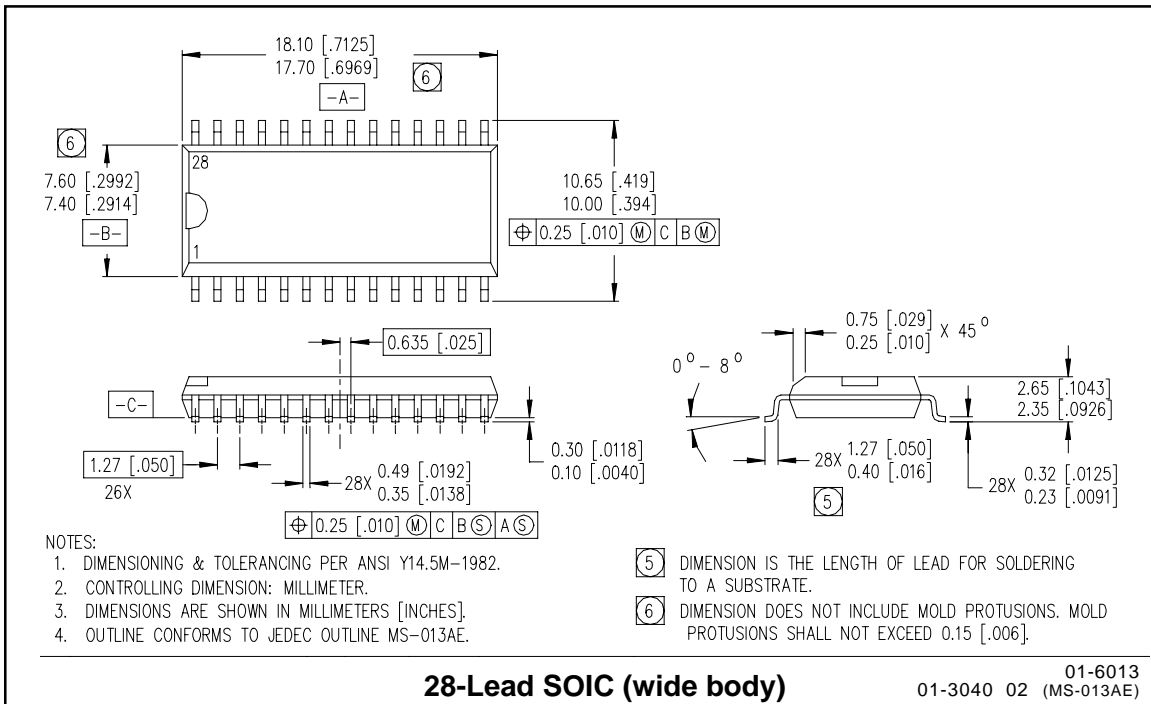
## Case outlines



**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-011AB.

- ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.25 [.010].



**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-013AE.

- ⑤ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



# IR2136/IR21362/IR21363/IR21365(J&S)

