OZ972/OZ976

Change Summary

CHANGES

No.	Applicable Section	Description	Page(s)
1.	Ordering Information	a) Add OZ972GN, OZ972IGN, OZ976TN & OZ976ITN	1
2.	OZ972 Typical Application Circuit	Change C18 value from “0.1u” to “open”	16
3.	Throughout data sheet	Miscellaneous corrections	---

REVISION HISTORY

Revision No.	Description of change	Release Date
0.97	Initial release	10/21/02
0.98	**1.** Revise part number in header and footer to read “OZ972/OZ976” and ensure text diagrams and figures are in this sequence throughout data sheet; **2.** Add alpha to part numbers in “Ordering Information”; **3.** Add patent number in footer of first page; **4.** Update the OZ972 and OZ976 functional block diagrams, application circuit figures and functional specifications; **5.** Revise "Functional Specifications" for OZ972 and OZ976 as follows: **OZ972** - **a)** first test condition listed, **b)** add note (2), **c)** add note (2) to Input Offset Voltage and change Max. limit, **d)** add note (2) to Input Voltage Range, Open Loop Voltage Gain and Unity Gain Bandwidth under Error Amplifier, **e)** delete Power Supply Rejection parameter, **f)** add Source and Sink Current parameters [with note (2)] under Error Amplifier, **g)** add note (2) to NDR-PDR Output Resistance (current source) and change Max. limit, **h)** add note (2) to NDR-PDR Output Resistance (current sink) and change Typ. & Max. limits, **i)** change Max./Min. Overlap title to “Maximum Overlap”, **j)** Maximum Overlap between Diagonal Switches Min. & Typ. limits, **k)** delete Gate Drive (A,B,C,D) Off Condition parameter, **l)** Break-Before-Make PDR_A/NDR_B and PDR_C/NDR_D Min. & Max. limits, **m)** OVP test condition, Min. and Typ. limits; **OZ976** - **n)** Add notes (4) & (5), **o)** add note (4) to Reference Voltage-Nominal and change Min., Typ. & Max. limits, **p)** add note (5) to Reference Voltage-Line Regulation and change Max. limit, **q)** add note (5) to Reference Voltage-Load Regulation and change Max. limit, **r)** add Source and Sink Current parameters under Reference Voltage, **s)** delete CT Oscillator Initial Accuracy parameter, **t)** add note (5) to CT Oscillator Ramp Peak and Valley and change Min. & Max. limits, **u)** CT Oscillator CLK Frequency Min., Typ. & Max limits, **v)** LCT Oscillator Initial Accuracy Min., Typ. & Max limits, **w)** add note (5) to LCT Oscillator Ramp Peak and Valley and change Min. & Max. limits, **x)** Threshold ENA Min. & Max. limits, **y)** change Threshold VIN title to “Threshold VINS” and change Min. & Max. limits, and **z)** add TALK parameter under Threshold; **6.** Correct subtitle under item “15.” to read “VINS”; **7.** Update the formulas for the operation frequency (under item “16.”) and internal LCT frequency (under item “18.”); and **8.** Misc. corrections.	04/23/03
0.99	**1.** Features & Gen’l Description--correct application lamp numbers; **2.** Correct package type in part name in Ordering Information; **3.** Update Functional Block Diagram; **4.** Update OZ976 Typical Application Circuit; **5.** OZ976 Pin Description--delete note ref. for pin #’s 38, 44 & 45; **6.** Complete ‘Package Power Dissipation’ value in Absolute Max. Ratings; **7.** OZ972 Functional Specs **a)** replace ‘Input voltage range‘ parameter & limits with ‘Reference voltage at non-inverting input pin (internal)’ parameter & limits, **b)** correct ‘Max. Overlap between diagonal switches’ test condition, **c)** correct Break-Before-Make ‘PDR_A/NDR_B’ test conditions, Typ & Max limits, and ‘PDR_C/NDR_D test conditions, Min & Max limits, **d)** correct ‘OVP’ Min, Typ & Max limits, **e)** correct ‘Supply Current’ test conditions, Typ & Max limits, **f)** correct ‘Supply current’ test conditions, Typ & Max limits, and **g)** ‘SST current’ Min, Typ & Max limits; **8.** OZ976 Functional Specs **a)** add note (5) to CT Oscillator ‘Temp. stability’, and **b)** correct ‘Supply Current’ test conditions; **9.** Functional Description, 7, 6th line, correct voltage referenced; **10.** Functional Description, 8, 1st line, correct voltage referenced; **11.** Functional Description, correct voltage referenced in last line; **12.** Functional Description, 18, correct Internal LCT frequency formula; **13.** Package Information, delete symbol ‘C’ in table; not included in the drawing; and **14.** Misc. corrections.	05/13/03
1.0	**1**. Add OZ972IG & OZ976IT packages and table that include temp range of each package in Ordering Information and General Description, **2.** Delete “I/O” columns in Pin Description tables, **3.**Absolute Max. Ratings **a)** Modify table title, **b)** move note “(1)” from “VDDA, VDDA2, VDDD, VDD” to the table title, **c)** change “Logic Inputs” to read “Signal Inputs”, **d)** revise Resonator Frequency’, and **e)** add separate Operating Temp. table that breaks out commercial and industrial temp ranges, **4.** OZ972 Electrical Characteristics Revise **a)** table title, **b)** add temp range before the table, **c)** first test condition at beginning of table, **d)** delete ‘Input offset voltage’ parameter, **e)** add test conditions and Min, Typ & Max limits for ‘Reference voltage at non-inverting input pin’ and revise current Min, Typ & Max limits, **f)** delete ‘Open loop voltage gain’ and Unity gain bandwidth’ parameters, **g)** change ‘Source Current’ title to read ‘Output voltage’, add symbol and test condition, and revise Min, Typ, Max limits & units, **h)** delete ‘Sink Current’ parameter, **i)** test conditions for ‘NDR-PDR Output’ parameters, adding Min, Typ, Max limits & units for new test conditions, **j)** ‘Break-Before-Make’ parameters Min, Typ & Max limits, **k)** add test condition plus Min, Typ, Max limits & unit to ‘Threshold OVP’ and update current test conditions, Min, Typ & Max limits, and add ‘Talk’ parameter, **l)** ‘Supply current (ON)’ test conditions, **m)** ‘SST current Min, Typ & Max limits, and **n)** add ‘CTIMR current’ test conditions, adding Min, Typ, Max limits & units for new test conditions, and revising current Min, Typ & Max limits, **5.** OZ976 Electrical Characteristics Revise **a)** table title, **b)** add temp range before the table, **c)** first test condition at beginning of table, **d)** add ‘Nominal voltage’ test conditions, adding Min, Typ, Max limits & units for new test conditions, and revising current Min, Typ & Max limits, **e)** ‘Line regulation’ note numbers and Max limit, **f)** delete ‘Load regulation’, ‘Source Current’ and ‘Sink Current’, **g)** add test condition plus Min, Typ, Max limits & unit to ‘CLK Frequency’ and update current test conditions, Min, Typ & Max limits, **h)** add test condition plus Min, Typ, Max limits & unit to ‘Initial Accuracy’ and update current test conditions, Min, Typ & Max limits, **i)** delete ‘Ramp peak/valley’ parameters, **j)** add note (3) to ‘Low Frequency PWM’, **k)** add symbol and test conditions (9) plus Min, Typ, Max limits & units to ‘Duty Cycle Range’ and update current Max limit, **l)** ’Threshold’ parameter names, deleting ‘ENA’ and VINS’, and all limits, **m)** add note (5) to ‘Talk’ parameter, **n)** ‘Supply current (low)’ Max lilmit, **o)** ‘Supply current (high)’ test condition and Max limit, and **p)** note (3), **6.** OZ972 & OZ976 Functional Block Diagrams **a)** Revise ENA non-inverting node voltage, SST current, and OVP threshold voltage, and **b)** delete phase shift in OZ976 diagram, **7**. Functional Description **a)** Item 7., revise voltage in line 6, **b)** Item 8., revise OVP threshold voltage in line 1, **c)** Item 11., revise non-inverting voltage in last line, and **d)** Item 18., update formula, **8.** Change C116 value to 33p in OZ976 Typical Application Circuit, **9.** Add part numbers to titles of Package Information & **10.** Misc.	

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OZ972/OZ976

Intelligent CCFL Inverter Controller

FEATURES

- Low cost synchronized inverter solution
- Fixed synchronized operating frequency for up to 48 CCFLs
- Programmable operating and PWM frequencies
- Zero-voltage-switching full bridge topology
- 90% efficiency vs. typical 70% efficiency of conventional designs
- Supports up to 12 equal-delay PWM signals
- PWM signals synchronized with either external or internal signal
- Intelligent time-sharing dimming control
- Constant-frequency design eliminates interference between CCFLs and LCD panel.
- Built-in intelligence for ignition and normal operation of CCFLs
- Internal open lamp and over voltage protection
- Fewer components and smaller board size
- Low stand-by power

ORDERING INFORMATION

Part Number	Temp Range	Package
OZ972G	**0°C to 70°C**	16-pin SOP
OZ972IG	**-40°C to 85°C**	16-pin SOP
OZ972GN	**0°C to 70°C**	16-pin SOP, Leadfree
OZ972IGN	**-40°C to 85°C**	16-pin SOP, Leadfree
OZ976T	**0°C to 70°C**	48-pin LQFP
OZ976IT	**-40°C to 85°C**	48-pin LQFP
OZ976TN	**0°C to 70°C**	48-pin LQFP, Leadfree
OZ976ITN	**-40°C to 85°C**	48-pin LQFP, Leadfree

GENERAL DESCRIPTION

The Phase Array (OZ972/OZ976) is a unique, high-efficiency, CCFL backlight controller chipset that is targeted for LCD applications requiring 6 to 48 lamps. The Phase Array chipset consists of two devices, the OZ976 Array Hub and OZ972 Power Controller. Depending on the number of lamps, each application requires one OZ976 device and either 6, 8, 10 or 12 OZ972 Power Drivers. The number of OZ972 devices used in an application is user-selectable. Figure 1, page 8, illustrates the Phase Array topology.

The OZ972, Power Controller, drives a zero-voltage-switching full-bridge circuit, providing output voltage and current waveforms to the CCFLs. Operating in a zero-voltage switching configuration; the inverter circuit minimizes EMI emission. In addition, the inverter circuit achieves very high power conversion efficiency resulting in lower heat and higher system reliability.

A smart protection circuit is incorporated in the Power Controller to achieve a high safety requirement. This circuit provides lamp ignition, normal operation, open lamp and broken lamp protection, and communicates the status to the OZ976. Intelligent open-lamp and over-voltage protection provides design flexibility with various transformer characteristics.

The OZ976, Array Hub, generates and distributes the operating frequency to all OZ972 Power Controllers, to ensure that all lamps operate at one frequency. This eliminates interference among lamps that result from different lamp operation frequencies. Interference causes EMI problems and may create visual effects (waterfall) on the LCD panel. The operating frequency of the OZ976 is programmable via an external resistor and capacitor.

The OZ976 utilizes the pulse-width-modulation (PWM) dimming method to achieve a wide dimming range. The PWM dimming frequency can be synchronized with an external TTL-level signal or an internal signal, programmed via an internal (LCT) oscillator circuit. If an external TTL level signal does not exist, the OZ976 will automatically follow the pre-programmed LCT frequency to generate the PWM signals. Otherwise, the external TTL level frequency will be used to generate the PWM signals.

The OZ976 provides a set of PWM signals with a different phase delay to each OZ972. This method reduces power supply ripple. Without the PWM phase shift, a system utilizing a large number of lamps, for example 12, would cause a large power supply current surge (spike) if the lamps turned on and off simultaneously. This abrupt power demand increases the power supply design burden and degrades EMI performance. By splitting a large power demand into smaller segments, the OZ976 minimizes the peak power bus ripple and in-rush current. The OZ976 monitors the power supply voltage to prevent an under-voltage lockout condition. OZ976 will disable all the inverters if it detects an under-voltage condition.

The OZ972 is available in a 16-pin SOP package and the OZ976 in a 48-pin LQFP package. Both devices are specified over the commercial temperature range from 0^oC to 70^oC, and the industrial temperature from -40^oC to 85^oC.

OZ972 PIN DESCRIPTION

Name	Pin No.	Description
VDD	1	IC Power
REF	2	Reference Voltage Input
CT	3	Saw tooth wave with double inverter operating frequency
CLK	4	Square wave with inverter operating frequency
TALK	5	Strike/Normal/Shut Down indicator
ENA	6	Enable input; TTL signal – Active High
CTIMR	7	CCFL ignition period timer
SST	8	Soft-start timer
OVP	9	Output voltage sense, Vth=2.0V
FB	10	CCFL current feedback signal
CMP	11	Compensation output of the error amplifier
GND	12	Ground
PDR_C	13	PMOSFET drive output
NDR_D	14	NMOSFET drive output
PDR_A	15	PMOSFET drive output
NDR_B	16	NMOSFET drive output

OZ976 PIN DESCRIPTION

Name	Pin No.	Description
ENA_PP	3	Enable OZ972
VDDA2	4	Analog Power
VDDA	5	Analog Power
VDDD	6	Digital Power
OSCA	7	Connected to 4MHz Resonator
OSCY	8	Connected to 4MHz Resonator
VSYNC	9	External synchronization input, TTL signal
TALK	10	OZ972 feedback Ignition/Normal/Abnormal
L11	14	Low frequency PWM signal with x11 phase delay
L10	15	Low frequency PWM signal with x10 phase delay
L9	16	Low frequency PWM signal with x9 phase delay
L8	17	Low frequency PWM signal with x8 phase delay
L7	18	Low frequency PWM signal with x7 phase delay
L6	19	Low frequency PWM signal with x6 phase delay
L5	20	Low frequency PWM signal with x5 phase delay
L4	21	Low frequency PWM signal with x4 phase delay
L3	22	Low frequency PWM signal with x3 phase delay
L2	23	Low frequency PWM signal with x2 phase delay
L1	27	Low frequency PWM signal with x1 phase delay
L0	28	Low frequency PWM signal with no phase delay
GNDD	29	Digital Ground
GNDA	30	Analog Ground
GNDA2	31	Analog Ground
REF	32	Reference voltage output; 2.5V typical @ 100uA
CLK	33	Inverter operating clock
CT	34	Timing capacitor set inverter operating frequency
POL	38	POL(Polarity), Select dimming voltage polarity
IND	39	IND(Individual), Select OZ972 system protection mode
ENA	40	Enable input; TTL signal
RT	41	Timing resistor set operating frequency
RT1	42	Timing resistor for programming ignition frequency and PWM frequency
LCT	43	Timing capacitor set internal PWM frequency
SEL1	44	Lamp number selector, work with SEL0
SEL0	45	Lamp number selector, work with SEL1
VDIM	46	A DC voltage for dimming control
VINS	47	Input voltage sense, Vth=1.5V
NC	1, 2, 11, 12, 13, 24, 25, 26, 35, 36, 37, 48	No Connection

ABSOLUTE MAXIMUM RATINGS[1]

VDDA, VDDA2, VDDD, VDD	7.0V
GNDA, GNDA2, GNDD, GND	+/-0.3V
Signal Inputs	-0.3V to VDDA +0.3V
Resonator Frequency	8MHz

	OZ972	OZ976
Package Power Dissipation	86 °C/W	63 °C/W

Maximum Junction Temp.	125°C
Storage Temp.	-55°C to 150°C

RECOMMENDED OPERATING RANGE

VDDA, VDDA2, VDDD, VDD	4.7V ~ 5.3V
Inverter Operating Frequency (2)	30KHz to 150KHz
R_T for Inverter Operating	40kΩ to 150kΩ
Resonator Frequency Selection (3)	3MHz to 4MHz

Operating Temp.	OZ972/OZ976	OZ972I/OZ976I
	0°C to 70°C	-40°C to 85°C

Notes:

(1) The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The "Functional Specifications" table defines the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

(2) The frequency of PDR_A, NDR_B, PDR_C, and NDR_D output pulses, f_{ABCD}, are half of CT frequency value.

(3) See Table 2, page 16 for more detail.

OZ972 ELECTRICAL CHARACTERISTICS

OZ972: 0°C < Tamb < 70°C, unless otherwise specified
OZ972I: -40°C < Tamb < 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions VDD = 5.0V; REF = 2.5V; unless otherwise specified	Limits			Unit
			Min	Typ	Max	
Error Amplifier						
Reference voltage at non-inverting input pin (internal)		Tamb=25°C	1.26	1.28	1.31	V
		Temp coefficient	-	50	-	ppm/°C
Output voltage (2)	V_{11}	V_{10}=0V; R_{load}=15k	3.0	-	-	V
NDR-PDR Output						
Output resistance (2)	R_p	Tamb=25°C; R_{load}=30Ω	-	27	33	Ω
		Temp coefficient	-	3000	-	ppm/°C
Output resistance (2)	R_n	Tamb=25°C; R_{load}=30Ω	-	27	33	Ω
		Temp coefficient	-	3000	-	ppm/°C
Maximum Overlap						
Max. Overlap between diagonal switches		CLK = 63kHz Ca=Cb=Cc=Cd=1nF(1)	78	-	-	%
Break-Before-Make						
PDR_A/NDR_B		CLK = 63kHz Ca=Cb=Cc=Cd=1nF(1)	70	115	160	ns
PDR_C/NDR_D		CLK = 63kHz Ca=Cb=Cc=Cd=1nF(1)	55	105	150	ns
Threshold						
OVP		Tamb=25°C	2.16	2.22	2.28	V
		Temp coefficient	-	500	-	ppm/°C
Talk(2)		Logic High	2.0	-	-	V
		Logic Low	-	-	1.0	V
Supply						
Supply current	I_{OFF}	ENA = low	-	150	200	µA
Supply current	I_{ON}	ENA = High; CLK = 63kHz	-	4.0	5.0	mA
SST current	I_{SST}		2.5	5.0	7.6	µA
CTIMR current	I_{CTIMR}	Tamb=25°C	1.9	2.6	3.3	µA
		Temp coefficient	-	4500	-	ppm/°C

Notes:
(1) Ca: capacitor from PDR_A (Pin 15) to VDDA
Cb: capacitor from NDR_B (Pin 16) to ground
Cc: capacitor from PDR_C (Pin 13) to VDDA
Cd: capacitor from NDR_D (Pin 14) to ground
(2) Denotes that parameter is guaranteed by design and not production tested.

OZ976 ELECTRICAL CHARACTERISTICS

OZ976: 0°C < Tamb < 70°C, unless otherwise specified
OZ976I: -40°C < Tamb < 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions		Limits		Unit
		VDDA/VDDA2/VDDD = 5V; unless otherwise specified	Min	Typ	Max	
Reference Voltage						
Nominal voltage [(4)]	REF	Tamb = 25°C; I_{load} = 0.25mA	2.39	2.55	2.71	V
		Temp coefficient	-	200	-	ppm/°C
Line regulation [(2, 4)]		VDDA = 4.7V – 5.3V	-	4	-	mV/V
CT Oscillator						
CLK Frequency		Tamb = 25°C; CT = 220pF, RT = 48.7kΩ [(1)]	58	63	68	KHz
		Temp coefficient	-	200	-	ppm/°C
LCT Oscillator						
Initial accuracy		Tamb = 25°C; LCT = 10nF, RT = 48.7kΩ[(2)]	190	210	230	Hz
		Temp coefficient	-	-500	-	ppm/°C
Low Frequency PWM (L0-L11) [(3)]						
Duty Cycle Range	L0-L11	VDIM = 1V; POL = 0V; VSYNC frequency = 70Hz; LCT = 10nF, RT = 48.7kΩ[(2)]	0	-	0	%
		VDIM = 1.5V; POL = 0V; VSYNC frequency = 70Hz; LCT = 10nF, RT = 48.7kΩ[(2)]	-	18	-	%
		VDIM = 3.2V; POL = 0V; VSYNC frequency = 70Hz; LCT = 10nF, RT = 48.7kΩ[(2)]	-	70	-	%
		VDIM = 1V;POL = 0V; VSYNC = GNDA; LCT = 10nF, RT = 48.7kΩ[(2)]	0	-	0	%
		VDIM = 1.5V;POL = 0V; VSYNC = GNDA; LCT = 10nF, RT = 48.7kΩ[(2)]	-	50	-	%
		VDIM = 2.2V;POL = 0V; VSYNC = GNDA; LCT = 10nF, RT = 48.7kΩ[(2)]	100	-	100	%
		VDIM ≥ 3.2V; POL = 5V; VSYNC = GNDA; LCT = 10nF, RT = 48.7kΩ[(2)]	0	-	0	%
		VDIM = 2.5V; POL = 5V; VSYNC = GNDA; LCT = 10nF, RT = 48.7kΩ[(2)]	-	50	-	%
		VDIM ≤ 1.8V; POL = 5V; VSYNC = GNDA; LCT = 10nF, RT = 48.7kΩ[(2)]	100	-	100	%

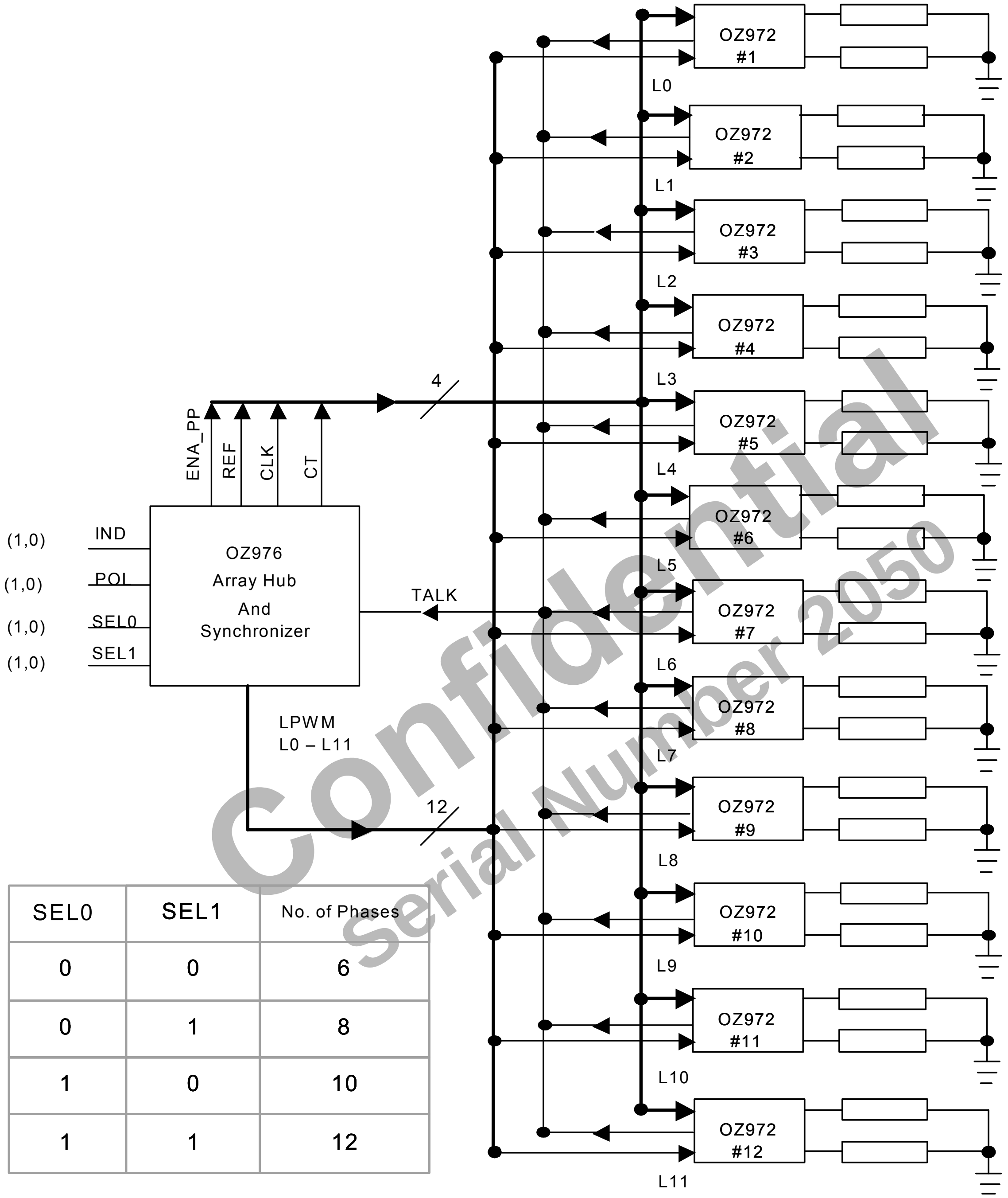
OZ976 ELECTRICAL CHARACTERISTICS (CONTINUED)

OZ976: 0°C < Tamb < 70°C, unless otherwise specified
OZ976I: -40°C < Tamb < 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions		Limits		Unit
		VDDA/VDDA2/VDDD = 5V; unless otherwise specified	Min	Typ	Max	
Threshold						
ENABLE	ENA		2.0	-	-	V
DISABLE			-	-	1.0	V
VINS (ON)			1.65	-	-	V
VINS (OFF)			-	-	1.25	V
TALK(5)		Logic High	3.5	-	-	V
		Logic Low	-	-	1.6	
Supply						
Supply current		ENA = low	-	165	280	µA
Supply current		ENA = high 12-phase selection VDIM = 2V; L0-L11 = 50kΩ (3) CLK = 63kHz; LCT = 210Hz	-	4.4	5.5	mA

Notes:
(1) CT: capacitor from CT (pin 34) to ground
RT: resistor from RT (pin 41) to ground
(2) LCT: capacitor from LCT (Pin 43) to ground
RT: resistor from RT (pin 41) to ground
(3) L0-L11: 50kΩ resistor is connected from L0-L11 (Pins 14-23 and 27-28) to ground
A 4MHz resonator is connected to OSCA and OSCY
(4) Reference voltage measured when CT, CLK, LCT & resonator are not active.
(5) Denotes that parameter is guaranteed by design and not production tested.

PHASE ARRAY TOPOLOGY


(1,0) IND
(1,0) POL
(1,0) SEL0
(1,0) SEL1
OZ976
Array Hub
And
Synchronizer
ENA_PP
REF
CLK
CT
4
TALK
LPWM
L0 – L11
12
OZ972 #1
OZ972 #2
OZ972 #3
OZ972 #4
OZ972 #5
OZ972 #6
OZ972 #7
OZ972 #8
OZ972 #9
OZ972 #10
OZ972 #11
OZ972 #12
L0
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11

SEL0	SEL1	No. of Phases
0	0	6
0	1	8
1	0	10
1	1	12

Figure 1

FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

OZ972 POWER CONTROLLER

The functional block diagram of the OZ972, Power Controller, is shown in Figure 2, page 10. The reference block receives a reference voltage from the REF pin and generates precise voltages for internal use. The drive circuit consists of four outputs, PDR_A, NDR_B, PDR_C and NDR_D. The drive circuit is designed to achieve a zero-voltage switching full-bridge application.

An error amplifier is provided to regulate the CCFL current. The Soft-Start Time (SST) circuit offers a gradual power increase to the CCFL during the ignition period. The Soft-Start Time (SST) is programmable by using an external capacitor coupled with the SST current source.

The over-voltage protection block limits the striking voltage for the CCFLs. The striking time is programmable by using an external capacitor with the CTIMR current source.

The Protection block intelligently differentiates between lamp ignition, normal operation, open-lamp condition and broken lamp condition. The OZ972 communicates its' status to the OZ976 via the open drain TALK pin. The OZ972 is enabled when the ENA circuitry receives an enable signal from the OZ976 (ENA_PP). The ADJ (Adjust) Control block provides an increased reference voltage during SST and a preset reference voltage once the lamp current is regulated.

OZ976 ARRAY HUB

The functional block diagram of the OZ976, Array Hub, is shown in Figure 3, page 11. A Precision Reference block provides reference voltages for both internal and external use.

The CT Oscillator circuit generates a user-programmable operating frequency to the OZ972's by utilizing an external capacitor and timing resistor. To select the striking frequency, add an external resistor to RT1. The striking frequency is programmable.

The LCT Oscillator block utilizes a quarter of the current through the timing resistor (RT) to charge and discharge the external capacitor. This creates the LCT triangular waveform.

The Protection block monitors supply voltage, system enable and OZ972 status. Through VINS,

the OZ976 monitors the supply voltage and provides under-voltage lock out protection. When VINS and ENA pins are satisfied, the OZ972's are enabled through the ENA_PP pin. When the supply voltage drops below specification, the OZ976 disables the inverters. The OZ976 operation is enabled through a TTL signal interface via the ENA circuitry.

The IND (Individual) pin is used to select the system protection mode. When IND is set high, all OZ972's act independent of each other. When IND is set low, all OZ972's act as a group. The TALK pin is used to monitor and communicate the status of the OZ972 power controllers to the OZ976.

A PWM signal is generated when VDIM exceeds a threshold voltage. A LCT oscillator generates a triangle waveform (1V to 3V) and accepts a VDIM DC voltage to generate the pulse width of the PWM dimming signals.

The Synchronize circuit selects the PWM frequency source from either the internal LCT or an external TTL signal to the VSYNC pin. If an external signal to VSYNC exists, that signal becomes the PWM frequency source. Otherwise, LCT is the PWM frequency source.

An x2 Frequency circuit doubles the PWM source frequency to eliminate low frequency flicker detected by the human eye. The Phase Delay circuit divides the PWM source period into multiple phases according to the number of lamps used in the application. The user selects the number of phases by selecting the logic levels of pins SEL0 and SEL1.

The Pulse Width Extractor extracts the PWM width from the output of LCT comparator. By selecting the POL (Polarity) logic level, the designer programs the relationship between VDIM and the panel brightness. Setting POL high, an increase in VDIM, will increase panel brightness. Conversely, setting POL low, a decrease in VDIM, will increase panel brightness. The PWM Generator circuit combines the Phase Delay, x2 Frequency and Pulse Width information to generate a set of new PWM waveforms with different phase delays.

An external resonator, connected to pins OSCY and OSCA, is needed to generate precise frequency and pulse width information to generate the PWM signals L0 to L11.

OZ972 POWER CONTROLLER FUNCTIONAL BLOCK DIAGRAM

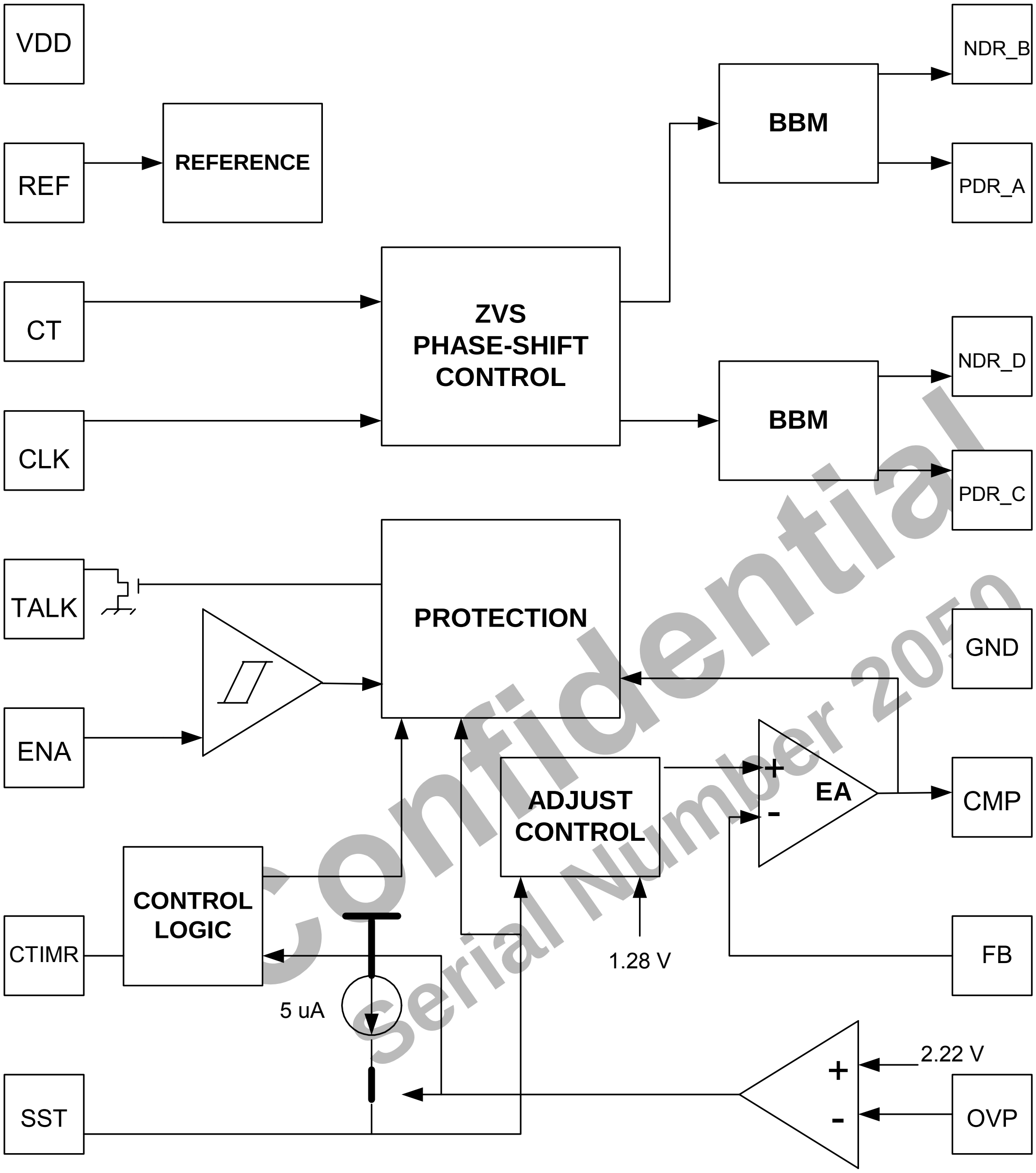

VDD
REF
REFERENCE
CT
CLK
ZVS
PHASE-SHIFT
CONTROL
BBM
BBM
NDR_B
PDR_A
NDR_D
PDR_C
TALK
PROTECTION
ENA
GND
EA
+
-
CMP
ADJUST
CONTROL
CONTROL
LOGIC
CTIMR
1.28 V
FB
5 uA
2.22 V
+
-
SST
OVP

Figure 2

OZ976 ARRAY HUB FUNCTIONAL BLOCK DIAGRAM

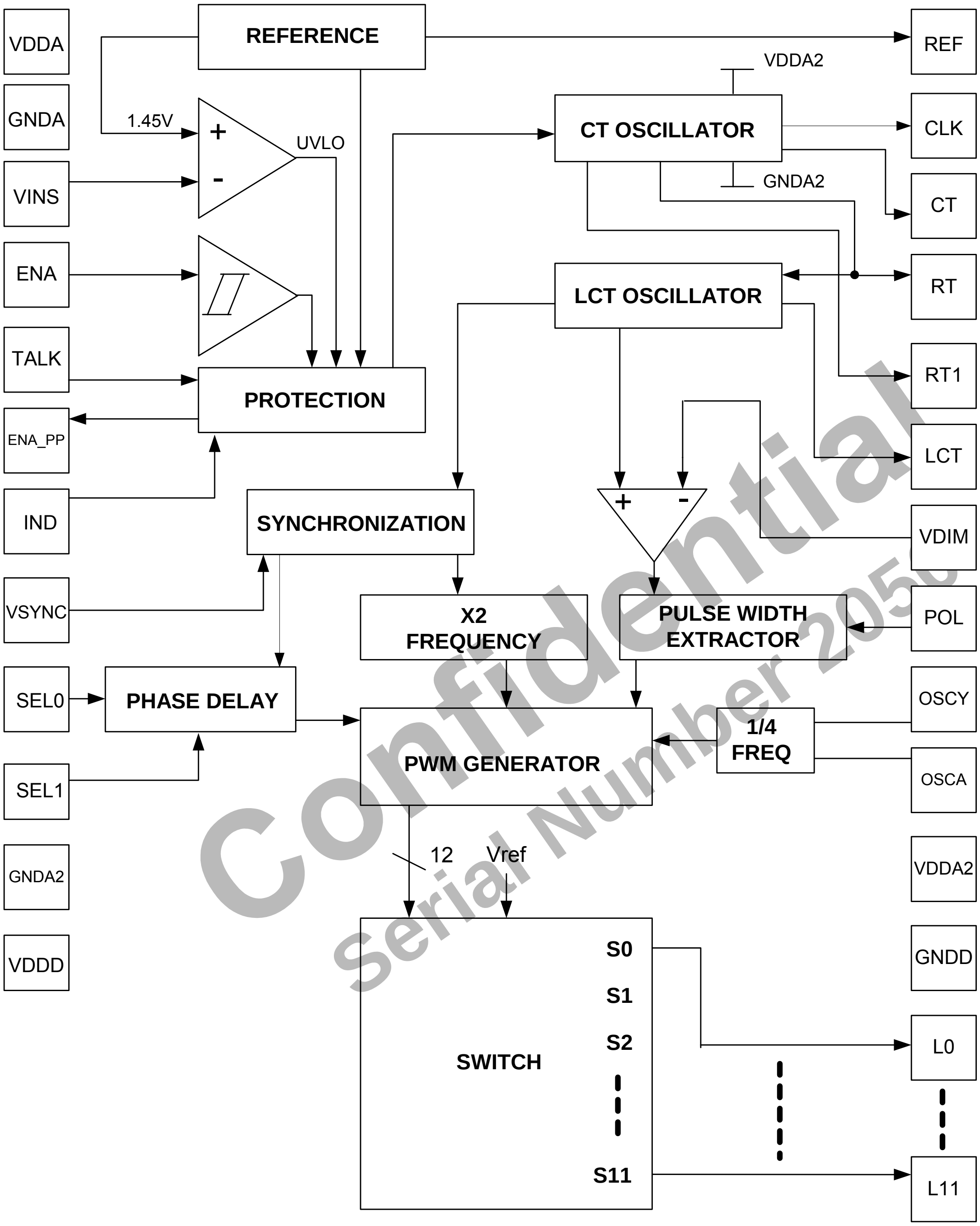

VDDA
GNDA
VINS
ENA
TALK
ENA_PP
IND
VSYNC
SEL0
SEL1
GNDA2
VDDD
REFERENCE
1.45V
+
-
UVLO
PROTECTION
SYNCHRONIZATION
PHASE DELAY
X2
FREQUENCY
PWM GENERATOR
12
Vref
SWITCH
S0
S1
S2
S11
CT OSCILLATOR
VDDA2
GNDA2
LCT OSCILLATOR
+
-
PULSE WIDTH
EXTRACTOR
1/4
FREQ
REF
CLK
CT
RT
RT1
LCT
VDIM
POL
OSCY
OSCA
VDDA2
GNDD
L0
L11

Figure 3

FUNCTIONAL DESCRIPTION

1. Concept

The Phase Array is designed for a multiple-lamp CCFL panel. The OZ976 provides the reference voltage, enable signal, programmable synchronized operating frequency and PWM signals to each OZ972. In addition, when in common mode, the OZ976 monitors the status of the OZ972 via TALK. Each OZ972 operates its own lamps to reach the ultimate performance. This structure minimizes process tolerance and over-head cost while each lamp operates on its designed condition to provide the best performance.

2. OZ972 Steady-State Operation

Referring to the schematic shown in Figure 4, page 17, the OZ972 drives a full-bridge power train where the transformer couples the energy from the power supply source to the CCFL. The switches in the bridge denoted as QA, QB, QC and QD are configured such that QA/QB and QC/QD are turned-on complementarily. The turn-on duration of QA/QD and QB/QC simultaneously determines the amount of energy delivered to the transformer and subsequently to the CCFL. The current in the CCFL is sensed and then regulated by adjusting the turn-on time (overlap) for both diagonal switches. This is accomplished through an error amplifier in the current feedback loop.

A voltage loop is used to regulate the output voltage to achieve the striking voltage, which is programmable by using a capacitor divider. Over voltage protection (OVP) limits transformer voltage under an open lamp condition. A soft-start circuit ensures a gradual power increase to the lamp. The soft-start capacitor determines the rise rate of the voltage on the SST pin. The voltage level determines the on-time duration (overlap) of diagonal switches QA/QD and QB/QC.

The output drives for power MOSFET gates include, PDR_A, NDR_B, PDR_C and NDR_D, which output a complementary square pulse. The operation of the four switches is implemented with zero-voltage-switching to provide a high-efficiency power conversion.

3. OZ972/OZ976 Interface Signals

Referring to the schematics in Figures 4 and 5, pages 17 and 18, the OZ976 provides a reference voltage, enable signal, CLK and CT signals, to each OZ972. The OZ976 provides a precise reference voltage to the REF pin of each OZ972. All OZ972's are enabled by the OZ976 via the ENA_PP pin. The CLK and CT signals are used to direct each OZ972 to drive QA, QB, QC and QD. All OZ972's are synchronized to one frequency. By sharing the reference voltage, CT and CLK, the difference in each lamp's performance is minimized. The OZ976 Controller senses the system power supply voltage. In addition, when in common mode, the OZ976 monitors OZ972 operation status via the TALK pin to determine whether to maintain normal operation or disable the inverters.

Once the system is powered-on, the OZ972 enters the Start-Up stage. Refer to Section 4 for more detailed information.

4. OZ972 Operation - Individual

The OZ972 operates in a constant-frequency mode. This eliminates any undesired interference between the inverter and LCD panel where interference is usually associated with variable-frequency designs.

Start- Up
Based on a 4MHz resonator, the OZ976 sends out a reference voltage and approximately 1ms later enables all the OZ972's. CLK and CT signals are sent out at this moment. After receiving a reference voltage and enable, CLK and CT signals, the OZ972 initiates operation. The result is a series of complementary output square pulses from PDR_A, NDR_B, PDR_C and NDR_D. The OZ972 holds the TALK pin low through an open-drain structure to inform the OZ976 to start the ignition period.

Soft Start Time to Normal Operation
An external resistor RT1 provides the flexibility to set a higher operating frequency for CCFL striking. In addition, the striking time is programmable through an external capacitor CTIMR. The Soft Start function gradually increases the energy delivered to the load from the diagonal switches during start-up. During Soft Start, the TALK pin is pulled low requesting the OZ976 to send a higher operating frequency to ignite the lamp. This process continues until the CCFL current is detected and reaches a regulated value. The output of the error amplifier, CMP, follows the feedback signal and controls the overlap of output drives QA/QD and QB/QC to maintain lamp current regulation. The operation of the four switches is implemented with zero-voltage switching to provide a high-efficiency power conversion. Once the lamp current is sensed and regulated, the OZ972 releases TALK. When the TALK signal is released, the external resistor pulls TALK high and communicates to the OZ976 to switch the lamp to a normal operating frequency. The last OZ972 and the external pull-up resistor decide the TALK level.

Soft Start Time to Open Lamp

The striking voltage, or open-lamp voltage, is regulated through a voltage feedback loop. This voltage feedback loop is monitored by the OVP and controls the overlap of the output drivers to achieve a regulated striking voltage. Once the striking time has expired (CTIMR) and no lamp current is sensed, the OZ972 shuts down and releases TALK. The external resistor pulls TALK high informing the OZ976 to switch to a normal operating frequency. Approximately 20us later, the open lamp OZ972 pulls TALK low indicating to the OZ976 that an abnormal condition exists.

Normal Operation to Lamp Broken

A protection feature is needed to disable a damaged lamp during normal operation. Once the OZ972 senses the missing current signal through the error amplifier, the protection circuit shuts down the output drives. The OZ972 with the broken lamp then pulls TALK low informing the OZ976 of an abnormal situation.

Dimming

Dimming control of the inverter is implemented by adjusting the amount of energy processed and delivered to the CCFL. A PWM dimming control scheme is internally generated which provides a recommended PWM duty cycle of 0% to 85%. The OZ976 provides the phase delay PWM signals. The PWM frequency source can be provided externally from the system or internally by programming the LCT circuit.

5. OZ972 Operation - Group

Soft-Start Time to Normal Operation

The OZ972s drive the power train to the CCFLs after receiving an enable signal. In the soft-start period, TALK is pulled low and a striking frequency is provided by the OZ976. Each OZ972 takes a different time to regulate the CCFL current due to lamp and component tolerances. When the lamp current is regulated on all OZ972's, the TALK signal is released. An external resistor pulls TALK high informing the OZ976 to provide a normal operating frequency to all lamps. Refer to Figure 6, page 19.

Soft-Start Time and Open Lamp

During the Soft Start Time, an OZ972 in open lamp condition attempts to ignite the CCFL. Once the striking time has expired and no lamp current is sensed, the OZ972 shuts down. By this time, the remaining OZ972's successfully regulate their lamp current and TALK is released. The external resistor pulls TALK high. The TALK rising edge informs the OZ976 to switch all lamps to a normal operating frequency. Approximately 20us later, the OZ972 with the open lamp pulls TALK low.

The OZ976 will check the setting of the IND pin to decide whether to disable all the inverters. Refer to Figures 7 and 8 on pages 20 and 21, respectively.

Lamp Broken

When an OZ972 senses no CCFL current in normal operation, its protection block shuts down the circuit. The shut down behavior does not affect the operation of the other OZ972's and lamps. The OZ972, in shut down condition, pulls TALK low and informs the OZ976 of an abnormal condition. The OZ976 will check the setting of the IND pin and decide whether to disable all the inverters.

Dimming

Refer to Cases 1 and 2 on pages 22 and 23, respectively. After TALK goes high and VDIM is within the LCT signal range of 1V to 3V, the OZ976 PWM Generator sends out a set of PWM signals to all the OZ972s. The VDIM voltage level and LCT signal decide the Pulse Width of the PWM dimming signals. The PWM frequency is decided by the internal LCT signal or external VSYNC signal. Each PWM signal has the same Pulse Width and frequency. Each signal has an equal amount of phase delay between them.

The delay time is determined by the following equations:

Case 1: External VSYNC Signal

$$\textbf{Delay Time} = \frac{\textbf{T2}}{\textbf{2 x Number of Phases}}$$

Case 2: Internal LCT Signal

$$\textbf{Delay Time} = \frac{\textbf{T1}}{\textbf{2 x Number of Phases}}$$

Each OZ972 adjusts the power delivered to its corresponding lamp following the PWM signal. This phase shift dimming control method minimizes the ripple current on the power line.

6. Protection

During the ignition period, open-lamp protection is provided through both CTIMR and OVP. This ensures that a rated voltage is achieved and a required timing period is satisfied. Removal of the CCFL during normal operation will trigger the error amplifier output and shut down the OZ972.

7. CTIMR-CCFL Ignition Time

The ignition time varies for CCFLs, depending on their length, diameter, module package, manufacturer and temperature. OZ972 provides a flexible design where a capacitor is connected to the CTIMR pin to set the maximum striking time. When the OVP pin reaches a 2.22V threshold, the CTIMR capacitor starts to charge. When the CTIMR has expired (CTIMR capacitor voltage reaches approximately 3V) and no current is sensed, the OZ972 shuts down. An approximation of the timing calculation is:

$$T[\text{second}] = C[\text{uF}]$$

This capacitor remains reset at no charge if the lamp is connected and in normal operation.

8. OVP

The OVP threshold is set at 2.22V nominal. When the output voltage reaches the threshold, it commands the QA/QD and QB/QC switches to maintain a regulated striking voltage. This ensures that the output has sufficient striking voltage while operating the transformer safely.

9. OZ972 ENA

A logic high TTL signal from the OZ976 to the ENA pin of the OZ972 enables the power controllers. A logic low signal to the ENA pin will disable the operation of the inverter. Toggling this signal resumes the operation of the OZ972.

10. Soft-Start Time -- SST

The soft-start function is provided with a capacitor connected to SST pin. The SST provides a rate of rise for the pulse width where diagonal switches are turned on. This function reduces in-rush current and prevents unnecessary stress to both the CCFL and the transformer.

11. Error Amplifier

CCFL current is regulated through the error amplifier. It also provides the intelligence of differentiating open-lamp striking versus removing the lamp during normal operation. The non-inverting reference is at 1.28V nominal.

12. Operating Frequency

The programmable operating frequency is decided by OZ976. CT and CLK signals are necessary for OZ972 operation. The OZ972 combines the CLK, CT and SST or CMP signals to drive the four output drives.

13. Output Drives

The four power MOSFET gate output drives are designed so that switches QA/QB and QC/QD never turn on simultaneously. The configuration prevents any shoot-through issue associated with bridge-type power conversion applications. By adjusting the overlap conduction between QA and QD, QB and QC, the CCFL current regulation is achieved. The overlap is adjusted when the power source voltage varies. The four output drive pins provide drive to two P-channel level shifters and two direct gate drive N-channel MOSFETs.

14. OZ976 Operation Principle

Referring to Figures 1 (page 8) and 5 (page 18), the OZ976 provides the DC reference voltage, enable signal, synchronized operating frequency, PWM dimming signals and protection services to each OZ972. Each OZ972 provides operating status to the OZ976 through TALK.

15. OZ976 Protection Block

VINS

The OZ976 provides VINS to sense the input power supply voltage to the inverter. When under-voltage lock out is triggered, the OZ976 disables the OZ972's through the ENA_PP pin.

ENA

A logic high TTL signal to the ENA pin enables the operation of the IC. A logic low signal to the ENA pin disables the operation of the inverter. Toggling this signal allows the turn-on and turn-off of the inverter.

IND (Individual) and TALK

The IND feature is user programmable. When IND is set high, all OZ972s work individually. In this situation, when a lamp is damaged or open, the corresponding OZ972 will shut down and pull TALK low, indicating to the OZ976 that an abnormal situation exists. The OZ976 will ignore the falling edge of TALK and maintain system operation. When IND is set low, all OZ972s work as a group. Once the OZ976 detects a TALK falling edge, the OZ976 pulls ENA_PP low to disable all the inverters. Refer to Figures 7 and 8 on pages 20 and 21, respectively.

ENA_PP

The OZ976 ENA_PP pin connects to all ENAs of OZ972. When VINS, ENA, IND and TALK are satisfied, ENA_PP goes high to enable the operation of the OZ972s. The system will be disabled when VINS is in an under-voltage lock out condition or ENA is low. In addition, when TALK has a falling edge with IND set low, ENA_PP goes low and disables the system. In this condition, only when VINS and ENA are satisfied, toggling VDDA will resume system operation.

16. Operation Frequency

A resistor RT and capacitor CT determine the operating frequency of the OZ976. The frequency is calculated as follows:

$$f_{CLK[KHz]} = \frac{675 \bullet 10^3}{C_T[pF] \bullet R_T[k\Omega]}$$

The OZ976 also provides an optional striking frequency if desired. When RT1 is used, it is connected in parallel with RT during the ignition period, and provides a higher frequency for striking. After enable, OZ976 detects TALK pin's first rising edge and RT1 is disconnected.

CT is a saw-tooth waveform and its frequency is double the f_{CLK} operation frequency. CLK is a square waveform and its frequency is the operation frequency. Both of these signals are used by the OZ972 to control the output drivers, PDR_A, NDR_B, PDR_C and NDR_D.

17. Reference Voltage

OZ976 is the voltage source providing all OZ972 the reference voltage through REF pin. All OZ972s follow the REF voltage and generate internal references. The reference voltage is activated approximately 1ms before ENA_PP goes high and it lasts 1ms after ENA_PP goes low. The time delay relates to the resonator frequency of OSCA and OSCY.

18. PWM Dimming Control

OZ976 provides PWM dimming signals to each OZ972 with an equal phase delay.

Internal LCT Frequency

The internal pre-programmed PWM frequency T1 (see Case 2, page 23) is determined by a capacitor connected to the LCT pin. An approximation of the frequency can be calculated by:

$$f_{LCT}[Hz] = \frac{102 \bullet 10^3}{C_{LCT}[nF] \bullet R_T[k\Omega]}$$

The peak and valley of the LCT signal is nominally 3V and 1V respectively. The VDIM signal is compared to the triangle wave in LCT and yields a proper pulse width to modulate the CCFL current. By programming POL, the positive or negative pulse width will be duplicated and imposed on the PWM signal. The designer defines the relationship between VDIM and panel brightness. Setting POL high, an increase in VDIM, will increase the panel brightness. Conversely, setting POL low, a decrease in VDIM, will increase the panel brightness.

PWM Frequency

Through VSYNC, PWM signals can be synchronized with an external control signal with a TTL level frequency range from 65Hz to 180Hz. If a VSYNC signal does not exist, the OZ976 uses the LCT signal to synchronize the PWM signals. All PWM signals are synchronized with either the internal (LCT) or external (VSYNC) signal. The PWM signals are twice the frequency of the internal or external signal.

PWM Dimming Signals

The PWM dimming signal frequency is extracted from either an internal LCT signal or from the external VSYNC signal. The pulse width of PWM dimming signal comes from the comparison result of LCT and VDIM. There is a fixed phase delay between sequential PWM dimming signals. The PWM Generator generates a new set of PWM dimming signals resulting from the combination of Pulse Width, X2 PWM dimming frequency and Phase Delay. All PWM signals have the same pulse width and frequency. The only difference among the PWM signals is the phase delay, which is determined by the PWM dimming period divided by the number of phases. No two PWM signals have the same phase shift amount.

SEL0 and SEL1

The SEL0 and SEL1 pins are used to select the number of lamps, from 6, 8, 10 and 12.

Table 1. OZ976 Phase Select Logic

SEL0	SEL1	No. of Phases
0	0	6
0	1	8
1	0	10
1	1	12

L0 to L11

L0 to L11 are the PWM signal output pins. All of the outputs are a 3-state buffer.

19. Resonator

A 4MHz resonator is used to provide a precise Pulse Width and frequency to the PWM Generator in order to generate the PWM dimming signals. OSCA and OSCY pins are provided to connect a resonator.

Table 2. Resonator Frequency Selector

Resonator	LCT/VSYNC Minimum Frequency
4MHz	61Hz
3.59MHz	55Hz
3MHz	46Hz

OZ972 TYPICAL APPLICATION CIRCUIT

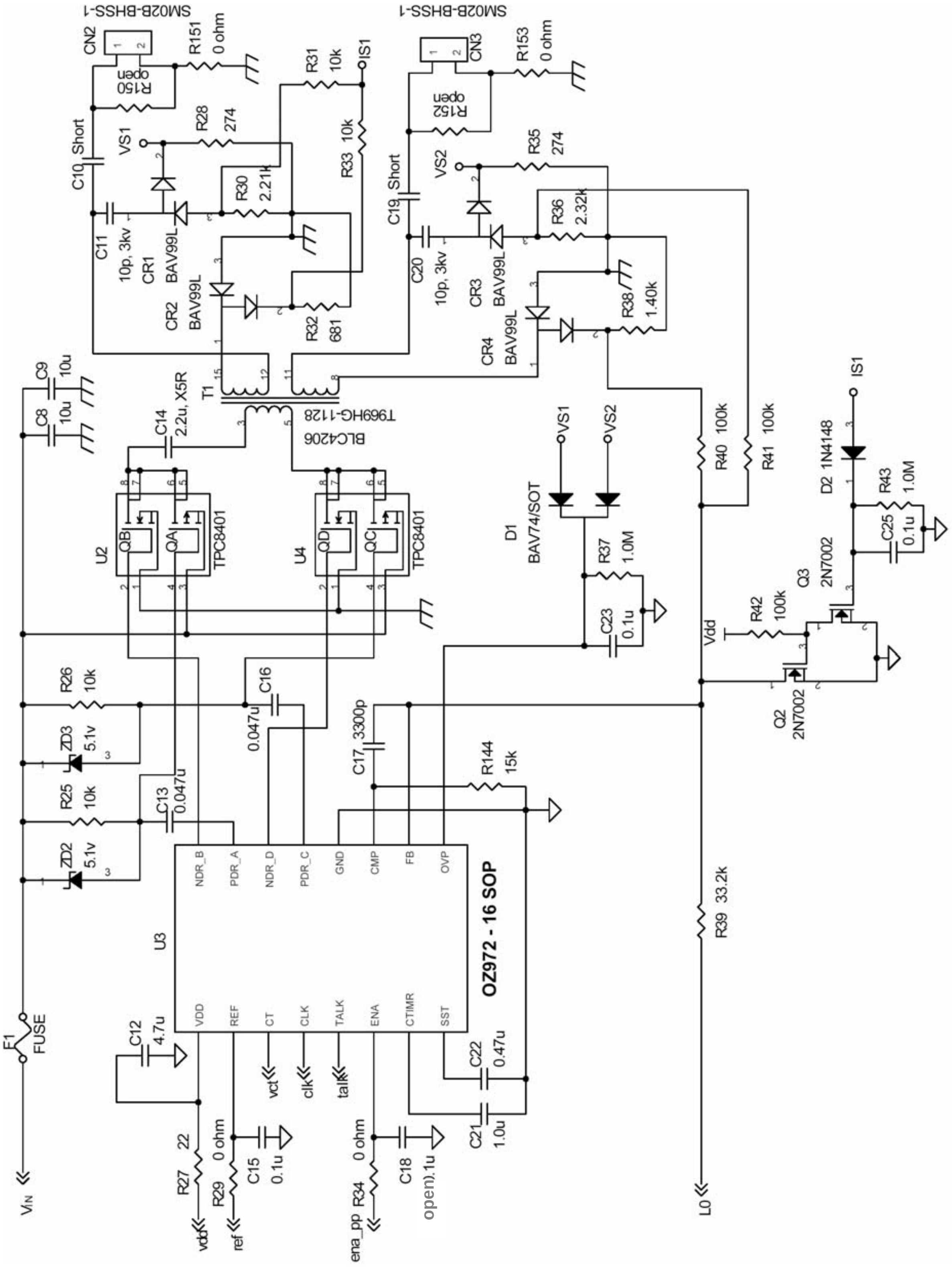

SM02B-BHSS-1
CN2
R151 0 ohm
R150 open
C10 Short
VS1
R28 274
R31 10k
IS1
R33 10k
R30 2.21k
C11 10p, 3kv
CR1 BAV99L
CR2 BAV99L
R32 681
SM02B-BHSS-1
CN3
R153 0 ohm
R152 open
C19 Short
VS2
R35 274
R36 2.32k
C20 10p, 3kv
CR3 BAV99L
CR4 BAV99L
R38 1.40k
C9 10u
C8 10u
T1
C14 2.2u, X5R
T969HG-1128
BLC4206
U2
QB
QA
TPC8401
U4
QD
QC
TPC8401
VS1
VS2
D1 BAV74/SOT
R37 1.0M
C23 0.1u
R40 100k
R41 100k
IS1
D2 1N4148
R43 1.0M
C25 0.1u
Q3 2N7002
Vdd
R42 100k
Q2 2N7002
R26 10k
ZD3 5.1v
C16 0.047u
R25 10k
ZD2 5.1v
C13 0.047u
C17 3300p
R144 15k
U3
NDR_B
PDR_A
NDR_D
PDR_C
GND
CMP
FB
OVP
OZ972 - 16 SOP
VDD
REF
CT
CLK
TALK
ENA
CTIMR
SST
F1 FUSE
C12 4.7u
vct
clk
talk
C22 0.47u
C21 1.0u
R39 33.2k
VIN
R27 22
vdd
R29 0 ohm
ref
C15 0.1u
ena_pp
R34 0 ohm
C18 (open).1u
L0

Figure 4

OZ976 TYPICAL APPLICATION CIRCUIT

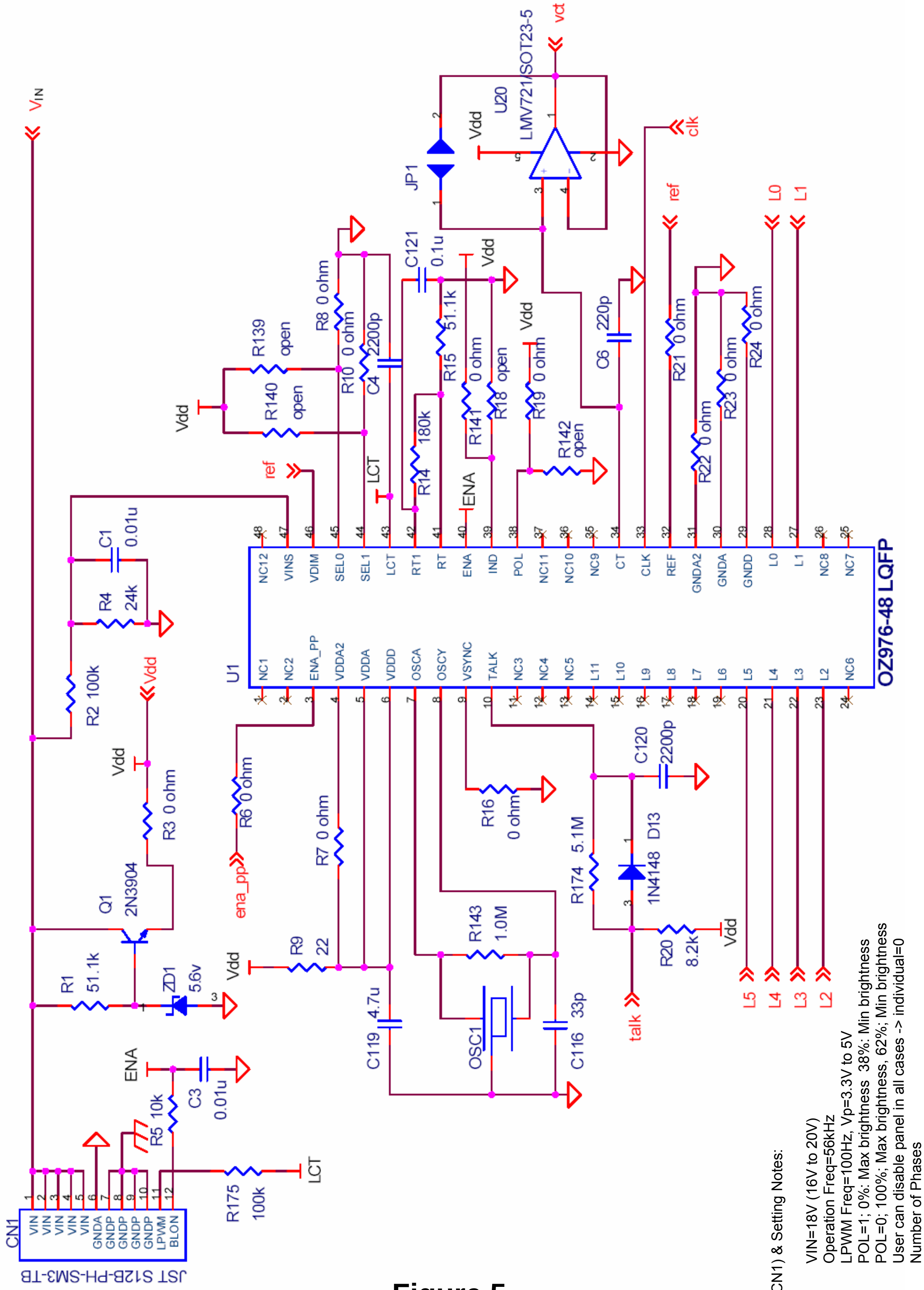

VIN
U1
OZ976-48 LQFP
NC1
NC2
ENA_PP
VDDA2
VDDA
VDDD
OSCA
OSCY
VSYNC
TALK
NC3
NC4
NC5
L11
L10
L9
L8
L7
L6
L5
L4
L3
L2
NC6
NC12
VINS
VDIM
SEL0
SEL1
LCT
RT1
RT
ENA
IND
POL
NC11
NC10
NC9
CT
CLK
REF
GNDA2
GNDA
GNDD
L0
L1
NC8
NC7
CN1
JST S12B-PH-SM3-TB
VIN
GNDA
GNDP
LPWM
BLON
R175 100k
LCT
R5 10k
C3 0.01u
ENA
R1 51.1k
ZD1 5.6v
Q1 2N3904
R3 0 ohm
Vdd
R2 100k
R4 24k
C1 0.01u
R6 0 ohm
ena_pp
R7 0 ohm
R9 22
C119 4.7u
OSC1
R143 1.0M
C116 33p
R16 0 ohm
R174 5.1M
D13 1N4148
C120 2200p
R20 8.2k
talk
L5
L4
L3
L2
ref
R140 open
R139 open
R8 0 ohm
R10 0 ohm
C4 2200p
C121 0.1u
R14 180k
R15 51.1k
R141 0 ohm
R18 open
R19 0 ohm
R142 open
C6 220p
R21 0 ohm
R22 0 ohm
R23 0 ohm
R24 0 ohm
JP1
U20
LMV721/SOT23-5
vct
clk
ref
L0
L1

Figure 5

Input (CN1) & Setting Notes:

1. VIN=18V (16V to 20V)
2. Operation Freq=56kHz
3. LPWM Freq=100Hz, Vp=3.3V to 5V
   POL=1; 0%: Max brightness 38%: Min brightness
   POL=0; 100%; Max brightness, 62%; Min brightness
4. User can disable panel in all cases -> individual=0
5. Number of Phases
   6 Phases : SEL0=0, SEL1=0
   8 Phases : SEL0=0, SEL1=1
   10 Phases : SEL0=1, SEL1=0
   12 Phases : SEL0=1, SEL1=1

Note: Input LPWM signal to CN1 pin 11 (LPWM)

SST TO NORMAL OPERATION

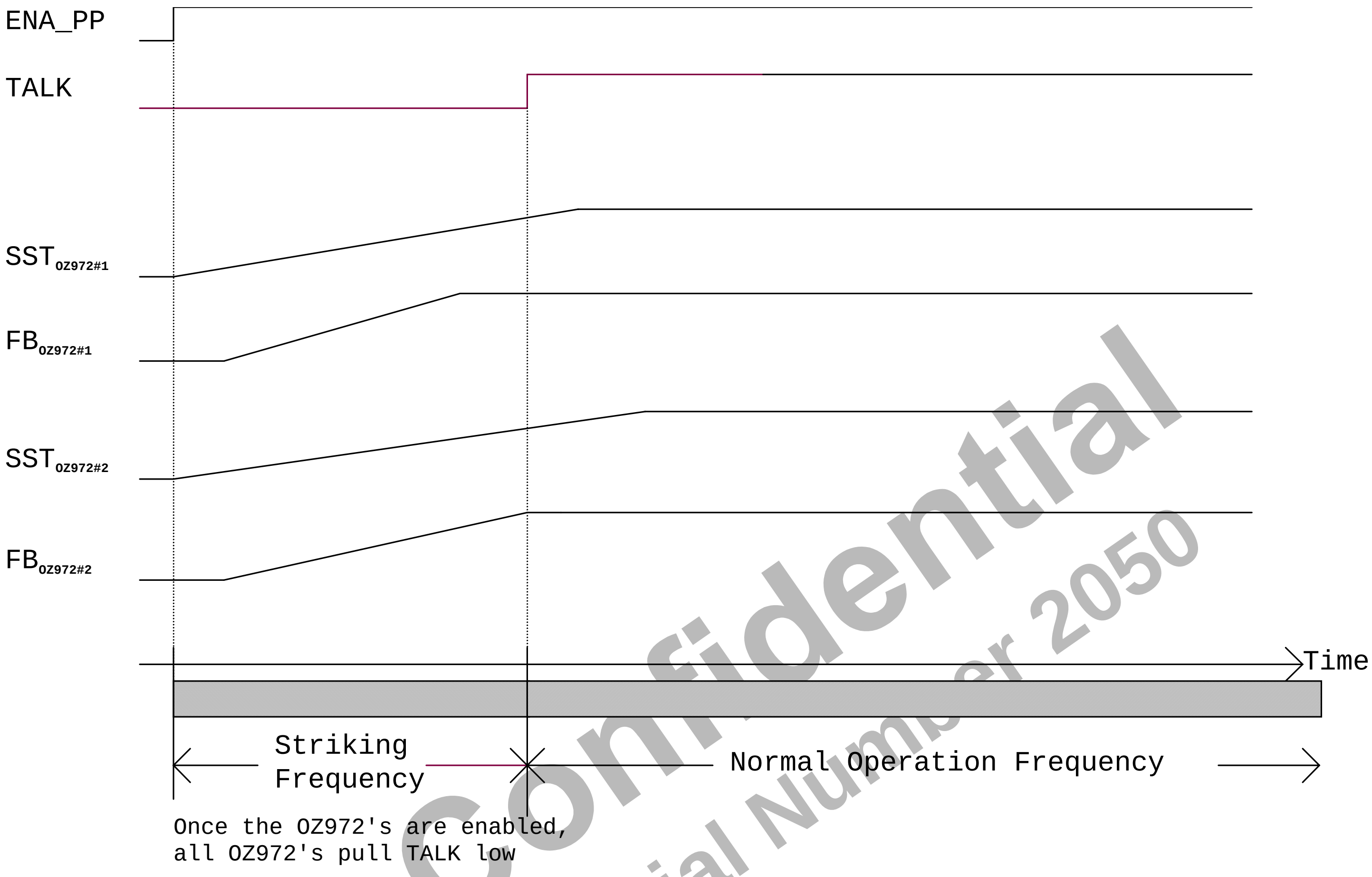
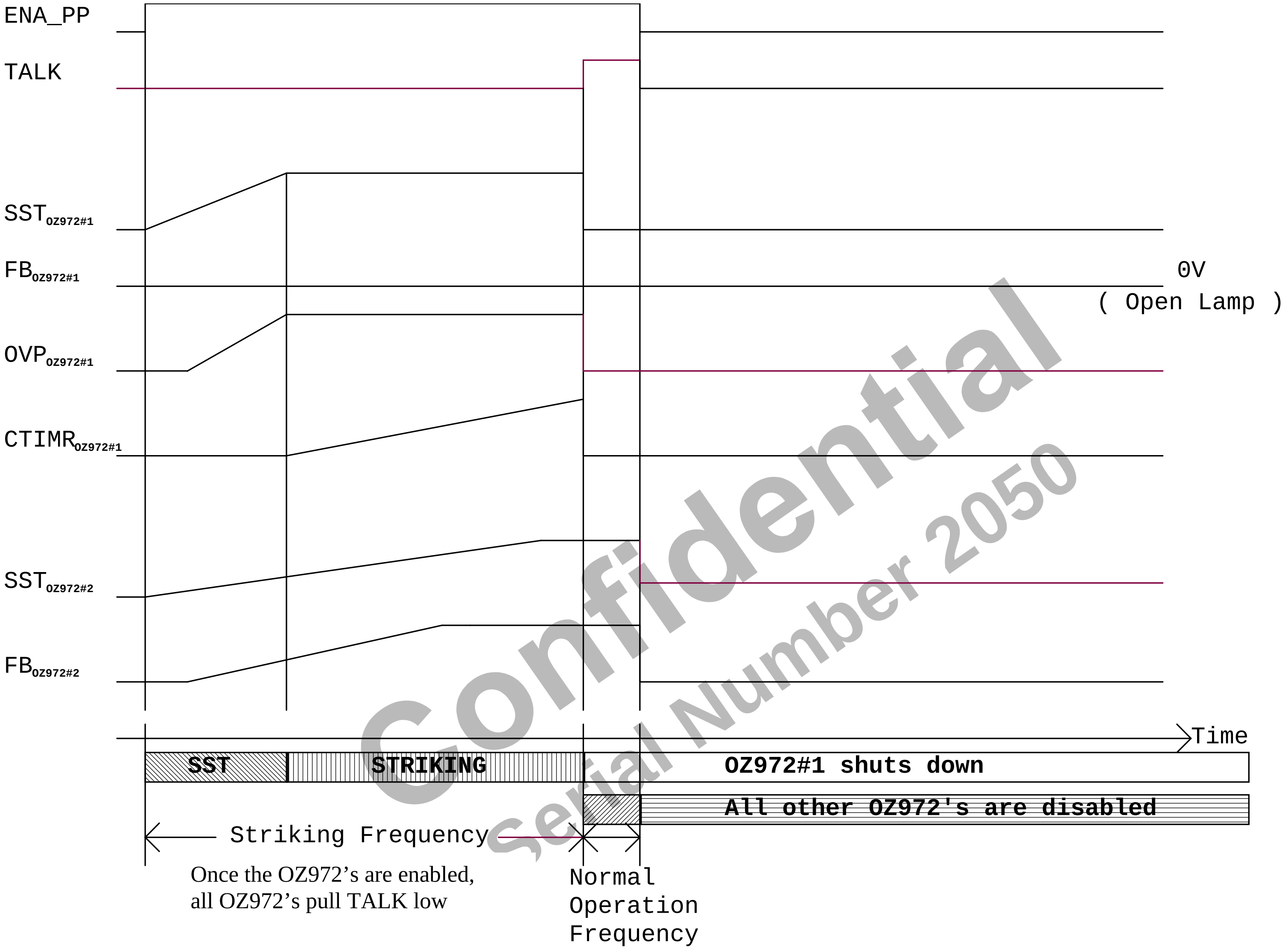

ENA_PP
TALK
SST OZ972#1
FB OZ972#1
SST OZ972#2
FB OZ972#2
Time
Striking Frequency
Normal Operation Frequency
Once the OZ972's are enabled,
all OZ972's pull TALK low

Figure 6

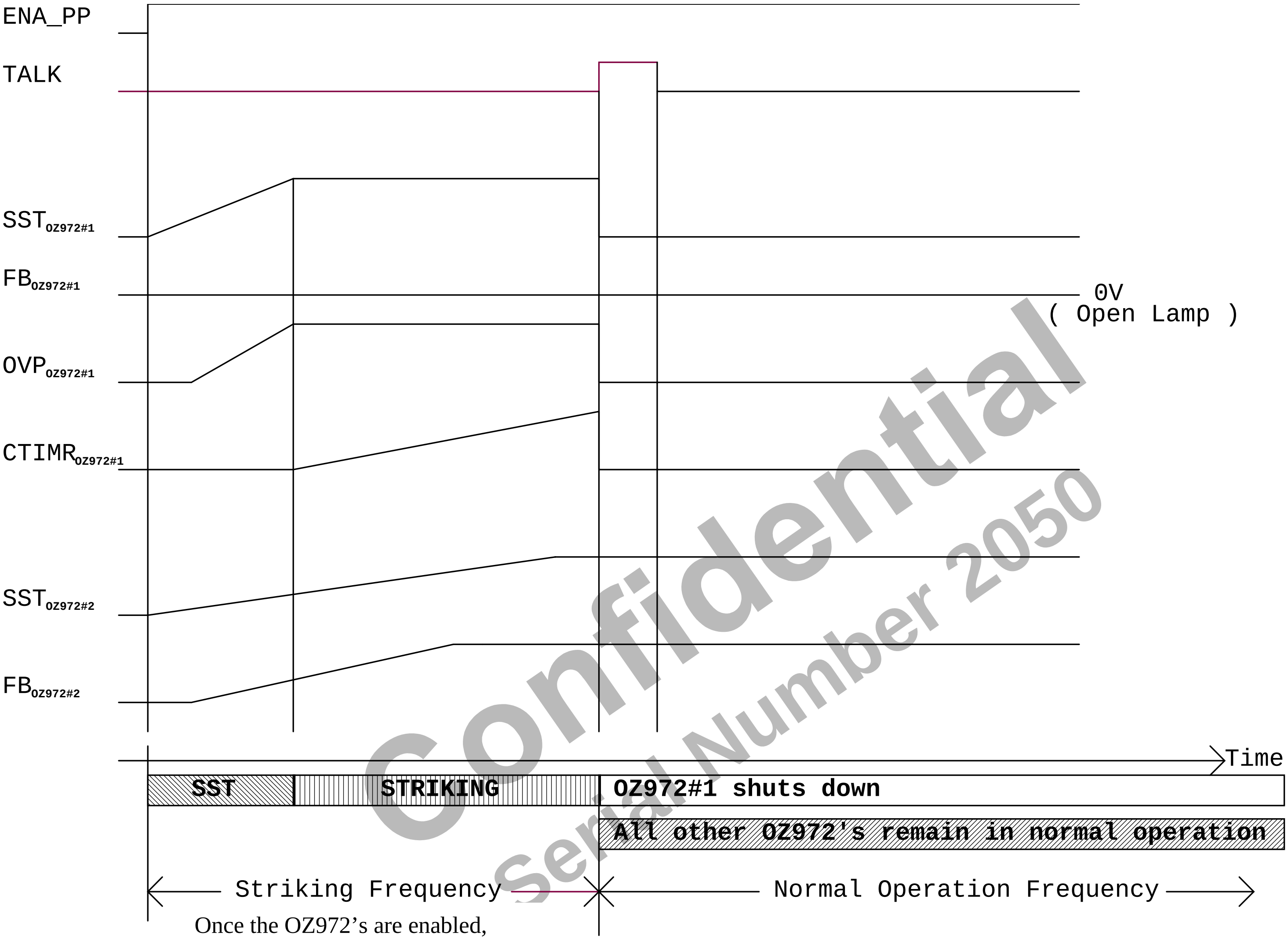
SST to OPEN LAMP- GROUP OPERATION
OZ976 IND PIN SET LOW


ENA_PP
TALK
SST OZ972#1
FB OZ972#1
OVP OZ972#1
CTIMR OZ972#1
SST OZ972#2
FB OZ972#2
0V
(Open Lamp)
Time
SST
STRIKING
OZ972#1 shuts down
All other OZ972's are disabled
Striking Frequency
Normal
Operation
Frequency

Once the OZ972's are enabled, all OZ972's pull TALK low

Figure 7

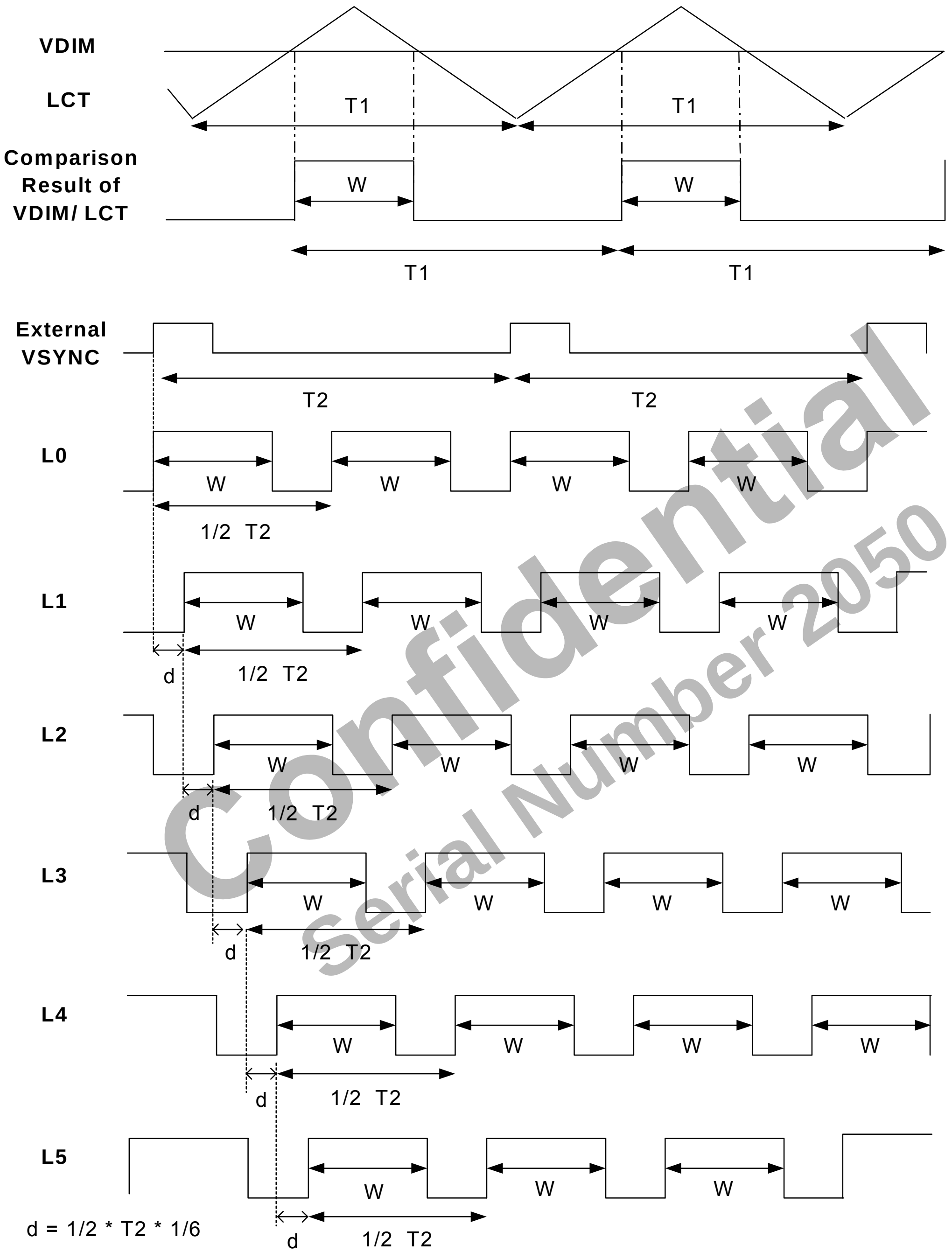
SST TO OPEN LAMP- INDIVIDUAL OPERATION
OZ976 IND PIN SET HIGH


ENA_PP
TALK
SST$_{OZ972\#1}$
FB$_{OZ972\#1}$
0V
(Open Lamp)
OVP$_{OZ972\#1}$
CTIMR$_{OZ972\#1}$
SST$_{OZ972\#2}$
FB$_{OZ972\#2}$
Time
SST
STRIKING
OZ972#1 shuts down
All other OZ972's remain in normal operation
Striking Frequency
Normal Operation Frequency

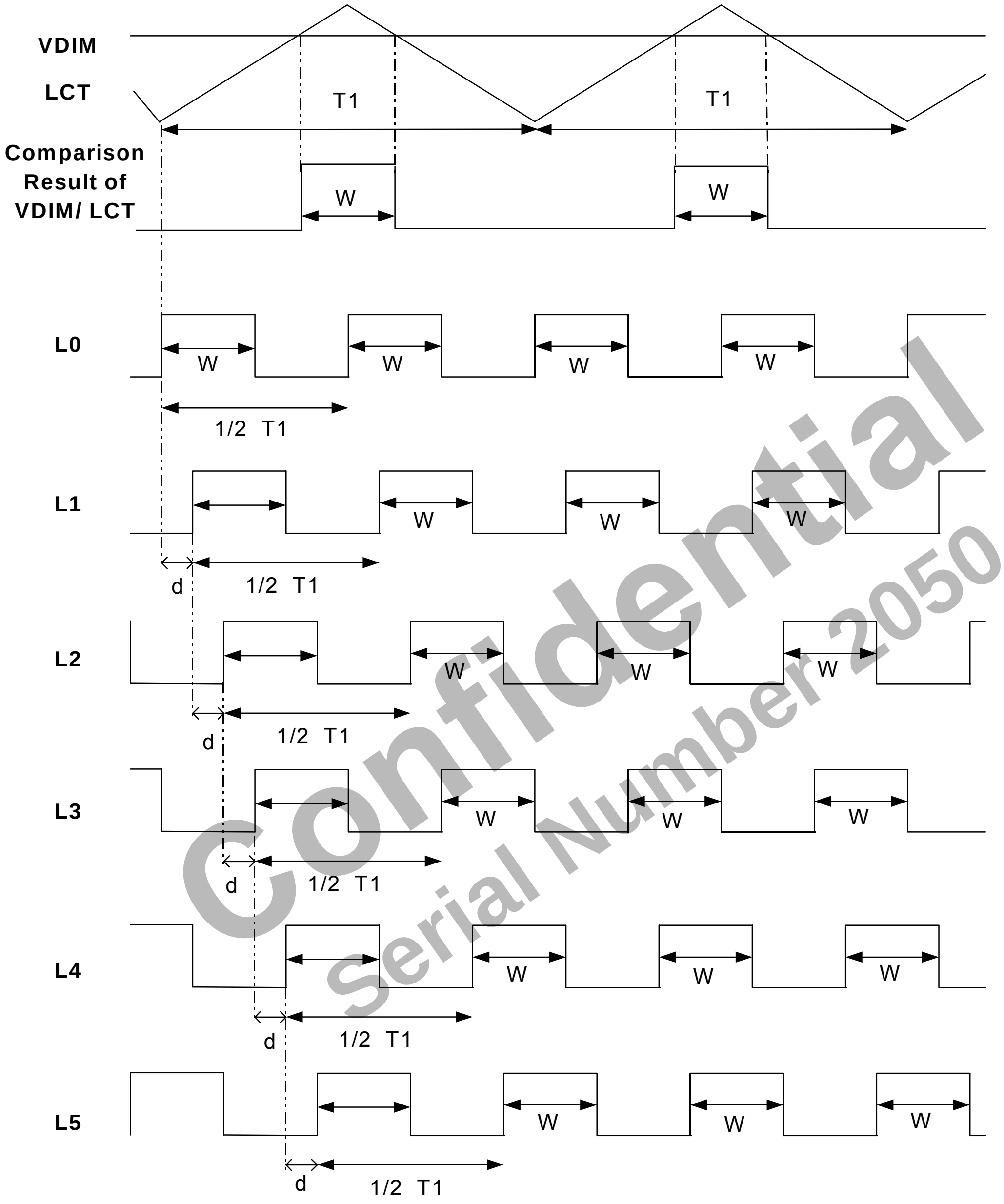
Once the OZ972's are enabled,
All OZ972's pull TALK low.

Figure 8

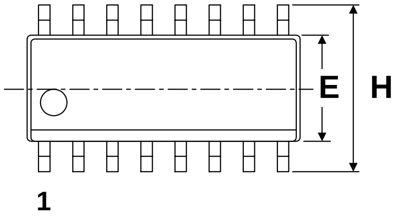
CASE 1: EXTERNAL VSYNC SIGNAL
6 LAMP APPLICATION WITH POL=1


VDIM
LCT
T1
T1
Comparison Result of VDIM/ LCT
W
W
T1
T1
External VSYNC
T2
T2
L0
W
W
W
W
1/2 T2
L1
W
W
W
W
d
1/2 T2
L2
W
W
W
W
d
1/2 T2
L3
W
W
W
W
d
1/2 T2
L4
W
W
W
W
d
1/2 T2
L5
W
W
W
d = 1/2 * T2 * 1/6
d
1/2 T2

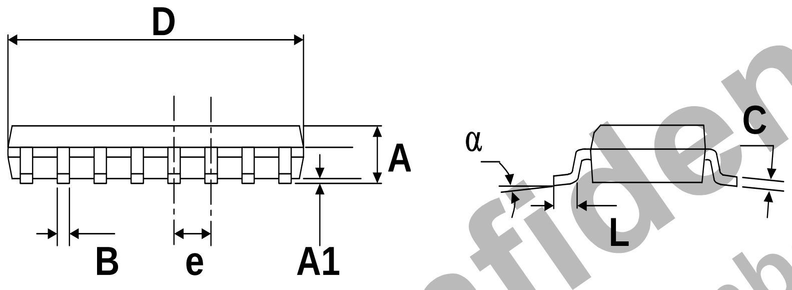
CASE 2: INTERNAL LCT SIGNAL
6 LAMP APPLICATION WITH POL=1


VDIM
LCT
T1
T1
Comparison Result of VDIM/ LCT
W
W
L0
W
W
W
W
1/2 T1
L1
W
W
W
d
1/2 T1
L2
W
W
W
d
1/2 T1
L3
W
W
W
d
1/2 T1
L4
W
W
W
d
1/2 T1
L5
W
W
W
d
1/2 T1

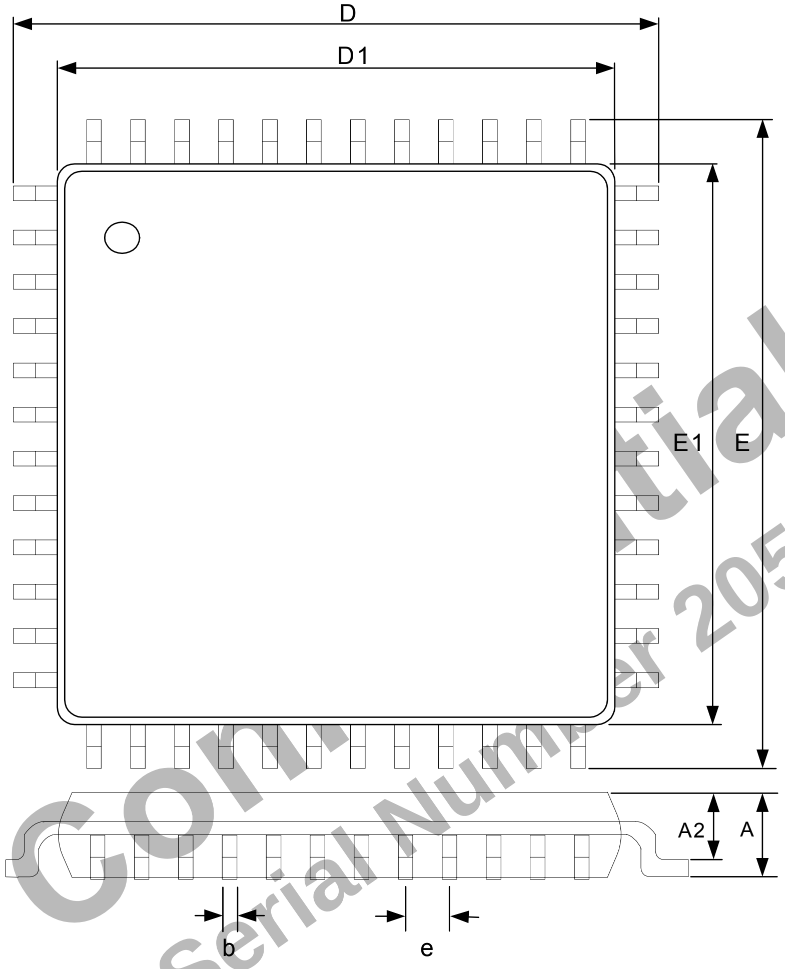
PACKAGE INFORMATION - 16-Pin SOP: OZ972G Power Controller



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.0532	0.0688	1.35	1.75
A1	0.0040	0.0098	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.0075	0.0098	0.19	0.25
D	0.3859	0.3937	9.80	10.00
E	0.1497	0.1574	3.80	4.00
e	0.050 BCS.		1.27 BCS.	
H	0.2284	0.2440	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°



PACKAGE INFORMATION - 48-Pin LQFP: OZ976T Array Hub



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.40	1.50	1.60	0.052	0.059	0.063
A2	1.35	1.40	1.45	0.050	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
D1	6.90	7.00	7.10	0.272	0.276	0.280
D	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
e	-	0.50	-	-	0.020	-

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