Control System Design and Small-Signal Analysis of a Phase-Shift-Controlled Series-Resonant Inverter for Induction Heating

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Abstract - **A phase-shift-controlled series-resonant inverter operating at zero-voltage-switching (ZVS) is used as the power supply for an induction heating system. This system has two control loops: the phase-shift control loop regulates the output power, and the frequency control loop ensures ZVS for all load conditions. The design and implementation of these control loops are explained. The complete closed-loop small-signal model is obtained using the extended describing function method. The model predictions are compared with experimental data measured from a lab prototype.**

I. INTRODUCTION

A phase-shift controlled series-resonant inverter (PSC-SRI) operating at 500 kHz, 10 kW is used as the power supply for an induction heating system. A PSC-SRI has been suggested for induction heating applications because of its hardware simplicity [Grajales, Nakaoka]. The PSC-SRI does not require a pre-regulator and the resonant inductor is composed of the coil, work-piece and transformer leakage inductance. In addition the PSC-SRI operates over a narrow frequency range because the switching frequency varies only to maintain zero turn-on losses, also called zero-voltage switching (ZVS). The proposed PSC-SRI has two control loops: the phase-shift control loop regulates the output power, and the frequency control loop ensures ZVS. The phase-shift is regulated with a PWM duty-cycle control strategy. The frequency is regulated using an adaptation of the current charge control method.

Most induction heating applications require heating the work-piece at a given temperature for a given time. During the heating process the load resistance and inductance vary, especially when the work-piece reaches the Curie temperature. Therefore, since the load inductance is part of the resonant inductance, the resonant frequency of the system will vary. The frequency control strategy for the PSC-SRI keeps track of the resonant frequency to maintain ZVS while switching as close as possible to resonance to minimize circulating energy. Because of the high risk of MOSFET damage when ZVS is not achieved, it is important to know the response time and the reliability of the frequency control loop. At the same time, depending on the application, there might be a demand for an accurate power control for a given temperature profile. Hence, the bandwidth, phase margin, and gain margin of the frequency and power control loops should be properly designed to guarantee a robust system. The small-signal model is a useful tool to analyze the performance of the control loops. It helps corroborate hardware loop measurements, and it allows experimenting with several compensation schemes before they are implemented.

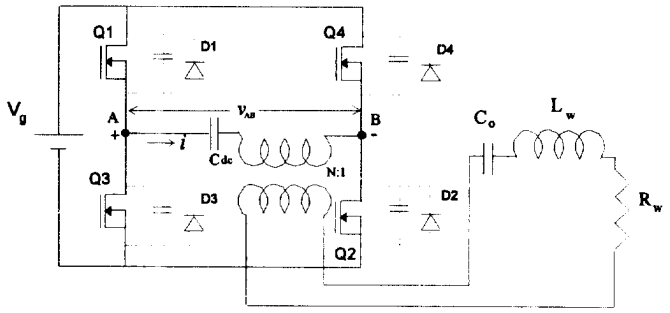

Fig. 1 PSC-SRI power stage circuit

This paper will describe the PSC-SRI operation. It will use the extended describing function method for modeling the inverter power-stage. The closed-loop small-signal model will be derived for both the phase-shift and the frequency control loops. Loop-gain transfer functions will be obtained and compared with experimental data measured from a laboratory prototype.

II. PHASE-SHIFT CONTROLLED SERIES-RESONANT INVERTER PROPERTIES

The power stage of the circuit, a full-bridge series-resonant inverter, is shown in Fig. 1. L_W and R_W are the coil plus work-piece equivalent inductance and resistance, respectively. C_O is the resonant capacitance, and C_{dc} is the dc current blocking capacitor. Also, f_s is the switching frequency, and f_o is the resonant frequency, where $f_o = \frac{1}{2\pi\sqrt{L_w C_o}}$.

Power MOSFETs are selected as the switching devices for this application because of the high switching frequency requirement. The four transistors, Q1-Q4, are operated with a 50% duty cycle. The switches in each leg of the bridge are turned on and off 180 degrees out of phase. When operating above resonance, the load current, i, lags the quasi-square wave voltage, v_{AB}, as shown in Fig. 2(a). Body diodes conduct current after the MOSFET's output capacitance is discharged. During this diode conduction period, the MOSFETs can be turned on at zero voltage [Sabaté]. Zero voltage switching (ZVS) must be ensured at all times to prevent possible device damage. Output power of the inverter is regulated by varying the phase-shift between switches Q1 and Q2. The resulting voltage across the tank is a quasi-square wave with a duty ratio ***d***. If the switching frequency is kept constant and close to resonance, ZVS will be lost for decreasing values of ***d*** because the load current becomes positive before Q2 turns on. To prevent loosing ZVS, the controller increases the switching frequency to allow for more

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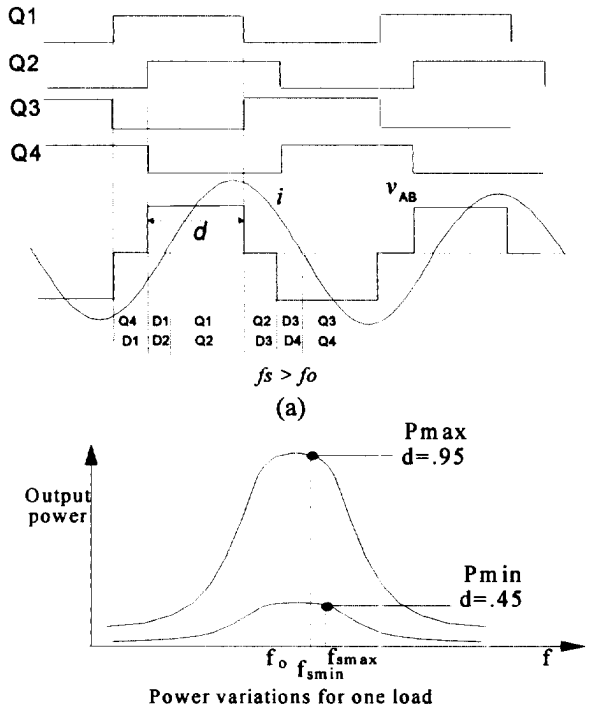

Fig. 2 (a) PSC-SRI Power stage circuit waveforms (b) Power regulation for one load condition.

negative load current before Q2 turns on, ensuring a full discharge of the MOSFET's output capacitance.

Figure 2(b) shows an example of the control strategy for a particular load condition. This example shows that when $d = 0.95$, maximum power is obtained and that the switching frequency is very close to resonance (ZVS is maintained), whereas when low output power is desired for the same load condition, $d = 0.45$. The switching frequency that ensures ZVS is farther from resonance when $d = 0.45$ than when $d = 0.95$.

III. Small-Signal Model

Figure 3 shows the system's diagram with the two control loops: frequency and phase-shift. The slow loop is the phase-shift control loop, which senses the output power, P_O, and varies the phase-shift to maintain P_O at the desired value.

The fast loop is the frequency control loop, which senses the tank current and determines how far above resonance it should operate to maintain ZVS. In this section, the small-signal model will be obtained, first for the power stage, and subsequently for each of the control loops. The modeling method used is known as "extended describing function method".

A. Power Stage Small Signal Model

In this section, a summarized procedure of how to obtain the small-signal model of the power stage of the PSC-SRI will be given. For further extended describing function modeling techniques and other circuit models see [Yang, 1991].

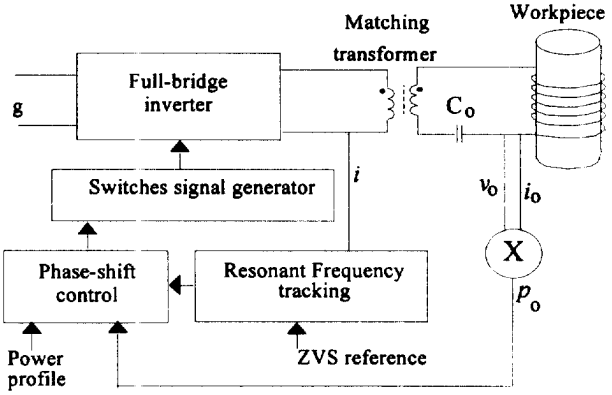

Fig. 3 PSC-SRI system diagram.

The PSC-SRI power stage circuit can be represented by the equivalent circuit shown in Fig. 4.

First, Kirchhoff's voltage law is applied to the circuit in Fig. 4 to give

$$L\frac{di}{dt}+v+iR=v_{AB}\,, \tag{1}$$

$$C\frac{dv}{dt}=i\,. \tag{2}$$

The output variable is the average power at the resistance:

$$P_o=\frac{Ri^2}{2}\,. \tag{3}$$

The harmonic approximation is used for the inductor current and capacitor voltage so that

$$i(t)\approx i_c(t)\cdot cos(\omega_s t)+i_s(t)\cdot sin(\omega_s t)\,, \tag{4}$$

$$v(t)\approx v_c(t)\cdot cos(\omega_s t)+v_s(t)\cdot sin(\omega_s t)\,, \tag{5}$$

and the extended describing function is applied to the input voltage,

$$v_{AB}=\frac{4}{\pi}v_g sin(\frac{\pi}{2}d)sin(\omega t)=v_e sin(\omega t)\,. \tag{6}$$

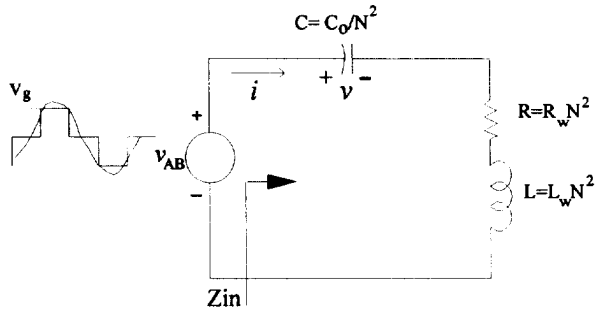

Fig. 4 Equivalent PSC-SRI Circuit

Substituting (4)-(6) into (1)-(2), and using the harmonic balance procedure, we can decompose (1)-(2) into four equations by grouping separately the sine terms and the cosine terms to obtain:

sine terms:
$$\frac{dv_s}{dt}=\frac{i_s}{C}+\omega_s v_c\,, \tag{7}$$

$$\frac{di_s}{dt}=\frac{-v_s-i_s R+v_e}{L}+\omega_s i_c\,, \tag{8}$$

cosine terms:

$$\frac{dv_c}{dt}=\frac{i_c}{C}-\omega_s v_s, \quad (9)$$

$$\frac{di_c}{dt}=\frac{-v_c-i_c R}{L}-\omega_s i_s. \quad (10)$$

Equations (7)-(10) can now be used to solve for the operating point by letting all the derivatives be zero. Their solutions are given in appendix A.

The linearized model is found by perturbing the large-signal system given by (7)-(10) around the operating point [V_g, D, W_s, Q], where V_g is the input voltage, W_s is the switching frequency, D is the duty ratio, and Q is the load factor defined as $Q=\frac{W_s L}{R}$. The perturbed variables are the inputs, the state variables, and the output. Each will have the form of

$$h(t)=H+\hat{h}(t), \quad (11)$$

where H is at the operating point, and $\hat{h}(t)$ is a small amplitude perturbation. Hence, these perturbed variables are replaced in (7)-(10), and then, by finding the Taylor expansion and considering only the first partial derivatives, we obtain the linearized model [Kassakian]. For example, (8) can be expressed as:

$$\frac{di_s}{dt}=f(v_s,v_c,i_s,i_c,d,v_g,w_s); \quad (12)$$

hence, its linearized equation is

$$\frac{d\hat{i}_s}{dt}\approx\frac{\partial f}{\partial v_s}\hat{v}_s+\frac{\partial f}{\partial v_c}\hat{v}_c+\frac{\partial f}{\partial i_s}\hat{i}_s+\frac{\partial f}{\partial i_c}\hat{i}_c+\frac{\partial f}{\partial \omega_s}\hat{\omega}_s+\frac{\partial f}{\partial v_g}\hat{v}_g+\frac{\partial f}{\partial d}\hat{d}, \quad (13)$$

where each $\frac{\partial f}{\partial x}$ is evaluated at the operating points.

Equation (13) is acceptable as long as the perturbation is small-signal, since higher order terms can be neglected. This linearization procedure is done to (7)-(10) to obtain the complete linearized model:

$$\frac{d\hat{v}_s}{dt}=\frac{\hat{i}_s}{C}+W_s\hat{v}_c+V_c\hat{\omega}_s, \quad (14)$$

$$\frac{d\hat{i}_s}{dt}=\frac{\hat{v}_s}{L}-\frac{R}{L}\hat{i}_s+W_s\hat{i}_c+I_c\hat{\omega}_s+\frac{2V_g}{L}\cos(\frac{\pi}{2}D)\hat{d}+\frac{4}{\pi L}\sin(\frac{\pi}{2}D)\hat{v}_g, \quad (15)$$

$$\frac{d\hat{v}_c}{dt}=\frac{\hat{i}_c}{C}-W_s\hat{v}_s-V_s\hat{\omega}_s, \quad (16)$$

$$\frac{d\hat{i}_c}{dt}=-\frac{\hat{v}_c}{L}-\frac{R}{L}\hat{i}_c-W_s\hat{i}_s-I_s\hat{\omega}_s. \quad (17)$$

This model can also be expressed in matrix form,

$$\dot{x}=Ax+B_1u_1+B_2u_2+B_3u_3,$$
$$y=Cx, \quad (18)$$

where, y is a vector that includes the output variables and x is a vector that includes the state variables, such as,

$$x=\left[\hat{i}_s\ \ \hat{i}_c\ \ \hat{v}_s\ \ \hat{v}_c\right]', \qquad y=\hat{p}_o. \quad (19)$$

Hence,

$$\dot{x}=\begin{bmatrix}\frac{-R}{L} & W_s & \frac{-1}{L} & 0\\ -W_s & \frac{-R}{L} & 0 & \frac{-1}{L}\\ \frac{1}{C} & 0 & 0 & W_s\\ 0 & \frac{1}{C} & -W_s & 0\end{bmatrix}x+\begin{bmatrix}\frac{4}{\pi L}\sin(\frac{\pi}{2}D)\\ 0\\ 0\\ 0\end{bmatrix}\hat{v}_g+\begin{bmatrix}\frac{2V_g}{L}\cos(\frac{\pi}{2}D)\\ 0\\ 0\\ 0\end{bmatrix}\hat{d}+\begin{bmatrix}I_c\\ -I_s\\ V_c\\ -V_s\end{bmatrix}\hat{\omega}_s$$

$$y=\begin{bmatrix}RI_s & RI_c & 0 & 0\end{bmatrix}x. \quad (20)$$

The eigen values of the A matrix are the same as the poles of the open loop system. These poles are calculated from

$$det(sI-A)=0 \quad (21)$$

which results in four poles located at:

$$\text{Poles } p_1 \text{ and } p_2: -\frac{1}{2}\frac{R}{L}\pm j\left(\omega_o\sqrt{1-\frac{1}{4Q^2}}-\omega_s\right) \quad (22)$$

$$\text{Poles } p_3 \text{ and } p_4: -\frac{1}{2}\frac{R}{L}\pm j\left(\omega_o\sqrt{1-\frac{1}{4Q^2}}+\omega_s\right) \quad (23)$$

Poles p_1 and p_2 have been considered to be "beat frequency poles", that is, because they are assumed to be located at the frequency $\omega=\omega_o-\omega_s$, but as the pole equations show, the pole location is dependent on the load factor Q. The beat frequency approximation is not satisfactory for low values of Q, and/or when ω_s is very close to ω_o. The remaining poles, p_3 and p_4 are located at high frequencies, and their effect on the small-signal response can be neglected.

B. Power Regulation Loop Small-Signal Model

The output power is regulated by varying the duty cycle of the tank voltage, as explained in section II.

As shown in Fig. 5, the control strategy for the power regulation loop is very simple. Its main components are the multiplier and a PWM controller IC. The output power is measured by multiplying the coil voltage and current. This signal is compared against a reference voltage, if the output power signal is higher than the reference, the duty cycle will decrease. If the output power is lower than the reference, the duty cycle will increase.

Figure 5 shows the close loop for the power regulation, from which (after perturbing and linearizing), the following relationship for $\hat{d}$ is obtained:

$$\hat{d}=-F_m K_i G_d(s)\frac{e^{-sTd}}{(s+a_p)R_b C_b}\hat{p}_o, \quad (24)$$

where F_m is the gain of the pulse width modulator (PWM), K_i is the total gain of the power sensor, $G_d(s)$ is the compensator's transfer function, $\hat{p}_o$ is the perturbed output power, and T_d takes into account the driver's propagation delay. Hence,

$$G_d(s)=\frac{Z_d}{R_a}. \quad (25)$$

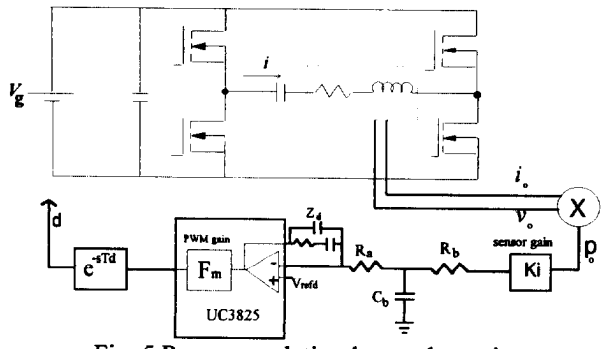

Fig. 5 Power regulation loop schematic

Also,

$$F_m = \frac{\hat{d}}{\hat{v}_d} = \frac{1}{S_n T_s}, \tag{26}$$

where S_n is the on-time slope magnitude of the PWM ramp, and $T_s = \frac{2\pi}{\omega_s}$.

Since the controller is designed to regulate the average output power, resistors R_a, R_b, and C_b have been added to average the multiplier instantaneous output power. These components contribute to the addition of pole a_p in (24) so that

$$a_p = \frac{1}{(R_a // R_b) C_b}. \tag{27}$$

The perturbed output power, given in (24), can be expressed as,

$$\hat{p}_o = RI_s \hat{i}_s + RI_c \hat{i}_c. \tag{28}$$

C. Frequency Loop Analysis

The frequency control circuit is composed of a charge measurement circuit, a compensator, and a voltage-controlled oscillator (VCO), as shown in Fig. 6(a). This circuit regulates the tank current charge during the ZVS transition (shaded area) to guarantee that ZVS is always achieved. If the measured charge is lower than desired, the circuit will increase the switching frequency to allow for additional time lagging between the tank voltage and the tank current, increasing the amount of charge. If the measured charge is larger than desired, then the switching frequency is decreased to improve the power factor. In summary, the charge circuit measures the primary current i_p, rectifies it, and measures the integral of the current during the time $\beta\tau$. The result of the integration is represented by v_c. Voltage v_c is compared with the reference voltage v_{refw}, to produce a compensated error voltage v_f. A simple VCO is built for the PWM 3825 IC which ensures that the output frequency varies directly proportionally to v_f [Jovanović].

In this section, the closed loop small-signal model of the frequency-loop will be derived. Hence, it is necessary to find an equation that relates the output frequency, ω_s, with the input current i_p. This equation is then linearized and attached to the power stage model to complete the close-loop model. The derivation of the charge model will be carried out in three steps.

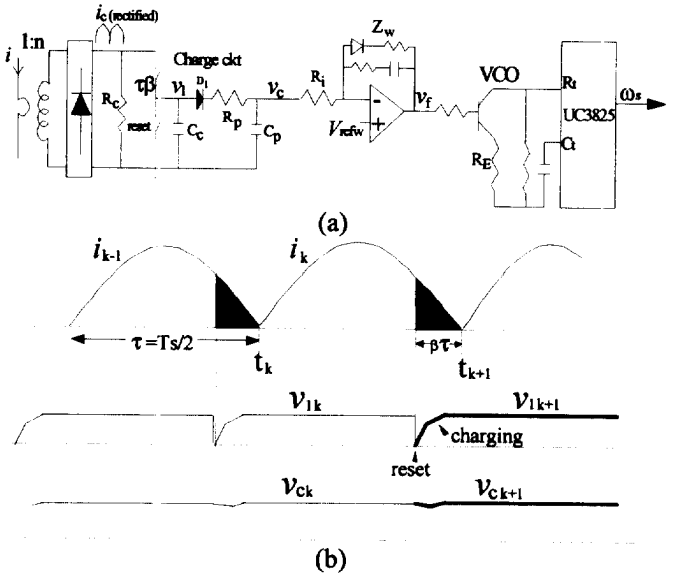

Fig. 6 Frequency control: (a) circuit implementation, (b) charge circuit waveforms.

1) Solving for v_1, and v_c as a function of i_p: Figure 7 shows the equivalent circuit during the period $\tau\beta$. During this time, capacitor C_c is charged with i to produce voltage v_1. Diode D_1 is assumed to be off during the charging of C_c, but even if D_1 turns on some time during the charging of C_1, the circuit of Fig. 7 is still a good approximation, since $R_p // R_i >> R_c$ and $C_c >> C_p$.

Thus, applying Kirchhoff's current law to the circuit in Fig. 7 results in

$$C_c \frac{dv_1}{dt} = \frac{i}{n} - \frac{v_1}{R_c}. \tag{29}$$

Equation.(29) provides the solution for v_1 during the time $\tau\beta$; however, from Fig. 6 (b) we see that v_1 remains constant during a period τ until it is reset. Hence, using (29) we can find the value reached by v_1 at t_{k+1} (k=0,1,2...∞.), and assume that it will remain at this value until it is reset. There is a slight decrease of v_1 during the non-charging time due to resistor $R_p // R_i$, and its effect will be included later. From (29) and Fig. 6(b) we can observe that $v_{1(k+1)}$ is a function of i_k, as well as $\tau_k\beta_k$. Since we are studying perturbations at frequencies lower than the resonant frequency, we can assume that v_{1k}, i_k, and $\tau_k\beta_k$ remain constant during each k period.

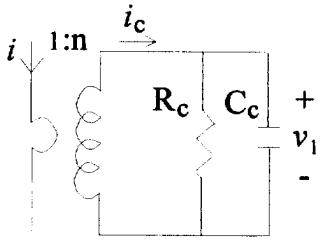

Fig. 7 Equivalent charge circuit during $\tau\beta$.

The expression for $v_{1(k+1)}$ is then

$$v_{1(k+1)}=\int_{t_{k+1}-\beta_k\tau_k}^{t_{k+1}}\frac{e^{-a(t_{k+1}-s)}}{nC_c}\left|i_k(s)\right|ds\,, \qquad (30)$$

where $i_k(s)$ can be replaced by (4). The solution of (30) is

$$v_{1(k+1)}= \left|\frac{i_{sk}\omega_{sk}-i_{ck}a-e^{-\beta_k\tau_k a}\left[(i_{sk}a+i_{ck}\omega_{sk})\sin\beta_k\pi+(i_{sk}\omega_{sk}-i_{ck}a)\cos\beta_k\pi\right]}{nC_c\left(a^2+\omega_{sk}^2\right)}\right| \qquad (31)$$

where a and β_k are defined in appendix A.

Equation (31) can be perturbed and linearized with a mathematical software package such as MapleV or Mathematica. The linearized solution around the operating point [V_g, D, W_S, Q], is

$$\hat{v}_{1(k+1)}=A\left(E_{\omega\omega}\hat{\omega}_{sk}+E_{d\omega}\hat{d}_k+H_{is\omega}\hat{i}_{sk}+H_{ic\omega}\hat{i}_{ck}\right) \qquad (32)$$

where A, $E_{\omega\omega}$, $E_{d\omega}$, $H_{is\omega}$, $H_{ic\omega}$ are gains that depend on the operating points; their definitions are given in appendix A. The selection of "E" or "H" depends on whether the multiplying variable is a current-controlled voltage source or a voltage-controlled voltage source. This will become clear in section *E*, where the circuit model is derived.

Equation (32) shows a discrete relationship between the output voltage $v_{1(k+1)}$ and ω_{sk}, d_k, i_{sk}, and i_{ck}. Hence, a z-transformation can be applied [Tang] as follows:

$$z\hat{v}_1(z)=A\left(E_{\omega\omega}\hat{\omega}_s(z)+E_{d\omega}\hat{d}(z)+H_{is\omega}\hat{i}_s(z)+H_{ic\omega}\hat{i}_c(z)\right). \qquad (33)$$

Equation (33) can now be transformed into a sampled continuous time expression such as [Franklin]

$$\hat{v}_1(s)=\frac{s\tau}{(e^{s\tau}-1)}A\left(E_{\omega\omega}\hat{\omega}_s(s)+E_{d\omega}\hat{d}(s)+H_{is\omega}\hat{i}_s(s)+H_{ic\omega}\hat{i}_c(s)\right). \qquad (34)$$

The sample and hold expression outside the brackets in (34) has been approximated to a power series expansions; an example of a second order polynomial is given in [Ridley].

Having v_1, we now can solve for v_c and take into account the slight discharging caused by (R_p // R_i). Diode D_1 and the (R_p // R_i)C_p circuit in Fig. 6(b) do not let v_c discharge during the resetting and charging of v_1. The disadvantage is that (R_p // R_i)C_p contributes a pole to the system; therefore, it should be designed as a high frequency pole so that it would not affect the closed loop performance. Hence, $\hat{v}_c$ is

$$\hat{v}_c(s)=\frac{\hat{v}_1(s)}{(s+b)R_pC_p}\,, \qquad (35)$$

where

$$b=\frac{1}{(R_p\|R_i)C_p}\,. \qquad (36)$$

2) Solving for v_f after the compensation circuit: the relationship between v_f(s) and v_c(s) is found from Fig. 6(a). This solution is perturbed and linearized to give,

$$\hat{v}_f(s)=-\hat{v}_c(s)\frac{Z_w}{R_i}=-\hat{v}_c(s)G_w(s)\,. \qquad (37)$$

3) Expressing ω_s as a function of v_f using the VCO linear relationship: in [Jovanovic] an equation that shows the linear relationship between ω_s and v_f is given. The small signal solution for $\hat{\omega}_s$ is then,

$$\hat{\omega}_s(s)=K_{VCO}\hat{v}_f(s)\,. \qquad (38)$$

where K_{VCO} can be measured experimentally, or it can be approximated by the equation given in [Jovanovic].

The final solution for $\hat{\omega}_s$ is obtained by replacing (34)-(37) on (38), that is,

$$\hat{\omega}_s(s)=-G_e(s)G_w(s)A\left(E_{\omega\omega}\hat{\omega}_s(s)+E_{d\omega}\hat{d}(s)+H_{is\omega}\hat{i}_s(s)+H_{ic\omega}\hat{i}_c(s)\right), \qquad (39)$$

where

$$G_e(s)=\frac{s\tau}{(e^{s\tau}-1)}\frac{K_{VCO}}{(s+b)R_pC_p}\,, \qquad (40)$$

and

$$G_w(s)=\frac{Z_w(s)}{R_i}\,. \qquad (41)$$

D. Error-Amplifier Compensation

The compensation scheme selected for each of the control loops is just an example among many possible implementations. The compensation used for the power regulation loop is represented by (25) and it is shown in Fig 5. This compensation network provides: (a) a pole at zero (an integrator) for high DC gain, (b) a zero at low frequency, to increase the loop gain bandwidth, and (c) a high frequency pole. The performance of this compensation network will be discussed in part IV.

The compensation used for the frequency control loop is represented by (41), and its implementation is shown in Fig. 6(a). A diode has been placed in the op amp feedback path, in order to have two different compensation schemes, depending on the error sign. The purpose of this nonlinear compensation is to have fast response, regardless of saturation, when the error is positive, and to prevent saturation, although penalizing the response time, when the error is negative. Ideally, the diode will be *off* when v_c is lower than v_{refw}; hence, the error will be positive. The positive-error compensation includes a pole at zero frequency, for high DC gain, and a zero at low frequency. Positive error means that the inverter frequency is too low and that ZVS might be lost. Thus, it is acceptable to have the op amp saturated with a positive output to quickly regain ZVS. On the other hand, the diode will be *on* when v_c is greater than v_{refw}; thus, the error will be negative. In this case, the pole is not at zero, but moves to a slightly higher frequency, thus decreasing the high DC gain.. The negative error compensation will not saturate the op amp as quickly as in the positive case. A thorough analysis of the closed-loop performance of this nonlinear compensation is not simple, especially when analyzing its behavior during transient response. Transient behavior analysis is beyond the scope of this paper. Experimental loop-gain curves will be given in part IV. It will be shown that this compensation behaves satisfactorily; however, other combinations of pole and zero placements should be tested to further improve the gain and the bandwidth.

E. Complete Small-Signal Model

The complete small-signal model is shown in Fig. 8. This model was obtained from (14)-(17), (24), (28), and (39).

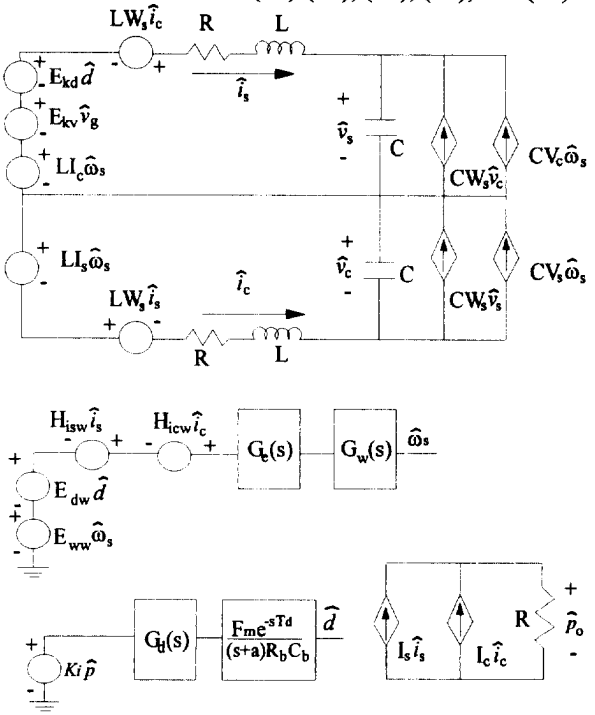

Fig. 8 Small-signal model includes power-stage, frequency control loop and phase-shift control loop.

The small-signal model as shown in Fig. 8 can now be implemented using PSPICE, MATLAB or similar simulation software, to obtain the frequency response of the system.

IV. Experimental Verifications

Figure 9 shows the experimental and analytical frequency loop-gain curves with the power regulation loop open. The operating point and the PSPICE program are given in appendix B. From these curves it can be seen that the frequency loop is stable. However, its gain is relatively low as well as the crossover frequency. Modifications to the compensation circuitry can be made to increase the gain and crossover frequency. Though, as explained in section III D, the DC gain can not be large when the error is negative to prevent saturation in the negative direction. Additional, analysis of the frequency loop-gain at different operating points show that the gain decreases as the load resistance increases, the load resistance increases during the heating cycle. Therefore, the compensation for this loop should be design for the highest load resistance point.

Figure 10 shows the experimental and analytical power regulation loop-gain curves with the frequency loop closed. The operating points of Fig. 10 curves are similar to that of Fig. 9 except for: f_s=554 kHz; V_g=103 V; D=0.62. The compensation used for the power regulation loop satisfactorily provides high DC gain and large phase margin.

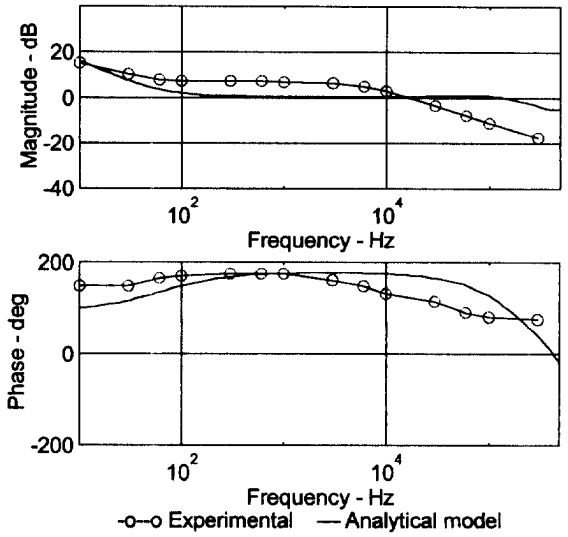

Fig. 9 Frequency control loop-gain.

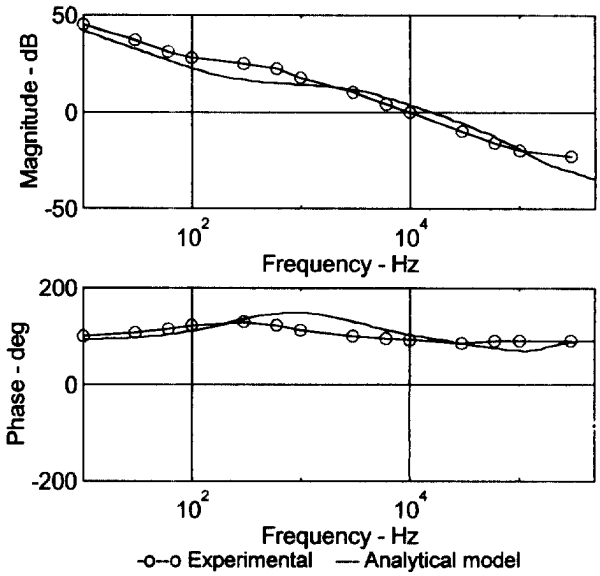

Fig. 10 Power regulation loop-gain.

V. Conclusions

The complete closed-loop small-signal model for a phase-shift-controlled series-resonant inverter used for induction heating was obtained using the extended describing function method. The model predictions were verified with experimental data measured from a lab prototype

The small signal model proved to be a useful tool to analyze the performance of the two control loops: the phase-shift control loop and the frequency control loop. In particular the frequency loop-gain analysis showed that improvements could be made to increase its gain and its bandwidth. This model will be used for further closed-loop performance studies at various load operating points, which generally occur during the heating cycle of an induction heating system.

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APPENDIX A

Operating Points:

$$I_s=\frac{V_g W_s^2 C^2 R}{\Delta},\quad I_c=\frac{V_g W_s C\,(1-W_s^2 LC)}{\Delta},\quad V_s=\frac{V_g(1-W_s^2 LC)}{\Delta},$$

$$V_c=\frac{V_g W_s CR}{\Delta},\quad \Delta=W_s^4C^2L^2-2W_s^2CL+1+W_s^2C^2R^2\,. \qquad \text{(A1)}$$

Power Stage Small-Signal Model Constants

$$E_{kd}=\frac{2V_g}{L}\cos(\frac{\pi}{2}D),\quad E_{kv}=\frac{4}{\pi L}\sin(\frac{\pi}{2}D) \qquad \text{(A2)}$$

Frequency Control Constants:

From (31) let

$$V_{1\_sign}=\frac{I_sW_s-I_ca-e^{-a\frac{B}{W_s}}\left[(I_sa+I_cW_s)\sin B+(I_sW_s-I_ca)\cos B\right]}{nC_c\left(a^2+W_s^2\right)}$$

then,

$$A=\begin{cases}1\,,\ when\ \left(V_{1\_sign}\right)>0\\ -1\,,\ when\ \left(V_{1\_sign}\right)<0\\ Not\ defined\ when\ \left(V_{1\_sign}\right)=0\end{cases} \qquad \text{(A3)}$$

$$B=\beta\pi=-\arctan(\frac{I_c}{I_s})-\frac{\pi}{2}(1-D) \qquad \text{(A4)}$$

$$H_{is\omega}=KK\left[\frac{I_ce^{-a\frac{B}{W_s}}}{(I_s^2+I_c^2)}\left[\frac{a}{W_s}H1+H2\right]-e^{-a\frac{B}{W_s}}\left(a\sin B+W_s\cos B\right)+W_s\right] \qquad \text{(A5)}$$

$$H_{ic\omega}=KK\left[\frac{I_se^{-a\frac{B}{W_s}}}{(I_s^2+I_c^2)}\left[-\frac{a}{W_s}H1-H2\right]+e^{-a\frac{B}{W_s}}\left(-W_s\sin B+a\cos B\right)-a\right] \qquad \text{(A6)}$$

$$E_{d\omega}=e^{-a\frac{B}{W_s}}KK\left[\frac{a\pi}{2W_s}H1+\frac{\pi}{2}H2\right] \qquad \text{(A7)}$$

$$E_{a\omega}=KK\left[I_s-e^{-a\frac{B}{W_s}}\left(H1(\frac{aB}{W_s^2}-\frac{2W_s}{a^2+W_s^2})+I_c\sin B+I_s\cos B\right)-\frac{2W_s}{a^2+W_s^2}(I_sW_s-I_ca)\right] \qquad \text{(A8)}$$

$$H1=\left((I_sa+I_cW_s)\sin B+(I_sW_s-I_ca)\cos B\right) \qquad \text{(A9)}$$

$$H2=\left(-(I_sa+I_cW_s)\cos B+(I_sW_s-I_ca)\sin B\right) \qquad \text{(A10)}$$

$$KK=\frac{1}{nC_c(a^2+W_s^2)},\quad a=\frac{1}{R_cC_c}, \qquad \text{(A11)}$$

APPENDIX B

Pspice frequency loop-gain implementation:

```
SRI-PSC frequency loop gain, Small Signal Model
* Circuit parameters  Q=2.2  L=6.77uH   C=19.3nF  N=4   R=10
* Operating Point     Vg=136 Fs=496 khz  D=0.97
**********************************
vg 20 0 ac 0
rg 20 0 1k
vd 50 0 ac 0
rd 50 0 1k
**********************************
* The upper part of the resonant tank
es   1  0  70  0  -.04263m
ekv  2  1  20  0  1.272
ekd  3  2  50  0  12.813
vpis  3  4  dc  0
hzs  5  4  vpic  21.0134
rs   5  6  10
ls   6  7  6.77u
cs   7  0  19.3n
gjs  0  7  8  0  0.0599
gws  0  7  70  0  -4.696u
**************************************
* The lower part of the resonant tank
ec    0  13  70 0 0.09868m
vpic  13  12  dc 0
hzc   12 10  vpis  21.0134
rc    10  9  10
lc    9  8  6.77u
cc    8  0  19.3n
gjc   8  0  7  0  0.0599
gwc   8  0  70  0  -2.029u
************************
* Opamp frequency loop
eopf  70  0  0  80  1000k
ropf  70  0  1000k
r4    85  80  5.6k
*r5    80  70  120k
r6    80  86  27k
c6    86  70  0.10u
* He(s) (The gain Kvco was included in His, Hic, Ew, Ed)
eGe   85  0  LAPLACE  {v(90)} = {13.77*s/((exp(s*1e-6)-1)*(s+14.077e6))}
eww   31  0  70  0  -0.0168
edw   32  31  50  0  287.22e3
hisw  33  32  vpis  -3.4913e3
hicw  84  33  vpic  -16.5e3
************************
* The injected signal
vcl   90  84   ac 1
rge   90  0   1000k
**********************************
*The loop gain measurement is V(84)/V(90)
* Vdb(84)/Vdb(90)= Vdb(84)-Vdb(90) Vp(V(84)/V(90))=Vp(84)-vp(90)
.print ac vdb(90) vdb(84) vp(90) vp(84)
****************************************
.ac dec 20 10 500k
.probe
.end
```