L6997

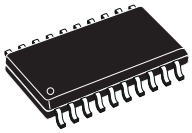
STEP DOWN CONTROLLER FOR LOW VOLTAGE OPERATIONS

FEATURES

- FROM 3V TO 5.5V V_{CC} RANGE.
- MINIMUM OUTPUT VOLTAGE AS LOW AS 0.6V.
- 1V TO 28V INPUT VOLTAGE RANGE.
- CONSTANT ON TIME TOPOLOGY ALLOWS. OPERATION WITH VERYLOW AND HIGH DUTY CYCLES.
- VERY FAST LOAD TRANSIENTS.
- 0.6V, ±1% VREF.
- SELECTABLE SINKING MODE.
- LOSSLESS CURRENT LIMIT, AVAILABLE ALSO IN SINKING MODE
- REMOTE SENSING.
- OVP,UVP LATCHED PROTECTIONS.
- 600µA TYP QUIESCENT CURRENT.
- POWER GOOD AND OVP SIGNALS.
- PULSE SKIPPING AT LIGTH LOADS.
- 94% EFFICIENCY FROM 3.3V TO 2.5V.

APPLICATIONS

- NETWORKING.
- DC/DC MODULES.
- DISTRIBUTED POWER.
- MOBILE APPLICATIONS.
- CHIP SET, CPU, DSP AND MEMORIES SUPPLY.



TSSOP20
ORDERING NUMBERS: L6997D
L6997DTR

DESCRIPTION

The device is a high efficient solution for networking dc/dc modules and mobile application compatible with 3.3V bus and 5V bus.

It's able to regulate an output voltage as low as 0.6V.

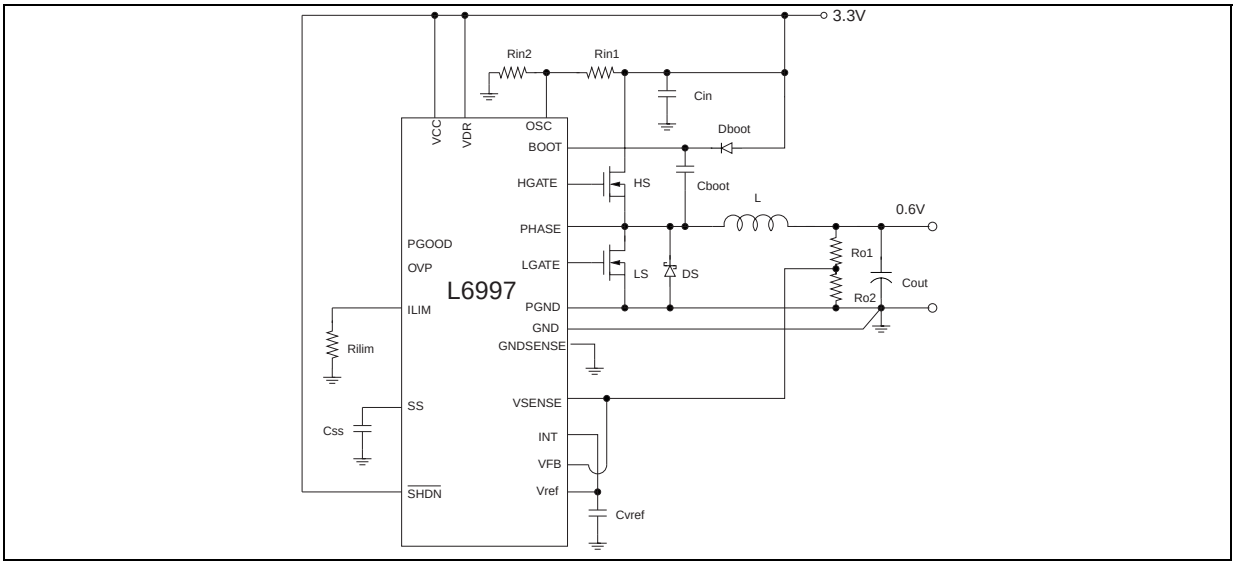
The constant on time topology assures fast load transient response. The embedded voltage feed-forward provides nearly constant switching frequency operation.

An integrator can be introduced in the control loop to reduce the static output voltage error.

The remote sensing improves the static and dynamic regulation, recovering the wires voltage drop.

Pulse skipping technique reduces power consumption at light loads. Drivers current capability allows output currents in excess of 20A.

MINIMUM COMPONENT COUNT APPLICATION



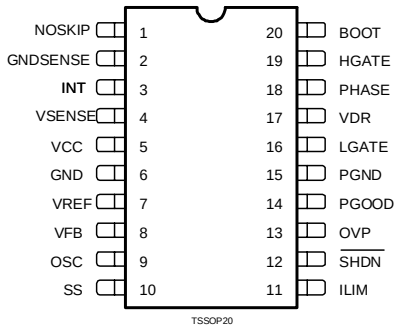
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	V_{CC} to GND	-0.3 to 6	V
V_{DR}	V_{DR} to GND	-0.3 to 6	V
	HGATE and BOOT, to PHASE	-0.3 to 6	V
	HGATE and BOOT, to PGND	-0.3 to 36	V
V_{PHASE}	PHASE	-0.3-to 30	V
	LGATE to PGND	-0.3 to V_{DR}+0.3	V
	ILIM, VFB, VSENSE, NOSKIP, SHDN, PGOOD, OVP, VREF, INT, GND_{SENSE} to GND	-0.3 to V_{CC}+0.3	V
P_{tot}	Power dissipation at T_{amb} = 25°C	1	W
T_{stg}	Storage temperature range	-40 to 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient	125	°C/W
T_j	Junction operating temperature range	-40 to 125	°C

PIN CONNECTION (Top View)



PIN FUNCTION

N°	Name	Description
1	NOSKIP	Connect to V_{CC} to force continuous conduction mode and sink mode.
2	GNDSENSE	Remote ground sensing pin
3	INT	Integrator output. Short this pin to VFB pin and connect it via a capacitor to V_{OUT} to insert the integrator in the control loop. If the integrator is not used, short this pin to VREF.
4	VSENSE	This pin must be connected to the remote output voltage to detect overvoltage and undervoltage conditions and to provide integrator feedback input.
5	V_{CC}	IC Supply Voltage.
6	GND	Signal ground
7	VREF	0.6V voltage reference. Connect max. a 10nF ceramic capacitor between this pin and ground. This pin is capable to source or sink up to 250uA

PIN FUNCTION (continued)

N°	Name	Description
8	VFB	PWM comparator feedback input. Short this pin to INT pin when using the integrator function, or to VSENSE pin without integrator.
9	OSC	Connect this pin to the input voltage through a voltage divider in order to provide the feed-forward function. It cannot be left floating.
10	SS	Soft start pin. A 5µA constant current charges an external capacitor which value sets the soft-start time.
11	ILIM	An external resistor connected between this pin and GND sets the current limit threshold.
12	SHDN	Shutdown. When connected to GND the device and the drivers are OFF. It cannot be left floating.
13	OVP	Open drain output. During the over voltage condition it is pulled up by an external resistor.
14	PGOOD	Open drain output. During the soft start and in case of output voltage fault it is low. It is pulled up by external resistor.
15	PGND	Low Side driver ground.
16	LGATE	Low Side driver output.
17	V_{DR}	Low Side driver supply.
18	PHASE	Return path of the High Side driver.
19	HGATE	High side MOSFETS driver output.
20	BOOT	Bootstrap capacitor pin. High Side driver is supplied through this pin.

ELECTRICAL CHARACTERISTICS

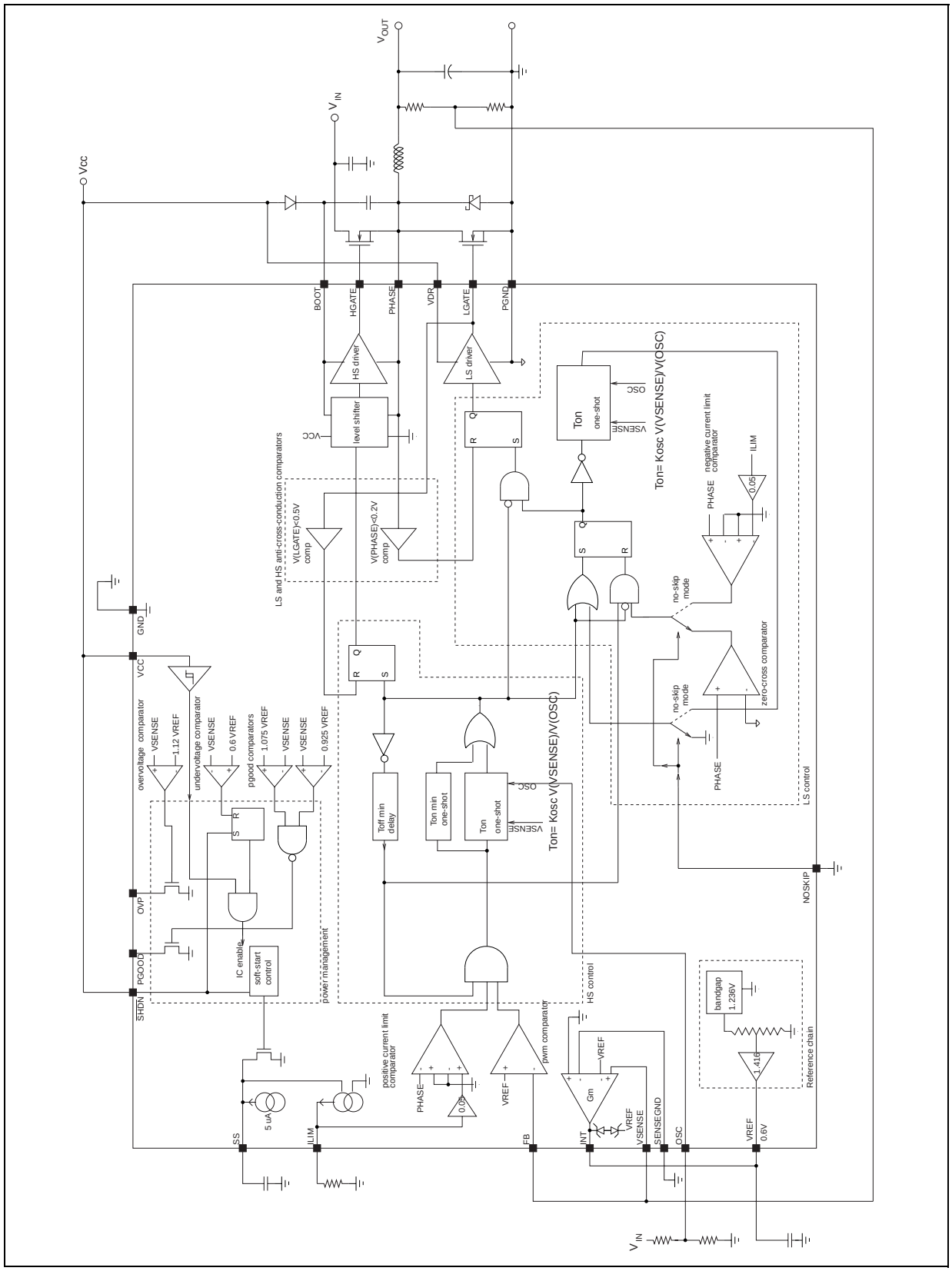
(V_{CC} = V_{DR} = 3.3V; T_{amb} = 0°C to 85°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SUPPLY SECTION						
Vin	Input voltage range	Vout=Vref Fsw=110Khz Iout=1A	1		28	V
V_{CC}, V_{DR}			3		5.5	V
V_{CC}	Turn-onvoltage		2.86		2.97	V
	Turn-off voltage		2.75		2.9	V
	Hysteresis			90		mV
IqV_{DR}	Quiescent Current Drivers	VFB > VREF		7	20	µA
IqVcc	Device Quiescent current	VFB > VREF		400	600	µA
SHUTDOWN SECTION						
SHDN	Device On		1.2			V
	Device Off				0.6	V
$I_{SH}V_{DR}$	Drivers shutdown current	SHDN to GND			5	µA
$I_{SH}V_{CC}$	Devices shutdown current	SHDN to GND		1	15	µA
SOFT START SECTION						
I_{SS}	Soft Start current	V_{SS} = 0.4V	4		6	µA
	Active Soft start and voltage		300	400	500	mV
CURRENT LIMIT AND ZERO CURRENT COMPARATOR						
	ILIM input bias current	R_{ILIM} = 2KΩ to 200KΩ	4.6	5	5.4	µA
	Zero Crossing Comparator offset Phase-gnd		-2		2	mV
DK_{ILIM}	Current limit factor		1.6	1.8	2	µA

ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = V_{DR} = 3.3V; T_{amb} = 0°C to 85°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ON TIME						
Ton	On time duration	V_{REF}=$V_{SENSE\ OSC}$=125mV	720	800	880	ns
		V_{REF}=$V_{SENSE\ OSC}$=250mV	370	420	470	ns
		V_{REF}=$V_{SENSE\ OSC}$=500mV	210	240	270	ns
OFF TIME						
T_{OFFMIN}	Minimum off time				600	ns
	K_{OSC}/T_{OFFMIN}	OSC=250mV		0.3	0.33	
VOLTAGE REFERENCE						
VREF	Voltage Accuracy	0µA < I_{REF} < 100µA	0.594	0.6	0.606	V
PWM COMPARATOR						
	Input voltage offset		-2		+2	mV
I_{FB}	Input Bias Current			20		nA
INTEGRATOR						
INT	Over Voltage Clamp	V_{SENSE} = V_{CC}	0.62	0.75	0.88	V
INT	Under Voltage Clamp	V_{SENSE} = GND	0.45	0.55	0.65	V
	Integrator Input Offset Voltage V_{SENSE}-V_{REF}		-4		-4	mV
I_{VSENSE}	Input Bias Current			20		nA
GATE DRIVERS						
	High side rise time	V_{DR}=3.3V; C=7nF HGATE - PHASE from 1 to 3V		50	90	ns
	High side fall time			50	100	ns
	Low side rise time	V_{DR}=3.3V; C=14nF LGATE from 1 to 3V		50	90	ns
	Low side fall time			50	90	ns
P_{GOOD} UVP/OVP PROTECTIONS						
OVP	Over voltage threshold	with respect to V_{REF}	118	121	124	%
UVP	Under voltage threshold		67	70	73	%
PGOOD	Upper threshold (V_{SENSE}-V_{REF})	V_{SENSE} rising	110	112	116	%
PGOOD	Lower threshold (V_{SENSE}-V_{REF})	V_{SENSE} falling	85	88	91	%
V_{PGOOD}		I_{Sink}=2mA		0.2	0.4	V

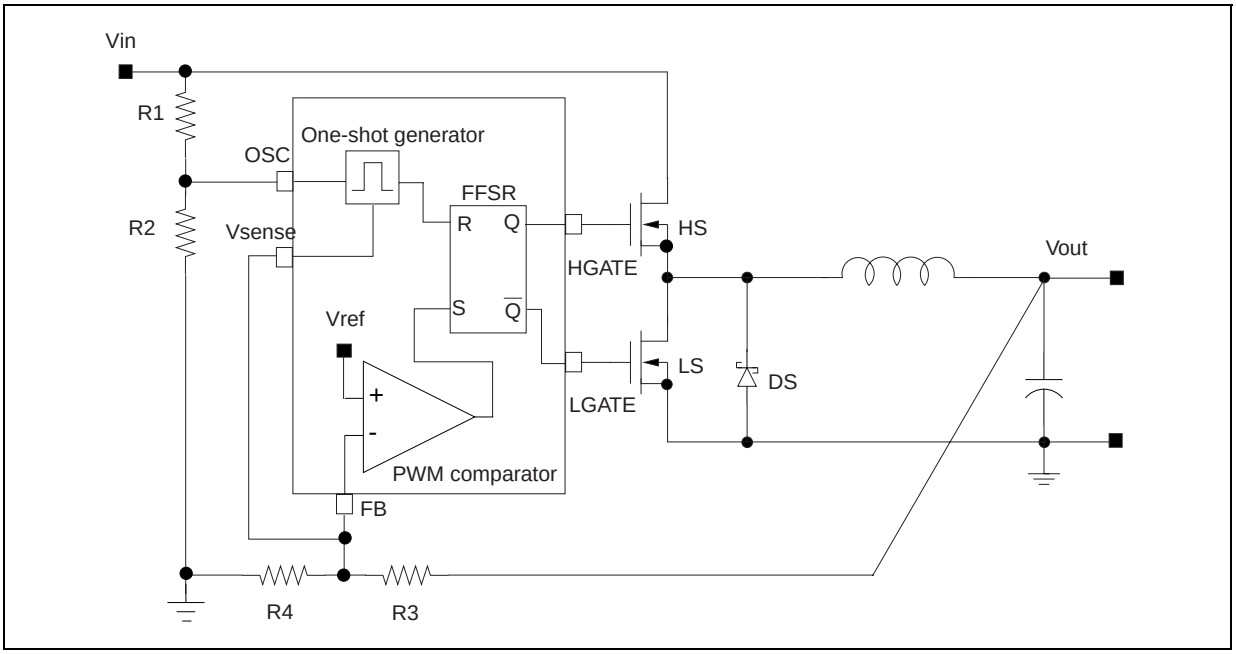
Figure 1. Functional & Block Diagram



1 DEVICE DESCRIPTION

1.1 Constant On Time PWM topology

Figure 2. Loop block schematic diagram



The device implements a Constant On Time control scheme, where the Ton is the high side MOSFET on time duration forced by the one-shot generator. The on time is directly proportional to VSENSE pin voltage and inverse to OSC pin voltage as in Eq1:

$$\text{Eq 1} \qquad T_{ON} = K_{OSC}\frac{V_{SENSE}}{V_{OSC}} + \tau$$

where K_{OSC} = 250ns and τ is the internal propagation delay time (typ. 70ns). The system imposes in steady state a minimum on time corresponding to V_{OSC} = 1V. In fact if the V_{OSC} voltage increases above 1V the corresponding Ton will not decrease. Connecting the OSC pin to a voltage partition from V_{IN} to GND, it allows a steady-state switching frequency F_{SW} independent of V_{IN}. It results:

$$\text{Eq 2} \qquad f_{SW} = \frac{V_{OUT}}{V_{IN}}\frac{1}{T_{ON}} = \frac{\alpha_{OSC}}{\alpha_{OUT}}\frac{1}{K_{OSC}} \rightarrow \alpha_{OSC} = f_{SW}K_{OSC}\alpha_{OUT}$$

where

$$\text{Eq 3} \qquad \alpha_{OSC} = \frac{V_{OSC}}{V_{IN}} = \frac{R_2}{R_2 + R_1}$$

$$\text{Eq 4} \qquad \alpha_{OUT} = \frac{V_{FB}}{V_{OUT}} = \frac{R_4}{R_3 + R_4}$$

The above equations allow setting the frequency divider ratio α_{OSC} once output voltage has been set; note that such equations hold only if V_{OSC}<1V. Further the Eq2 shows how the system has a switching frequency ideally independent from the input voltage. The delay introduces a light dependence from V_{IN}. A minimum off-time constrain of about 500ns is introduced in order to assure the boot capacitor charge and to limit the switching fre-

quency after a load transient as well as to mask PWM comparator output against noise and spikes.

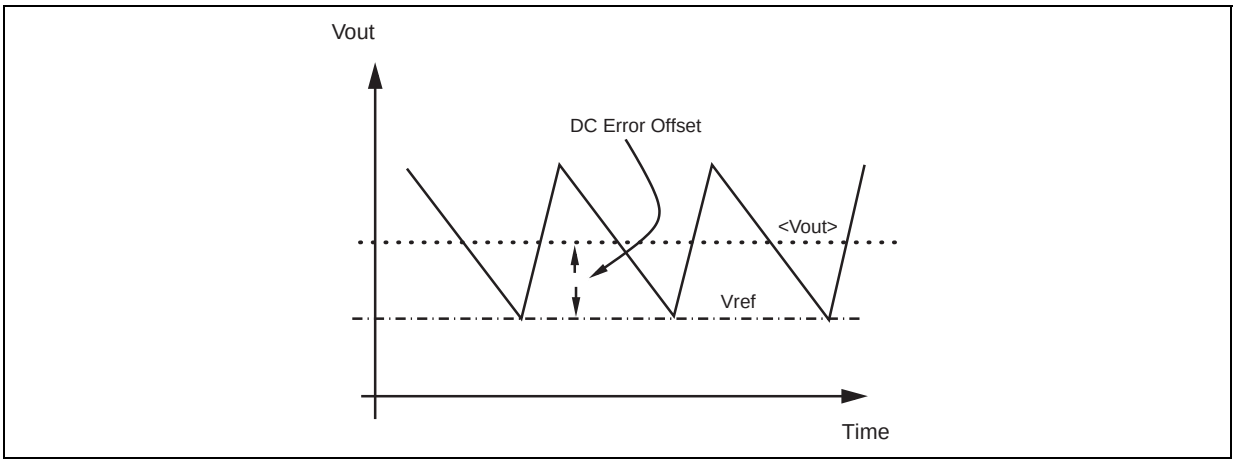
The system has not an internal clock, because this is a hysteretic controller, so the turn on pulse will start if three conditions are met contemporarily: the FB pin voltage is lower than the reference voltage, the minimum off time is passed and the current limit comparator is not triggered (i.e. the inductor current is below the current limit value). The voltage on the OSC pin must range between 50mV and 1V to ensure the system linearity.

1.2 Closing the loop

The loop is closed connecting the output voltage (or the output divider middle point) to the FB pin. The FB pin is linked internally to the comparator negative pin and the positive pin is connected to the reference voltage (0.6V Typ.) as in Figure 2. When the FB goes lower than the reference voltage, the PWM comparator output goes high and sets the flip-flop output, turning on the high side MOSFET. This condition is latched to avoid noise spike. After the on-time (calculated as described in the previous section) the system resets the flip-flop and then turns off the high side MOSFET and turns on the low side MOSFET. Internally the device has more complex logic than a flip-flop to manage the transition in correct way. For more details refers to the Figure 1.

The voltage drop along ground and supply metals connecting output capacitor to the load is a source of DC error. Further the system regulates the output voltage valley value not the average, as in the Figure 3 is shown. So the voltage ripple on the output capacitor is a source of DC static error (as the PCB traces). To compensate the DC errors, an integrator network must be introduced in the control loop, by connecting the output voltage to the INT pin through a capacitor and the FB pin to the INT pin directly as in Figure 4. The internal integrator amplifier with the external capacitor C_{INT1} introduces a DC pole in the control loop. C_{INT1} also provides an AC path for output ripple.

Figure 3. Valley regulation



The integrator amplifier generates a current, proportional to the DC errors, that increases the output capacitance voltage in order to compensate the total static errors. A voltage clamper within the device forces INT pin voltage ranges from V_{REF}-50mV, V_{REF}+150mV. This is useful to avoid or smooth output voltage overshoot during a load transient. Also, this means that the integrator is capable of recovering output error due to ripple when its peak-to-peak amplitude is less than 150mV in steady state.

In case of the ripple amplitude is larger than 150mV, a capacitor C_{INT2} can be connected between INT pin and ground to reduce ripple amplitude at INT pin, otherwise the integrator can operate out of its linear range. Choose C_{INT1} according to the following equation:

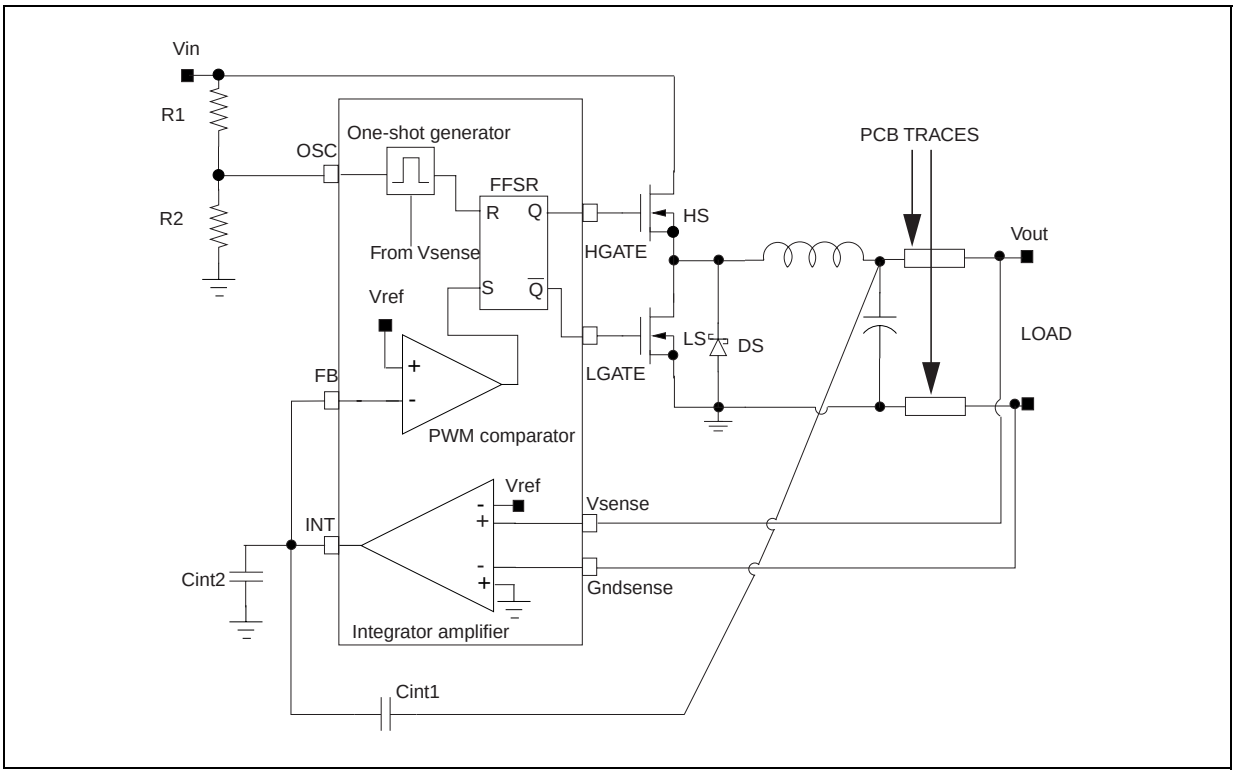
Eq 5 $$C_{INT1} = \frac{g_{INT} \cdot \alpha_{OUT}}{2 \cdot \pi \cdot F_u}$$

where GINT=50 µs is the integrator transconductance, α_{OUT} is the output divider ratio given from Eq4 and F_U is the close loop bandwidth. This equation also holds if C_{INT2} is connected between INT pin and ground. C_{INT2} is given by:

Eq 6 $$\frac{C_{INT2}}{C_{INT1}} = \frac{\Delta V_{OUT}}{V_{INT}}$$

Where ΔV_{OUT} is the output ripple and ΔV_{INT} is the ripple wanted at the INT pin (100mV typ).

Figure 4. Integrator loop block diagram



Respect to a traditional PWM controller, that has an internal oscillator setting the switching frequency, in a hysteretic system the frequency can change with some parameters (input voltage, output current). In L6997 is implemented the voltage feed-forward circuit that allows constant switching frequency during steady-sate operation with the input voltage variation. There are many factors affecting switching frequency accuracy in steady-state operation. Some of these are internal as dead times, which depend on high side MOSFET driver. Others related to the external components as high side MOSFET gate charge and gate resistance, voltage drops on supply and ground rails, low side and high side RDSON and inductor parasitic resistance.

During a positive load transient, (the output current increases), the converter switches at its maximum frequency (the period is TON+TOFFmin) to recover the output voltage drop. During a negative load transient, (the output current decreases), the device stops to switch (high side MOSFET remains off).

1.3 Transition from PWM to PFM/PSK

To achieve high efficiency at light load conditions, PFM mode is provided. The PFM mode differs from the PWM mode essentially for the off section; the on section is the same. In PFM after a turn-on cycle the system turns-on the low side MOSFET, until the inductor current reaches the zero A value, when the zero-crossing comparator turns off the low side MOSFET. In this way the energy stored in the output capacitor will not flow to ground, through the low side MOSFET, but it will flow to the load. In PWM mode, after a turn on cycle, the system keeps the low side MOSFET on until the next turn-on cycle, so the energy stored in the output capacitor will flow through the low side MOSFET to ground. The PFM mode is naturally implemented in hysteretic controller, in fact in PFM mode the system reads the output voltage with a comparator and then turns on the high side MOSFET when the output voltage goes down a reference value. The device works in discontinuous mode at light load and in continuous mode at high load. The transition from PFM to PWM occurs when load current is around half the inductor current ripple. This threshold value depends on V_{IN}, L, and V_{OUT}. Note that the higher the in-

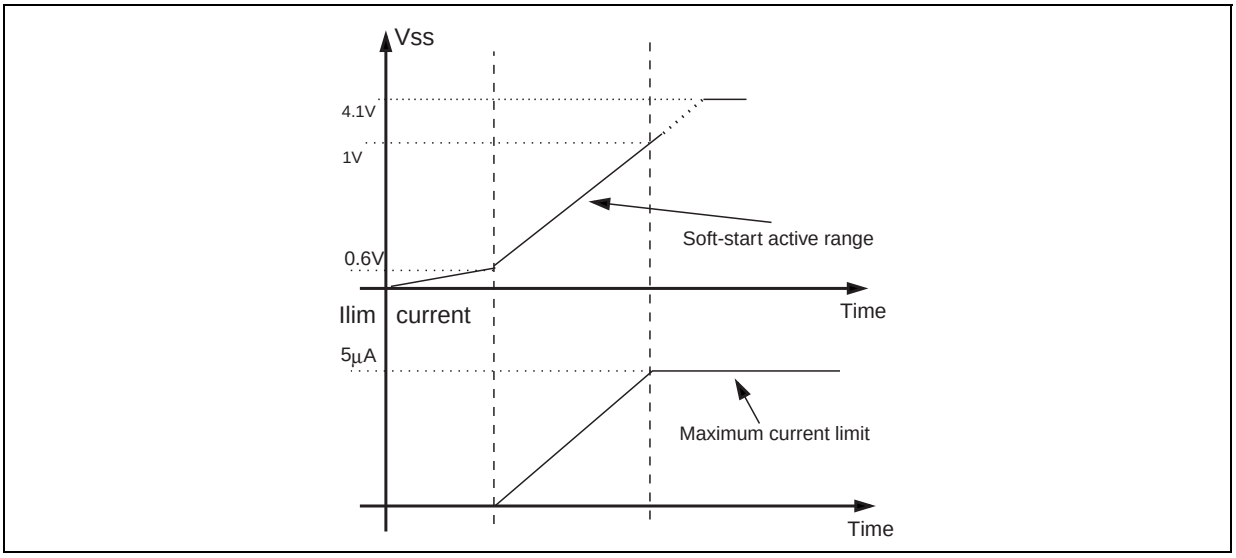
ductor value is, the smaller the threshold is. On the other hand, the bigger the inductor value is, the slower the transient response is. In PFM mode the frequency changes, with the output current changing, more than in PWM mode; in fact if the output current increase, the output voltage decreases more quickly; so the successive turn-on arrives before, increasing the switching frequency. The PFM waveforms may appear more noisy and asynchronous than normal operation, but this is normal behaviour mainly due to the very low load. If the PFM is not compatible with the application it can be disabled connecting to V_{CC} the NOSKIP pin.

1.4 Softstart

If the supply voltages are already applied, the SHDN pin gives the start-up. The system starts with the high side MOSFET and the low side MOSFET off (high impedance mode). After the SHDN pin is turned on the SS pin voltage begins to increase and the system starts to switch. The softstart is realized by gradually increasing the current limit threshold to avoid output overvoltage. The active soft start range for the V_{SS} voltage (where the output current limit increase linearly) starts from 0.6V to 1V. In this range an internal current source (5µA Typ) charges the capacitor on the SS pin; the reference current (for the current limit comparator) forced through ILIM pin is proportional to SS pin voltage and it saturates at 5µA (Typ.) when SS voltage is close to 1V and the maximum current limit is active. Output protections OVP & UVP are disabled until the SS pin voltage reaches 1V (see figure 5).

Once the SS pin voltage reaches the 1V value, the voltage on SS pin doesn't impact the system operation anymore. If the SHDN pin is turned on before the supplies, the correct start-up sequence is the following: first turn-on the power section and after the logic section (V_{CC} pin).

Figure 5. Soft -Start Diagram



Because the system implements the soft start controlling the inductor current, the soft start capacitor selection is function of the output capacitance, the current limit and the soft start active range (ΔV_{SS}).

In order to select the softstart capacitor it must be imposed that the output voltage reaches the final value before the soft start voltage reaches the under voltage value (1V). In other words the output voltage charging time has to be lower than the uvp time.

The UVP time is given by:

$$\text{Eq 7} \qquad T_{uvp}(C_{SS}) = \frac{V_{uvp}}{Iss} \cdot C_{SS}$$

In order to calculate the output volatge chargin time it should be calculated, before, the output volatrge function versus time. This function can be calculated from the inductor current function; the inductor current function can

be supposed linear function of the time.

Eq 8 $$I_L(t,C_{SS}) = \frac{(R_{ilim}/R_{dson} \cdot K_C \cdot I_{SS} \cdot t)}{(\Delta V_{SS} \cdot C_{SS})}$$

so the output voltage is given by:

Eq 9 $$V_{out}(t,C_{SS}) = \frac{Q(t,C_{SS})}{C_{out}} = \frac{(R_{ilim}/R_{dson} \cdot K_C \cdot I_{SS} \cdot t^2)}{(C_{out} \cdot \Delta V_{SS} \cdot C_{SS} \cdot 2)}$$

calling V_{out} as the V_{out} final value, the output charging time can be estimated as:

Eq 10 $$I_{out}(C_{SS}) = \left[\frac{(V_{out} \cdot C_{out} \cdot \Delta V_{SS} \cdot C_{SS} \cdot 2)}{(R_{ilim}/R_{dson} \cdot K_C \cdot I_{SS})}\right]^{0.5}$$

the minimum C_{SS} value is given imposing this condition:

Eq 11 $T_{out} = T_{uvp}$

1.5 Current limit

The current limit comparator senses the inductor current through the low side MOSFET RDS_{ON} drop and compares this value with the ILIM pin voltage value. While the current is above the current limit value, the control inhibits the one-shot start.
To properly set the current limit threshold, it should be noted that this is a valley current limit. Average current depends on the inductor value, V_{IN} V_{OUT} and switching frequency.
The average output current in current limit is given by:

Eq 12 $$I_{OUT_{CL}} = I_{max\ valley} + \frac{\Delta I}{2}$$

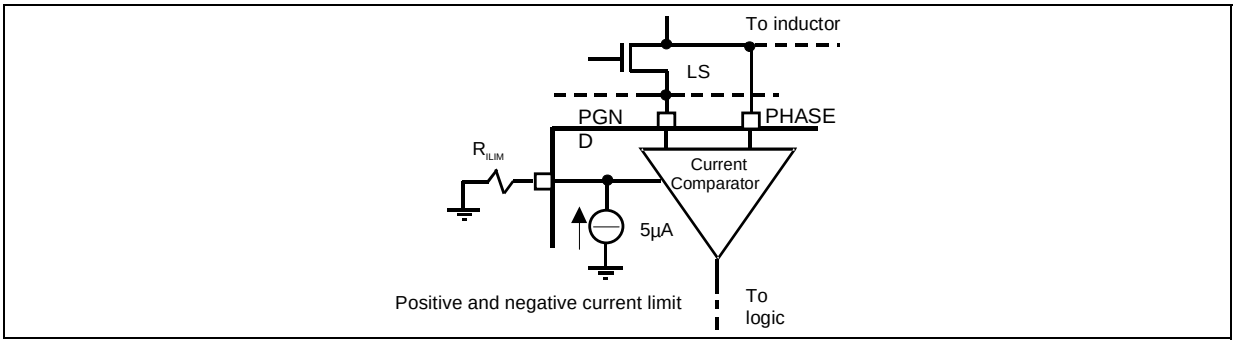
Thus, to set the current threshold, choose RILIM according to the following equation:

Eq 13 $$_{max\ valley} = \frac{R_{ILim}}{Rds_{on}} \cdot K_{ILIM}$$

In current limit the system keeps the current constant until the output voltage meets the undervolatge threshold. The negative valley current limit, for the sink mode, is set automatically at the same value of the positive valley current limit. The average negative current limit differs from the positive average current limit by the ripple current; this difference is due to the valley control technique.

The system accuracy is function of the exactness of the resistance connected to ILIM pin and the low side MOSFET RDS_{ON} accuracy. Moreover the voltage on ILIM pin must range between 10mV and 1V to ensure the system linearity.

Figure 6. Current limit schematic



1.6 Protection and fault

Sensing VSENSE pin voltage performs output protection. The nature of the fault (that is, latched OV or latched UV) is given by the PGOOD and OVP pins. If the output voltage is between the 89% (typ.) and 110% (typ) of the regulated value, PGOOD is high. If a hard overvoltage or an undervoltage occurs, the device is latched: low side MOSFET and, high side MOSFET are turned off and PGOOD goes low. In case the system detects an overvoltage the OVP pin goes high.

To recover the functionality the device must be shut down and restarted thought the SHDN pin, or the supply has to be removed, and restart with the correct sequence.

These features are useful to protect against short-circuit (UV fault) as well as high side MOSFET short (OV fault).

1.7 Drivers

The integrated high-current drivers allow using different size of power MOSFET, maintaining fast switching transition. The driver for the high side MOSFET uses the BOOT pin for supply and PHASE pin for return (floating driver). The driver for the low side MOSFET uses the VDR pin for the supply and PGND pin for the return. The main feature is the adaptive anti-cross-conduction protection, which prevents from both high side and low side MOSFET to be on at the same time, avoiding a high current to flow from VIN to GND. When high side MOSFET is turned off the voltage on the pin PHASE begins to fall; the low side MOSFET is turned on only when the voltage on PHASE pin reaches 250mV. When low side is turned off, high side remains off until LGATE pin voltage reaches 500mV. This is important since the driver can work properly with a large range of external power MOSFETS.

The current necessary to switch the external MOSFETS flows through the device, and it is proportional to the MOSFET gate charge and the switching frequency. So the power dissipation of the device is function of the external power MOSFET gate charge and switching frequency.

Eq 14 $$P_{driver} = V_{cc} \cdot Q_{gTOT} \cdot F_{SW}$$

The maximum gate charge values for the low side and high side are given from:

Eq 15 $$Q_{MAXHS} = \frac{f_{SW0}}{f_{SW}} \cdot 75nC$$

Eq 16 $$Q_{MAXLS} = \frac{f_{SW0}}{f_{SW}} \cdot 125nC$$

Where f_{SW0} = 500Khz. The equations above are valid for T_J = 150°C. If the system temperature is lower the Q_G can be higher.

For the Low Side driver the max output gate charge meets another limit due to the internal traces degradation; in this case the maximum value is Q_{MAXLS} = 125nC.

The low side driver has been designed to have a low resistance pull-down transistor, around 0.5 ohms. This prevents the voltage on LGATE pin raises during the fast rise-time of the pin PHASE, due to the Miller effect.

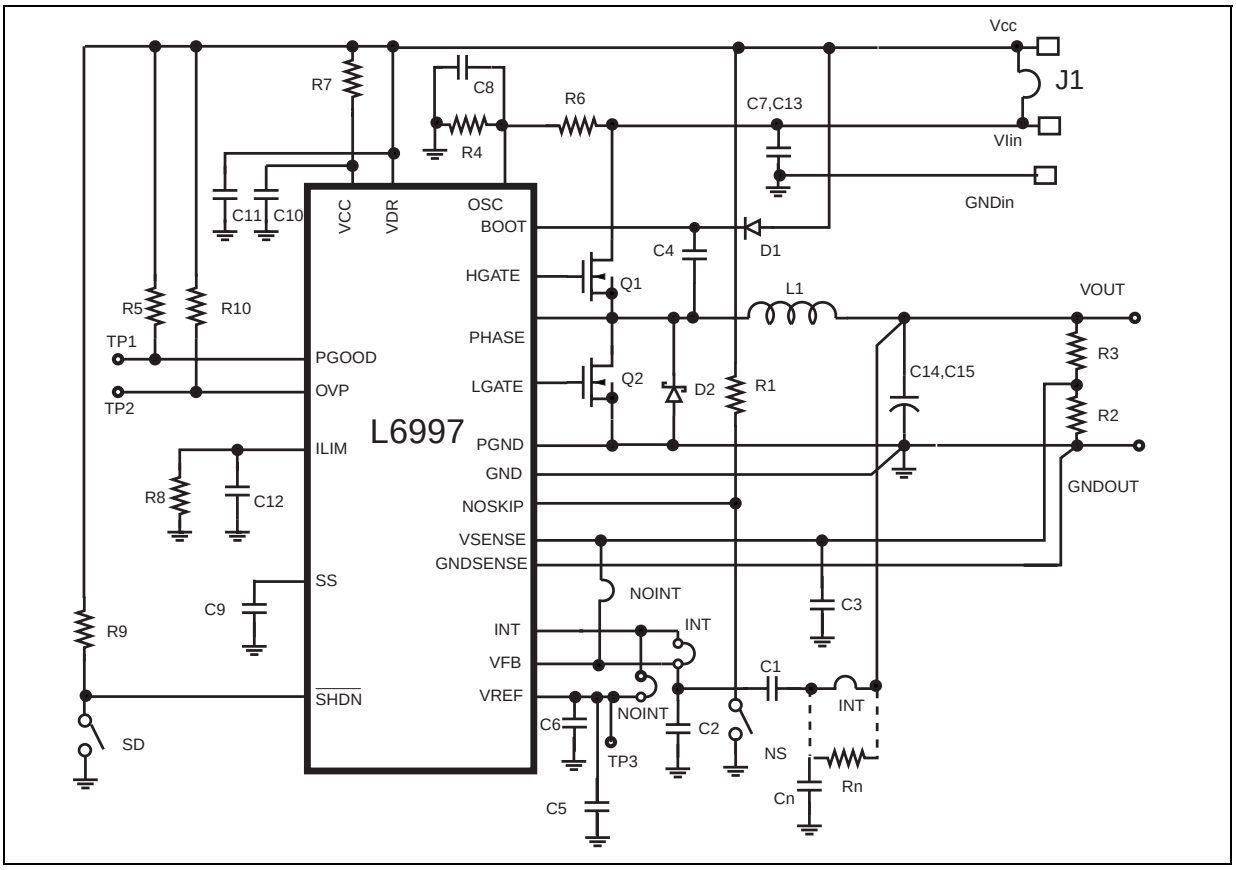
Because the driver voltage can be very low it should be considered also the ULTRA LOW VOLTAGE MOSFET. This kind of MOSFET has very low threshold voltage, so the overdrive voltage can be enough to ensure correct transition and low enough RDS_{ON}.

2 APPLICATION INFORMATION

2.1 5A Demo board description

The demo board shows the device operation in this condition: VI_N from 3.3V to 5V, I_{OUT}=5A V_{OUT}=1.25V. The evaluation board let use the system with 2 different voltages (V_{CC} the supply for the IC and V_{IN} the power input for the conversion) so replacing the input capacitors the power input voltage could be also 28V. When instead the input voltage (V_{IN}) is equal to the V_{CC} it should be better joining them with a 10Ω resistor in order to filter the device input voltage. On the topside demo there are two different jumpers: one jumper, near the OVP and POWER GOOD test points, is used to shut down the device; when the jumper is present the device is in SHUTDOWN mode, to run the device remove the jumper. The other jumper, near the V_{REF} test point, is used to set the PFM/PSK mode. When the jumper is present, at light load, the system will go in PFM mode; if there is not the jumper, at light load, the system will remain in PWM mode. In the demo bottom side there are two others different jumpers. They are used to set or remove the INTEGRATOR configuration. When the jumpers named with INT label are closed AND the jumpers named with the NOINT label are open the integrator configuration is set. Sometimes the integrator configuration needs a low frequency filter the to reduce the noise interaction. In this case instead close the INT jumpers put there a resistor and after a capacitor to ground (as in the schematic diagram); the pole value is around 500Khz but it should be higher enough than the switching frequency (ten times). On the opposite when the jumpers named with the NOINT are closed and the jumpers named with INT are open the NON INTEGRATOR configuration is selected. Refer to the Table 1 and 2 for the jumpers connection.

Figure 7. Demoboard Schematic Diagram



2.2 Jumper Connection

Table 1. Jumper connection with integrator

Component	Connection
C1	Mounted
C2	Mounted *
INT	Close
NOINT	Open

* This component is not necessary, depends from the output ESR capacitor. See the integrator section.

Table 2. Jumper connection without integrator

Component	Connection
C1	Not mounted
C2	Not Mounted
INT	Open
NOINT	Close

2.3 DEMOBOARD LAYOUT

Real dimensions: 4,7 cm X 2,7 cm (1.85 inch X 1. 063 inch)

Figure 8. Top side components placement

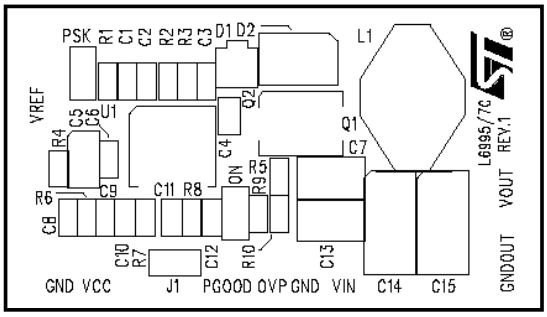


Figure 9. Bottom side Jumpers distribution

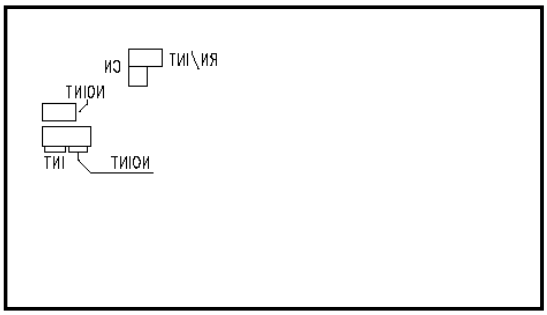


Figure 10. Top side layout

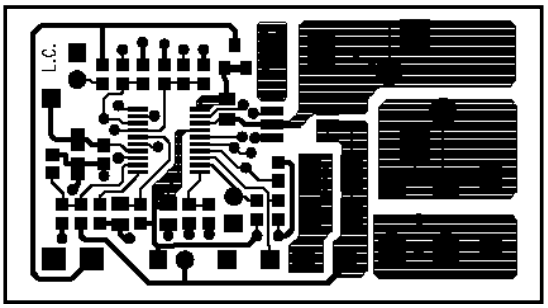


Figure 11. Bottom side layout

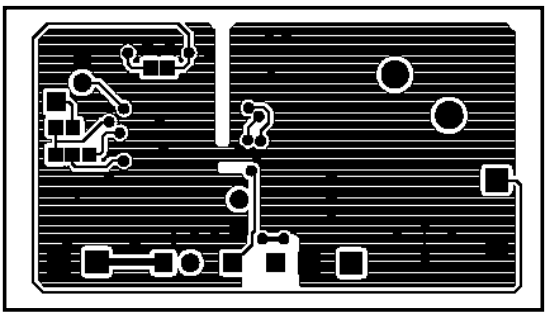


Table 3. PCB Layout guidelines

Goal	Suggestion
Low radiation and low magnetic coupling with the adjacent circuitry.	1) Small switching current loop areas. (For example placing C_{IN}, High Side and Low side MOSFETS, Shottky diode as close as possible). 2) Controller placed as close as possible to the power MOSFET. 3) Group the gate drive component (Boot cap and diode together near the IC.
Don't penalty the efficiency.	Keep power traces and load connections short and wide.
Ensure high accuracy in the current sense system.	Phase pin and PGND pin must be made with Kelvin connection and as close as possible to the Low Side MOSFETS.
Reduce the noise effect on IC.	1) Put the feedback component (like output divider, integrator network, etc) as close as possible to the IC. 2) The feedback traces must be parallel and as close as possible. Moreover they must be routed as far as possible from the switching current loops..

Table 4. Component list

The component list is shared in two sections: the first for the general-purpose component, the second for power section:

GENERAL-PURPOSE SECTION

Part name	Value	Dimension	Notes
RESISTOR			
R1, R5, R9, R10	33kΩ	0603	Pull-up resistor
R2	1kΩ	0603	Output resistor divider (To set output voltage)
R3	1.1kΩ	0603	
R4		0603	Input resistor divider (To set switching frequency)
R6	470kΩ	0603	
R7	0Ω	0603	
R8		0603	Current limit resistor
CAPACITOR			
C1	330pF	0603	First integrator capacitor
C2	N.M.	0603	Second integrator capacitor
C3	1nF	0603	
C4	100nF	0603	
C5	1μF	Tantalum	
C6	10nF	0603	
C9	10nF	0603	Softstart capacitor
C10	100nF	0603	
C11	100nF	0603	
C8, C12	47pF	0603	
DIODE			
D1	BAR18		

POWER SECTION

INPUT CAPACITORS			
C7, C13	47µF	ECJ4XF0J476Z PANASONIC	
OUTPUT CAPACITORS			
C14, C15	220µF	2R5TPE220M POSCAP	
INDUCTOR			
L1	2.7 µH	DO3316P-272HC COILCRAFT	
POWER MOS			
Q1,Q2	STS5DNF20V	STMicroelectronics	Double mosfet in sigle package
DIODE			
D2	STPS340U	STMicroelectronics	3

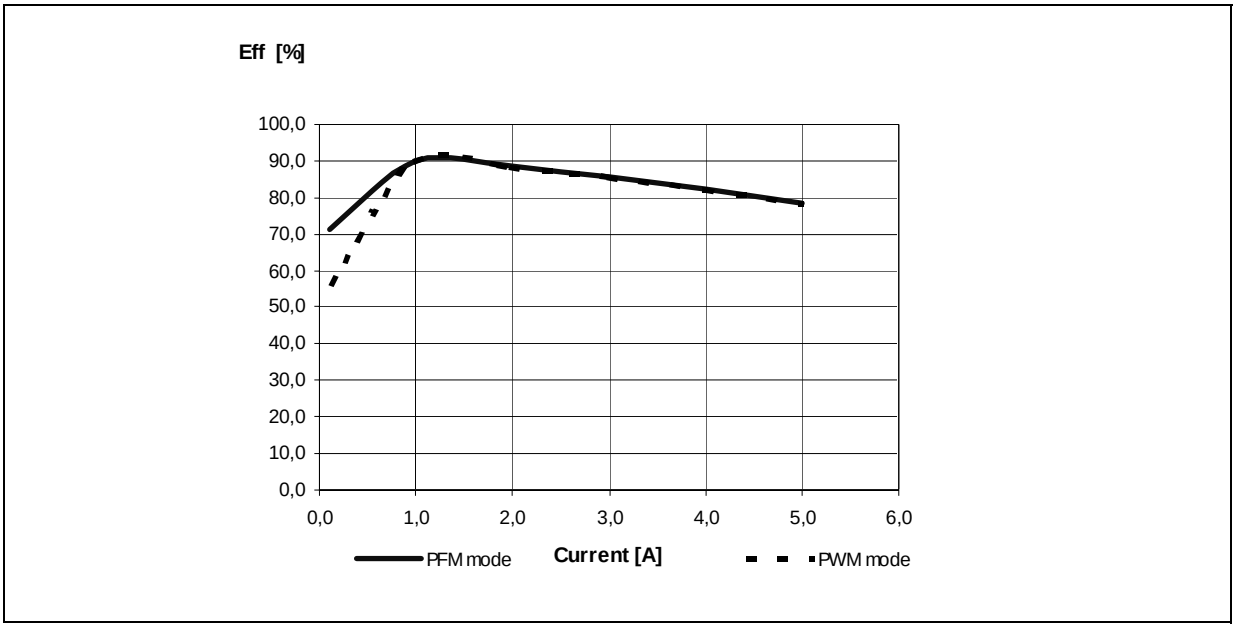
Notes: 1. N.M.=Not Mounted
2. The demoboard with this component list is set to give: V_{OUT} = 1.25V, F_{SW} = 270kHz with an input voltage around V_{IN} = V_{CC} = 3.3V-5V and with the integrator feature.
3. The diode efficiency impact is very low; it is not a necessary component.
4. All capacitors are intended ceramic type otherwise specified.

2.4 EFFICIENCY CURVES

Source mode

V_{IN} = 3.3V V_{OUT} = 1.25V F_{SW} = 270kHz

Figure 12. Efficiency vs output current



3 STEP BY STEP DESIGN

V_{IN} = 3.3V, ±10% V_{OUT} = 1.25V I_{OUT} = 5A F_{SW} = 270kHz

3.1 Input capacitor.

A pulsed current (with zero average value) flows through the input capacitor of a buck converter. The AC component of this current is quite high and dissipates a considerable amount of power on the ESR of the capacitor:

Eq 17 $$P_{CIN} = ESR_{CIN} \cdot Iout^2 \cdot \frac{Vin \cdot (Vin - Vout)}{Vin^2}$$

The RMS current, which the capacitor must provide, is given by:

Eq 18 $$Icin_{rms} = \sqrt{Iout^2 \delta(1-\delta) + \frac{\delta}{12}(\Delta I_L)^2}$$

Neglecting the last term, the equation reduces to:

Eq 19 $$Icin_{rms} = Iout\sqrt{\delta(1-\delta)}$$

which maximum value corresponds to to δ = 1/2.

$ICIN_{RMS}$, has a maximum equal to δ = 1/2 (@ VIN = 2×VOUT, that is, 50% duty cycle). The input, therefore, should be selected for a RMS ripple current rating as high as half the respective maximum output current.

Electrolytic capacitors are the most used cause are the cheapest ones and are available with a wide range of RMS current ratings. The only drawback is that, considering a requested ripple current rating, they are physically larger than other capacitors. Very good tantalum capacitors are coming available, with very low ESR and small size. The only problem is that they occasionally can burn if subjected to very high current during the charge. So, it is better avoid this type of capacitors for the input filter of the device. In fact, they can be subjected to high surge current when connected to the power supply. If available for the requested value and voltage rating, the ceramic capacitors have usually a higher RMS current rating for a given physical dimension (due to the very low ESR). The drawback is the quite high cost. Possible solutions:

10µF	C34Y5U1E106ZTE12 TOKIN
22µF	JMK325BJ226MM TAIYO-YUDEN
47µF	ECJ4XF0J476Z PANASONIC
33µF	C3225X5R0J476M TDK

With our parameter from the equation 3 it is found:

$$Icin_{rms} = 2.42A$$

3.2 Inductor

To define the inductor, it is necessary to determine firstly the inductance value. Its minimum value is given by:

Eq 20 $$Lmin \geq \frac{V_o \cdot (Vin_{max} - V_o)}{F_{SW} \cdot I_{out} \cdot RF \cdot Vin_{max}}$$

where RF is given from $\Delta I/I_{OUT}$ (basically it is around 30%).

With our parameters:

$$Lmin \geq 2\mu H$$

The saturation current is around 5A

3.3 Output capacitor and ripple voltage

The output capacitor is chosen by the output voltage static precision and also dynamic precision. The static precision regards the output voltage ripple value rated the output voltage in steady state at the end the ESR value; while the dynamic precision regards the load step positive and negative load transient.

If the static precision is around ±1% for the 1.25V output voltage, the output precision is ±12.5mV.

To determine the ESR value from the output precision is necessary to calculate the ripple current:

Eq 21 $$\Delta I = \frac{Vin - Vo}{L} \cdot \frac{Vo}{Vin} \cdot T_{sw}$$

One can consider a switching frequency around 270kHz.

From the Eq. above the ripple current is around 1.25A.

So the ESR is given from: RMS current in output capacitor is given by:

Eq 22 $$ESR = \frac{\Delta V_{ripple}}{\frac{\Delta I}{2}} = \frac{25mV}{1.25} = 20m\Omega$$

The dynamic specifications are sometimes more relaxed than the static requirements, so one can consider the ESR value around 20mΩ enough.

To allow the device control loop to properly work, output capacitor ESR zero must be at least ten times smaller than switching frequency. Low ESR tantalum capacitors, which ESR zero is close to ten kHz, are suitable for output filtering. Output capacitor value C_{OUT} and its ESR, $ESRC_{OUT}$, should be large enough and small enough, respectively, to keep output voltage within the accuracy range during a load transient, and to give the device a minimum signal to noise ratio.

The current ripple flows through the output capacitors, so the should be calculated also to sustain this ripple: the RMS current value is given by Eq. 18.

Eq 23 $$Icout_{rms} = \frac{1}{2\sqrt{3}} \Delta I_L$$

But this is usually a negligible constrain.

Possible solutions:

330µF	EEFUE0D331R PANASONIC
220µF	2R5TPE220M POSCAP

3.4 MOSFET's and Schottky Diodes

Since a 3.3V bus powers the gate drivers of the device, the use ultra low level MOSFET is highly recommended, especially for high current applications. The MOSFET breakdown voltage V_{BRDSS} must be greater than VINMAX with a certain margin, so the selection will address 20V or 30V devices (depends on applications).

The RDS_{ON} can be selected once the allowable power dissipation has been established. By selecting identical Power MOSFET as the main switch and the synchronous rectifier, the total power they dissipate does not depend on the duty cycle. Thus, if PON is this power loss (few percent of the rated output power), the required

RDS_{ON} (@ 25 °C) can be derived from:

Eq 24 $$RDS_{ON} = \frac{P_{ON}}{Iout^2 \cdot (1 + \alpha \cdot \Delta T)}$$

α is the temperature coefficient of RDS_{ON} (typically, $\alpha = 510^{-3}\ °C^{-1}$ for these low-voltage classes) and T the admitted temperature rise. It is worth noticing, however, that generally the lower RDS_{ON}, the higher is the gate charge Q_G, which leads to a higher gate drive consumption. In fact, each switching cycle, a charge Q_G moves from the input source to ground, resulting in an equivalent drive current:

Eq 25 $$Iq = Qg \cdot F_{SW}$$

The SCHOTTKY diode to be placed in parallel to the synchronous rectifier must have a reverse voltage V_{RRM} greater than VIN_{MAX}; for low current application the SCHOTTKY is not necessary to increase the efficiency. In order to use less space than possible, a double MOSFET in a single package is chosen: STS5DNF20V

3.5 Output voltage setting

The first step is choosing the output divider to set the output voltage. To select this value there isn't a criteria, but a low divider network value (around 100Ω) decries the efficiency at low current; instead a high value divider network (100KΩ) increase the noise effects. A network divider values from 1KΩ to 10KΩ is right. We chose:

R3 = 1KΩ

R2 = 1.1KΩ

The device output voltage is adjustable by connecting a voltage divider from output to VSENSE pin. Minimum output voltage is V_{OUT}=VREF=0.6V. Once output divider and frequency divider have been designed as to obtain the required output voltage and switching frequency, the following equation gives the smallest input voltage, which allows L6997 to regulate (which corresponds to $T_{OFF}=T_{OFFMIN}$):

Eq 26 $$\delta < 1 - \frac{\alpha_{OSC}}{\alpha_{OUT}} \cdot \frac{1}{\left(\frac{K_{OSC}}{T_{OFF,MIN}}\right)MAX}$$

3.6 Voltage Feedforward

From the equations 1,2 3 choosing the switching frequency around 270kHz it can be selected the input divider. For example:

R3 = 470KΩ

R4 = 8.5KΩ

3.7 Current limit resistor

From the equation 8 it can be set the valley current limit considering the STS5DNF20V Ultra logic Level Mosfet with a current around 5A:

R8 = 120KΩ

3.8 Integrator capacitor

Let it be F_U = 15kHz, V_{OUT} = 1.25V.

Since V_{REF} = 0.6V, from equation 2, of the device description, it follows αO_{UT} = 0.348 and, from equation 5 it follows C = 250pF. The output ripple is around 22mV, so the system doesn't need the second integrator capacitor.

3.9 Soft start capacitor

Considering the soft start equations:

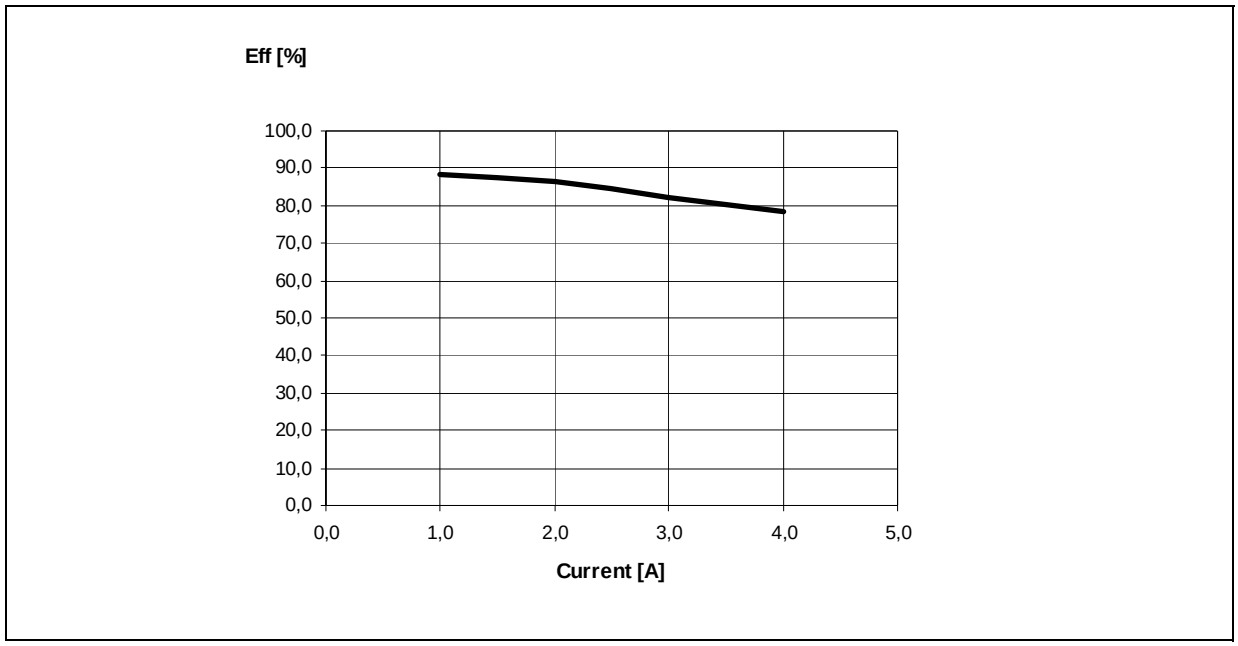
C_{SS} = 150pF

The equations are valid without load. When an active load is present the equations result more complex; further some active loads have unexpected effect, as higher current than the expected one during the soft start, can change the start up time.

In this case the capacitor value can be selected on the application; anyway the Eq11 gives an idea about the C_{SS} value.

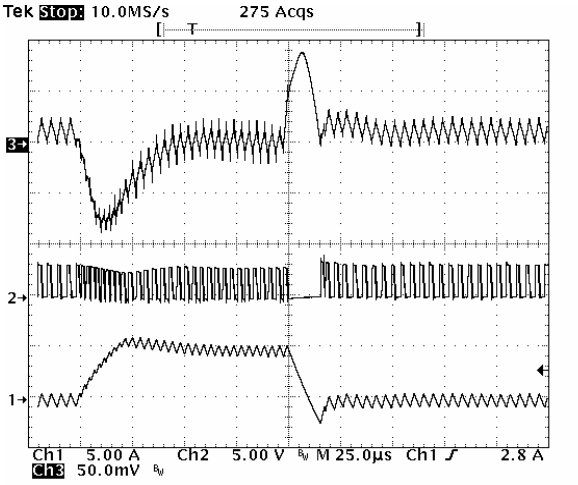
3.10 Sink mode

Figure 13. Efficiency vs output current



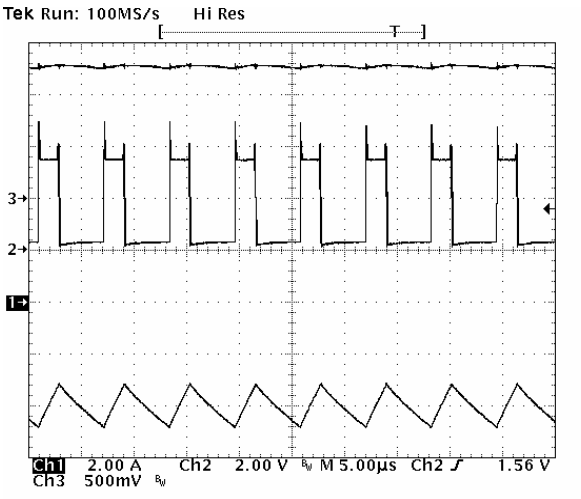
4 TYPICAL OPERATING CHARACTERISTICS

Figure 14. Load transient response from 0A to 5A..



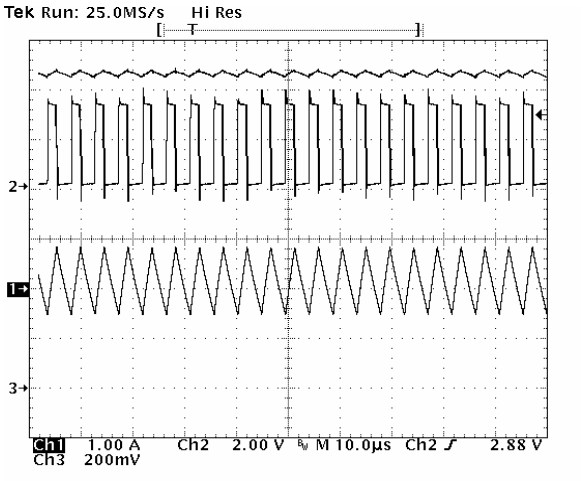
Ch1-> Inductor current
Ch2-> Phase Node
Ch3-> Output voltage

Figure 15. Normal functionality in SINK mode..



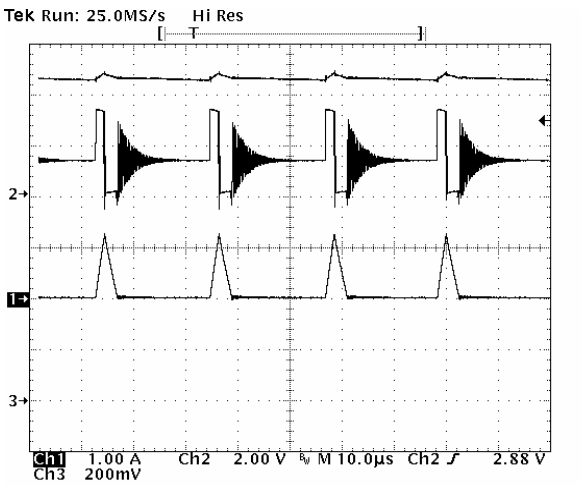
Ch1-> Inductor current
Ch2-> Phase Node
Ch3-> Output voltage

Figure 16. Normal functionality in PWM mode.



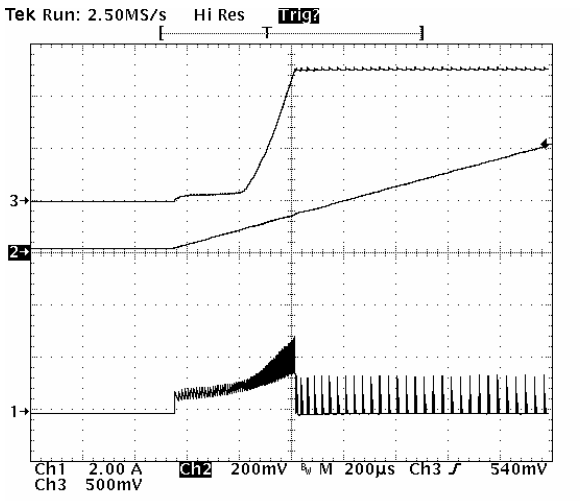
Ch1-> Inductor current
Ch2-> Phase Node
Ch3-> Output voltage

Figure 17. Normal functionality in PFM mode.



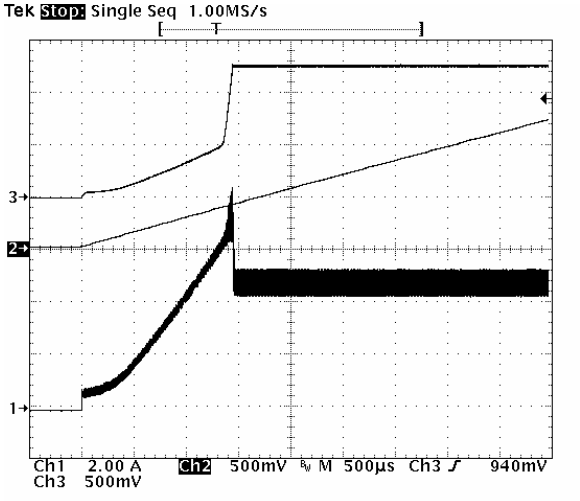
Ch1-> Inductor current
Ch2-> Phase Node
Ch3-> Output voltage

Figure 18. Start up waveform with 0A load.



Ch1-> Inductor current
Ch2-> Soft start Voltage
Ch3-> Output voltage

Figure 19. Start up waveform with 5A load..

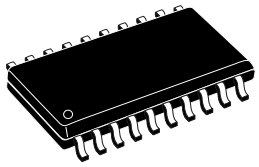


Ch1-> Inductor current
Ch2-> Soft start Voltage
Ch3-> Output voltage

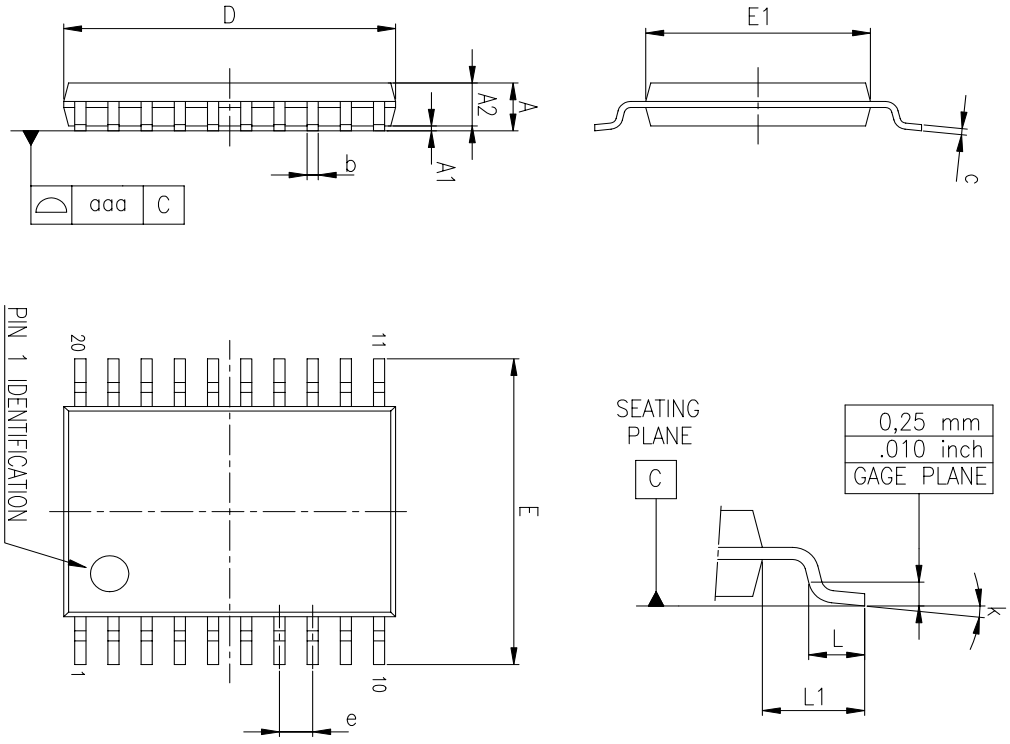
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.20			0.047
A1	0.050		0.150	0.002		0.006
A2	0.800	1.000	1.050	0.031	0.039	0.041
b	0.190		0.300	0.007		0.012
c	0.090		0.200	0.004		0.008
D (1)	6.400	6.500	6.600	0.252	0.256	0.260
E	6.200	6.400	6.600	0.244	0.252	0.260
E1 (1)	4.300	4.400	4.500	0.170	0.173	0.177
e		0.650			0.026	
L	0.450	0.600	0.750	0.018	0.024	0.030
L1		1.000			0.039	
k	0˚ (min.) 8˚ (max.)					
aaa			0.100			0.004

Note: 1. D and E1 does not include mold flash or protrusions. Mold flash or potrusions shall not exceed 0.15mm (.006inch) per side.

OUTLINE AND MECHANICAL DATA



TSSOP20
Thin Shrink Small Outline Package



0087225 (Jedec MO-153-AC)