Practical Control Design for Power Supplies

Power Seminar 2004

Practical Control Design for Power Supplies

- Refresher on closed loop feedback
- Special features of switch mode power supplies
- Stabilization and optimization of control loops
  - Example of stabilizing a flyback converter
- Advanced topics
  - Effect of input filter on transfer functions

Objectives for Controlling Power Supplies

- Most switch mode power supplies use closed loop negative feedback control
- Like all closed loop feedback control systems it is important to ensure that
  - The closed loop is stable
  - The response to a change does not have an excessive overshoot
  - The response to a change does not have excessive ringing
  - The cost of the control methodology is appropriate for the application

Basic Principles: Principles of an Oscillator Circuit

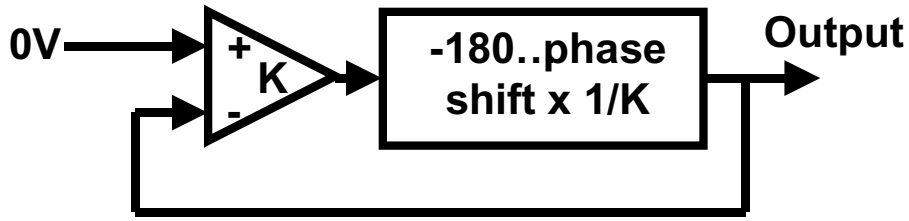
To understand how best to stop a power supply from oscillating, we will consider the conditions under which a circuit will oscillate

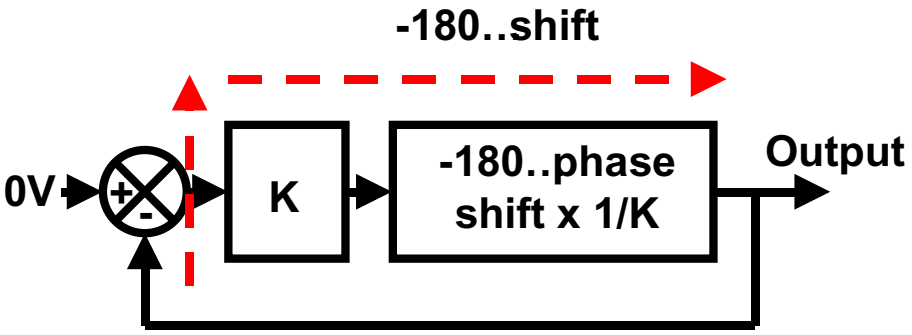
We can build an oscillator circuit using

- A differential amplifier with gain K
- A phase shift of -180…
- Unity gain negative feedback

When the oscillator is working

- The amplifier output is sinusoidal
- The output of the phase shift circuit is shifted -180…, and scaled to 1/K
- The negative feedback inverts the sinusoid, giving a further phase shift of -180…
- The amplifier has gain K, so the output is the same as where we started





Further -180..shift gives total -360..shift

Basic Principles: Generation of a Negative Phase Shift

- RC circuit
  - Gives a maximum phase shift of -90…
  - Three RC stages are necessary to generate a guaranteed phase shift of -180…
- LCR circuit
  - Gives a maximum phase shift of -180…
  - An LCR circuit, plus an additional phase shift element is necessary to generate a guaranteed phase shift of -180…
- A differential amplifier having a capacitor in the feedback generates a constant phase shift of -90…
- We introduce something known as a Right Half Plane Zero
  - This element generates a maximum phase shift of -90..in a similar way to an RC circuit
- We note that three circuits attenuate/reduce the input signal
  - The integrator has a gain greater than 1 at low frequencies

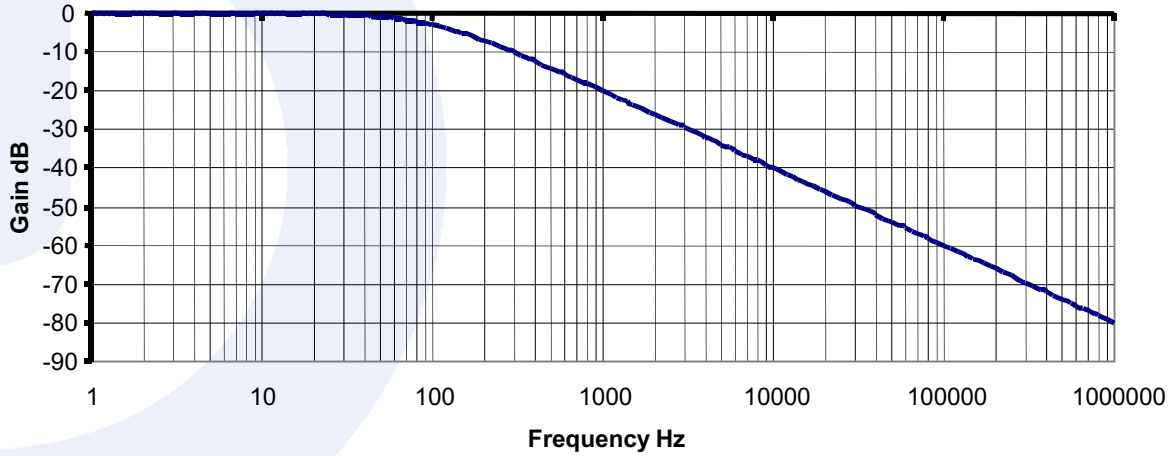
Basic Principles: Formal Names for Phase Shift Elements

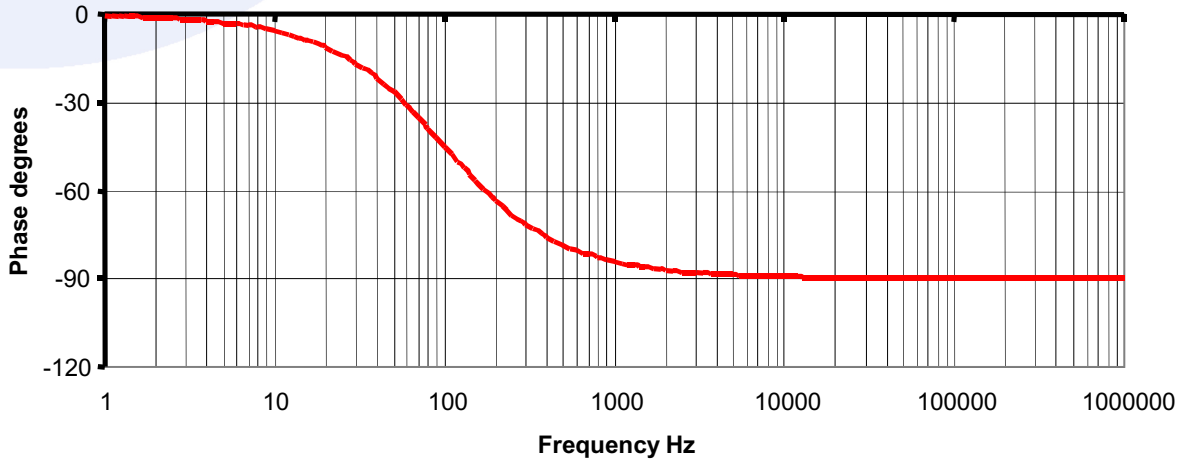
Our example	Formal name	Maximum shift	Transfer function
RC circuit	(single) pole	-90…	$\frac{V_o}{V_i} = \frac{1}{1 + j\omega CR}$
RLC circuit	quadratic pole	-180…	$\frac{V_o}{V_i} = \frac{1}{1 + j\omega CR - \omega^2 LC}$
Op-amp with cap in feedback	integrator pole	-90…	$\frac{V_o}{V_i} = \frac{1}{j\omega CR}$
Right half plane zero	right half plane zero	-90…	$\frac{V_o}{V_i} = 1 - j\frac{\omega}{\omega_z}$

Basic Principles: Standardized Forms

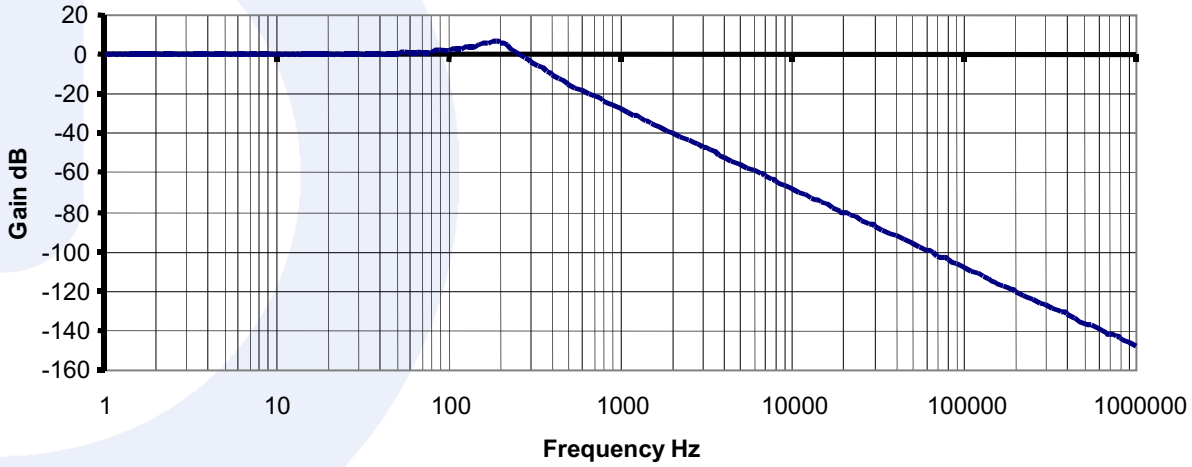
Our example	Formal name	Transfer function	Parameters
RC circuit	(single) pole	$\frac{V_o}{V_i} = \frac{1}{1 + j\frac{\omega}{\omega_p}}$	$\omega_p = \frac{1}{RC}$
RLC circuit (lossy L)	quadratic pole	$\frac{V_o}{V_i} = \frac{1}{1 + \frac{j\omega}{Q\omega_o} - \frac{\omega^2}{\omega_o{}^2}}$	$\omega_o = \frac{1}{\sqrt{LC}}$ $Q = \frac{1}{R}\sqrt{\frac{L}{C}}$
Op-amp with cap in feedback	integrator pole	$\frac{V_o}{V_i} = \frac{1}{j\frac{\omega}{\omega_i}}$	$\omega_i = RC$
Right half plane zero	right half plane zero	$\frac{V_o}{V_i} = 1 - j\frac{\omega}{\omega_z}$	

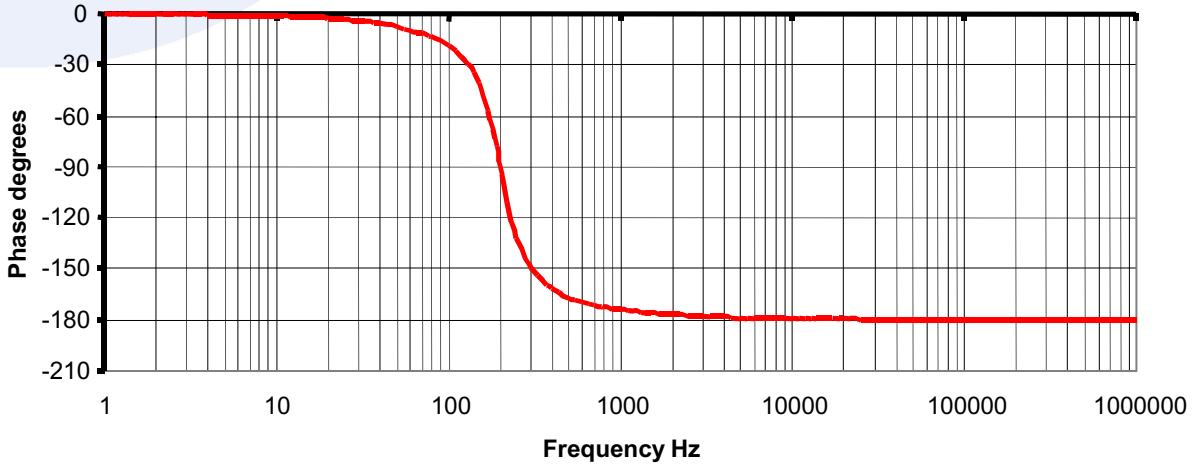
Pole at 100Hz



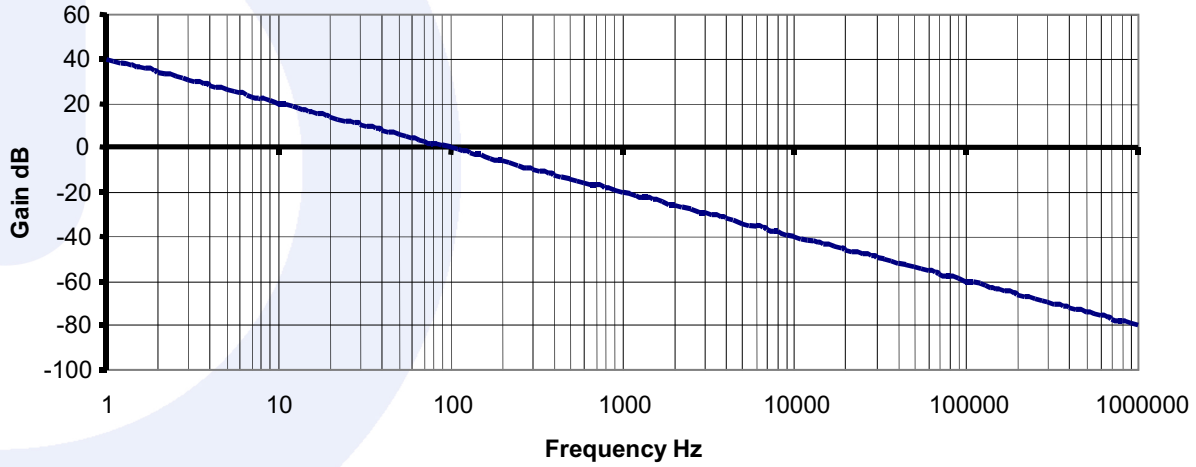


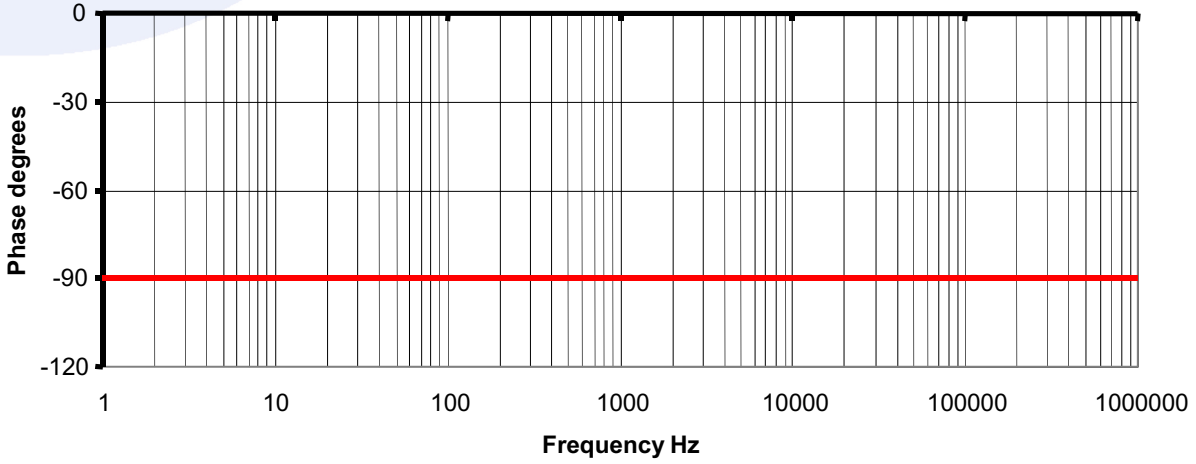
Quadratic Pole at 200Hz, Q = 2



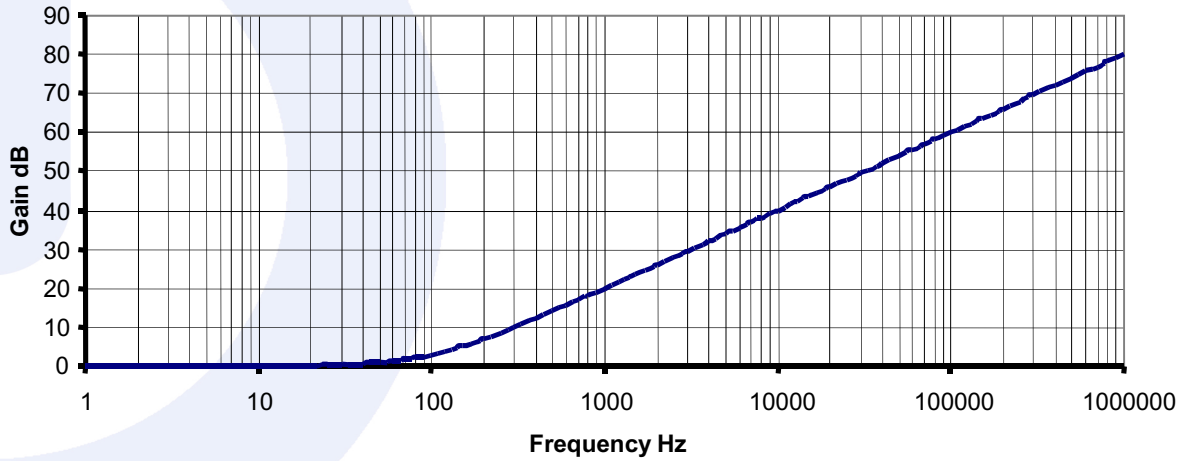


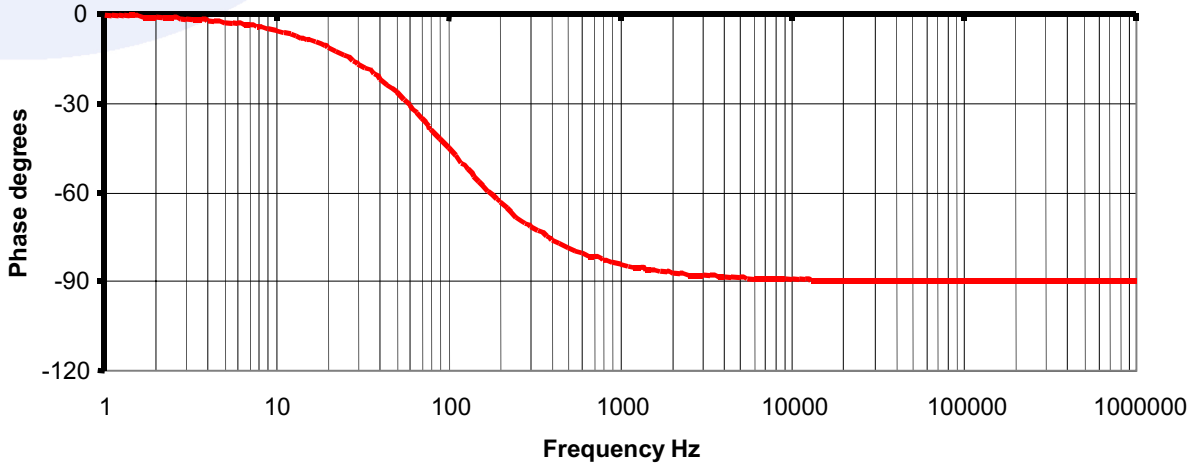
Integrator with Unity Gain at 100Hz





Right Half Plane Zero at 100Hz





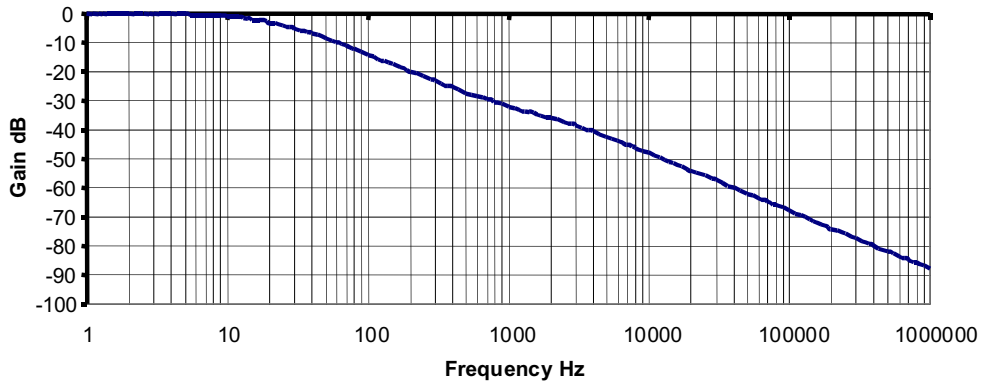
Basic Principles: Combining Elements

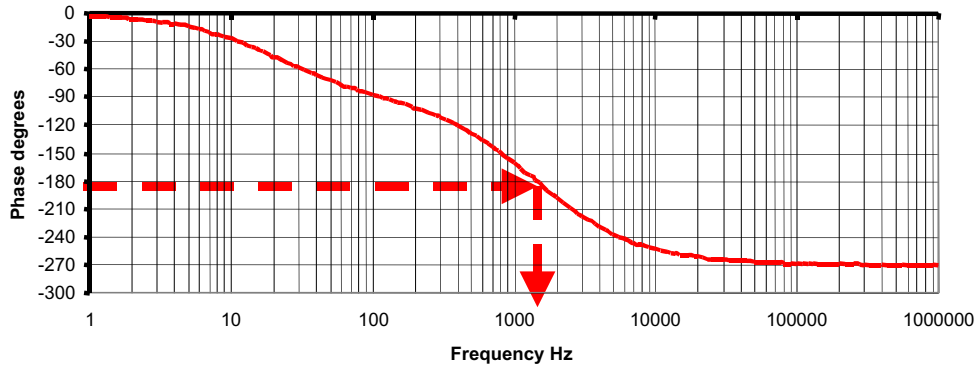
- The transfer function for a cascade of two or more elements is derived by
  - A multiplication of the transfer functions for each element
- The gain of a cascade
  - Is found by multiplying the magnitudes, or adding the magnitudes when expressed in dB
- The phase of a cascade
  - Is found by adding the phases

Note: $dB = 20 \log_{10} (Vo / Vi)$

Basic Principles: Building a -180..Phase Shift

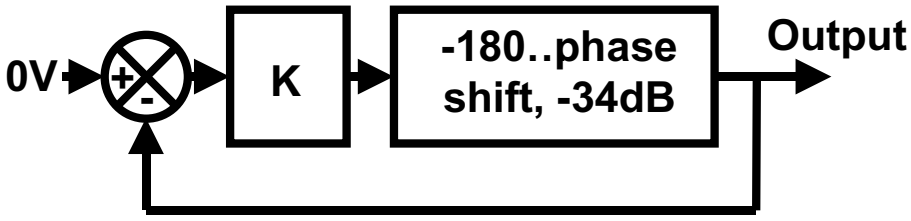
- We can now build a block to generate a guaranteed -180… phase shift
- For example, we could pick an LCR circuit, followed by an RC circuit
- Or we could pick an LCR circuit followed by a Right Half Plane Zero
- Or we could pick three RC circuits
- In the example, we have cascaded a right half plane zero of 1kHz, with a quadratic pole at 200Hz, Q=0.1
  - We have generated a phase shift of -180 degrees at 1400Hz-1500Hz

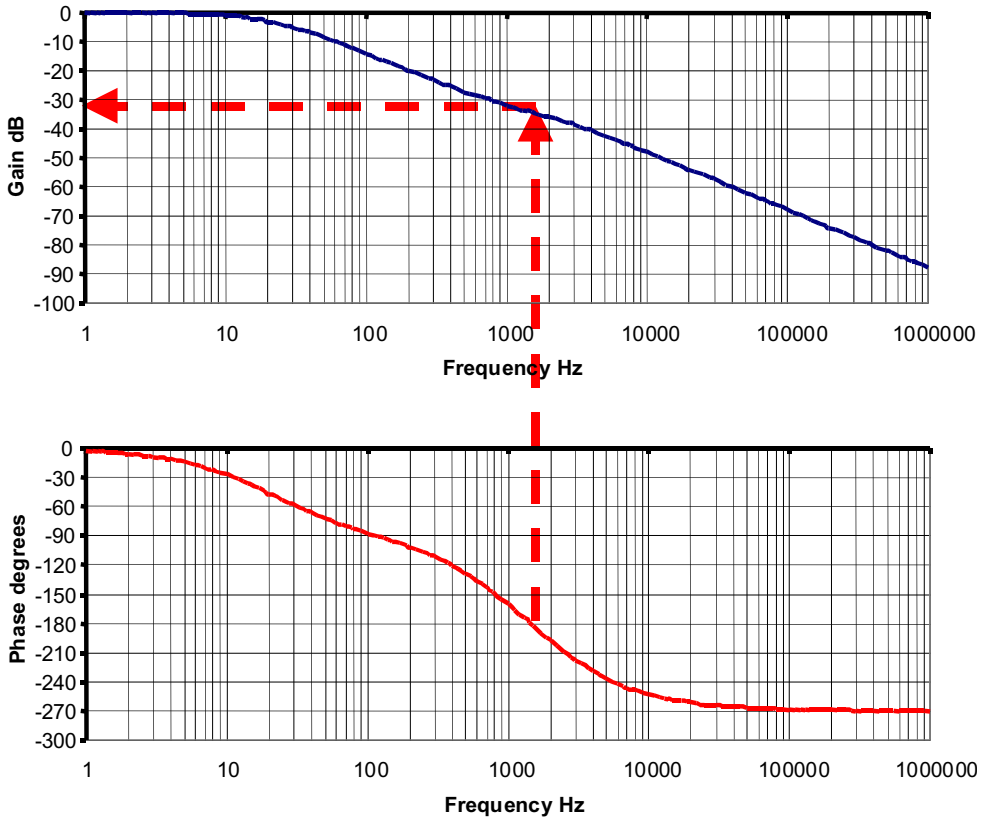




Basic Principles: Building an Oscillator

- Now we have
  - Unity gain feedback
  - A phase shift of greater than -180…
- But the gain is less than 0dB so the loop will not oscillate
- In the graph, the gain is -34dB
- So we need at least 34dB gain for oscillation





Basic Principles: Loop Gain

The attenuation of the phase shift network is combined with the gain of the amplifier, and any other elements such as a controller, to give a total called the loop gain

If the gain is 1 we say unity gain

We have added 100x = 40dB gain to the circuit

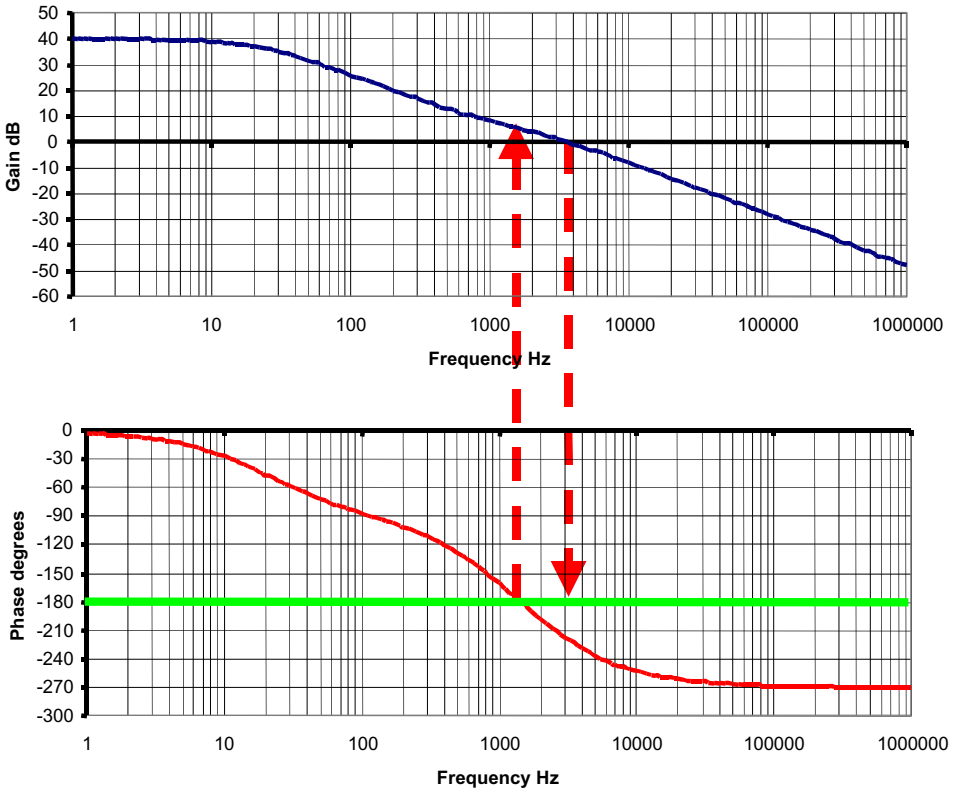
If the phase shift is not as much as -180..for unity loop gain, the loop will not oscillate

— In the example it is -225…

If the gain is less than 1 where the phase shift is -180… the device will not oscillate

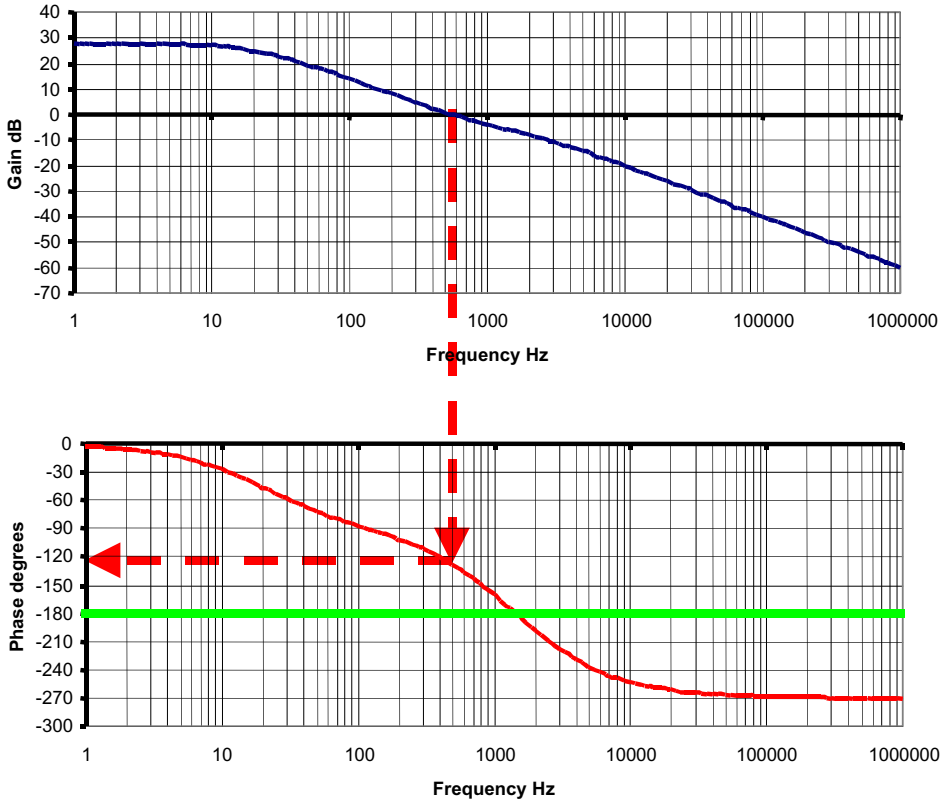
— In the example the gain is 6dB = 2x

So the circuit will oscillate / is unstable

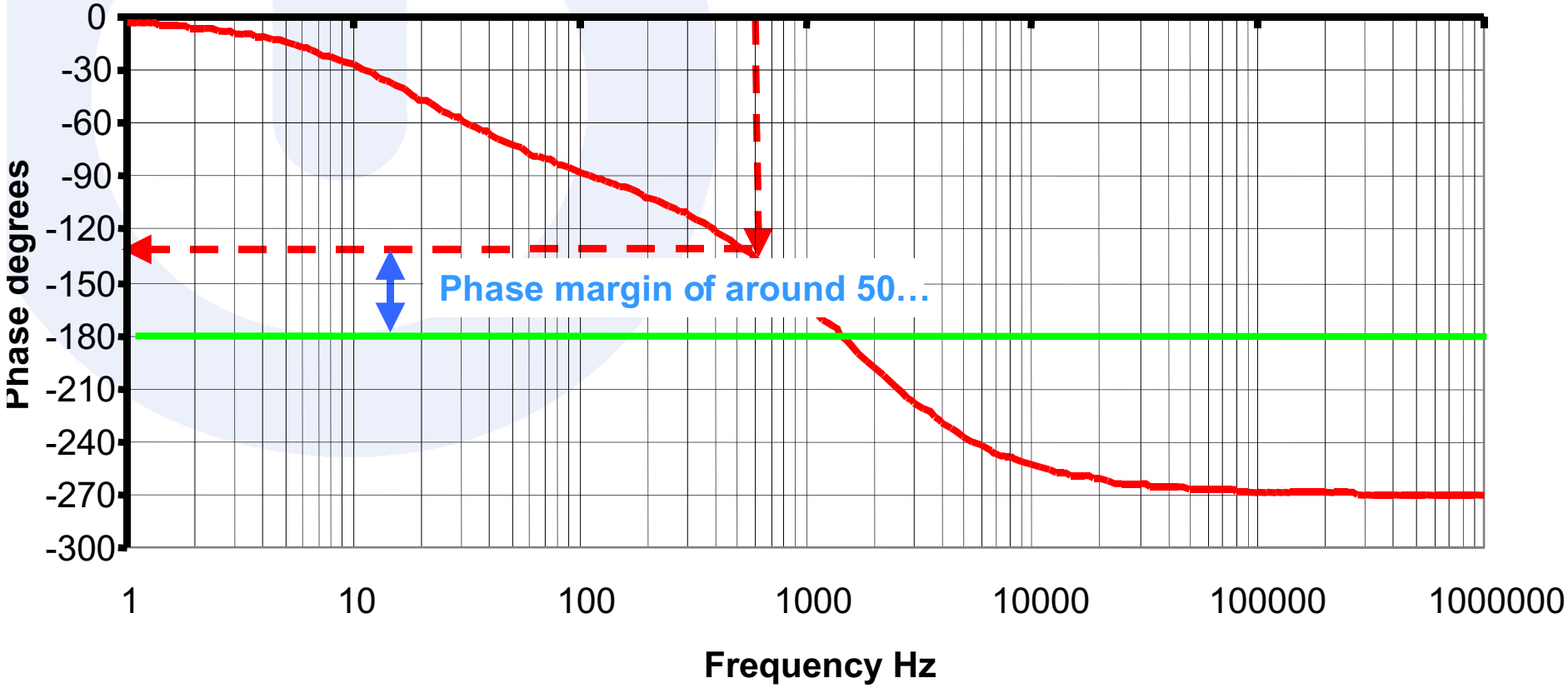


Basic Principles: Phase Margin

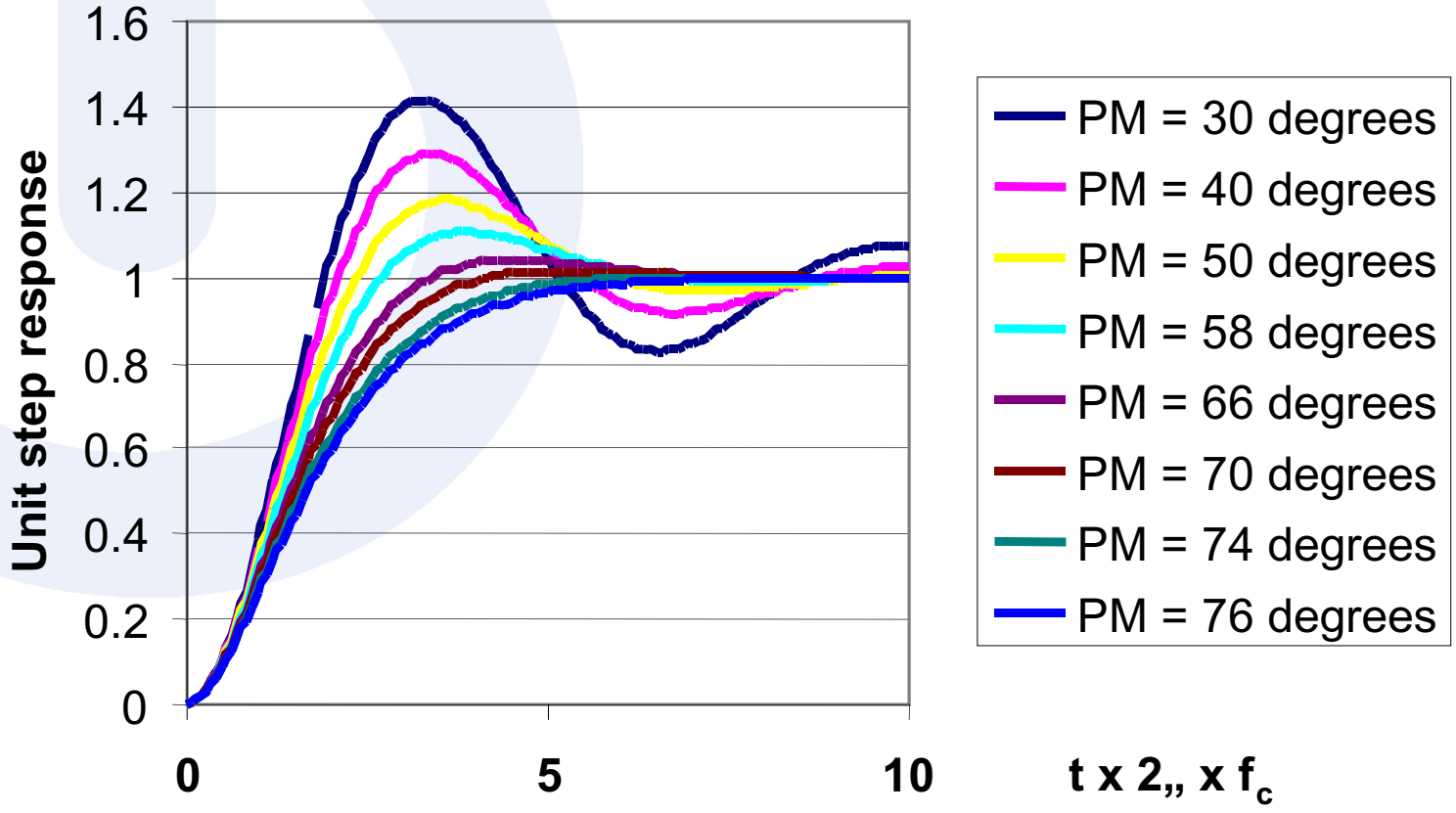
- Switched mode power supplies are required to be stable. Oscillation is not desired
- If the phase shift at unity loop gain is -179… the power supply will be stable BUT
  - Changes in component values may bring it over the edge
  - The closed loop response would have a very large overshoot, long settling time, and significant ringing
- The phase margin is defined as 180… minus the absolute phase shift at unity gain
  - If the phase shift is -130.,.the phase margin is 50…
  - So if the phase shift increases by 50..the loop will oscillate



Close Up View to Show Phase Margin



Step Response for Second Order System



If fc is 3kHz	265us	530us
If fc is 1kHz	796us	1592us (slower response)

Effect of Phase Margin on Overshoot and Timing

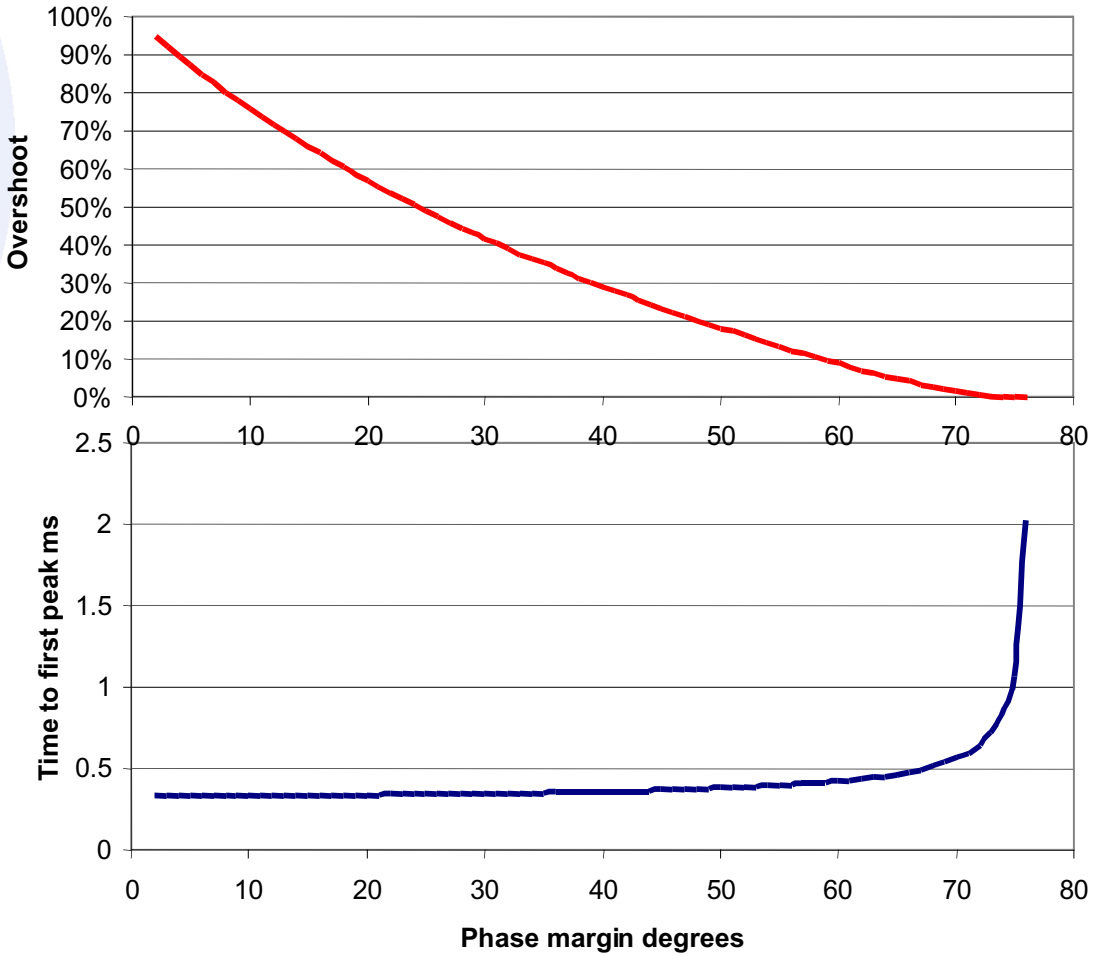
The two plots show the relationships in a second order system for

- Phase margin and overshoot
- Time to first peak for a crossover frequency of 3kHz

There is no peak for a phase margin above 78 degrees

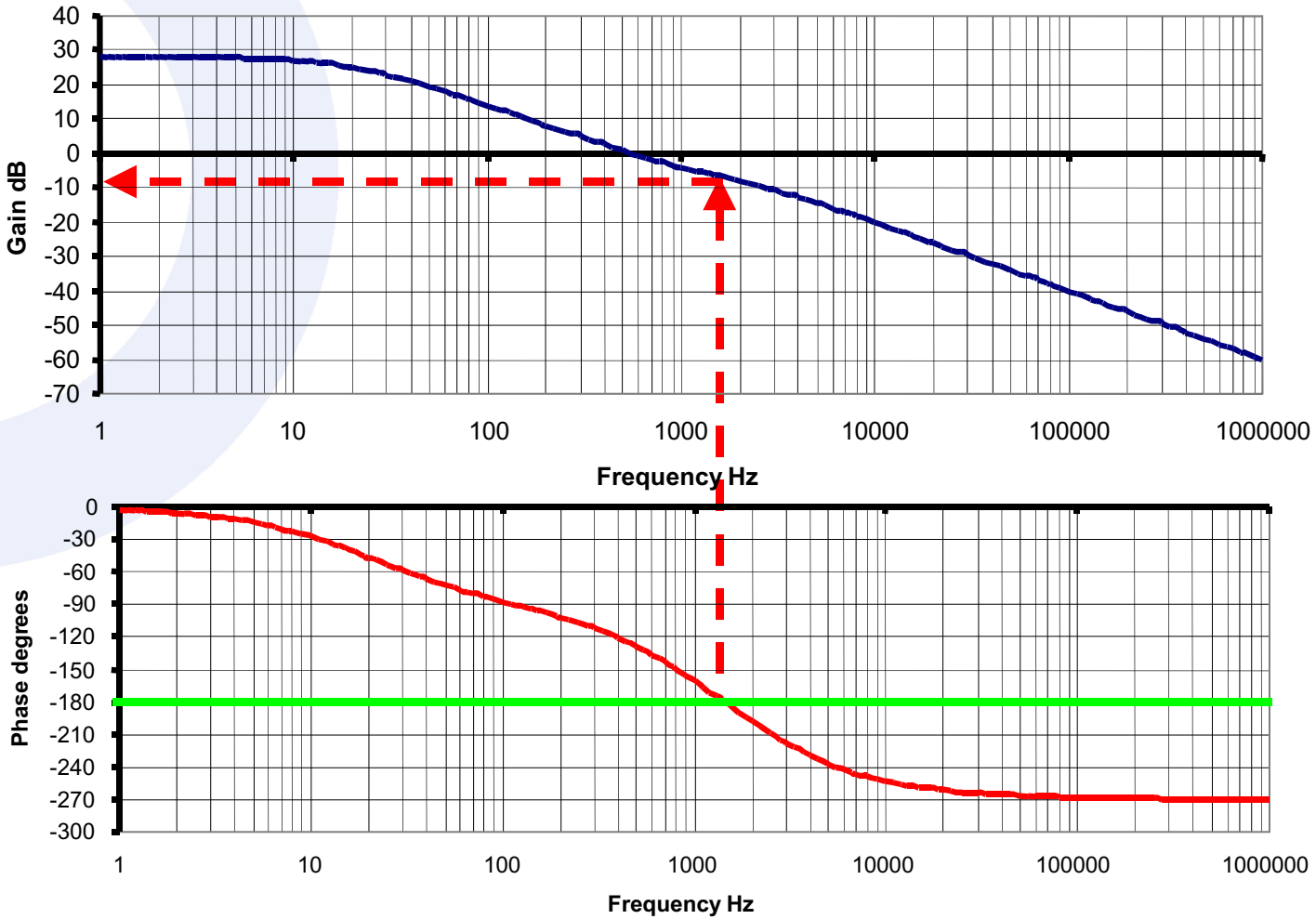
For example, if we had 62… phase margin and a crossover frequency of 3kHz

- This would result in an overshoot of 7%, with a time to first peak of less than 500us



Basic Principles: Gain Margin

- The gain margin is defined as the attenuation at -180… phase shift
- So the 6dB attenuation gives a gain margin of 6 dB
- If the gain rises by 6dB the loop will be unstable



Basic Principles: Laplace transforms

- We have used expressions for the transfer functions of the phase shift elements using j_
- This form of the transfer function is valid for the sinusoidal steady state
- To be more general, we write transfer functions in terms of s when we are not specifically focused on sinusoids
- The transfer function F(s) of a system block F(s) is derived from the Laplace transform of f(t)
  - The Laplace transform integral is shown for reference
  - f(t) is the response of the system block to an impulse

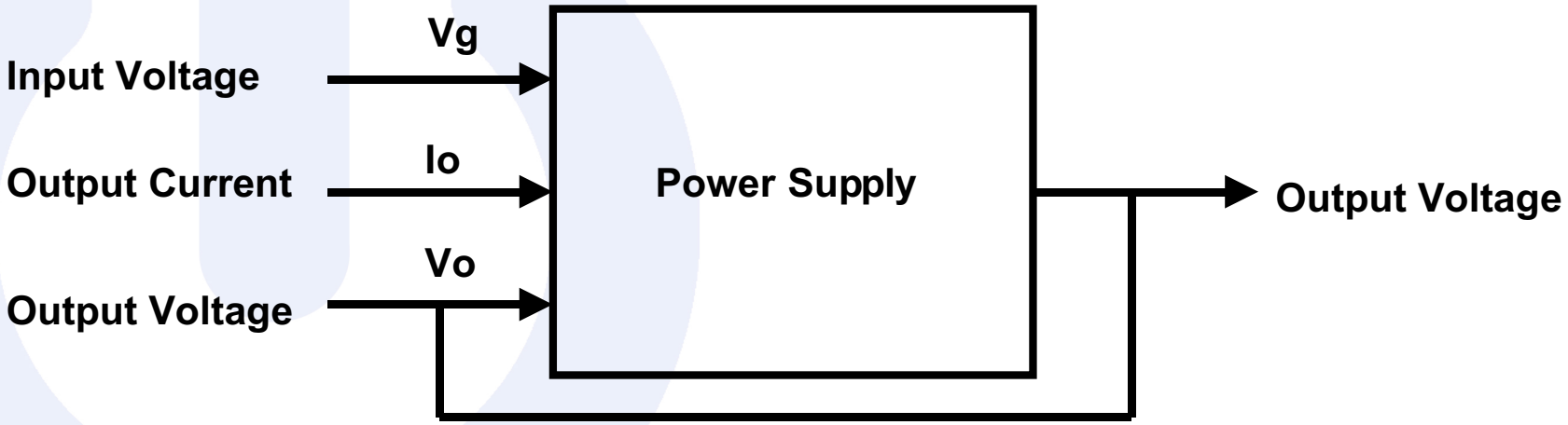
$$F(s) = \int_0^{\infty} f(t)e^{-st}dt$$

$$s = \sigma + j\omega$$

$$\sigma = 0 \text{ for sinusoidal steady sta}$$

$$s = j\omega$$

Transfer Functions for Power Supplies



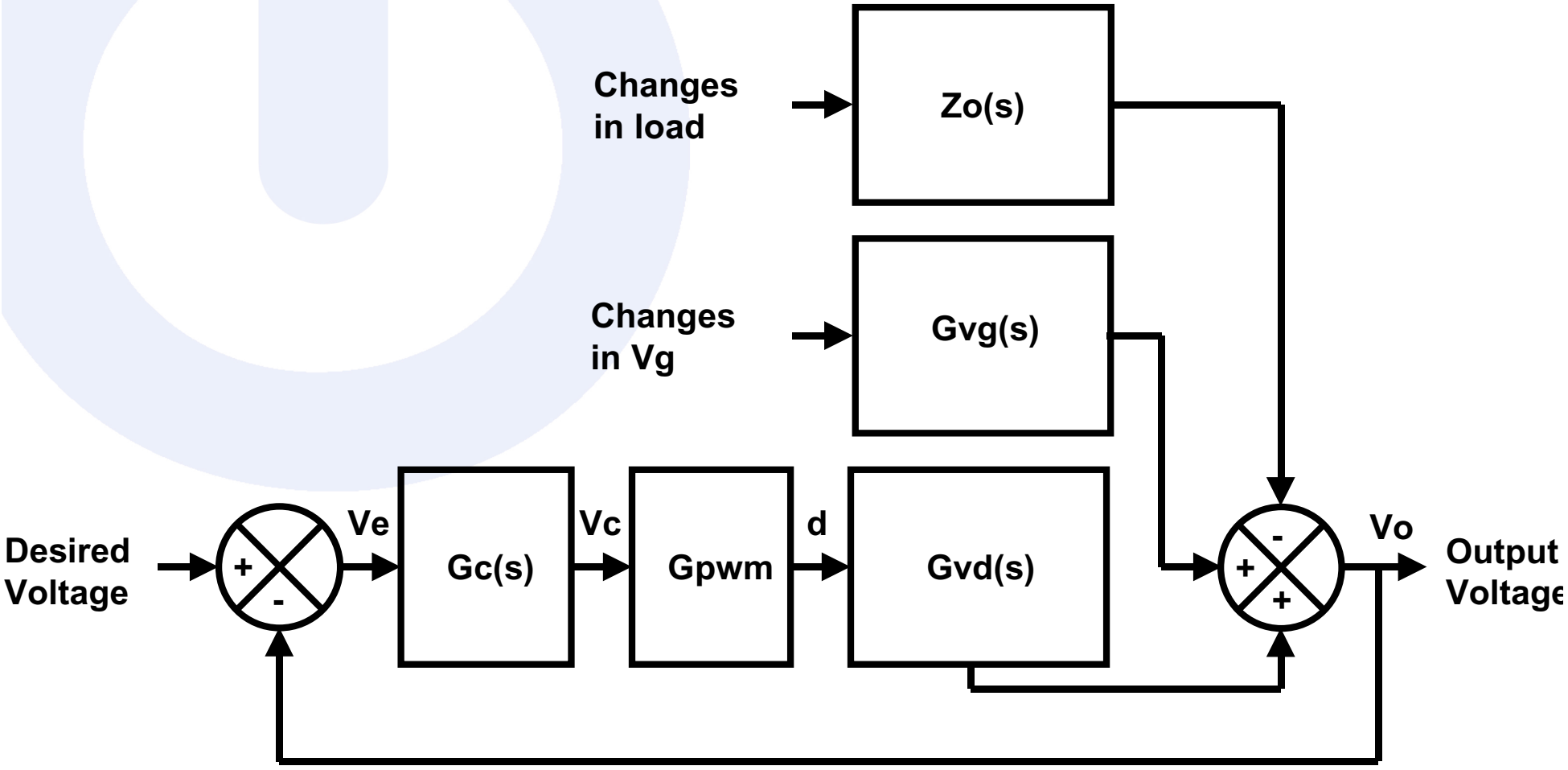
A power supply must respond to changes in three separate parameters. The transfer functions for these parameters needs to be known to understand these changes

- **The input voltage** **Gvg(s) input to output**
- **The output current** **Zo(s) output impedance**
- **The output voltage**

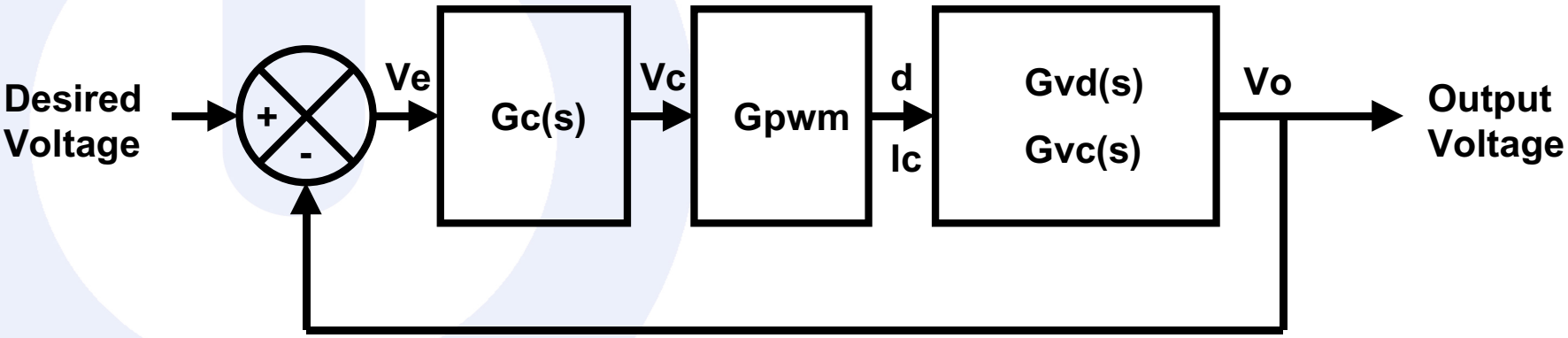
The output voltage control loop is usually defined in terms of the control to output transfer function, and not the voltage error to output transfer function

- **Voltage mode/duty cycle control** **Gvd(s) control to output**
- **Current mode/current programmed control** **Gvc(s) control to output**

Output Control Loop Including Load and Line Effects



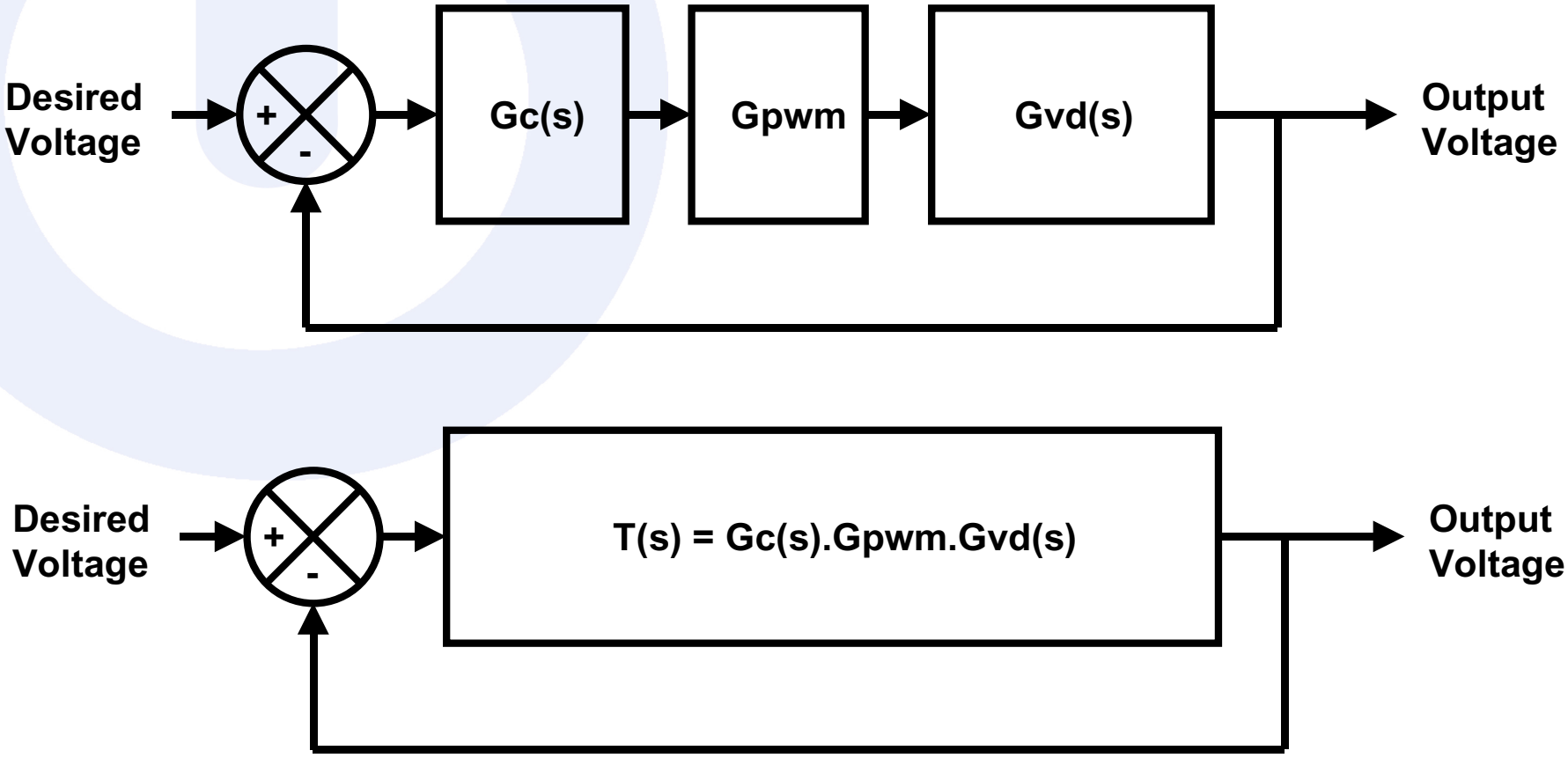
Output Voltage Control Loop



There are four elements in the output voltage control loop

- The subtractor element, which generates an error signal by subtracting the desired voltage from the output voltage
- The compensator element, Gc(s), added by the designer to stabilize the loop and improve the loop performance (more about what this improvement gives us later)
- The PWM element Gpwm which defines the relationship between the compensator output signal and the duty cycle/current-mode control current (more about this later)
- The control-to-output transfer function Gvd(s) or Gvc(s)

Output Voltage Control Loop —T(s) as Loop Gain



Composite Transfer Function for Power Supply

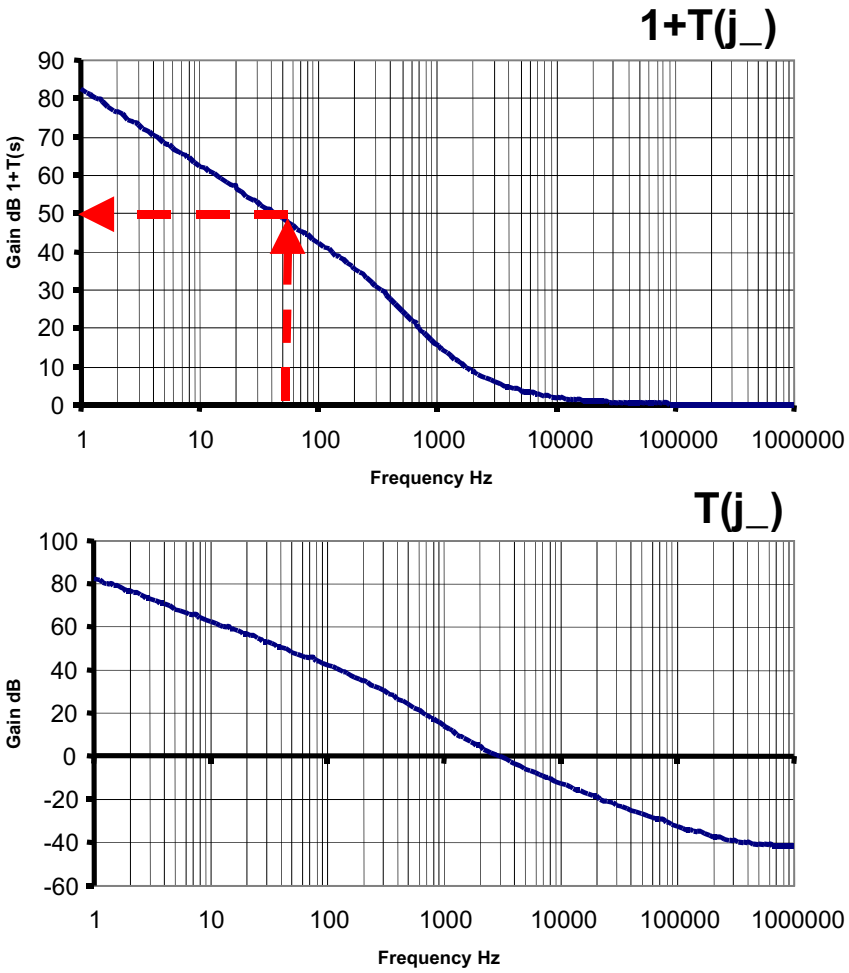
$$v = v_{ref}\frac{T(s)}{1+T(s)} + v_g\frac{Gvg(s)}{1+T(s)} - i_o\frac{Zo}{1+T(s)}$$

$$T(s) = Gc(s) \times Gpwm \times Gvd(s)$$

- The effect of changes in the set point, the input voltage and the output current on the output voltage is shown in the above equation
- The T(s) term corresponds the loop gain we have discussed in the introductory session
  - In the basic session we plotted the frequency and phase of T(j_)
- The open loop responses Gvg(s), Zo(s) and Gvd(s) are reduced by a factor of 1+T(s) if they are put into a unity gain closed loop. We will now review why this is important.

Importance of 1+T(s)

- If T(j_) is large at low frequency, 1+T(j_) will also be large at low frequency
  - On a gain plot, it will be difficult to tell the difference
- The closed loop will make changes in the output voltage caused by changes in the input voltage 1+T(j_) times smaller
- So a high gain helps to have a high rejection of changes in the input voltage, similarly for the output load, and disturbances in the duty cycle
- But gain cannot be high for all frequencies
  - The loop would be unstable
- So we recommend high gain at low frequencies only, which gives good low frequency ripple rejection



Power Supply Controller Requirements

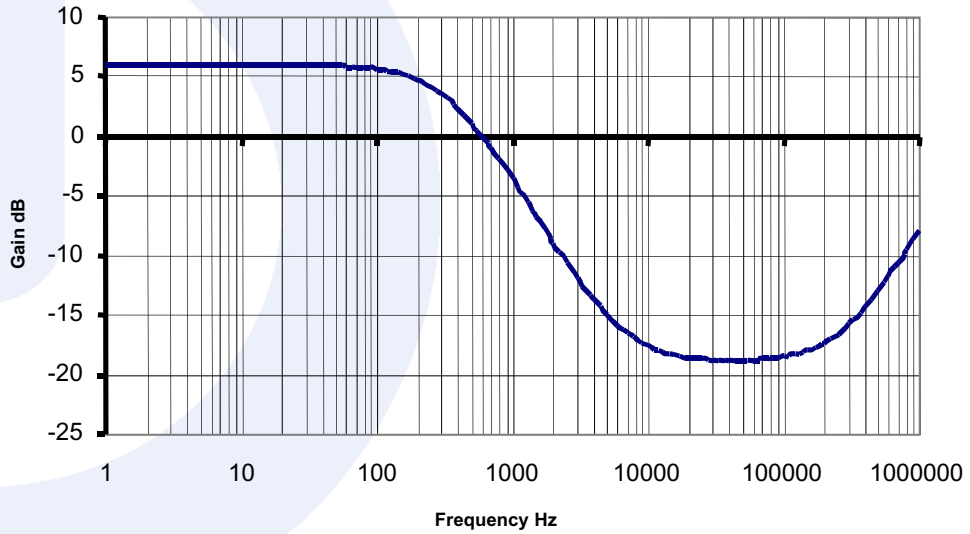
- Make the control loop stable
  - Provided by adequate phase margin
- Provide a sufficiently fast response
  - Provided by sufficiently high crossover frequency
- Provide an acceptable level of output damping
  - Provided by adequate phase margin
- Have a high gain to desensitize response to changes in line and load
  - This is achievable in reality at low frequency
- Minimize the steady state error to a step response
  - This is achieved by an integrator pole (1/s term) in the controller
  - This helps with low frequency rejection

Flyback Converter Design Example

- The next section focuses on the design of a controller for a continuous conduction mode (CCM) current mode flyback converter
- The design example will be covered in a number of steps
  - Selection of suitable parameters for the controller based on the gain and frequency plots discussed earlier
  - Implementation of the controller in an electronic circuit and discussion of some practical circuit aspects
  - Review of how the flyback circuit will respond to step changes in operating conditions
  - A review of how the operating conditions change these transfer functions

Plot For Uncompensated Current Mode Flyback Converter

Gpwm←Gvc(s)

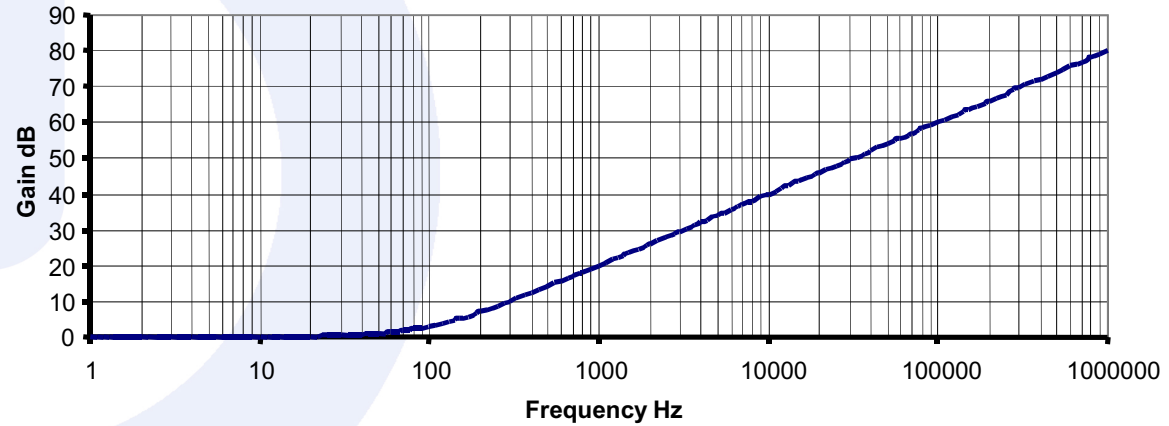


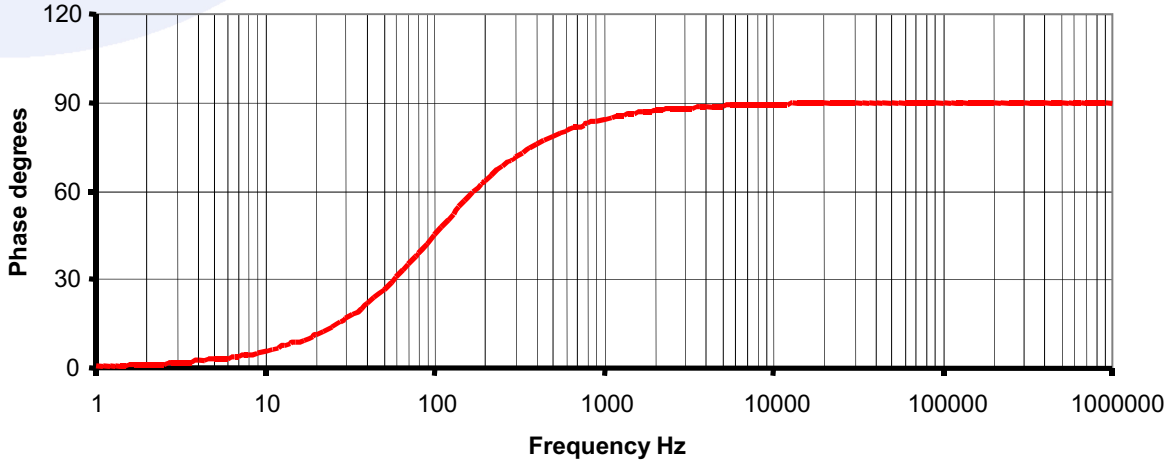
- The starting point is the transfer function for a selected current mode CCM flyback converter
- Our objective is to design a compensator for this converter to improve its performance
- Because of our focus on building the controller, we will not discuss the CCM flyback transfer function right now
  - As this is an important topic, we will review this later

Controller Elements

- Off-line power supplies based on flyback converters often use a feedback control circuit which provides the following elements
- An integrator pole
  - Improves low frequency rejection
  - Minimizes steady state error to step response
- A normal zero
  - INCREASES the phase at the desired crossover frequency
- A normal pole
  - The pole and zero are treated together as a pair as will be shown

Normal (Left Half Plane) Zero at 100Hz





Control Loop Optimization for Flyback Converter

- Step 1: Determine the loop gain without a compensator
  - We will assume this is given to us for the moment
  - This topic will be explored in detail later
- Step 2: Select the desired crossover frequency
- Step 3: Using the pole/zero pair, generate enough phase boost to ensure the correct phase margin at the desired crossover frequency
  - Remember that the integrator pole will add -90..phase shift
- Step 4: Set the gain of the integrator to zero out the gain at the crossover frequency
- Step 5: Combine the elements and review the resulting response

- Tools to help with this
  - Spreadsheet to generate the frequency and phase plots

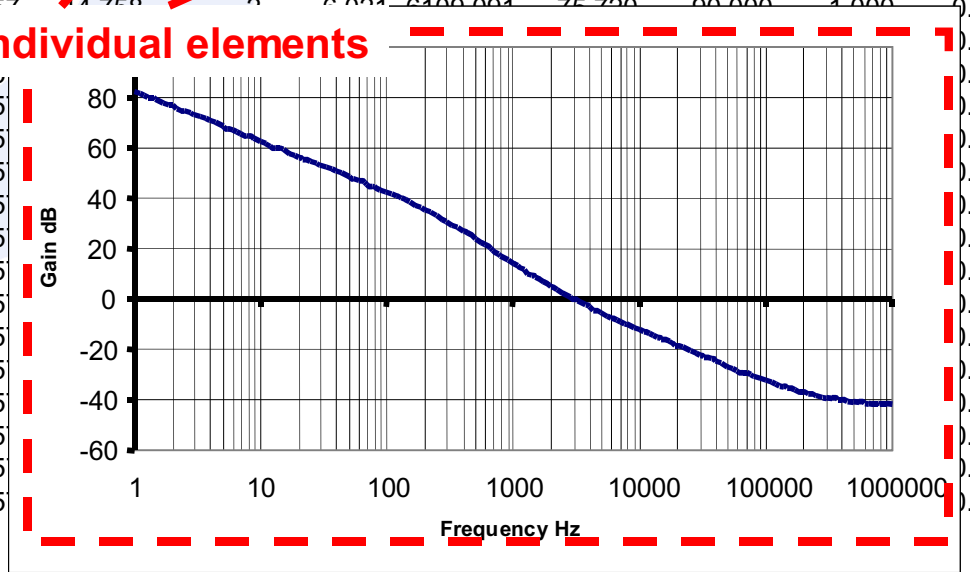
Spreadsheet to Generate Frequency and Phase Plots

For the chosen elements, fill in the one or two details

Output	PWM Gain	Gain	Integrator	Pole	Zero
	0.182857	2	6720 Hz (unity gain)	5200 Hz	1730
Active	NO	YES	YES	YES	YES

f/Hz	Gain dB	Phase deg	Gain	Inactive	Gain	Gain dB	Gain	Gain dB	Phase deg	Gain	Gain dB	Phase deg	Gain
1	82.56795	-90.13439	0.182857	-14.758	2	6.021	6720.000	76.547	-90.000	1.000	0.000	-0.011	1.000
1.4	79.64536	-90.18815	0.18285								.000	-0.012	1.000
1.5	79.04608	-90.20159	0.18285								.000	-0.013	1.000
1.7	77.95891	-90.22847	0.18285								.000	-0.014	1.000
1.9	76.99279	-90.25535	0.18285								.000	-0.015	1.000
2	76.54725	-90.26879	0.18285								.000	-0.017	1.000
2.2	75.71936	-90.29566	0.18285								.000	-0.019	1.000
2.5	74.60897	-90.33598	0.18285								.000	-0.021	1.000
2.8	73.62455	-90.3763	0.18285								.000	-0.022	1.000
3	73.02525	-90.40317	0.18285								.000	-0.024	1.000
3.3	72.19733	-90.44349	0.18285								.000	-0.028	1.000
3.7	71.20347	-90.49724	0.18285								.000	-0.031	1.000
4	70.52623	-90.53755	0.18285								.000	-0.033	1.000
4.4	69.69826	-90.5913	0.18285								.000	-0.036	1.000
											.000	-0.041	1.000
											.000	-0.044	1.000
											.000	-0.048	1.000

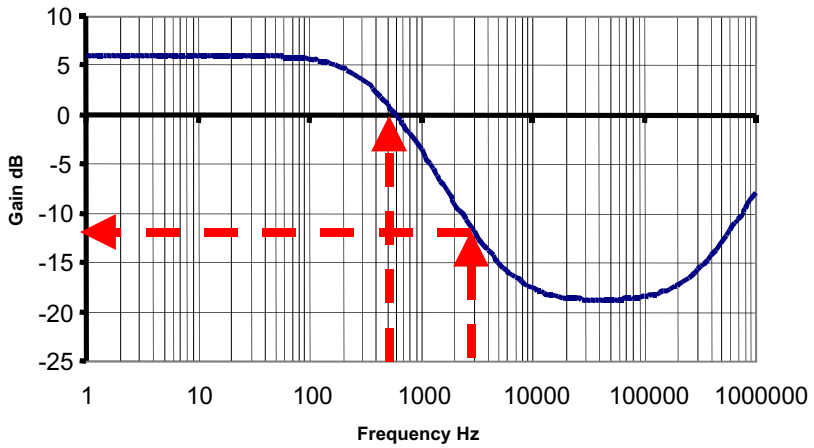
Type YES to activate individual elements

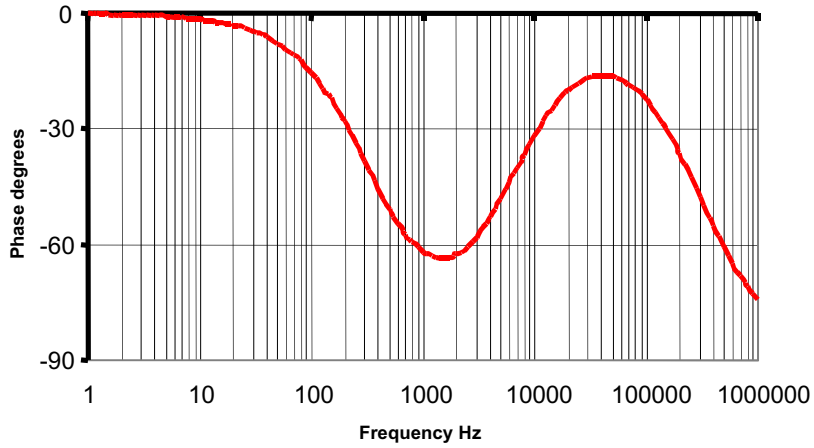


The gain plot and phase plot (not shown here) are automatically calculated

Select the Desired Crossover Frequency

- The following plots show the uncompensated transfer function for our selected example
- Set the crossover frequency fc to 3kHz
  - The crossover frequency should be well below any RHP zeros
- The gain at 3kHz is -11.8dB
  - The phase is -58…
- The phase shift seems to be very low. However, we will be adding an integrator which gives a constant phase shift of -90…
- Select the desired phase margin to be 60…
  - As we have -150..phase including the integrator, we need +30… phase shift





Phase Boost of Pole/Zero Pair

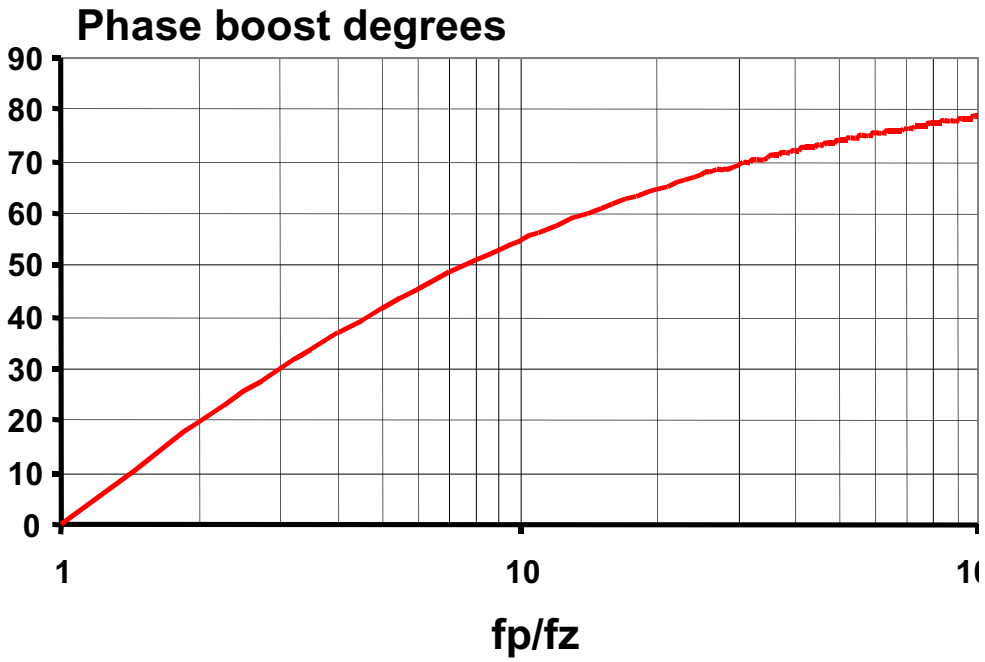
The phase boost of a pole/zero pair is maximum at frequency fc where:

— $fc^2 = fp \times fz$ where fp > fz

The pole should always have a higher frequency than the zero

The further apart the pole and the zero are, the higher the phase boost

— Typical values for boost are 30… to 60…

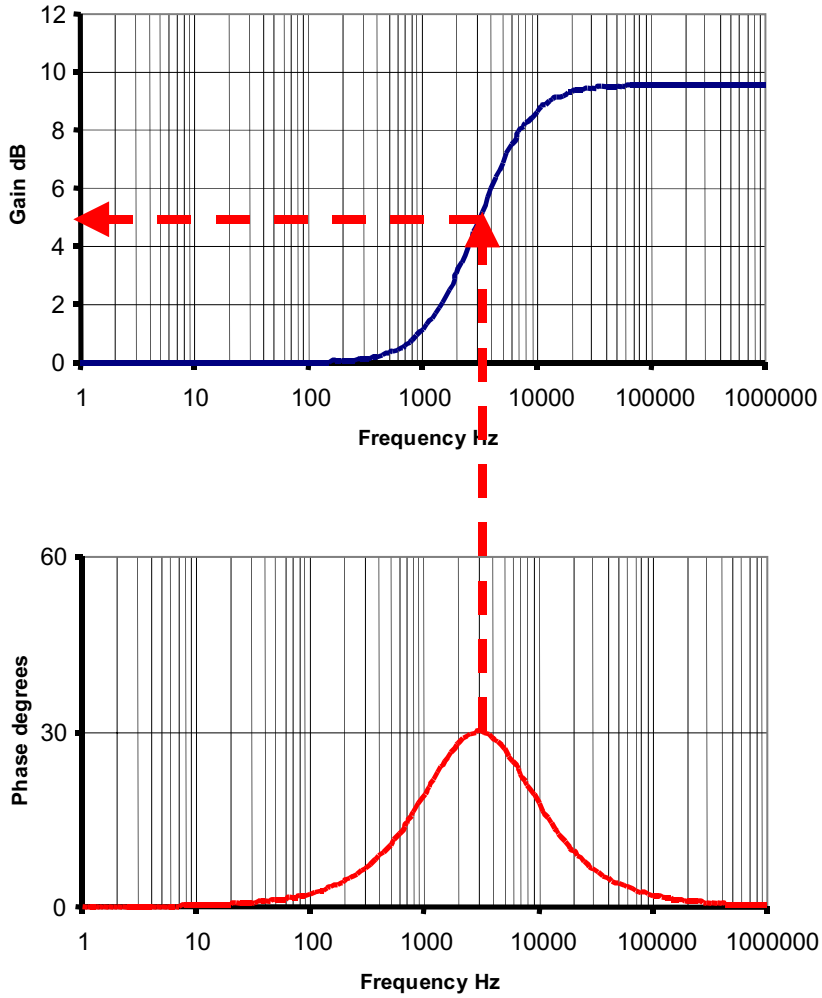


Formulas for calculating the gain and phase boost exist

— It is quicker putting in trial numbers with the spreadsheet to get to the answer

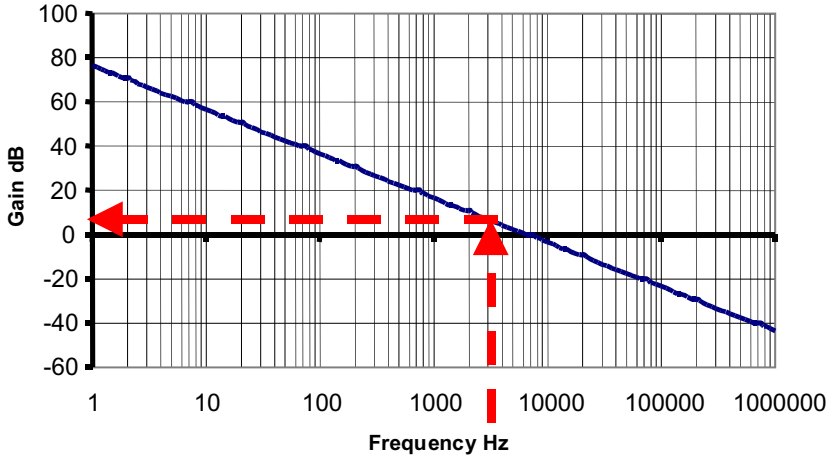
Phase Boost of Pole/Zero Pair —Resulting Data

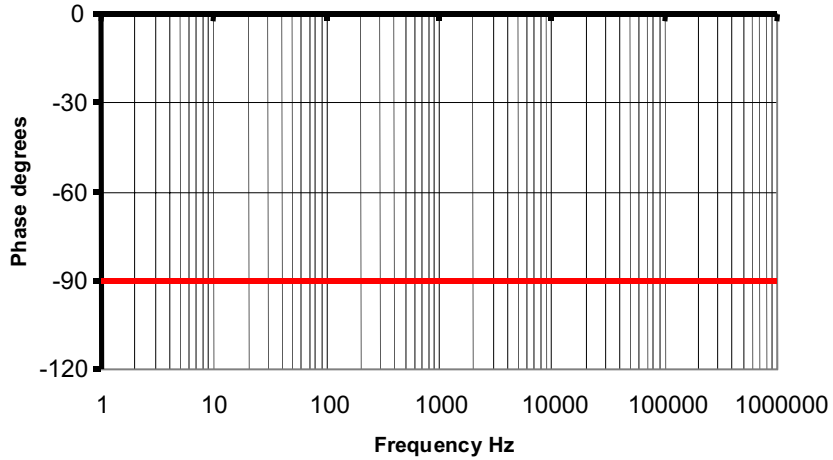
- For our example, we need a phase boost of 30…
- Using the spreadsheet, activate just one pole and one zero
- Select the zero to be 1kHz to start
- Set up a formula to calculate the pole as 3000*3000/fz (where fc=3kHz)
- Moving the zero nearer to 3kHz generates less phase boost. Change the value until the desired phase boost is reached
- fz =1.7kHz (zero) and fp = 5.3kHz (pole) gives a phase boost of 30…
- The gain at fc=3kHz is read to be +4.78dB



Integrator Gain Chosen to Set the Gain At fc to 1 (0db)

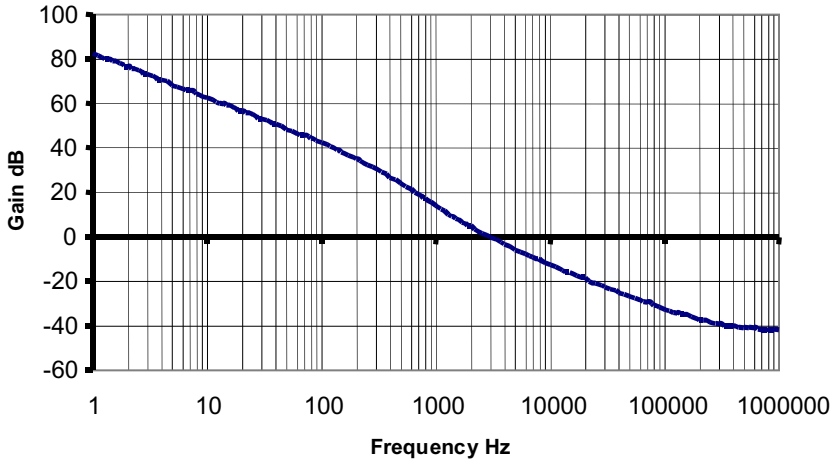
- From before
  - The gain of the uncompensated loop at fc = 3kHz is -11.8dB
  - The gain of the pole/zero pair at fc = 3kHz is 4.78dB
- The total gain excluding the integrator is -7dB, so the integrator gain at 3kHz needs to be +7dB to compensate for this
- In the spreadsheet, adjust the integrator unity gain frequency to get 7dB gain at 3kHz
- The frequency which meets this, fi, is found to be 6.72kHz

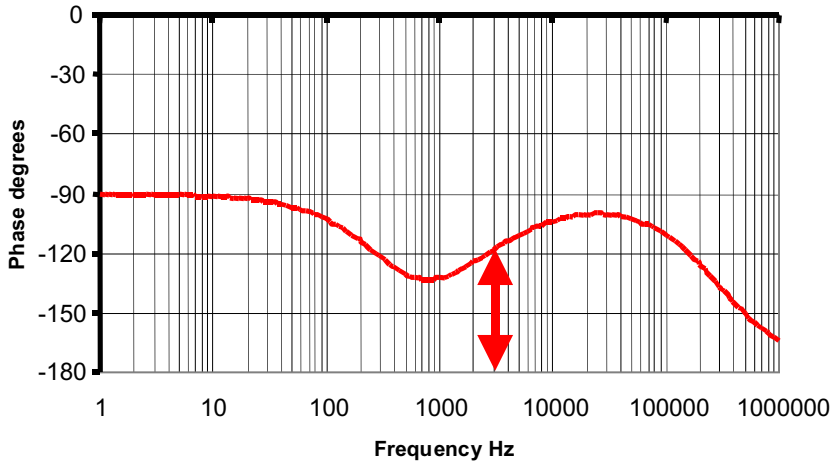




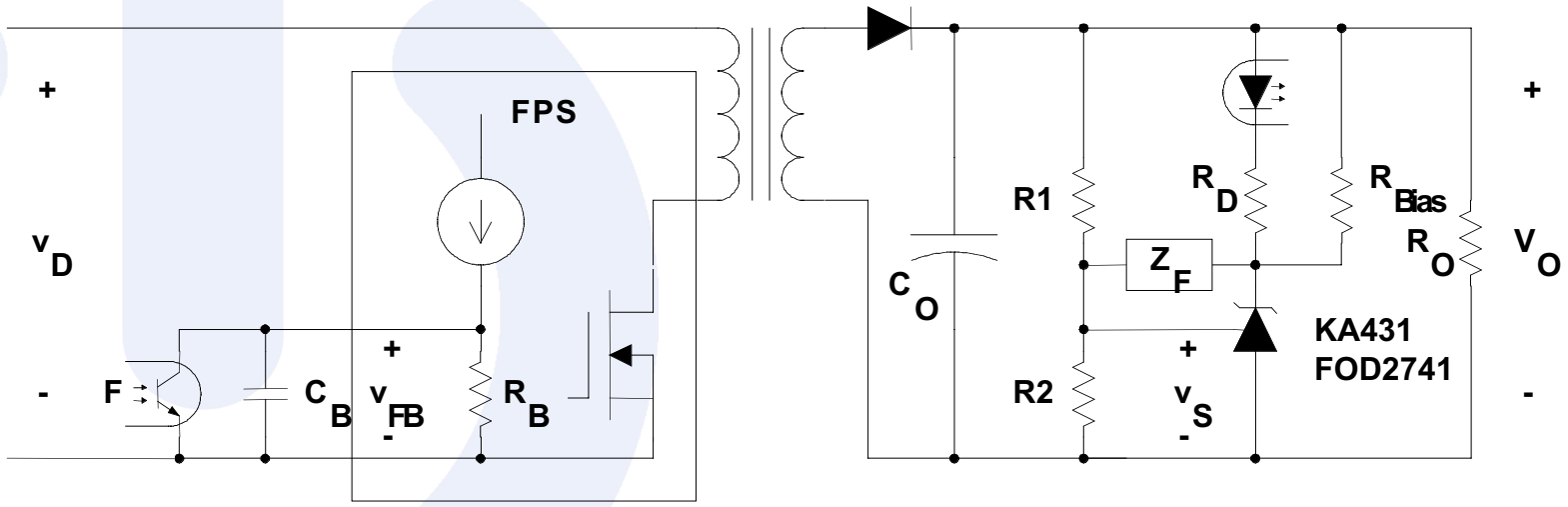
Final Result

- The phase margin is 62…
- The crossover frequency is 3kHz
- The control loop is stable as the phase shift is less than -180..at the crossover frequency
- The control loop is fast
- The control loop is adequately damped
- The control loop has a high gain at low frequencies which
  - Desensitizes the loop to low frequency changes in input voltage and output load
  - Has a 1/s term in the loop gain which gives zero steady state error to a step response





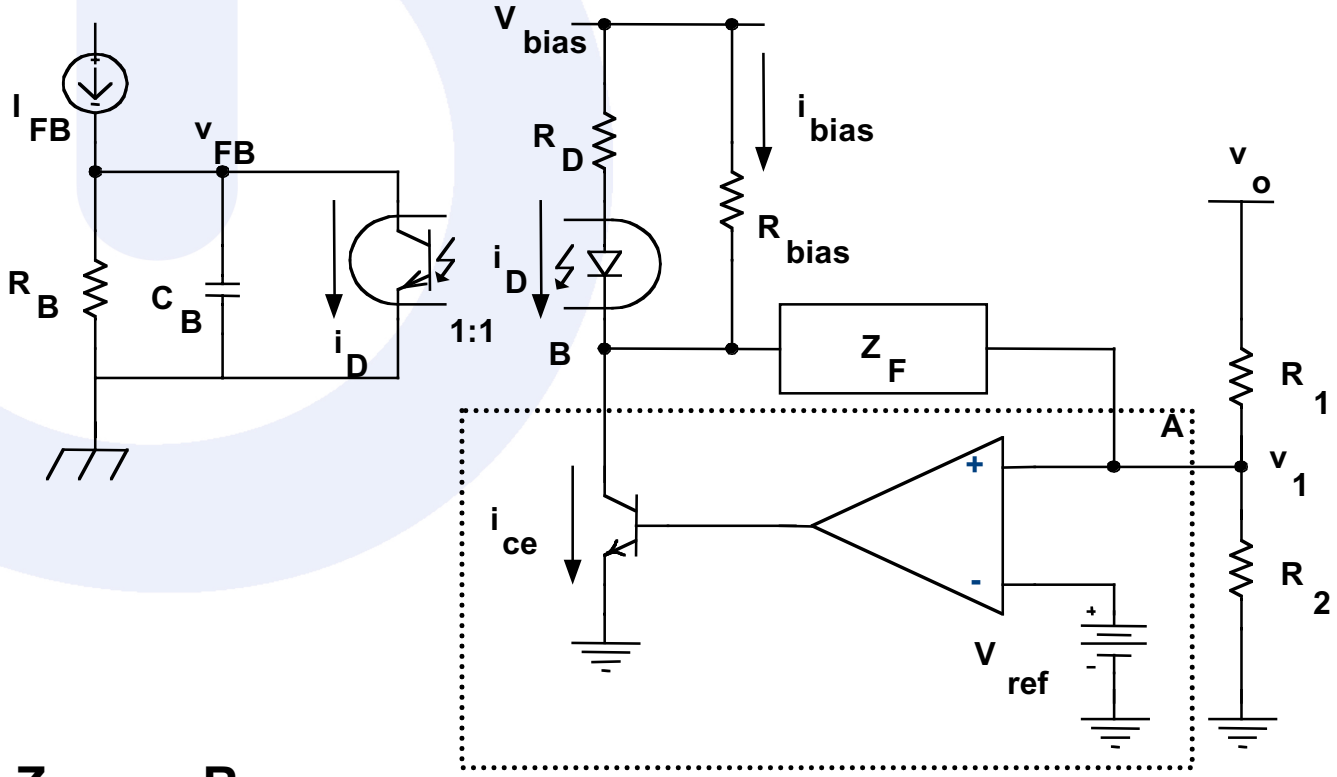
Implementation of the Controller Circuit



This circuit shows how the controller is implemented in practice

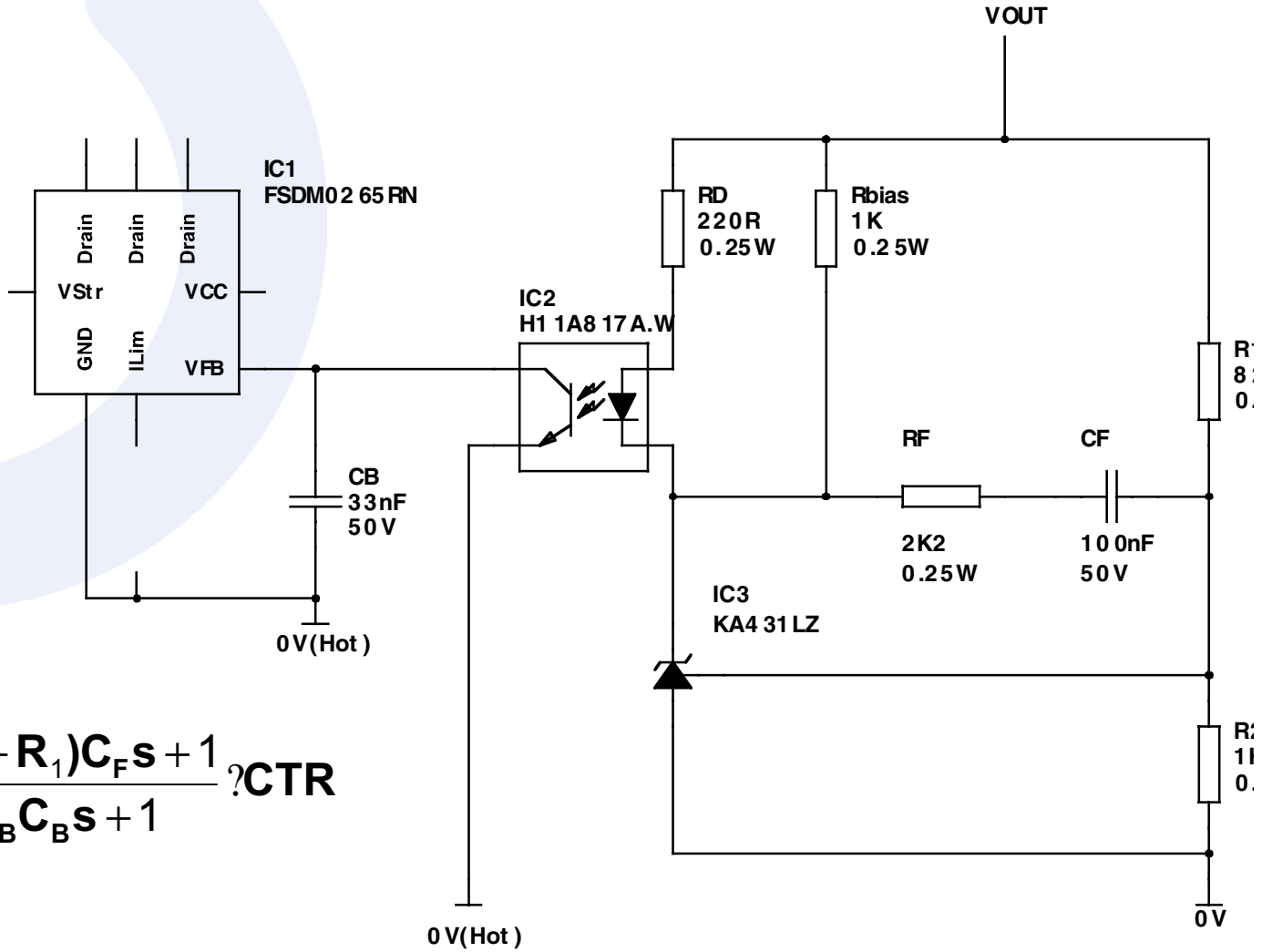
- The output voltage Vo is fed into the potential divider formed by R1 and R2
- The node formed by R1 and R2 is set to 2.5V by the KA431 reference
- The division ratio of R1/(R1+R2) is selected to give 2.5V at the desired output voltage
  - For example, for 5V output, R1 and R2 are set to be equal
- Small signal increases in the output voltage cause small signal increases in the opto-coupler LED current which are transmitted to the PWM controller (on the left) via the optocoupler
  - This reduces the PWM controller Vfb voltage, which will then ultimately reduce the output voltage

Small Signal Transfer Function for Generic Circuit



$$\frac{\hat{v}_{FB}}{\hat{v}_o} = -\frac{Z_f}{R_1 R_D} \cdot \frac{R_B}{R_B C_B s + 1} \cdot CTR$$

Small Signal Transfer Function for Standard Circuit



$$\frac{\hat{V}_{FB}}{\hat{V}_o} = -\frac{R_B}{R_1 R_D C_F s} \cdot \frac{(R_F + R_1)C_F s + 1}{R_B C_B s + 1} \cdot CTR$$

Setting the Values of the Compensator Components

- Choosing the component which sets fp
  - RB is internal to the FPS (3kohm)
  - Set CB for the right value of fp

$$fp = \frac{1}{2\pi R_B C_B}$$

- Choosing the components which set fi
  - R1 is typically in the range 1k-10k, as a tradeoff between power consumption and noise immunity
  - RD is set by the DC bias current requirements for the optocoupler photodiode
  - Choose CF and R1 to get the right integrator unity gain frequency

$$fi = \frac{R_1 R_D C_F}{2\pi R_B}$$

$$fz = \frac{1}{2\pi (R_F + R_1) C_F}$$

- Choosing the components which set fz
  - Choose RF to get the right value of fz

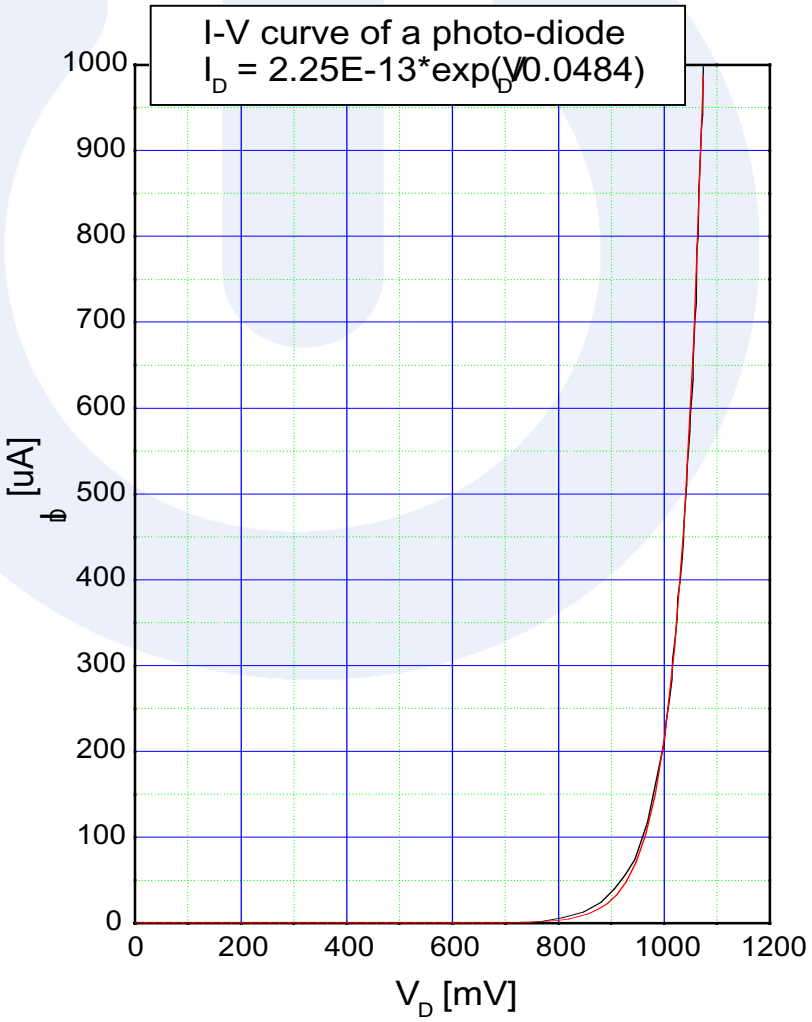
Practical Comments on the Controller Circuit

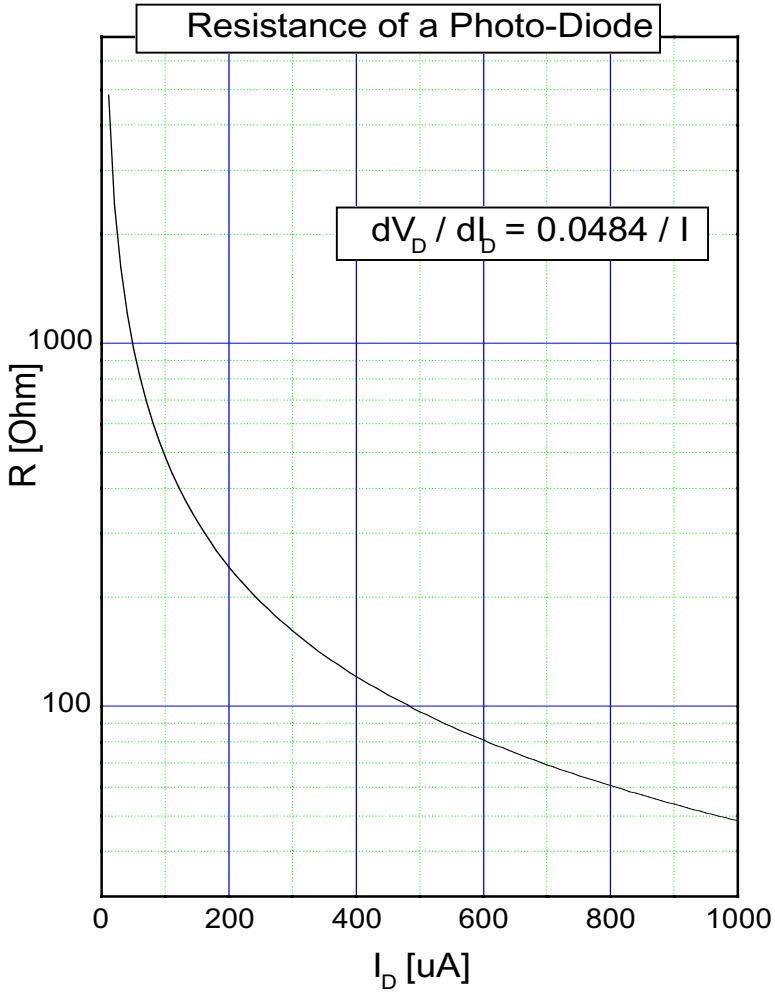
- Two components have no effect on the small signal transfer function
  - R2, the lower resistor in the potential divider
  - Rbias, the bias resistor for the KA431
- Practical tip: if the output voltage needs to be modified, change or vary R2 rather than R1
- The optocoupler generates the main source of variability
  - The CTR will vary from device to device and will reduce with temperature
  - The small signal resistance of the photodiode adds to RD in the formula. This resistance can vary from 50 ohms at light load to 5 kohm at heavy load

Practical Tips Regarding the Optocoupler

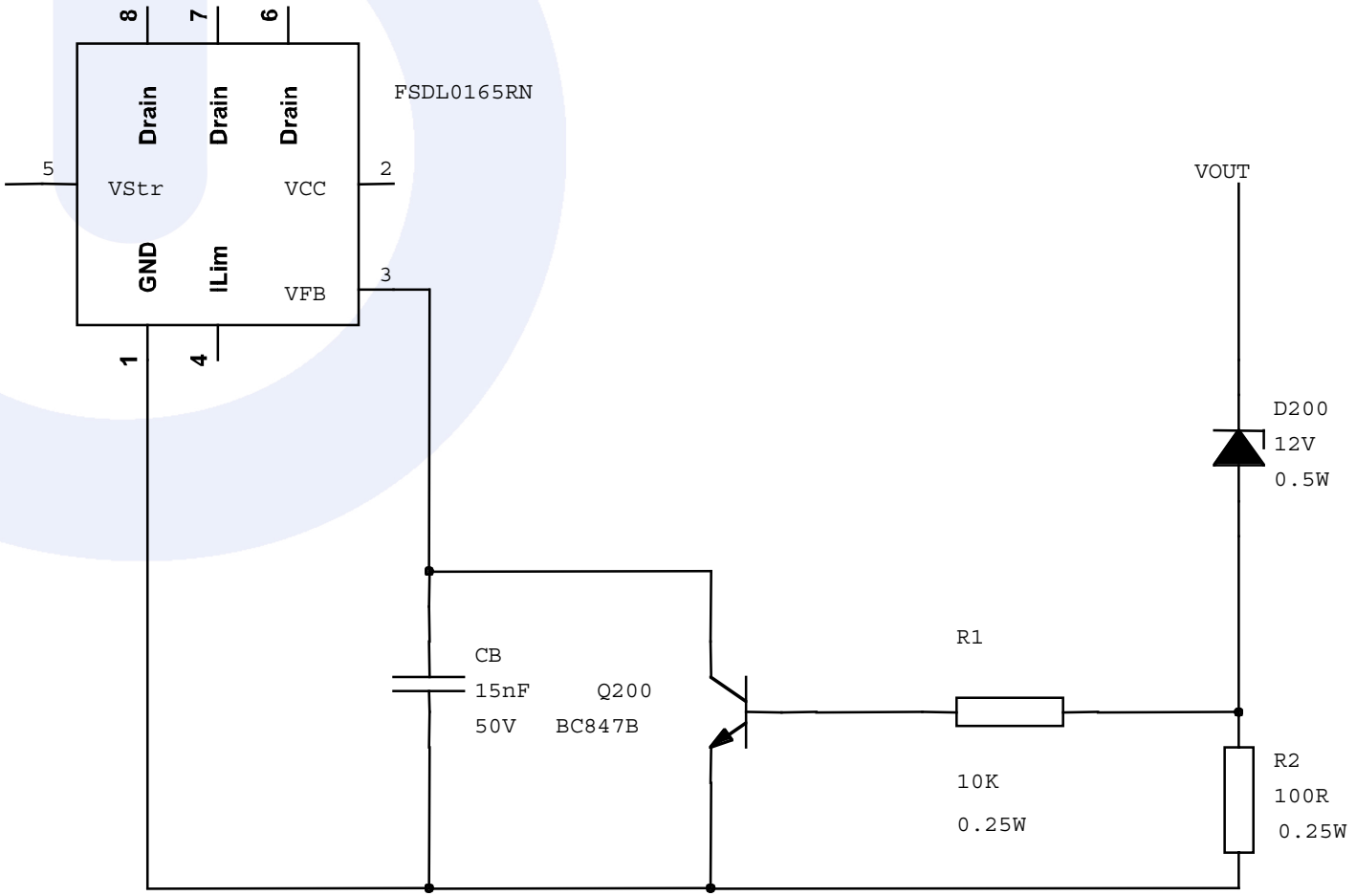
- Check the design at both light and heavy loads, and at temperature extremes.
- Check the output response for stability and adequate damping.
- The optocoupler current transfer ratio, dynamic resistance of the photodiode, and the effect on temperature of these two parameters all influence the closed loop performance
  - These aspects should be considered when considering multiple optocoupler suppliers
- If the output voltage is far higher than the setpoint, an isolated converter will drive the optocoupler into saturation
  - Confirm that the duty cycle is driven to zero in this condition

Characteristics of a Photo Diode





Low Cost Compensator Circuit



Practical Comments on the Low Cost Compensator

- Advantages
  - Low cost
  - Low component count
- Characteristics
  - The transfer function consists of a gain term, and a single pole
  - There is therefore no integrator term, or a zero
- Disadvantages
  - Slower response
  - Larger voltage output variation due to changes in load and line
    - The lack of a 1/s term in the controller forces a larger steady state error

Gain of PWM Stage

For complete analysis of the controller, we need to include the gain introduced by the PWM stage

This sets the averaged signal relationship between the feedback voltage and the duty cycle

For a voltage mode PWM controller, this is 1/Vm, where Vm is the (theoretical) voltage required to generate 100% duty cycle.

Maximum Duty Cycle	Dmax	Vfb = 3.5V	60	64	68	%
Minimum Duty Cycle	Dmin	Vfb = 0V	0	0	0	%

So Vm ranges between 3.5V/60% and 3.5V/68% for the FSD200 shown above

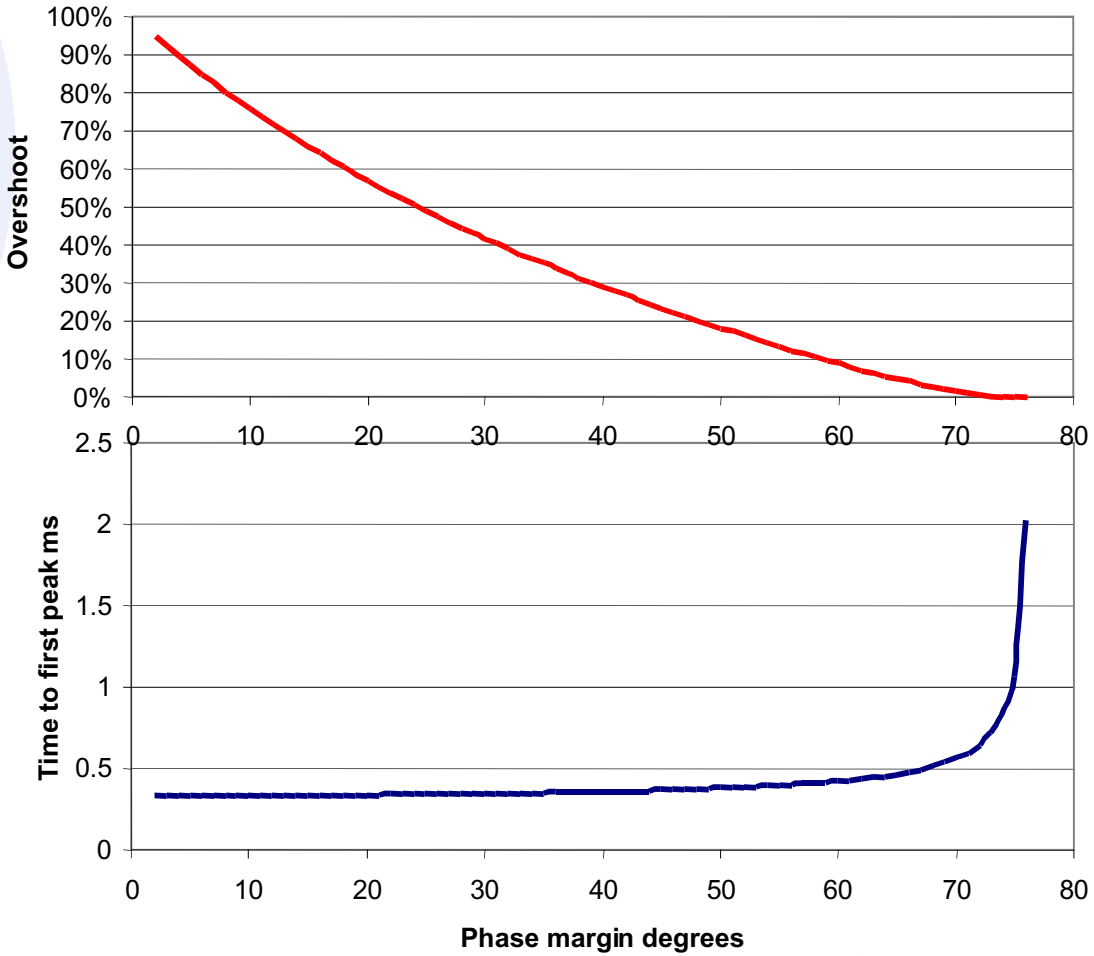
For a current mode FPS, this gain is the current limit of the FPS divided by 3V (the maximum compensator output voltage)

Response to Step Changes

- So far, we have reviewed the open and closed loop frequency responses of the flyback converter
- It is important to assess how these frequency responses affect the actual waveforms we will see on an oscilloscope when the input voltage or the load changes
- A formal mathematical analysis is one way of seeing how the closed loop transfer function affects the response to changes in inputs
  - This is done using inverse Laplace transforms and is quite detailed
- A simpler way is to approximate the closed loop transfer function to a simple second order system
  - This is not always accurate, but gives us insight into several important aspects

Effect of Phase Margin on Overshoot and Timing

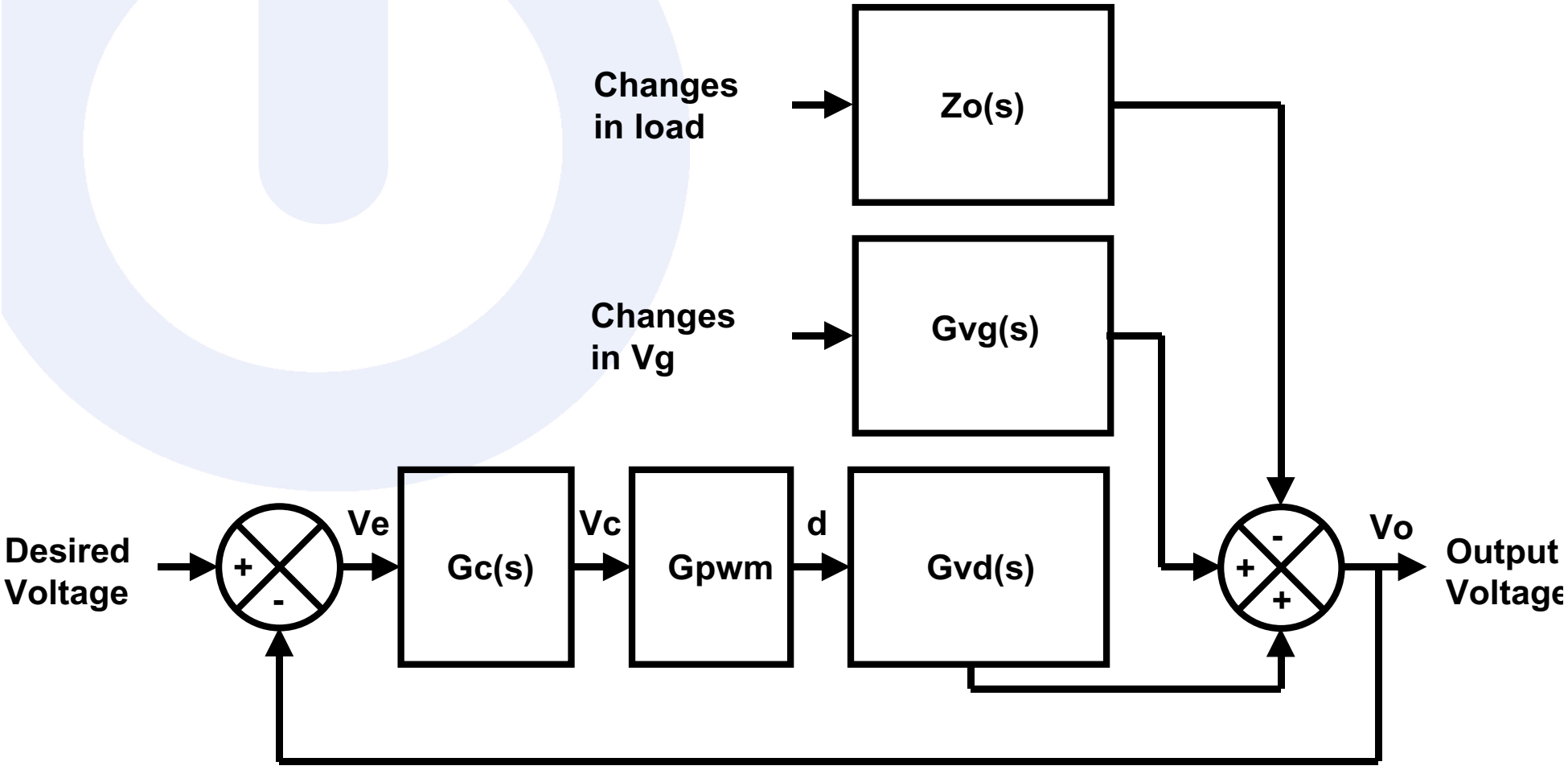
- The two plots show the relationship between
  - Phase margin and overshoot
  - Time to first peak for a crossover frequency of 3kHz
- There is no peak for a phase margin above 78 degrees
- For our example, we had 62… phase margin
  - This would result in an overshoot of 7%, with a time to first peak of less than 500us



Controlling Lower Input Voltage Topologies

- We used a CCM current mode flyback example to explain the control methodology in detail
  - Our example used an off-line system
- The same approach can be used to handle a wide range of topologies
- Fairchild Semiconductor s FAN5234/FAN5236 synchronous buck controller can be used for example to convert 24Vdc down to 3.3V
  - The FAN5234/FAN5236 uses the same type of control as discussed above using a built-in controller
  - External compensation is possible if needed
- A spreadsheet and Orcad PSPICE simulation setup is available for this part on http://www.fairchildsemi.com/collateral/AN-6002.zip

Output Control Loop Including Load and Line Effects



Comments on the Control-to-Output Transfer Functior

- The transfer functions for the common topologies buck, buck-boost, flyback and boost topologies are available in the literature
- Erickson and Maksimovic (see Literature at end) Fundamentals of Power Electronics details the methodology of the derivation which can be applied to other topologies
- The transfer functions for a given topology split up into four sets

Voltage mode CCM	Current mode CCM
Voltage mode DCM	Current mode DCM

CCM Current Mode Flyback Transfer Function

The CCM current mode transfer functions are taken from a standard reference

- Erickson and Maksimovic page 471 shows CCM transfer functions for buck/boost, buck and boost
- Fairchild Semiconductor FPS app note shows how the turns ratio is introduced and shows these equations in rearranged form as will be discussed below

The positions of the poles, zeros and gains are dependent on

- D, the actual duty cycle which varies with input voltage, and in practice, also with load
- R, the effective load resistance, which depends on the load current

$$G_{vc} = G_{c0} \frac{1 - \frac{s}{2\pi f_{rhpzero}}}{1 + \frac{s}{2\pi f_{pole}}}$$

where

$$G_{c0} = \frac{1-D}{1+D} \cdot \frac{n_p}{n_s} \cdot R \quad \text{gain}$$

$$f_{rhpzero} = \frac{(1-D)^2 R}{2\pi D L_p} \cdot \frac{n_p^2}{n_s^2} \quad \text{RHP zero}$$

$$f_{pole} = \frac{1+D}{2\pi RC} \quad \text{pole}$$

CCM Current Mode Flyback Transfer Function

- A CCM flyback converter working in current mode has
  - A gain, dependent on duty cycle and independently, the load
  - A pole, dependent on duty cycle and load
  - A right half plane zero, dependent on duty cycle and load
- The duty cycle in CCM is dependent mainly on the input voltage, and to some extent the variations in losses as the load changes
- In general, the transfer function of a switching regulator will vary significantly under load and line conditions
- An additional complexity is that under light load conditions, the converter will switch to DCM operation, further changing the transfer function
  - The changes for current mode controllers are less than for voltage mode controllers

Flyback and Buck-Boost Gvd(s) and Gvc(s) Structur

Voltage mode CCM Gvd(s)

Gain	
RHP Zero	**max —90…**
Complex pole	**max —180…**

Current mode CCM Gvc(s)

Gain	
RHP Zero	**max —90…**
Single pole	**max —90…**

Voltage mode DCM Gvd(s)

Gain	
Single pole	**max —90…**

Current mode DCM Gvc(s)

Gain	
Single pole	**max —90…**

Buck Gvd(s) and Gvc(s) Structure

Voltage mode CCM Gvd(s)

Gain

Complex pole **max —180…**

Current mode CCM Gvc(s)

Gain

Single pole **max —90…**

Voltage mode DCM Gvd(s)

Gain

Single pole **max —90…**

Current mode DCM Gvc(s)

Gain

Single pole **max —90…**

How to Estimate D in Terms of Vo and Vg

- The duty cycle is an unknown parameter
- We know the input voltage Vg, the output voltage Vo and the turns ratio n
- We know the voltage conversion relationship for a flyback converter
  - This can be derived from first principles or taken from a standard text
- Based on this, we can rewrite the gain, pole and zero equations in terms of Vg, Vo and n.

$$\frac{V_o}{V_g} = \frac{D}{n(1-D)}$$

$$D = \frac{nV_o}{nV_o + V_g}$$

$$n = \frac{n_p}{n_s}$$

$$V_{RO} = nV_o$$

$$\frac{1-D}{1+D} = \frac{V_g}{2nV_o + V_g} = \frac{V_g}{2V_{RO} + V}$$

Gvc(s) for Multiple Output Flyback

- The transfer function is now written in the form used in the Fairchild Power Switch Designer tool and application note
- As flyback very often have multiple outputs, the load resistance is calculated in a slightly different way than for a single output solution
  - Po is the total output power for all outputs
  - Vo here is the output voltage for the controlled outputs
  - The total effective load resistance R is calculated as shown

$$G_{c0} = \frac{V_g}{2nV_o + V_g} \cdot \frac{n_p}{n_s} \cdot \frac{V_o^2}{P_o}$$

$$f_{rhpzero} = \frac{(1-D)^2 R}{2\pi D L_p} \cdot \frac{n_p^2}{n_s^2}$$

$$f_{pole} = \frac{1+D}{2\pi RC}$$

$$R = \frac{V_o^2}{P_o}$$

How the Parameters Change with Line and Load

- The table shows how the input voltage and output power influence the transfer function
- The right half plane zero dramatically reduces at lower input voltages and at higher powers
- The simple pole frequency increases with increasing power and to a lesser extent with decreasing input voltages
- The gain increases with input voltage and input power
- In our FPS design tools, the plots are calculated for maximum power, minimum voltage

Vg	120	375	120	375	120	375	V
Po	16	16	10	10	5	5	W
Gain	1.8	2.8	2.9	4.6	5.9	9.1	ratio
Frhp	5,493	54,299	22,923	226,843	183,385	1,814,742	Hz
Fp	469	398	291	247	146	124	Hz

Further Issues to Consider

Effect of the equivalent series resistance of the output capacitor

- This introduces a zero into the transfer function
- This is no problem if the zero has a frequency much higher than fc
  - The frequency is 1 / (2„ x ESR x Cout)
- In our example we included this: ESR=38mohm Cout=680uF (6.2kHz)
- This is included in our FPS analysis software

For a flyback converter, the effect of the output LC filter used to filter the spikes generated by the equivalent series resistor of the flyback capacitor

- This is no problem if the pole has a frequency much higher than fc
  - The frequency is 1 / (2„ x sqrt(LC))

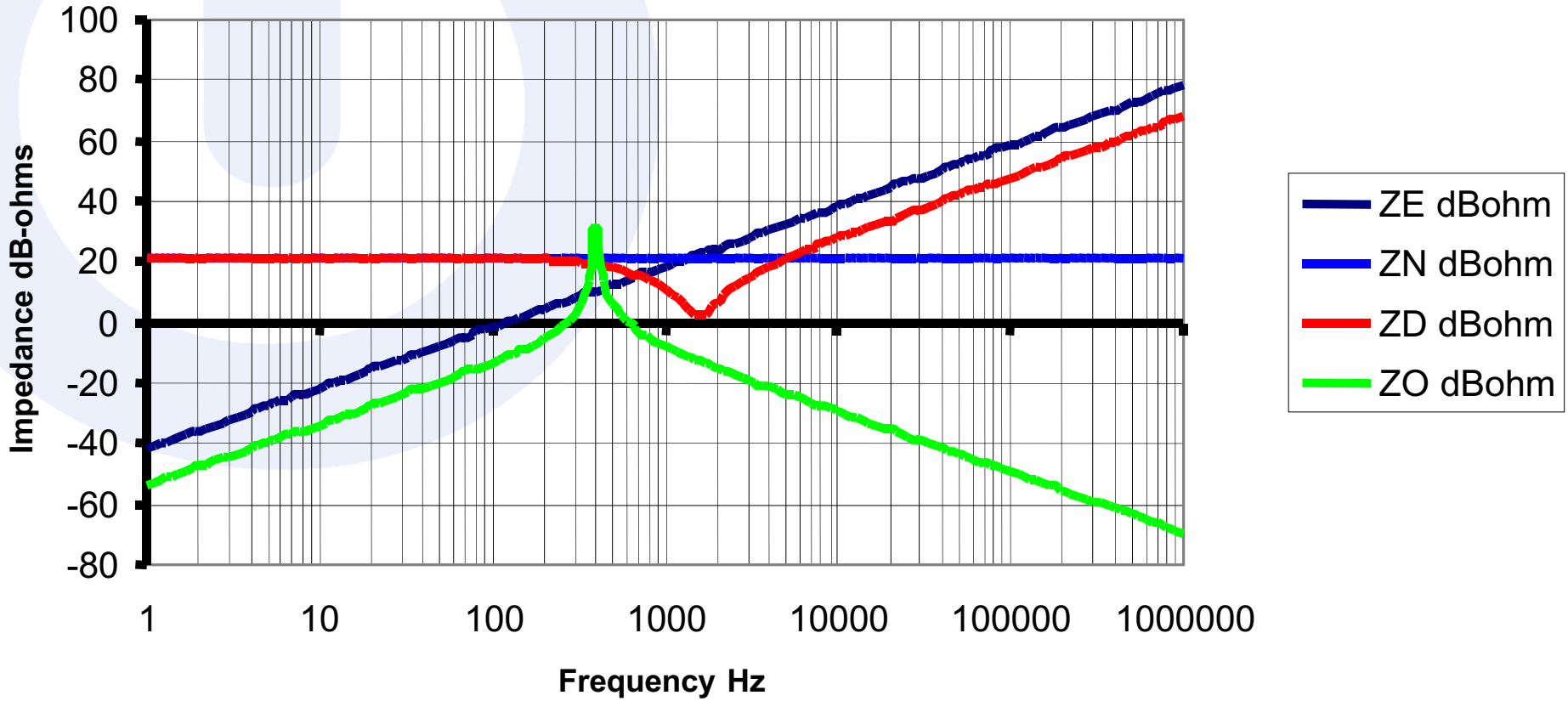
The effect of the input filter

- Incorrectly dimensioned input filters can destabilize a power supply

Effect of Input Filter on the Stability of a Converter

- The detailed analysis of this is quite complex
- Erickson and Maksimovic (p382) propose a simplified methodology to determine whether the stability of a power supply is adversely influenced by the input filter
- Explained in graphical terms
  - Plot the curves for the input impedance of the converter for three defined conditions
    - Zn(j_) (with d(s) set to 0)
    - Zd(j_) (with d(s) set such that v(s) = 0)
    - Ze(j_) (with Vout shorted to 0V)
  - These terms depend on the load resistance, the inductor value, the capacitor value and the duty cycle
  - Plot the curve for the output impedance of the input filter, Zo(j_)
  - The curve for Zo(j_) should be well below the other curves

Graphical Analysis of the Effect of the Input Filter



Practical Comments on the Input Filter

To prevent any problems:

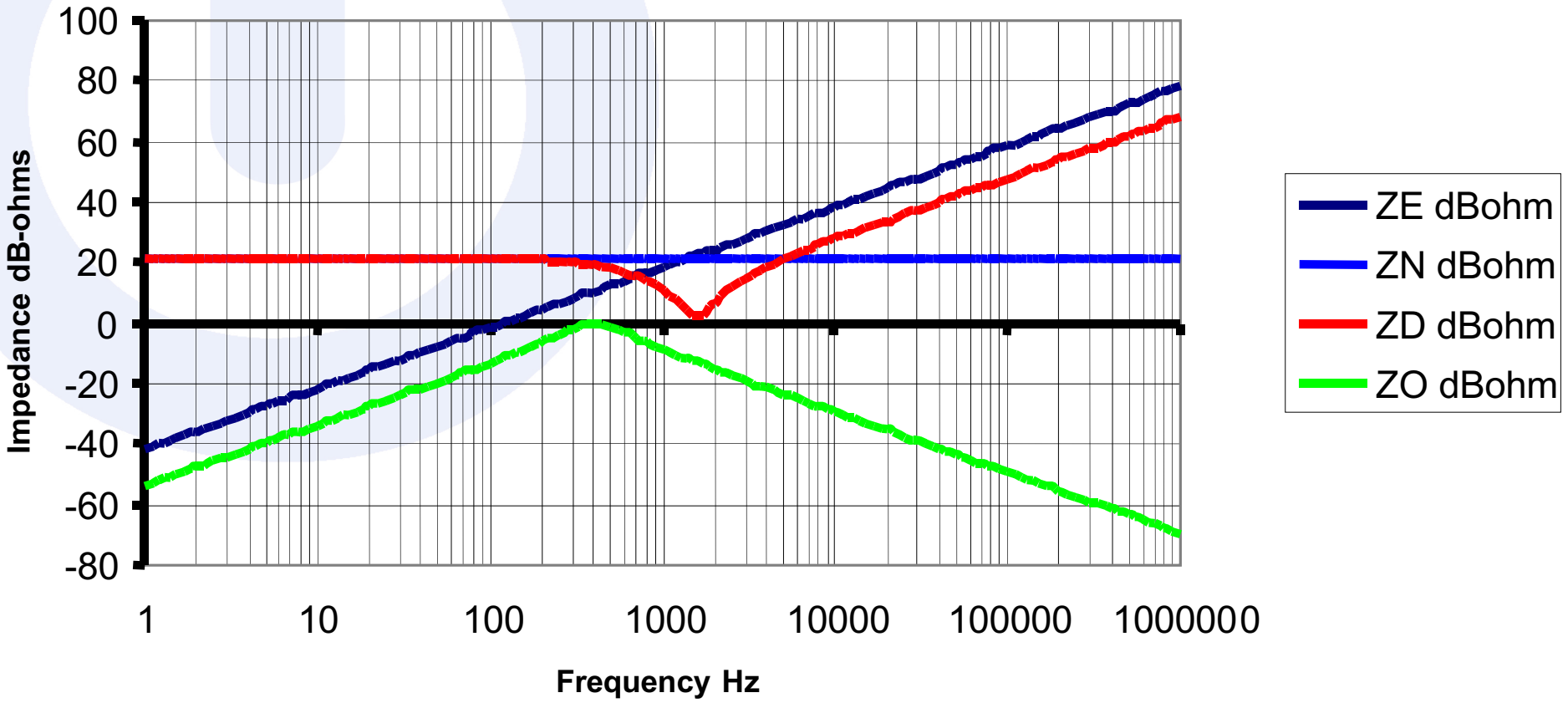
The input filter should be sufficiently damped

- Natural damping comes from the capacitor and inductor ESR s
- In some cases, extra damping resistors must be added

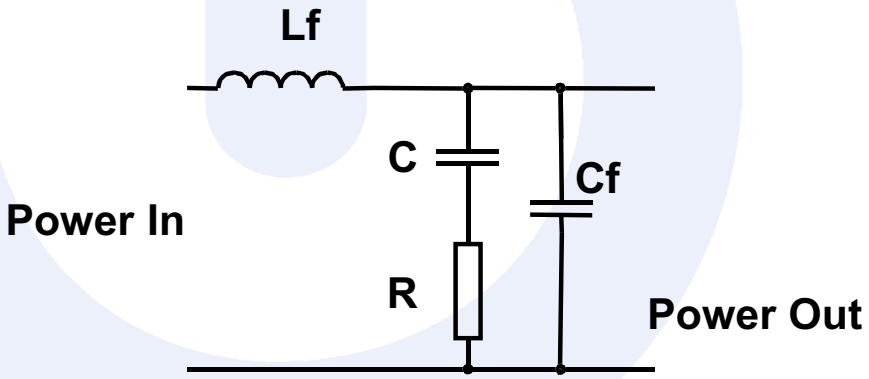
The frequency of the input filter should be chosen to be well away from the resonant frequency of Zd

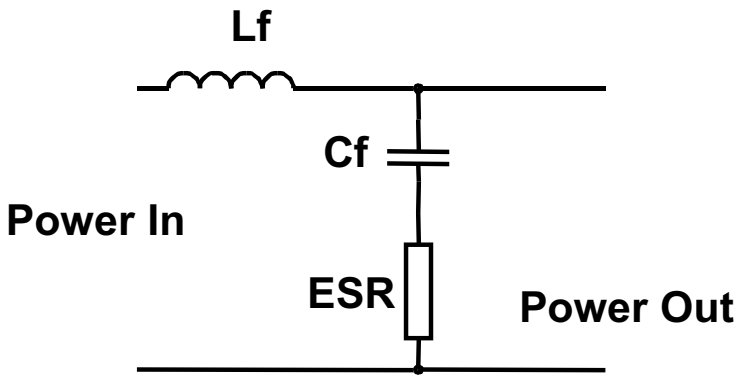
- The resonant frequency of Zd depends on the topology and can be checked from tables provided in the appendix
- For a voltage mode buck, the resonant frequency is 1/(2„ x sqrt(LC)) where L and C are the values of the buck output elements

Input Filter with 1 Ohm Damping Prevents Stability Problem



Schematic for Damping Element





For low ESR capacitors Erickson and Maksimovic recommend an extra C and series resistance

For high ESR capacitors, the intrinsic ESR will in practice provide enough damping

Literature

- We have referred to the following book

  Fundamentals of Power Electronics , Second Edition, Erickson & Maksimovic, Kluwer Academic Publishers, 2001, ISBN 0-7923-7270-0

- Among other things, the book explains in detail the derivation of the models behind the transfer functions, and in many cases the transfer functions themselves.