课程代码：**00830040**

第二章 数字逻辑基础(三)
——数字电路基础

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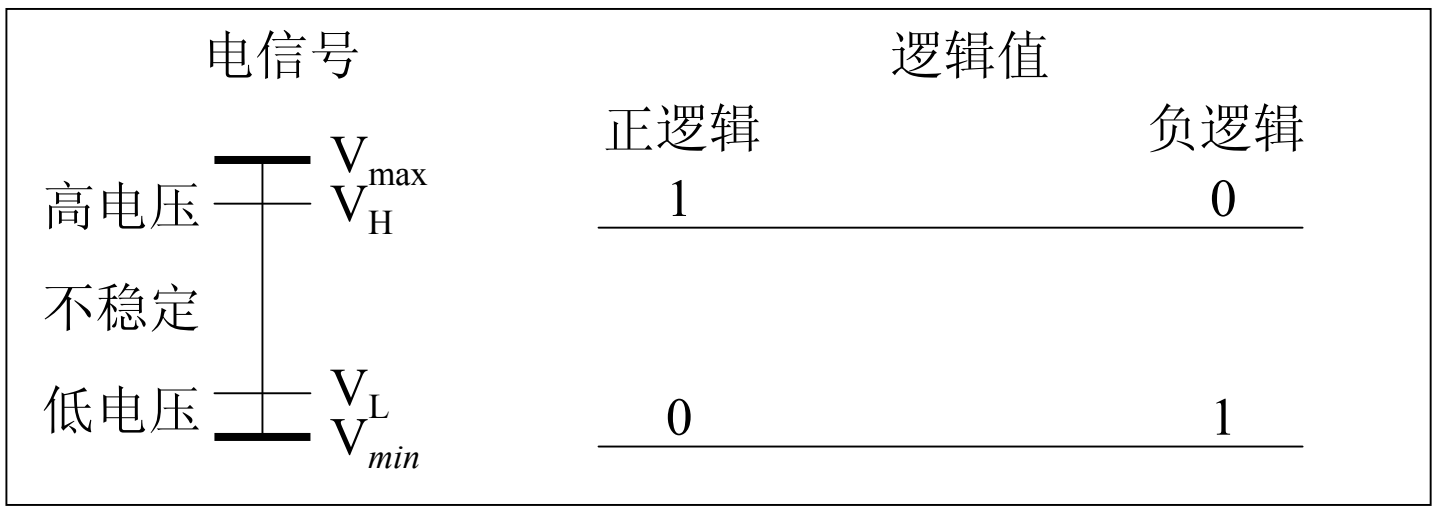
课程回顾

- 开关电路
  - 在电路中，用电压的高低来表示逻辑值
    - 正逻辑和负逻辑的区别



  - 基本逻辑门：AND, OR, NOT, NAND, NOR, XOR, NXOR
  - 门级网络

课程回顾(全加器)

$$s_i(x_i, y_i) = x_i\overline{y_i} + \overline{x_i}y_i$$

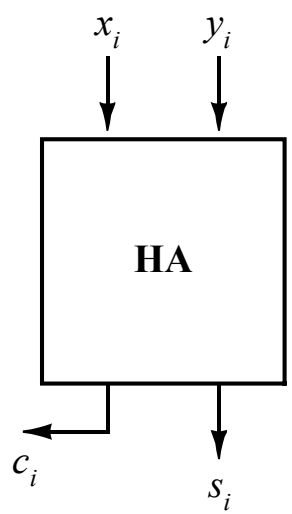
$$c_i(x_i, y_i) = x_i y_i$$

为什么采用与非门实现？

输入

逻辑功能

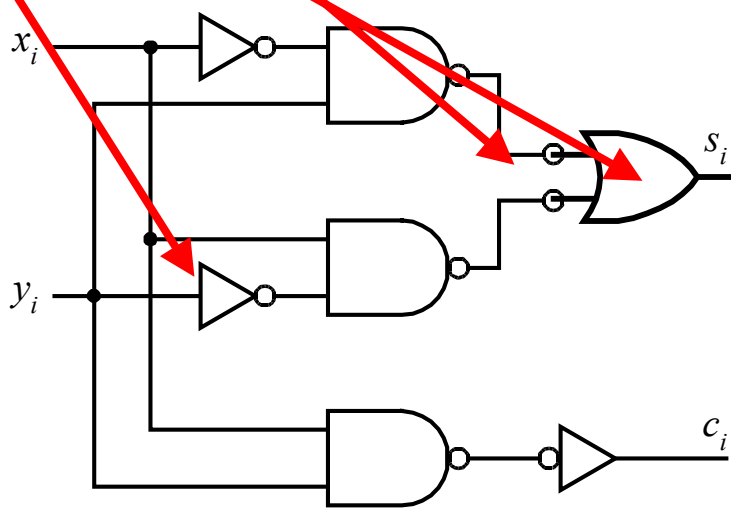
输出



(a)

x_i	y_i	c_i	s_i
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

(b)



(c)

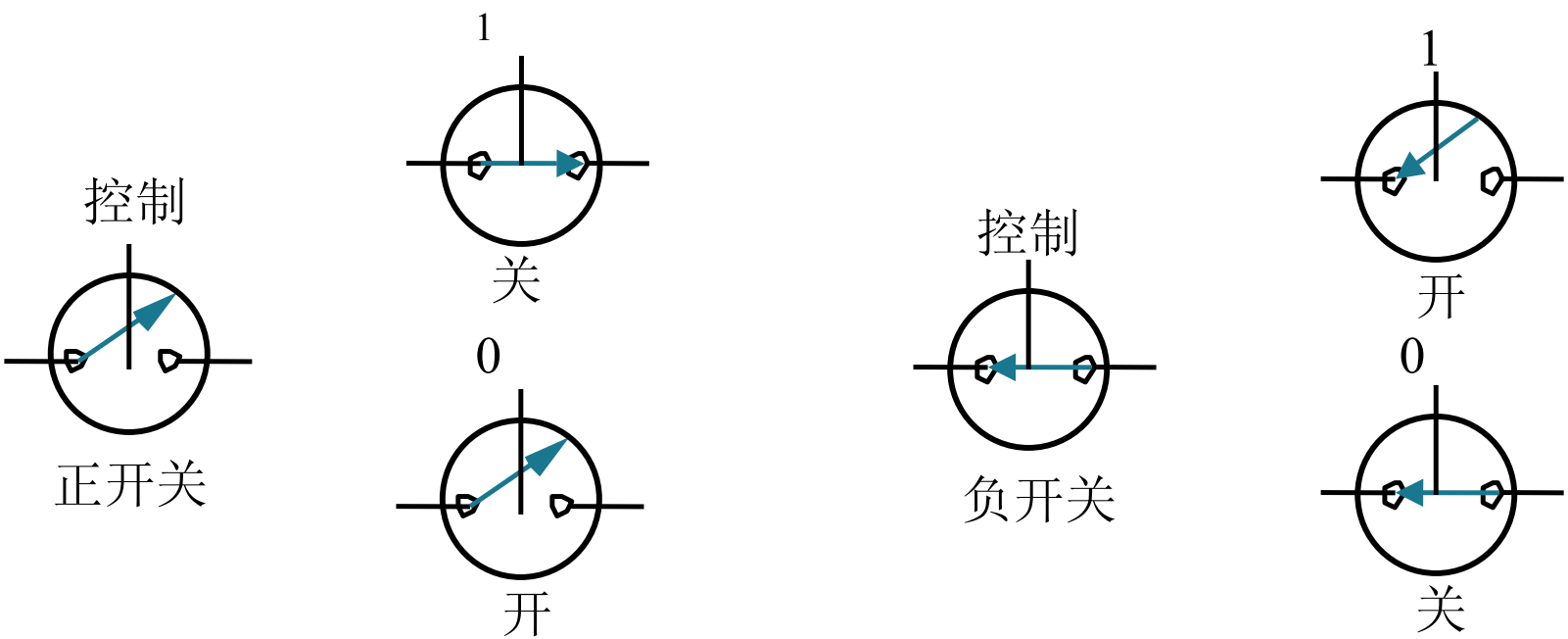
输入　　逻辑功能　　输出

主要内容

- 目标：了解逻辑门电路的实现
- 电子门系列（实现工艺）
  - TTL
  - ECL
  - MOS
  - CMOS

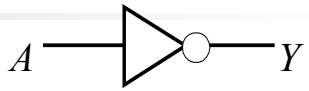
开关模型

- 开关(Switch)：开关在控制信号的控制下连接两个端点。
  - 正开关：在控制信号为0时开；为1时关，正逻辑。
  - 负开关：在控制信号为1时开；为0时关，负逻辑。



基本的逻辑门开关模型(1)

非门(NOT)



(c)

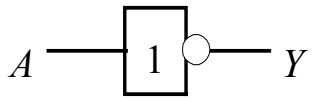
- 被动上拉模型
- 主动上拉模型
- 电源-逻辑1，地-逻辑0

a	$f_{NOT}(a) = \bar{a}$
0	1
1	0

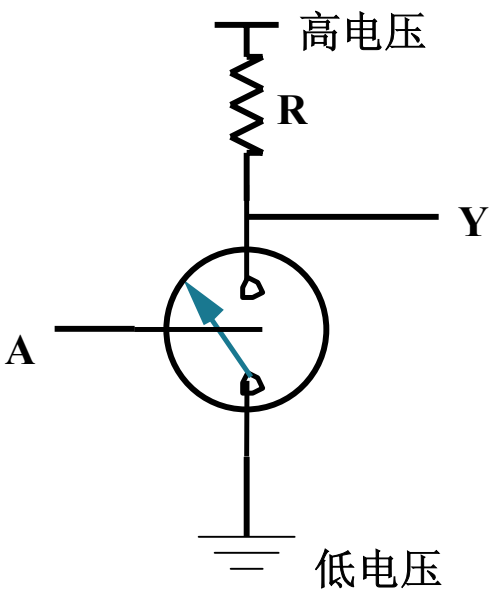
(a)

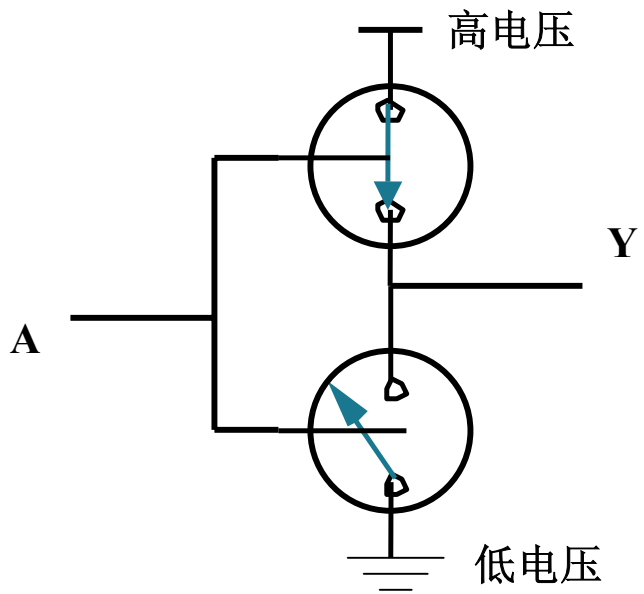
A	Y
L	H
H	L

(b)

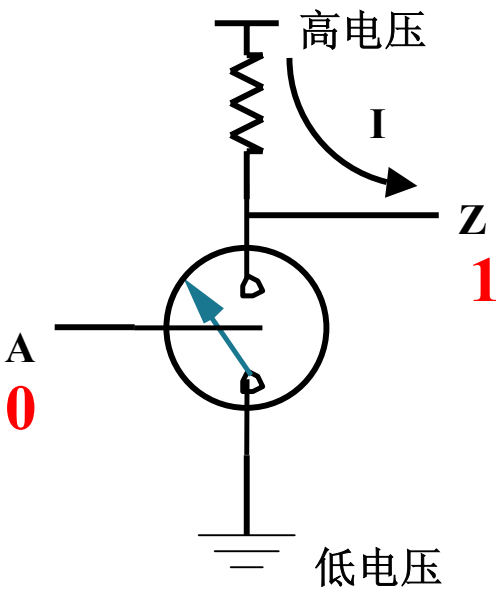


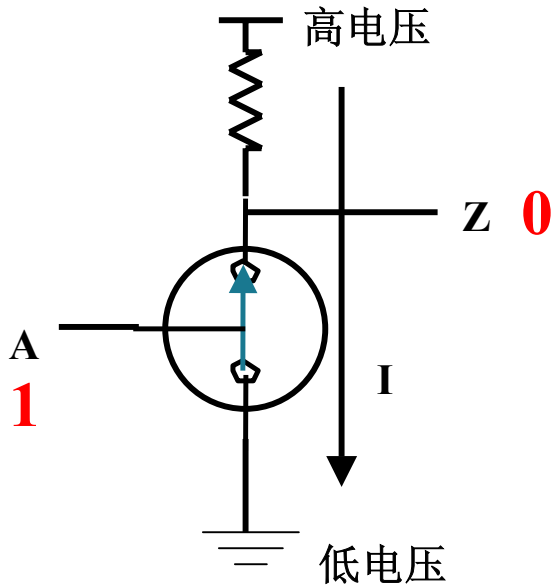
(d)



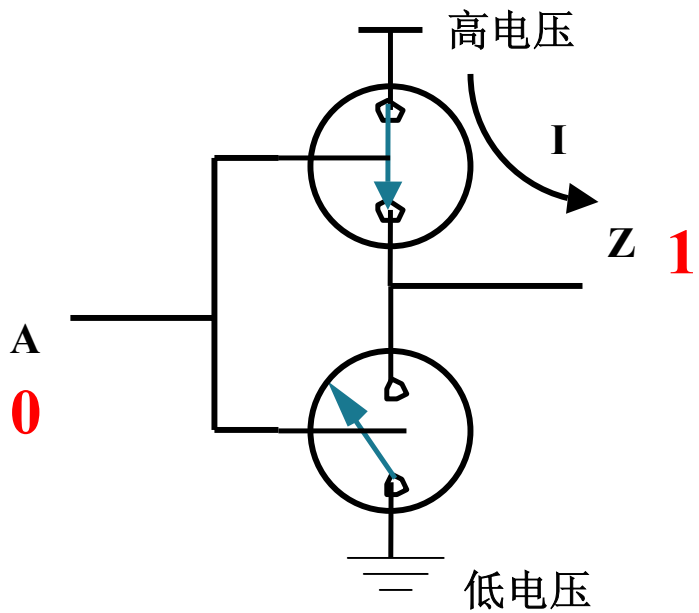


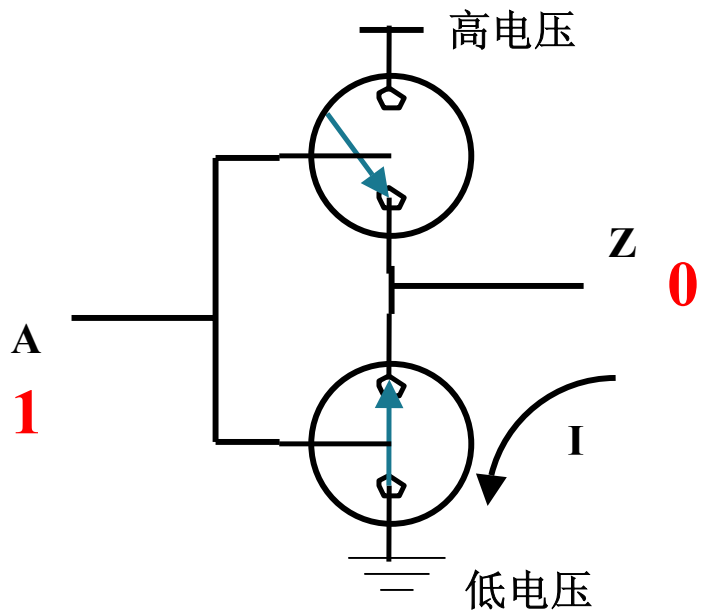
非门的开关模型分析





非门的开关模型分析





基本逻辑门开关模型(2)

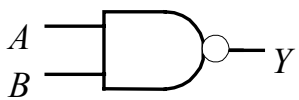
- 与非门(NAND)

a	b	$f_{NAND}(a, b) = ab$
0	0	1
0	1	1
1	0	1
1	1	0

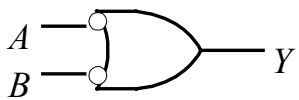
(a)

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

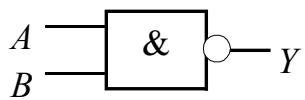
(b)



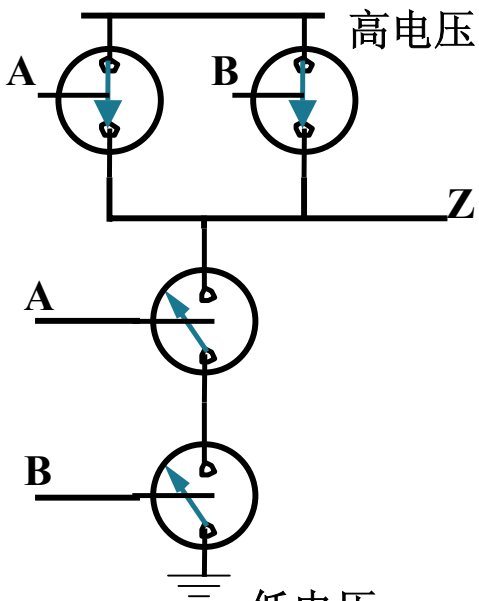
(c)

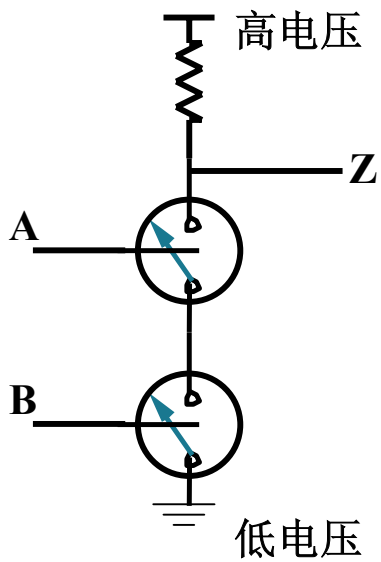


(d)



(e)





基本逻辑门开关模型(3)

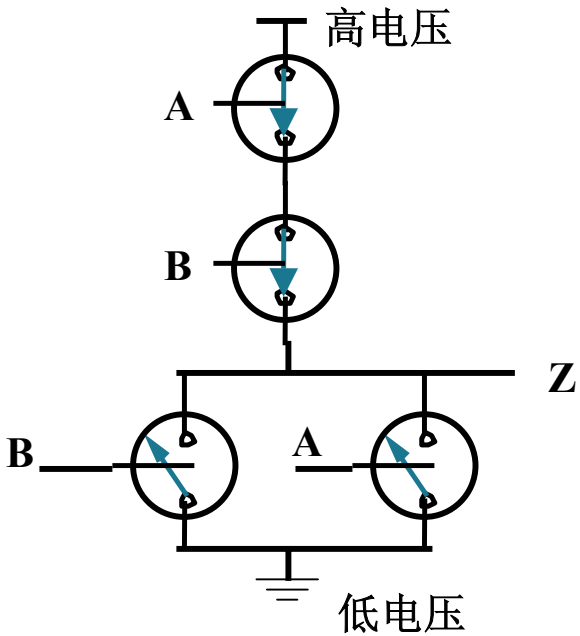
- 或非门(NOR)

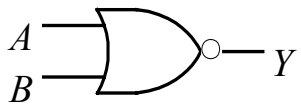
a	b	$f_{NOR}(a, b) = \overline{a + b}$
0	0	1
0	1	0
1	0	0
1	1	0

(a)

A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

(b)





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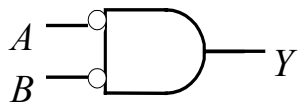

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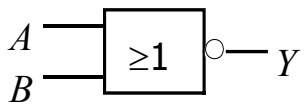

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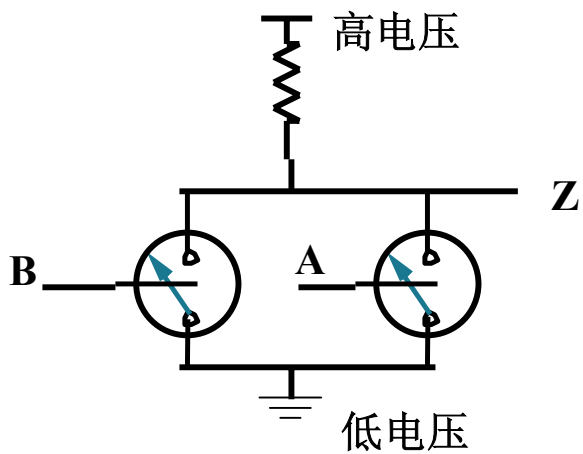
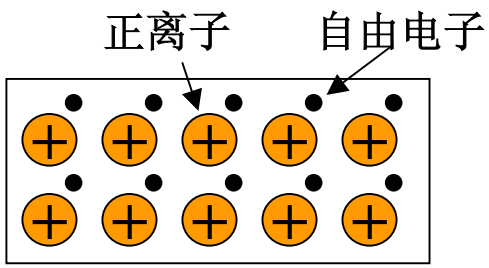
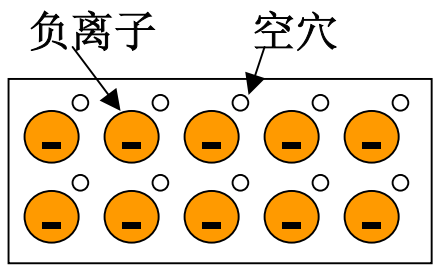


半导体器件

- 杂质半导体
  - N型半导体：硅(Silicon)+五价元素（如磷）。利用自由电子导电。
  - P型半导体：硅+三价元素（如硼），利用空穴导电。

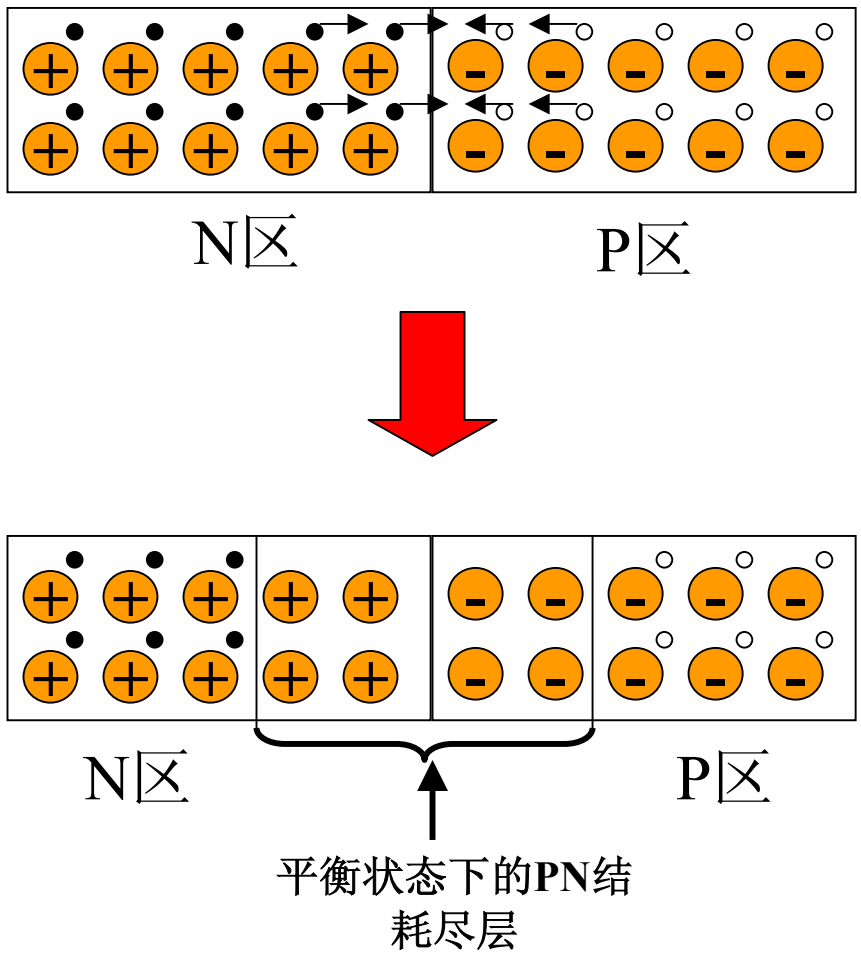


N型半导体

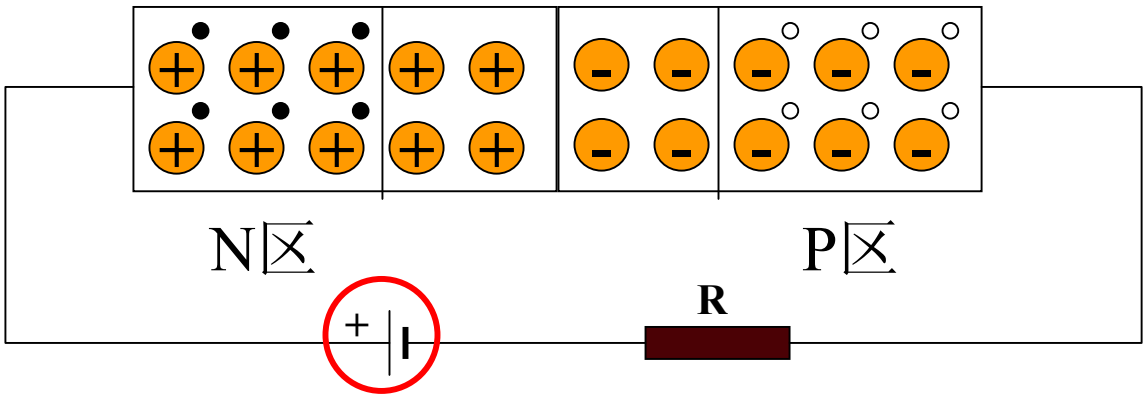


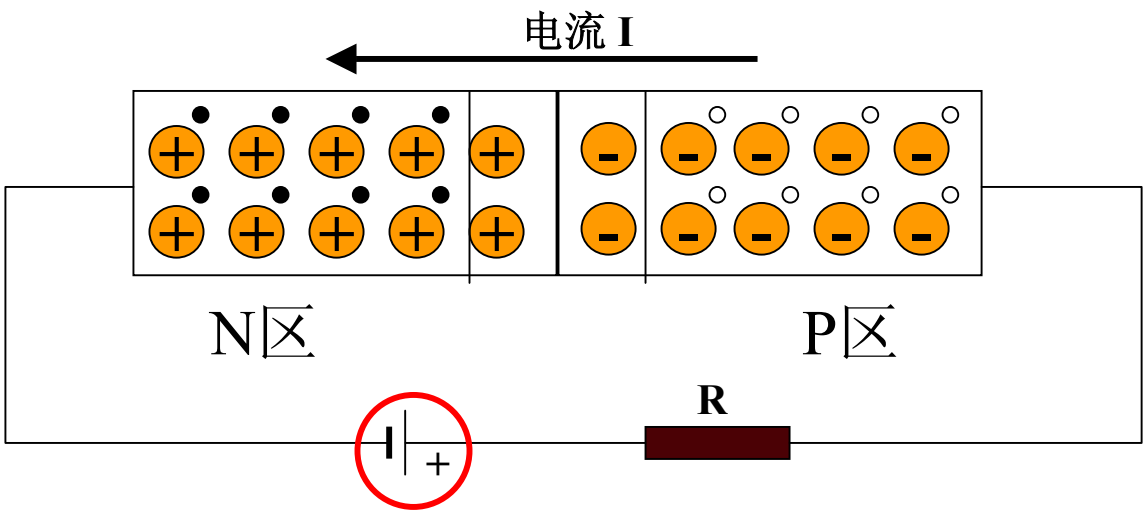
P型半导体

PN结



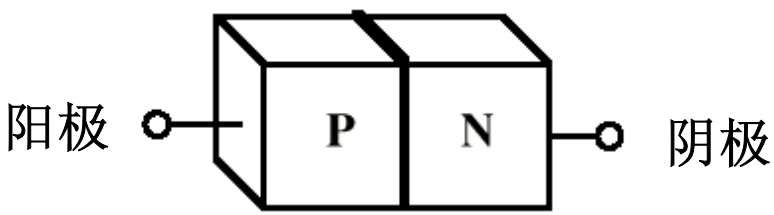
PN结的导电特性





二极管(Diode)

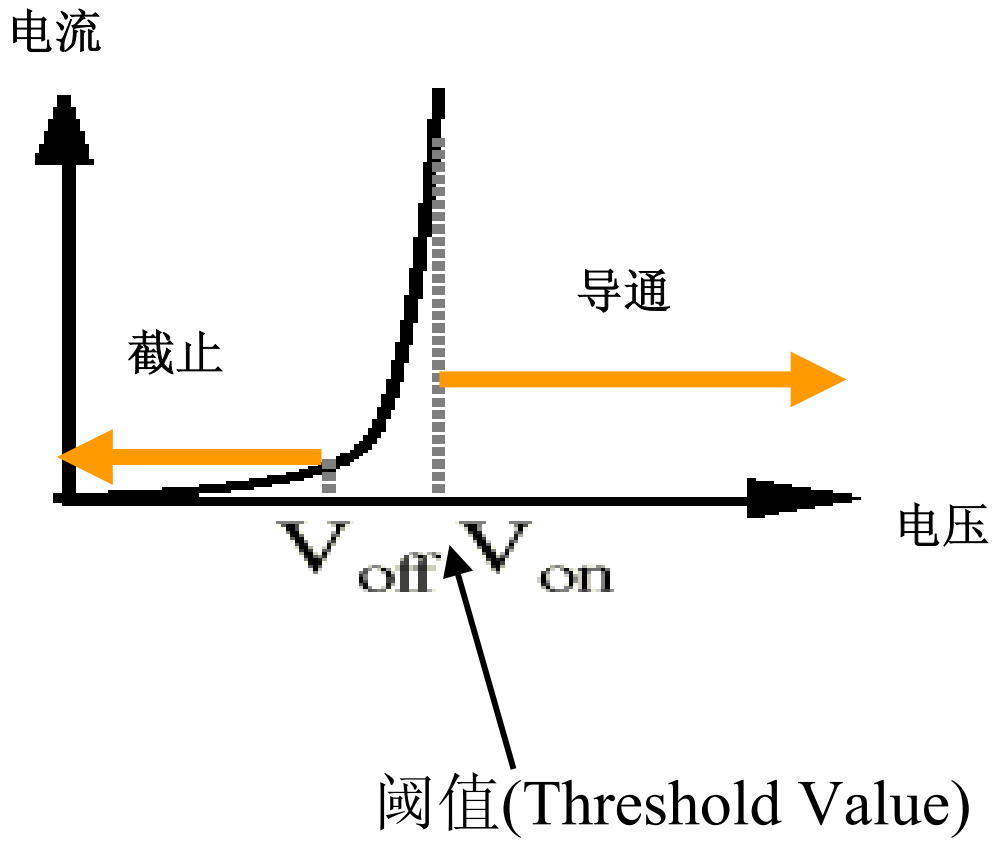
- 二极管的构成
  - 将金属线连接在PN结的两端，和P区连接的端口为阳极(Anode)，和N区相连接的为阴极(Cathode)。



二极管结构

二极管的符号

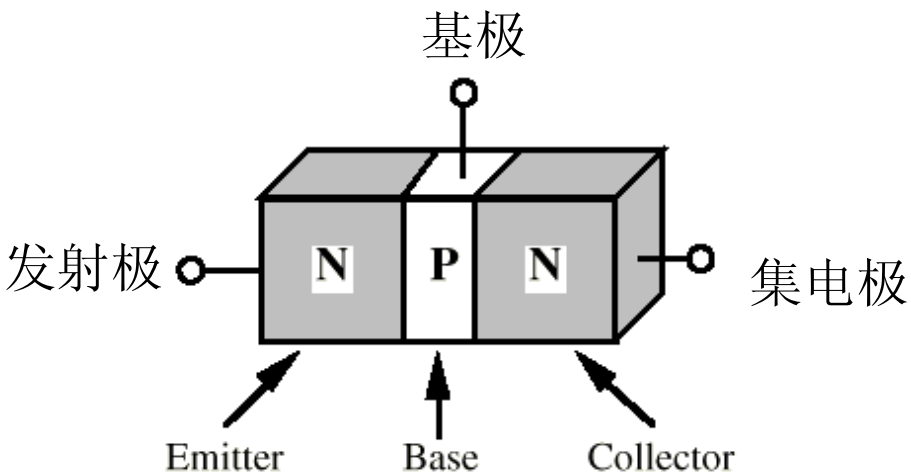
二极管的伏安特性



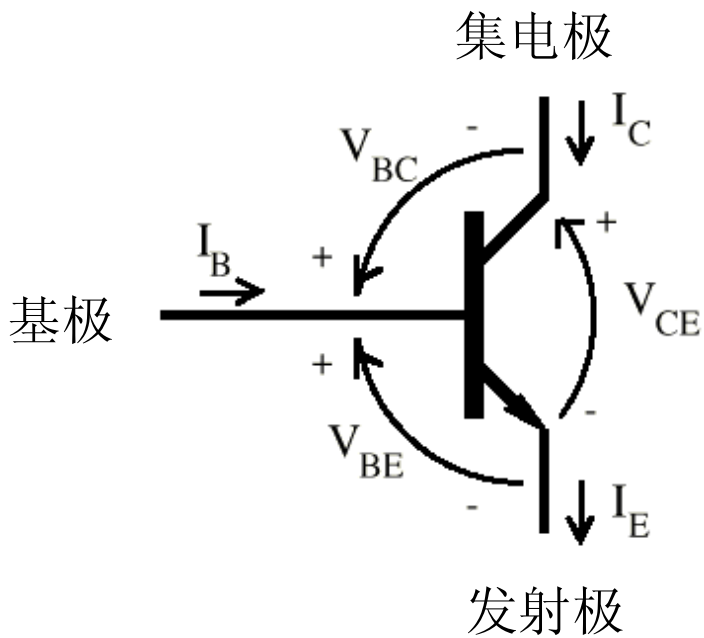
双极性晶体管(1)

双极性晶体管(Bipolar Junction Transistor)

- 也叫三极管。基极电压高于某个阈值，两个PN结道通，发射机和集电极在电压的作用下产生电流。
- 三极管具有电流放大功能，被广泛的用于放大电路。



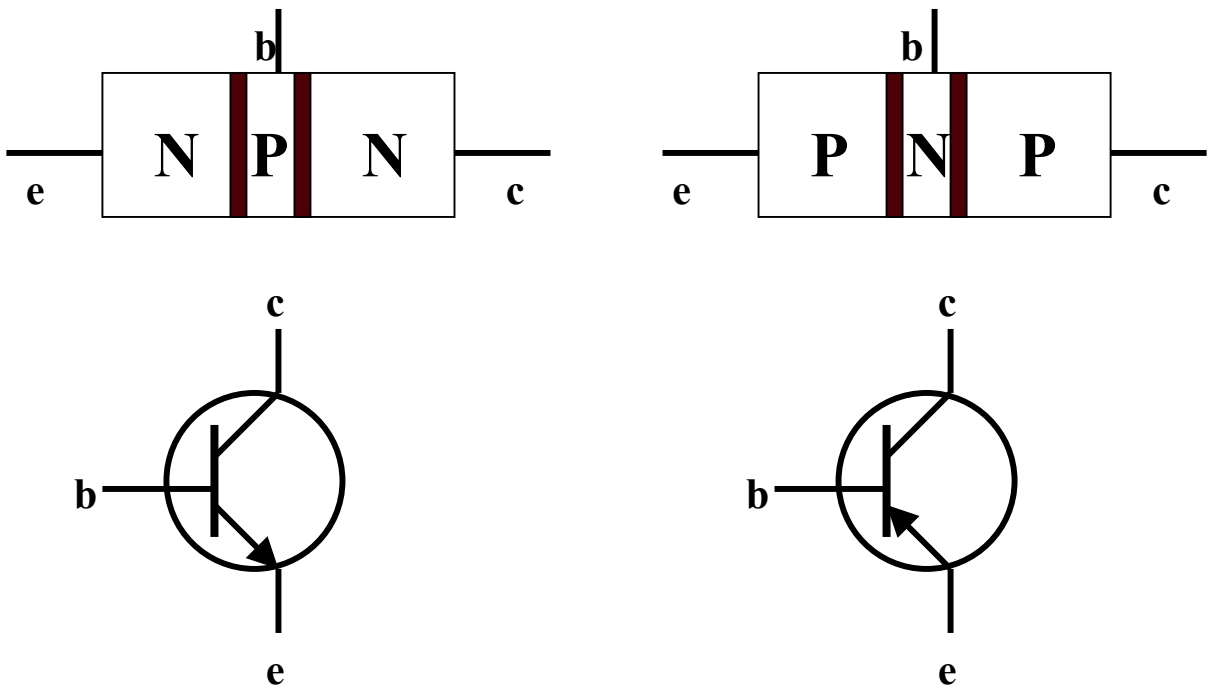
内部结构



符号

双极性晶体管(2)

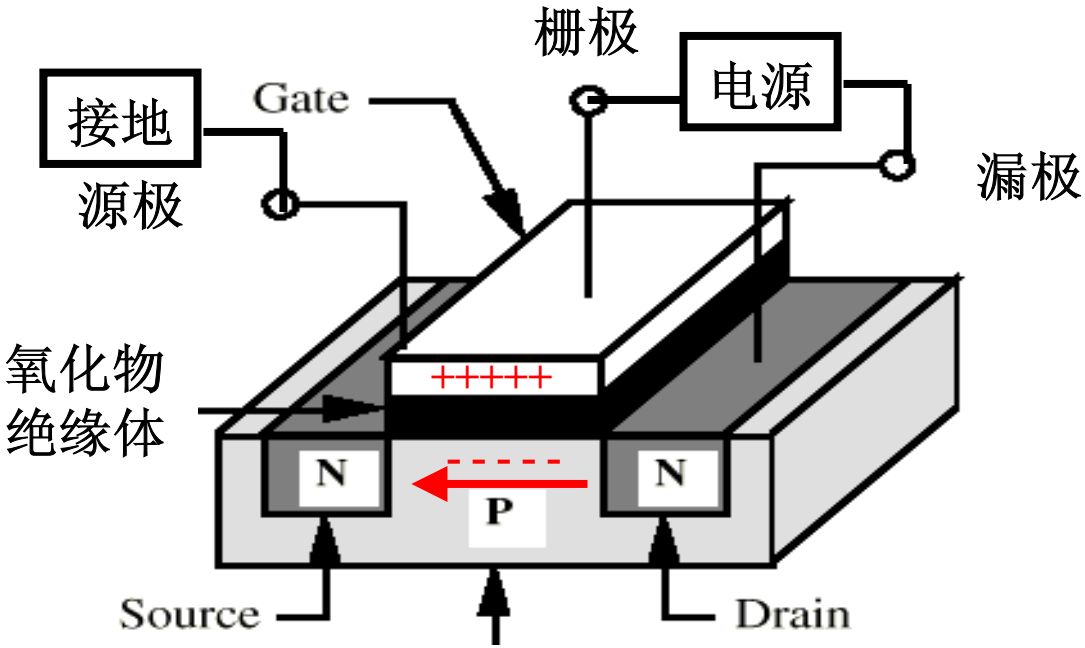
- 类型：
  - NPN型
  - PNP型



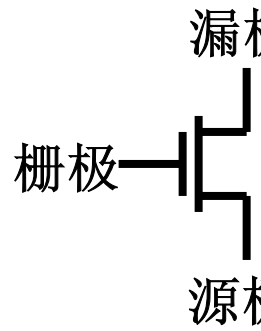
场效应管

- 场效应管(Field-Effect Transistor)
  - 金属氧化物半导体场效应管
  - Metal-oxide semiconductor FET(MOSFET)
  - 简称MOS
- 类型
  - N沟道MOS管——nMOS（增强型，耗尽型）
  - P沟道MOS管——pMOS（增强型，耗尽型）
  - 互补型MOS管——CMOS

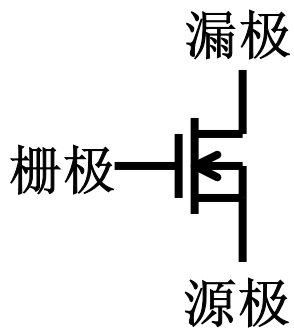
nMOS



N沟道MOSFET

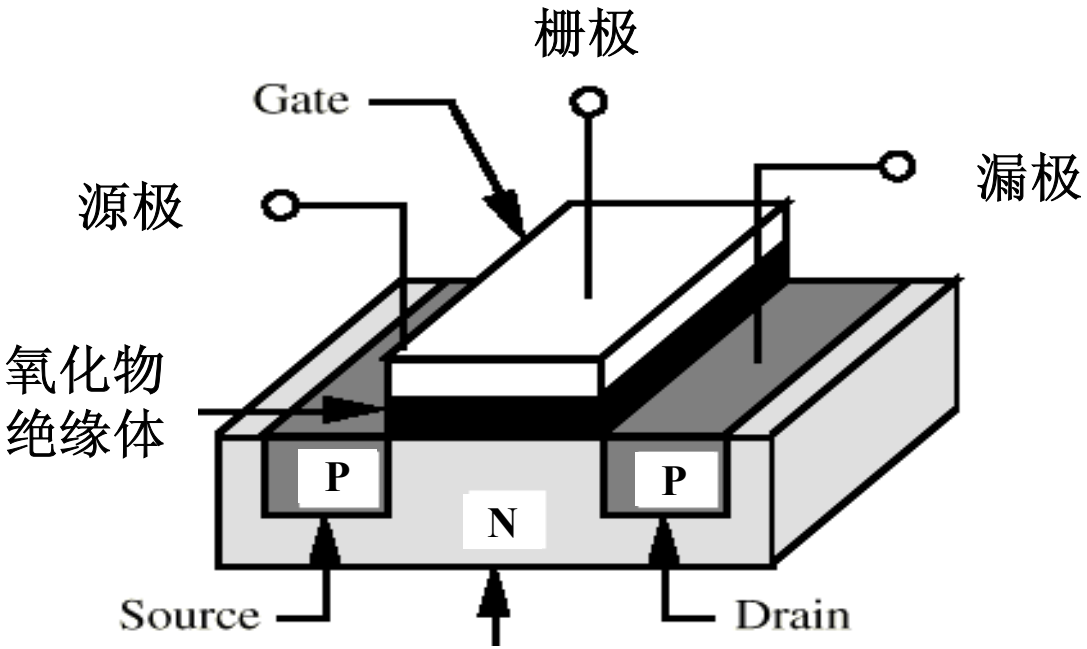


增强型nMOS 符号

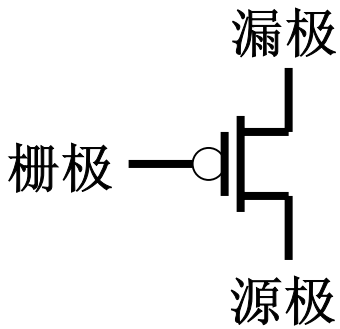


耗尽型nMOS 符号

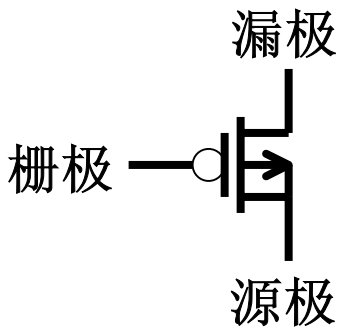
pMOS



P沟道MOSFET



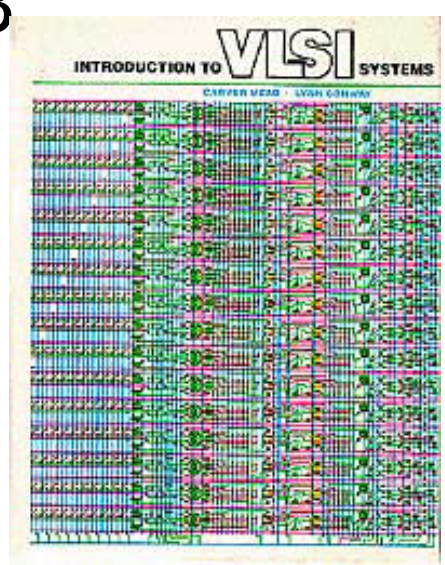
增强型pMOS 符号



耗尽型pMOS 符号

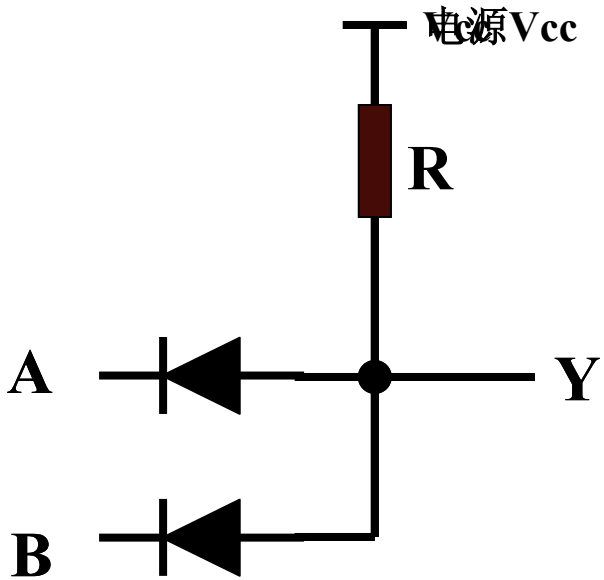
两本好书

- Carver Mead and Lynn Conway,
  "**An Introduction to VLSI system**", 1979.
- Weste, Neil H. E, **Principles of CMOS VLSI design : a systems perspective, 2nd ed,** Addison-Wesley,1993

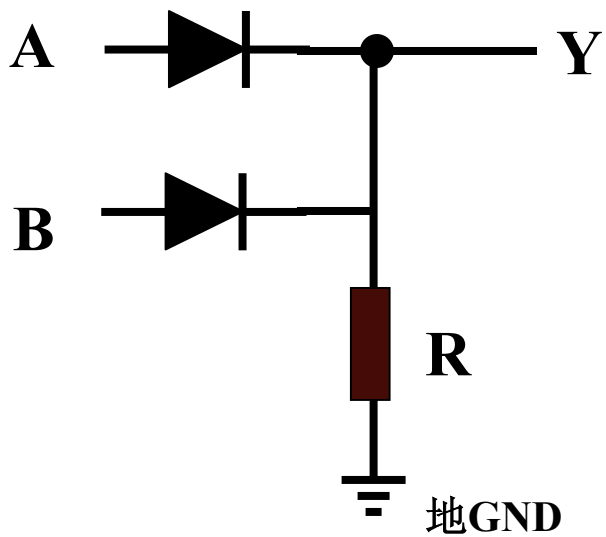


门电路的实现

- 二极管门电路



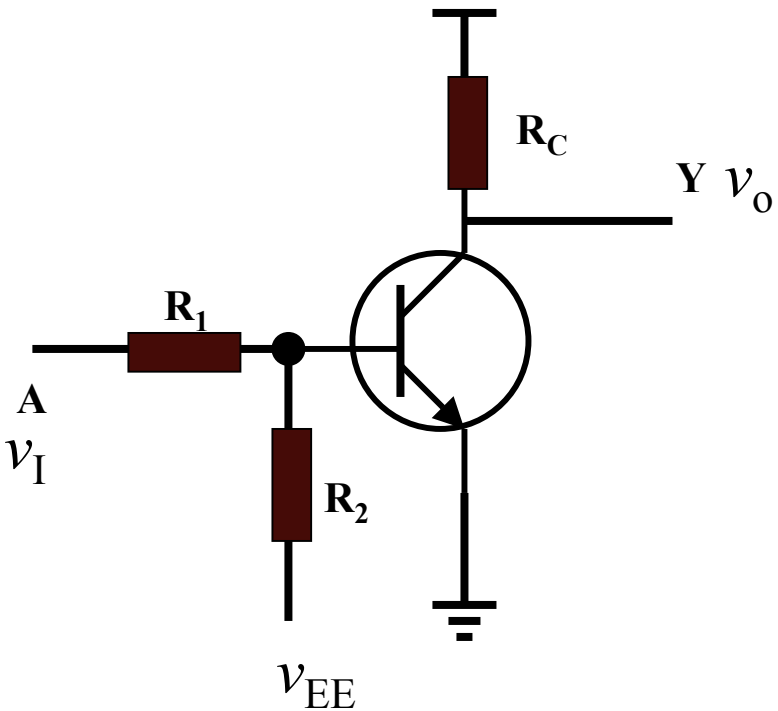
二极管与(AND)门



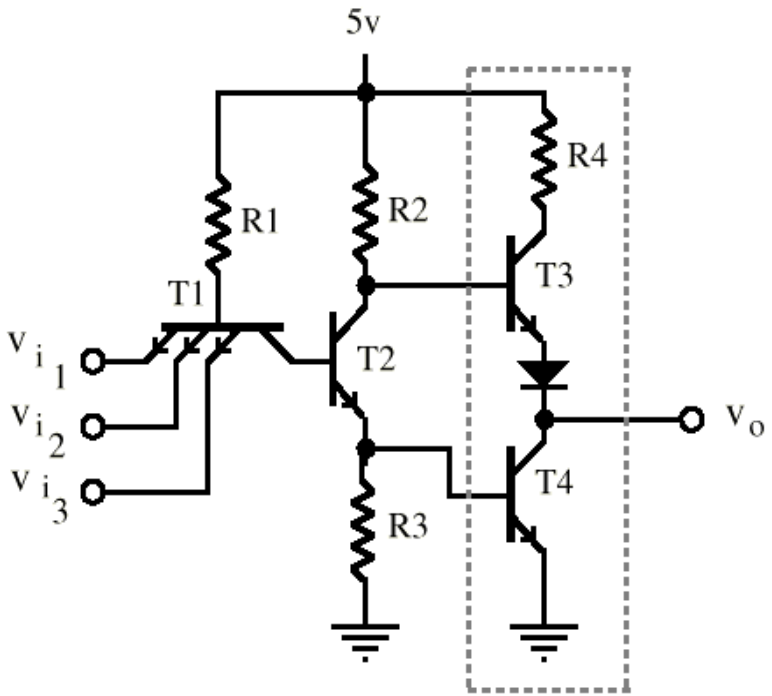
二极管或(OR)门

TTL系列

- 三极管门电路
- Transistor-Transistor Logic(TTL)



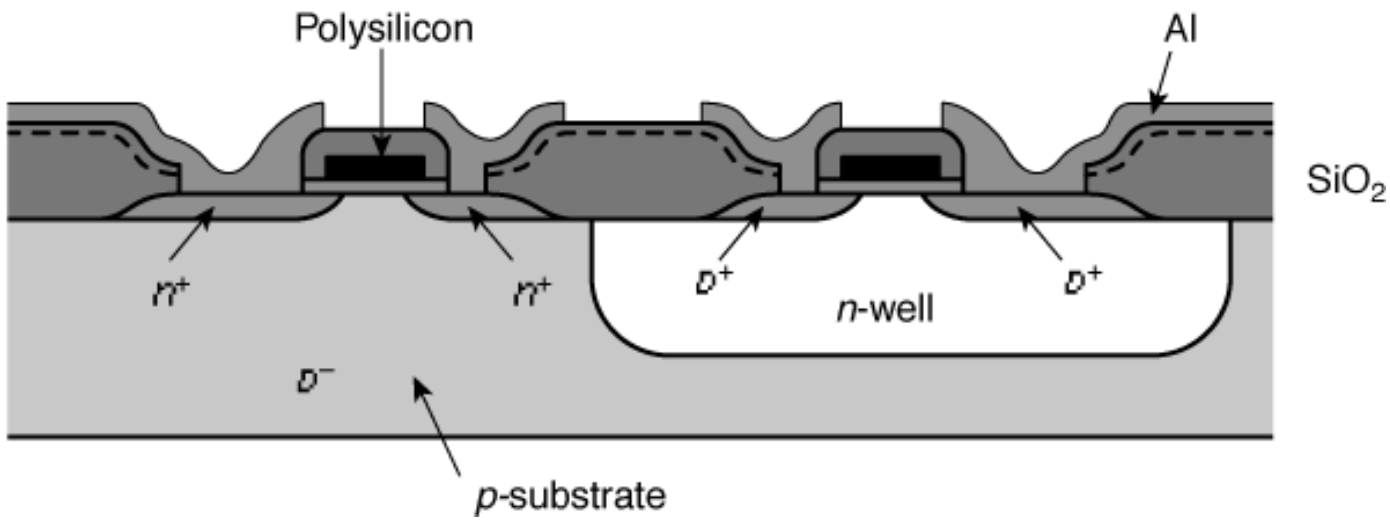
三极管非门（反向器）



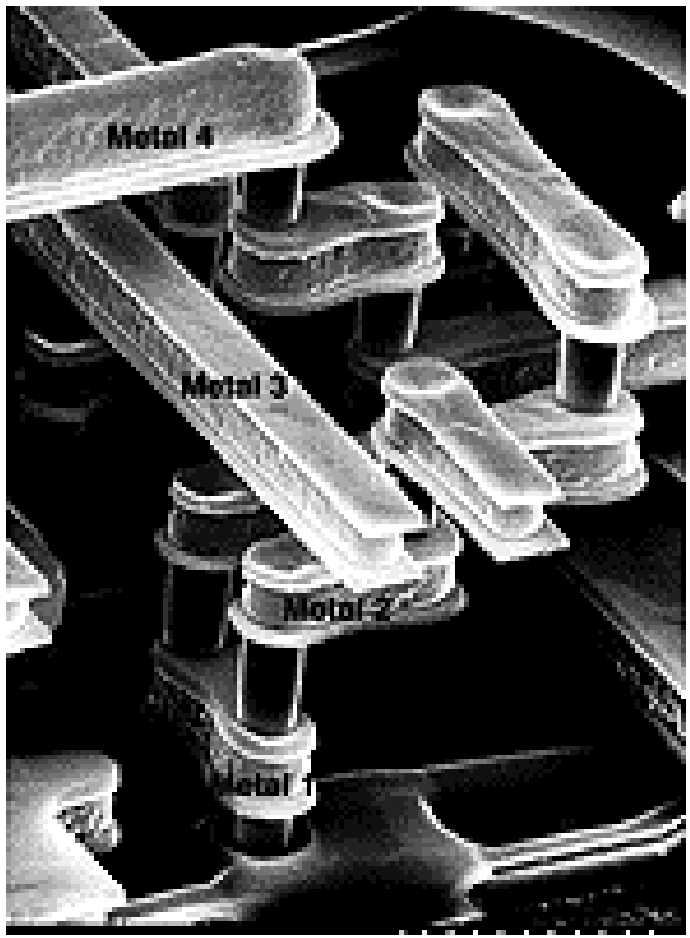
TTL与非(NAND)门

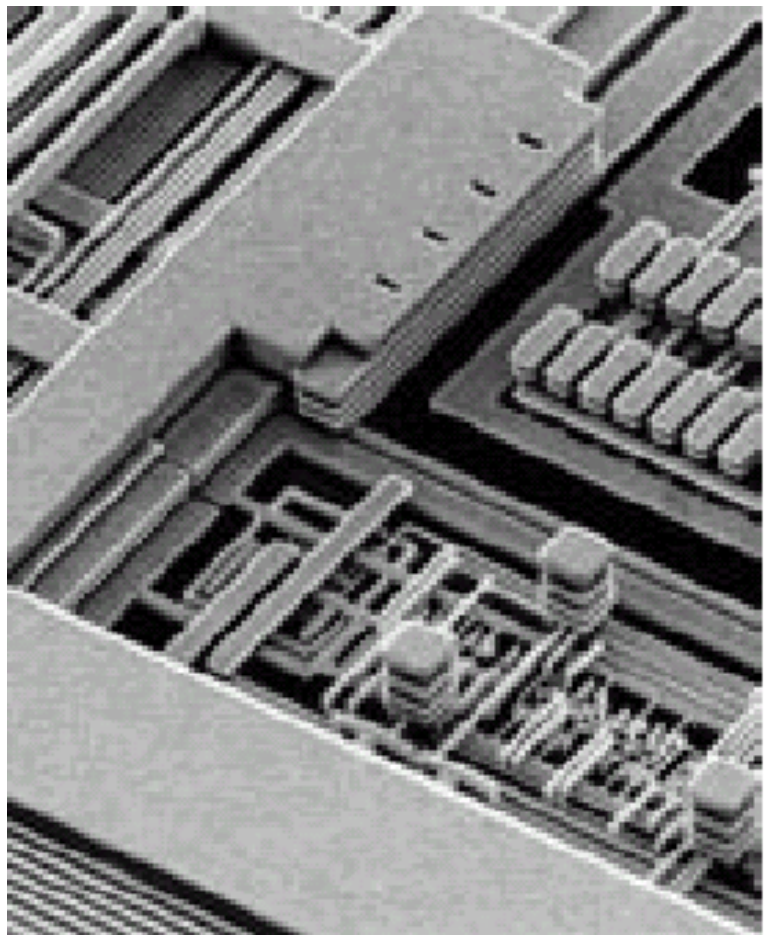
CMOS系列

- nMOS和pMOS形成互补电路
  - 电流小，功耗低
  - 集成度高
  - 速度慢（现代工艺已经解决了这个问题）

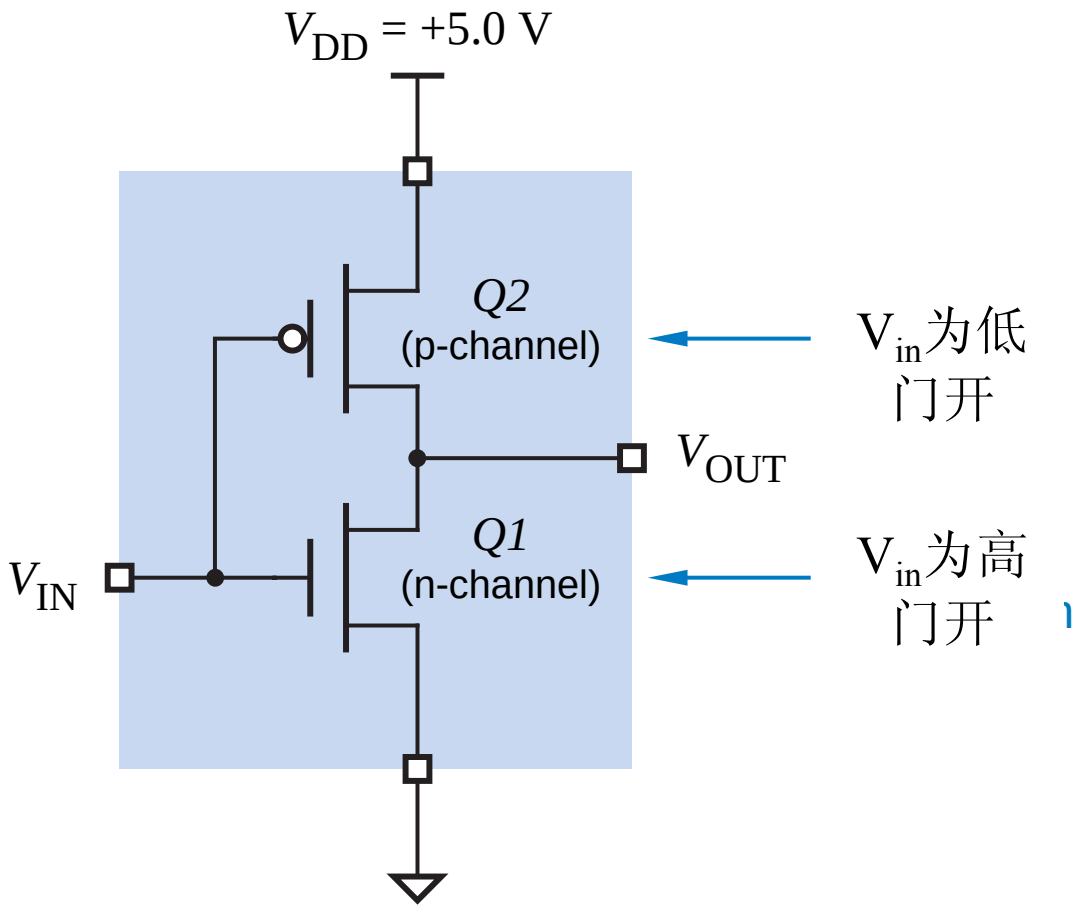


CMOS的微观照片



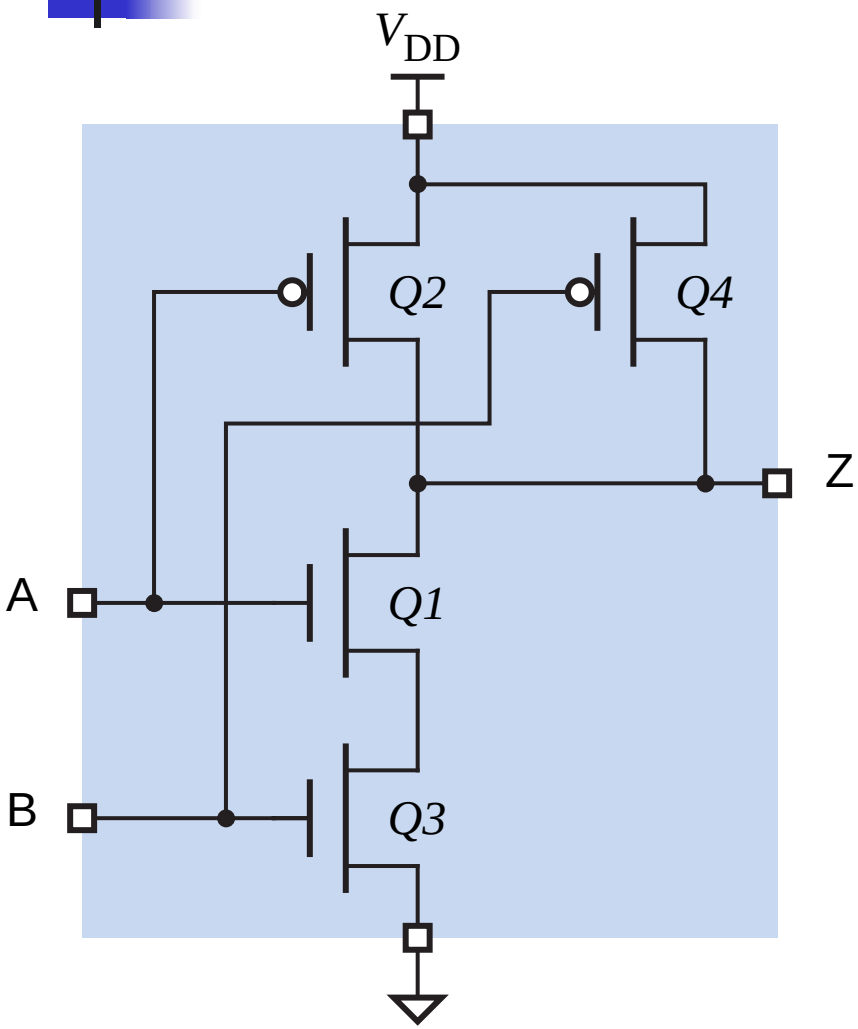


CMOS反向器



CMOS与非门(NAND)

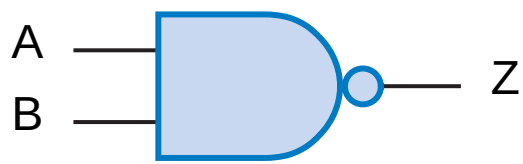
(a)



(b)

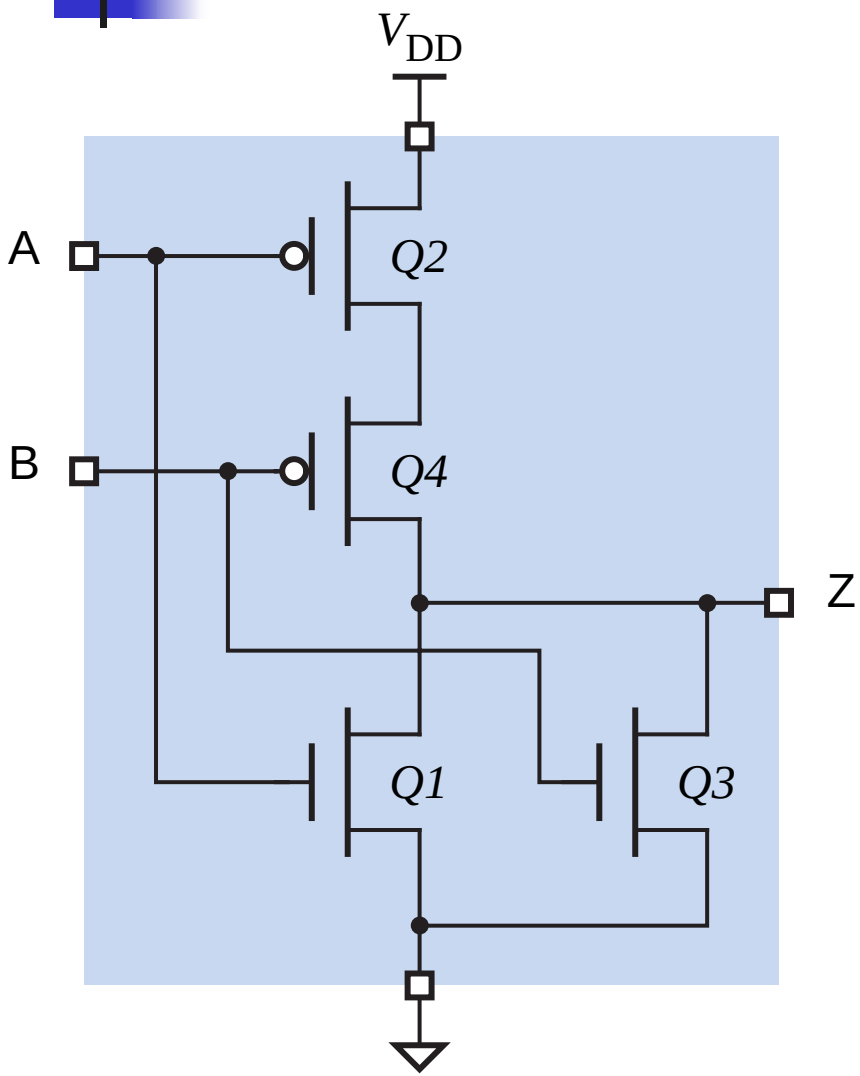
A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	H
H	L	on	off	off	on	H
H	H	on	off	on	off	L

(c)



CMOS或非门(NOR)

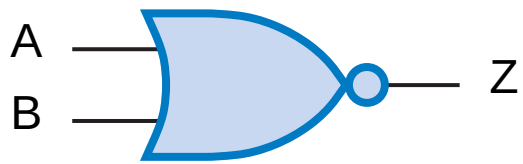
(a)



(b)

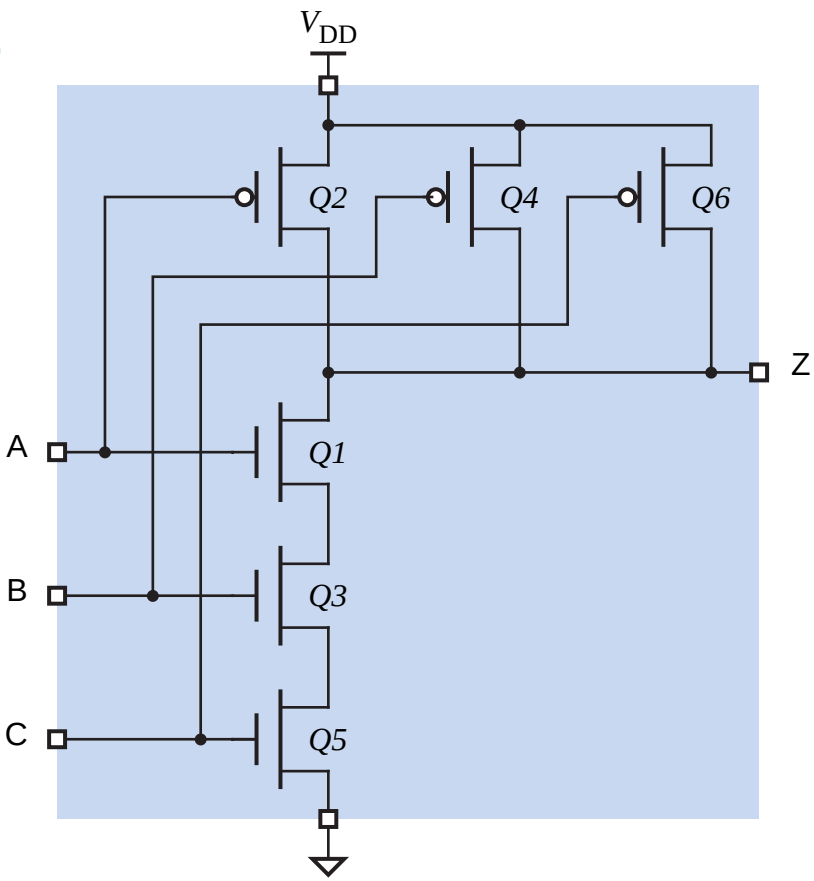
A	B	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	L	off	on	off	on	H
L	H	off	on	on	off	L
H	L	on	off	off	on	L
H	H	on	off	on	off	L

(c)



多输入CMOS与非门

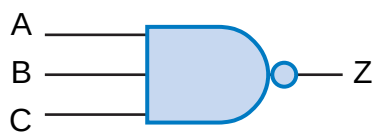
(a)



(b)

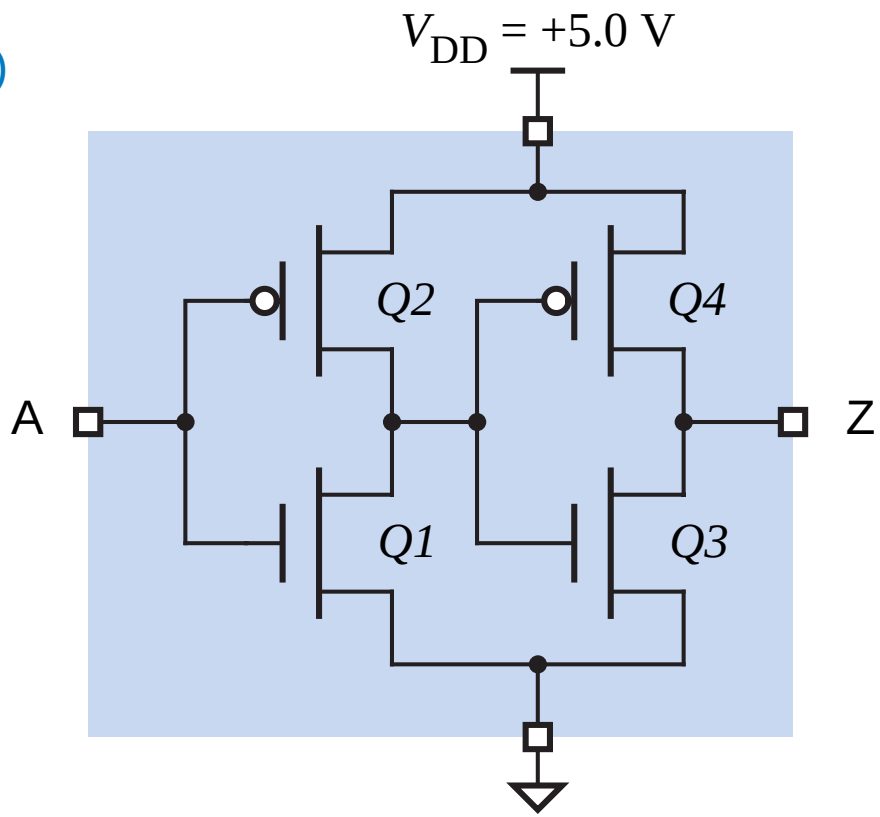
A	B	C	*Q1*	*Q2*	*Q3*	*Q4*	*Q5*	*Q6*	Z
L	L	L	off	on	off	on	off	on	H
L	L	H	off	on	off	on	on	off	H
L	H	L	off	on	on	off	off	on	H
L	H	H	off	on	on	off	on	off	H
H	L	L	on	off	off	on	off	on	H
H	L	H	on	off	off	on	on	off	H
H	H	L	on	off	on	off	off	on	H
H	H	H	on	off	on	off	on	off	L

(c)



CMOS缓冲器(buffer)

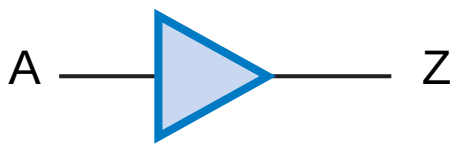
(a)



(b)

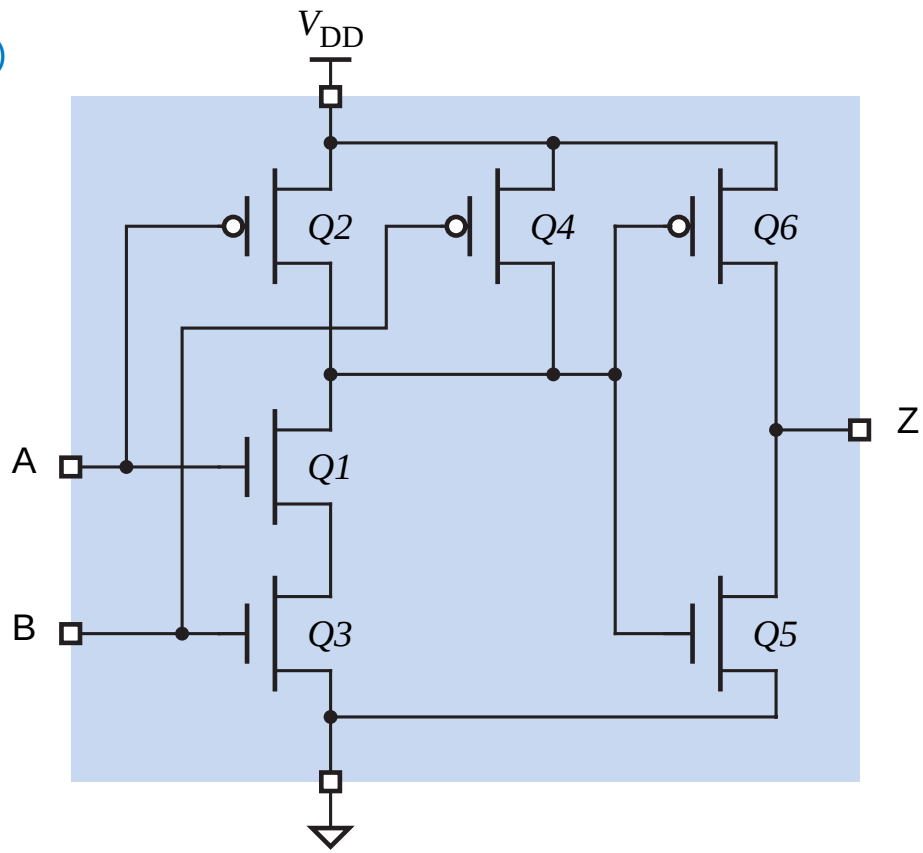
A	*Q1*	*Q2*	*Q3*	*Q4*	Z
L	off	on	on	off	L
H	on	off	off	on	H

(c)



2-输入CMOS与门(AND)

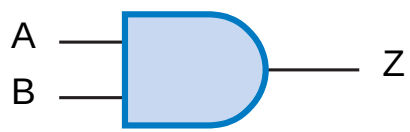
(a)



(b)

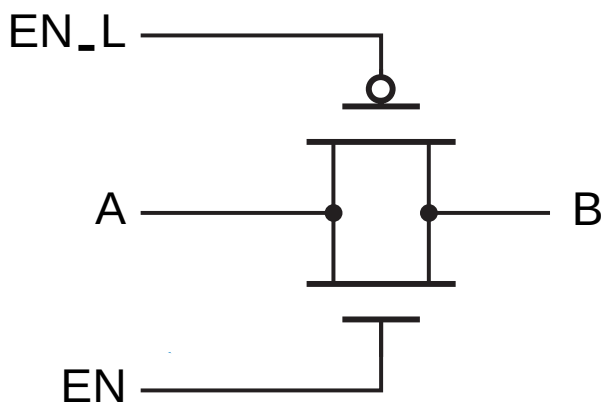
A	B	Q1	Q2	Q3	Q4	Q5	Q6	Z
L	L	off	on	off	on	on	off	L
L	H	off	on	on	off	on	off	L
H	L	on	off	off	on	on	off	L
H	H	on	off	on	off	off	on	H

(c)



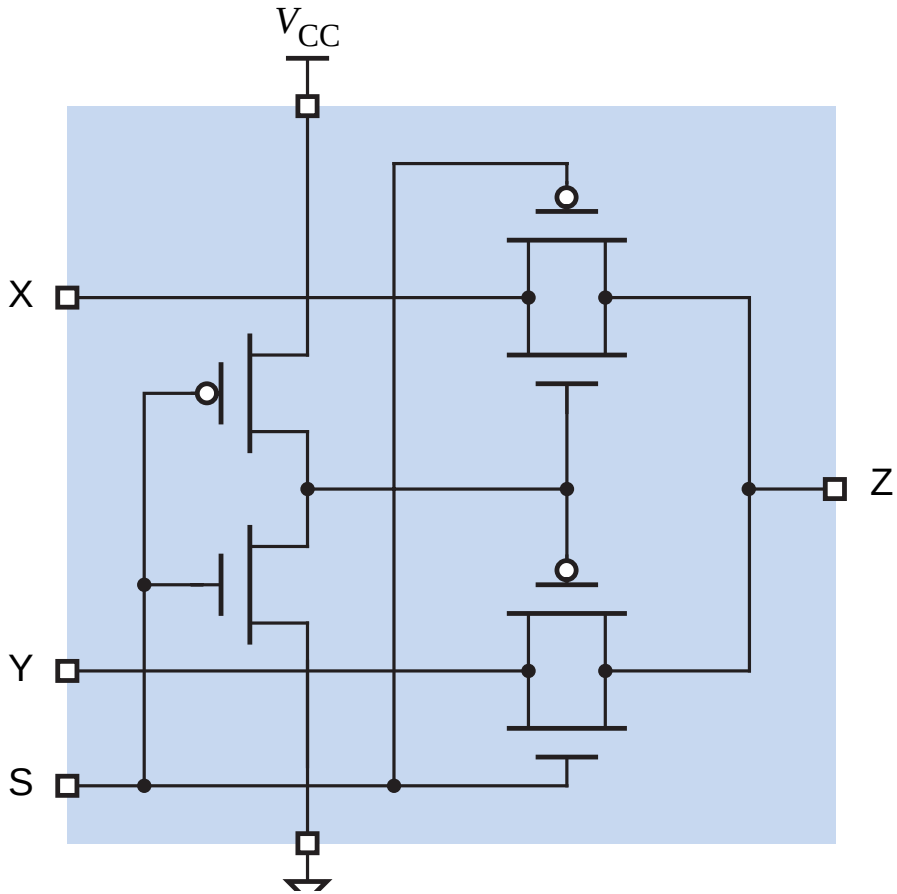
特殊的CMOS门(1)

- 传输门(Transmission gate)
  - nMOS开关和pMOS开关对接而成。
  - EN_L和EN应该是互补的。
  - 当nMOS和pMOS同时处于开状态，传输门两端的电阻非常小。



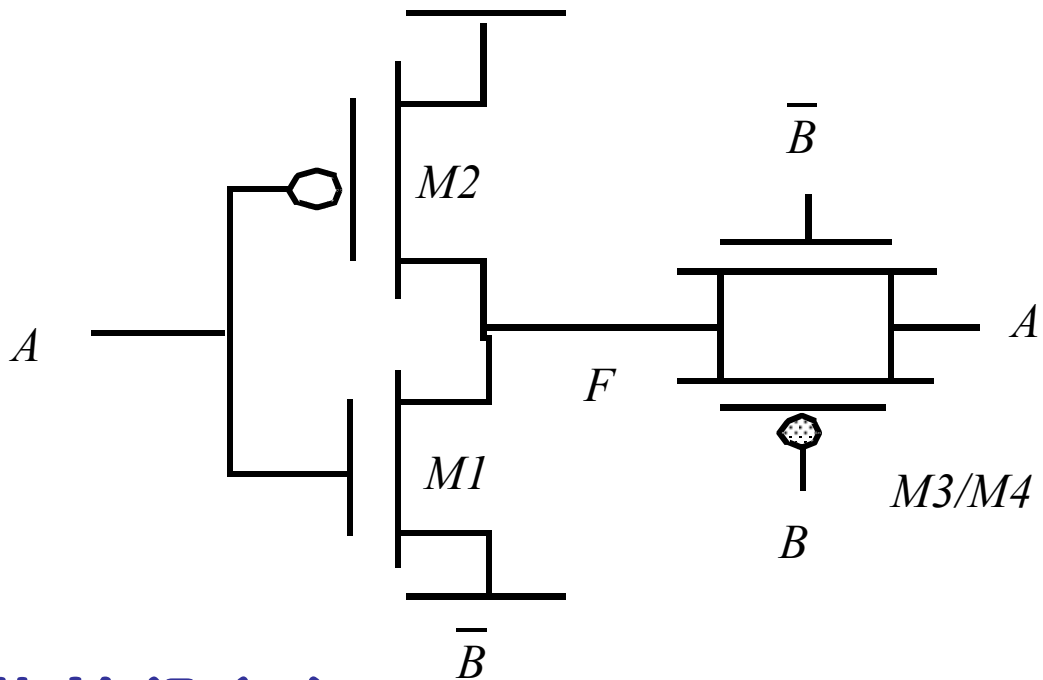
特殊的CMOS门(2)

- 用传输门实现的2选1逻辑
  - S=0：Z=X
  - S=1：Z=Y
  - $Z = \overline{S}X + SY$



特殊的CMOS门(3)

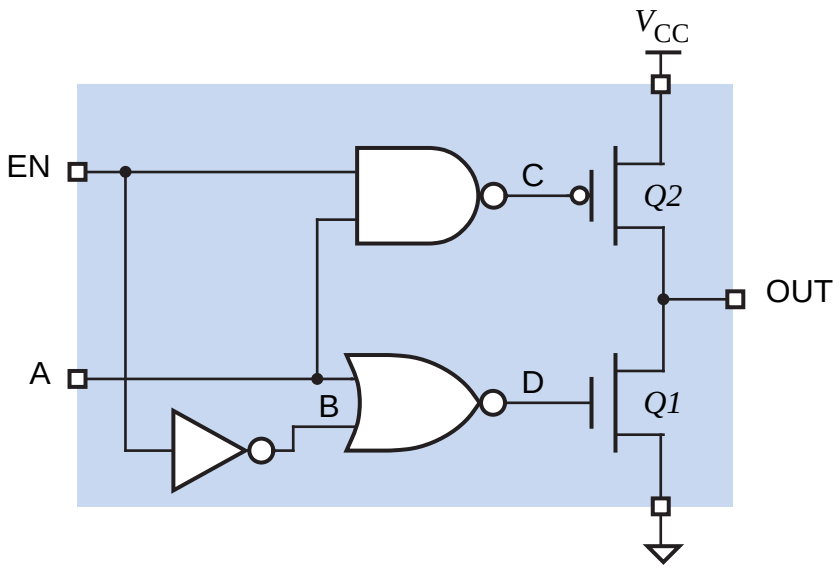
- 异或门(XOR)
  - 1取反，0通过
  - $F = A \oplus B = \overline{A}B + A\overline{B}$



特殊的CMOS门(4)

- 三态门(Tri-state gate)
  - 用于驱动总线

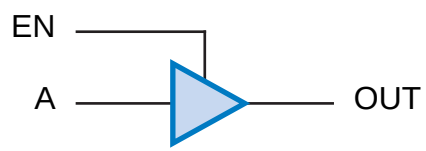
(a)



(b)

EN	A	B	C	D	*Q1*	*Q2*	OUT
L	L	H	H	L	off	off	Hi-Z
L	H	H	H	L	off	off	Hi-Z
H	L	L	H	H	on	off	L
H	H	L	L	L	off	on	H

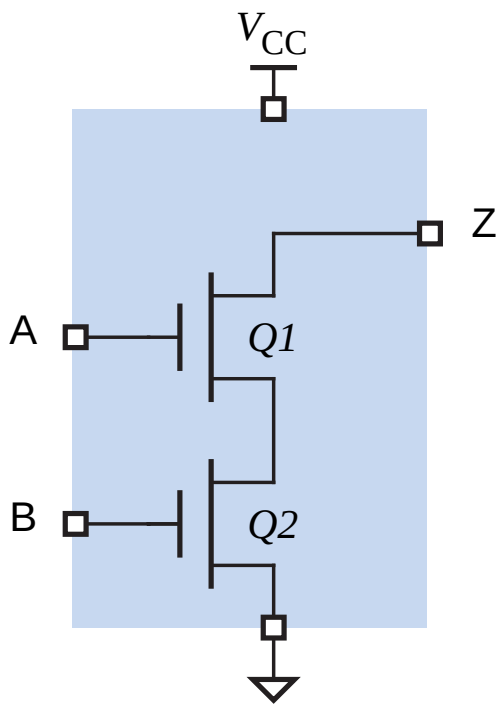
(c)



特殊的CMOS门(5)

- 漏开路门
  - 没有pMOS作为上拉电阻

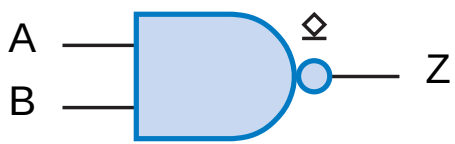
(a)



(b)

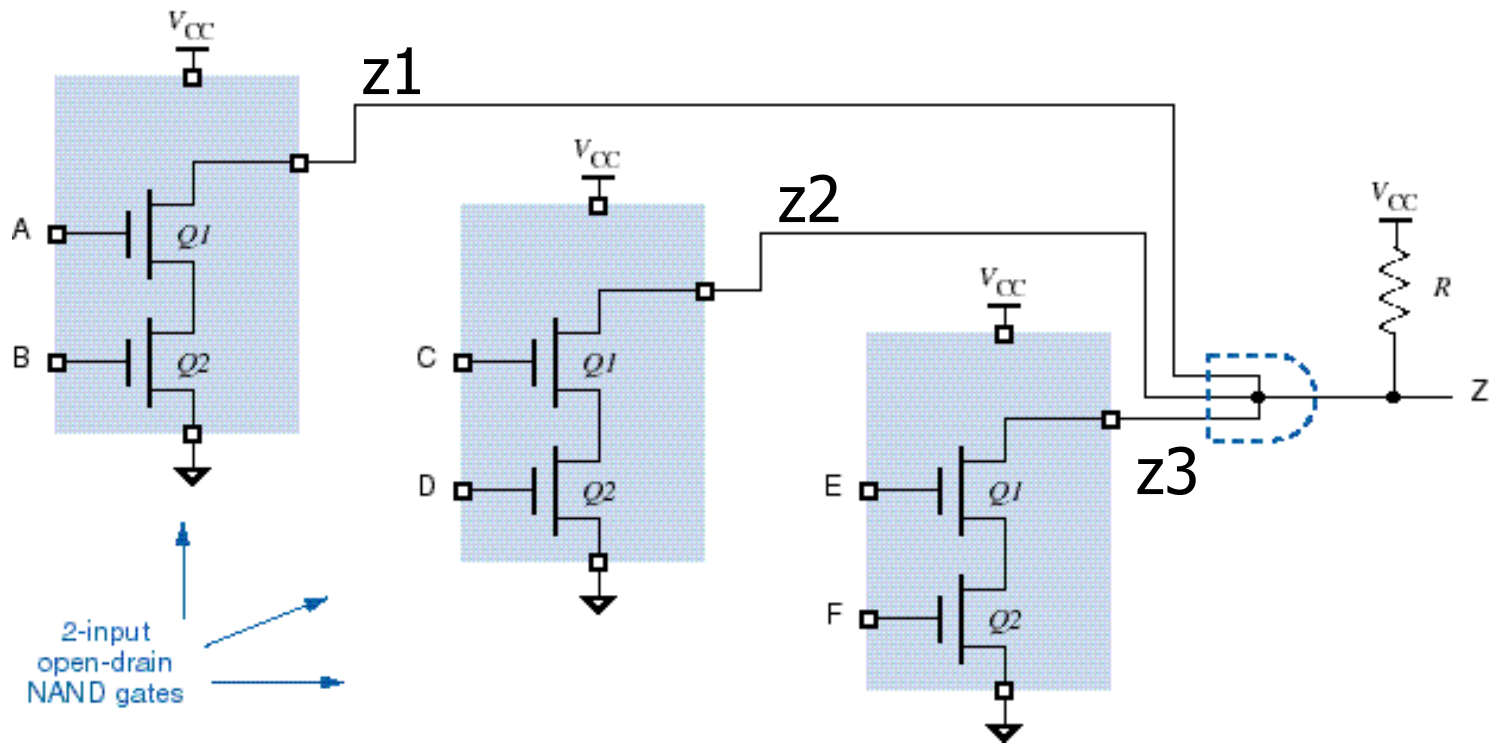
A	B	Q1	Q2	Z
L	L	off	off	open
L	H	off	on	open
H	L	on	off	open
H	H	on	on	L

(c)



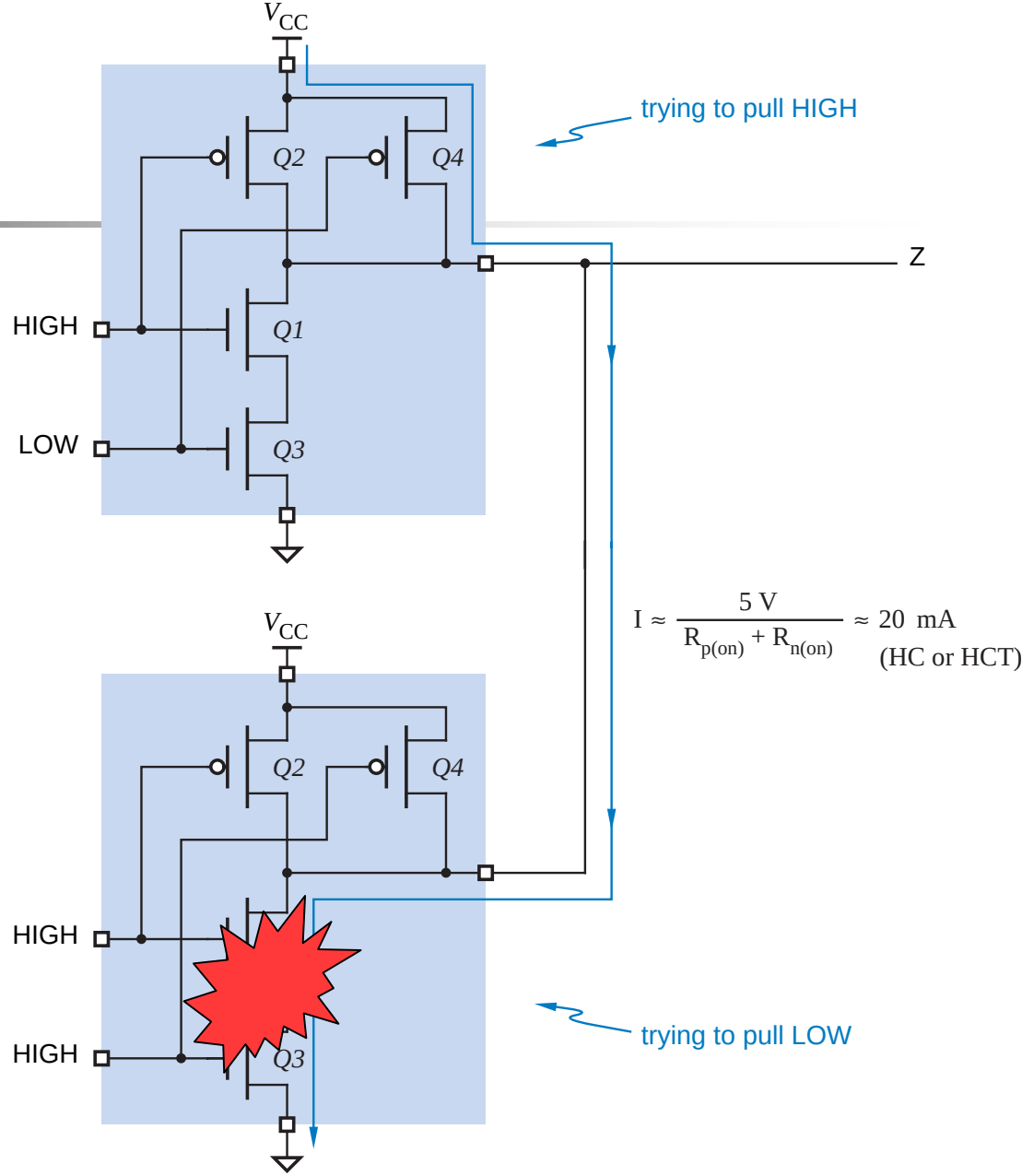
特殊的CMOS门(6)

- 逻辑开路门的应用
  - 线与($Z = z1 \bullet z2 \bullet z3$)



注意

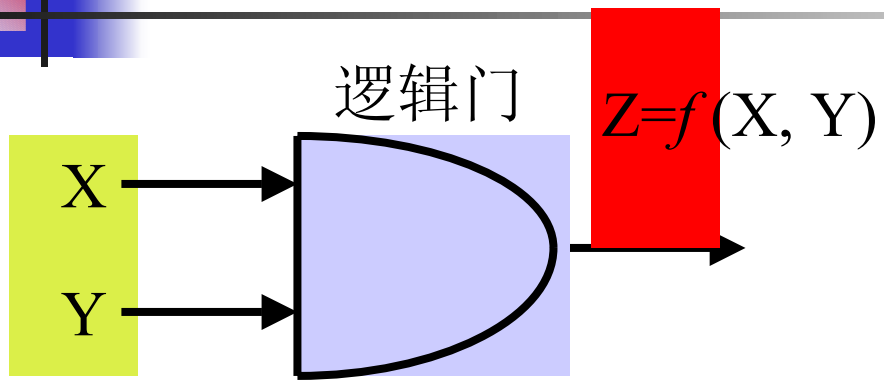
- 避免输出连接


V_{CC}
Q2
Q4
trying to pull HIGH
Z
HIGH
Q1
LOW
Q3
V_{CC}
$I \approx \frac{5\ V}{R_{p(on)} + R_{n(on)}} \approx 20\ mA$
(HC or HCT)
Q2
Q4
HIGH
HIGH
Q3
trying to pull LOW

基础部分总结

- 布尔代数基础
  - 6个公设；9个定理
- 开关代数基础
  - 开关函数;
  - 真值表；SOP；POS
- 开关电路基础
  - 正逻辑、负逻辑
  - 逻辑门：NOT, AND, NAND, OR, NOR, XOR, NXOR
- 数字电路基础
  - 开关模型
  - 逻辑门的实现(CMOS, TTL)

基础部分总结

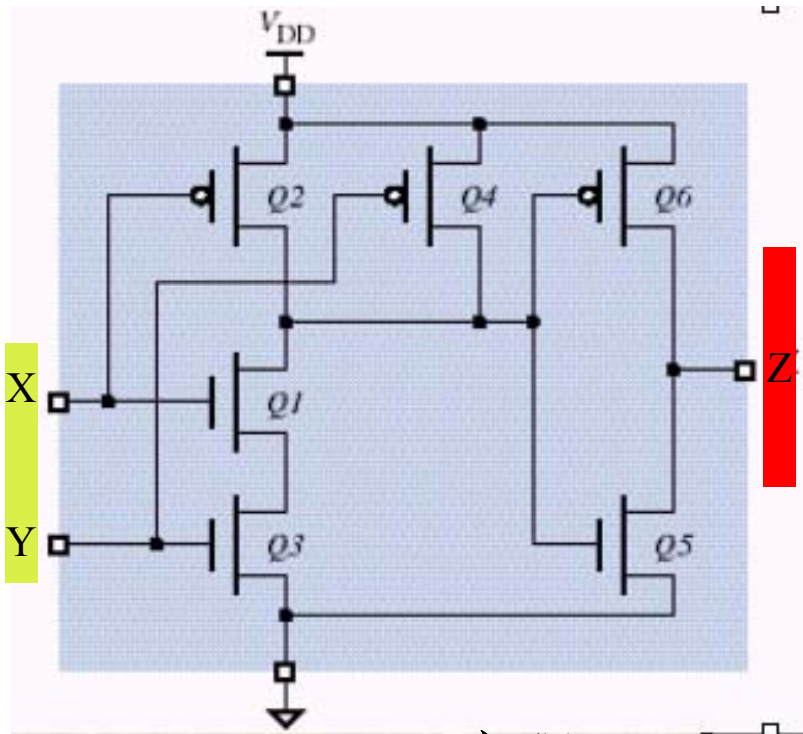


$$f(X,Y) = X \cdot Y$$

开关函数

XY	$f(X,Y)$
00	0
01	0
10	0
11	1

真值表



CMOS实现