[CR1]

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ASSY, POWER SUPPLY, -48V IN, 325W

SIZE	DRAWING NO.	REV
A	XXXXXX	X0.1

SUPPLEMENTS: EF

SHEET 1 OF 77

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. **SCOPE**

This document defines the functional requirements for a **325Watt POWER SUPPLY MODULE** to be developed by Compaq Computer Corporation, intended for world-wide use in electronic data processing equipment. The power supply unit does not contain any fan for cooling. Forced air-cooling for this module must be supplied from an external source. All specifications are applicable under all operating conditions when installed in the End Use system, unless otherwise stated.√

2. **REFERENCE DOCUMENTS**

2.1 **APPLICABLE DOCUMENTS**

The following documents form a part of this specification to the extent specified herein. Unless otherwise indicated, the document is of the issue in effect on the date of invitation to bid or request for proposal.

101045	"Specification, PCB Fabrication." Compaq Document.
106128	"Label, Blank, Thermal Print." Compaq Document.
106166	"Assembly, Manual, Workmanship and Quality Standards." Compaq Document.
106244	"Procedure, Test Electrostatic Discharge." Compaq Document.
106584	"Procedure, Printing, Label Thermal." Compaq Document.
109291	"Test Specification Packaging of Compaq Named Products." Compaq Document.
109893	"Specification, Raw Material, Supplier Packaging/Material Handling." Compaq Document.
114971	"Procedure, Supplier Process." Compaq Document.
117800	"PCB Design Rules and Guidelines, for PCB fabrication, Assembly & Test." Compaq Document.
131400	"Specification, Packaging, Finished Goods Distribution." Compaq Document.
137063	"Specification, Raw Material Supplier, Shipment Bar Codes." Compaq Document.
137114	"Procedure, Unitized Load Package Test." Compaq Document.
137169	"Procedure, Country of Origin Encoding." Compaq Document.
144499	"Specification, Regulated Materials." Compaq Document.
185411	"Standard Label, Commodity Tracking, OEM Assembly, New." Compaq Document.
ANSI C63.4 1992	"American National Standard for Methods of Measurement of Radio-Noise Emissions from Low-Voltage Electrical and Electronic Equipment in the Range of 9 kHz to 40 GHz." American National Standards Institute (ANSI), 1992.

Australian Communications Authority	"Electromagnetic Compatibility Framework - Information for Suppliers – Residential, Commercial and Light Industry"(and amendments), July 1995, URL: http://www.aca.gov.au/standards/emc/emc.htm
BT NR 2511	British Standards Institute (BSI)
CCIB EMC	"Related Regulations of Detailed Rules and Procedures for Implementing the Safety License System of Import Commodities", China Quality Certification Centre For Import and Export Commodities, URL: http://www.ciq.gov.cn/cqcchina/www/index-e.htm , 1999.
CSA C22.2 No.950	"Safety of Information Technology Equipment including Electrical Business Equipment, Third Edition." Canadian Standards Association, 1995.
CSA C22.2 No.234	"Safety of Component Power Supplies, First Edition." Canadian Standards Association, 1990.
C.I.S.P.R. Pub. 22	"Limits and methods of measurement of radio interference characteristics of information technology equipment." International Special Committee on Radio Interference (C.I.S.P.R.), Third Edition, 1997.
EMKO-TSE(74SEC) 207-95	"Summary of Nordic Deviations, CENELEC Common Modifications Explanations, and Other Information when Testing in the Nordic Countries." Electrical Material Control Organizations of the Nordic Countries 1995.
EN 55022	"Limits and methods of measurement of radio interference characteristics of information technology equipment." European Committee for Electro-technical Standardization (CENELEC), Third edition, 1998.
EN 55024	"Information Technology Equipment- Immunity Characteristics – Limits and Methods of measurement." European committee for Electro technical Standardization (CENELEC), 1998.
EN 60 320	"Appliance couplers for household and similar general purposes." European Committee for Electro-technical Standardization (CENELEC), 1987.
EN 60 555-2	"Disturbances in supply systems caused by Household appliances and Similar Electrical Equipment, part 2: Harmonics." European Committee for Electro-technical Standardization (CENELEC) 1987.
EN60 950	"Safety of Information Technology Equipment including Electrical Business Equipment." European Committee for Electro-technical Standardization (CENELEC), 1992 (IEC 950, Second Edition, including Amendments 1,2, 3 and 4).
IEC 61000-4 Sections 2-6,8, 11	"Electromagnetic Compatibility (EMC) Part 4: Testing and Measurement Techniques." International Electro-technical Commission (IEC).
IEC 801 Parts 2-5	"Electromagnetic Compatibility for Industrial Process Measurement and Control Equipment." International Electro-technical Commission (IEC).
ISO 7779	"Measurement of Airborne Noise Emitted By Computer to Business Equipment." International Organization for Standardization.
SDP Handbook	"Compaq Supplier Development Process Handbook." Compaq Document.

Taiwan EMC Law	"Commodity EMC Regulation" (Taiwan EMC Law), Bureau of Standards, Metrology, and Inspection under auspices of the Ministry of Economic Affairs, URL:http://www.bsmi.gov.tw/english/emc/e_emc_hp.htm .
UL 1950	"Safety of Information Technology Equipment including Electrical Business Equipment, Third Edition." Underwriters Laboratories, Inc., 1995

2.2 ORDER OF PRECEDENCE

In the event of a conflict between this specification and references cited herein, this specification shall take precedence.

NOTE:

All materials contained within the product must meet limits contained within the Regulated Material Specification Compaq Document 144499.

2.3 DEFINITIONS

In this document 'power supply module' refers to the complete power supply.
In this document 'converter' refers to a 3.3V, 5V, or 12V dc-dc converter within the power supply module.

3. GENERAL DESCRIPTION

This specification defines a modular, hot pluggable, multiple output, dc-dc switching power supply for use in Compaq Computer systems. This module is intended to be used as part of an N+1 distributed power system. This distribution model also includes one or more bulk power supplies that distribute -48 V dc throughout the host system to provide input power to many local dc-dc converters.

Each module converts the -48 V DC input voltage into regulated 3.3V, 5 V, 12 V, -12V and 3.3V(aux.) outputs. Each module shall be totally self-contained except for forced air-cooling. The maximum number of modules operating in the system is expected to be five. Each module is a self-contained 325W, three output power supply.

4. ELECTRICAL

4.1 DC INPUT

4.1.1 Voltage

The power supply module shall operate from a DC input voltage of -43V to –57V.

Nominal input voltage is -48V DC. The power supply module shall be capable of start-up (power-on) with rated power load, at line voltages as low as -43V DC measured at the input of the power supply.

Below the nominal low voltage cutoff of -43V, it is allowable for the module to shutdown. If the module shuts down, it shall resume normal operation when the input voltage comes back into the specified range.

The power supply module must be able to sustain an input voltage slew rate (dv/dt) up to 0.5V/µS, within the specified input voltage range.

The power supply module should not get damaged for input voltages in excess of -57V DC up to -60V DC.

Any requirements for auxiliary, bias, or control voltage must be generated within the module. The exception is the external +5VSB voltage provided by the host, and used to power the module's monitor circuit. The +5VSB return shall be connected to the power supply module output return.

4.1.2 Current

Maximum steady state input DC current from the 48V bus shall be 9.2 Amps.

For any output load transient as specified in Section 4.2.3, the input current di/dt must not exceed 1.0 A/µS.

Maximum steady state current drawn from the external +5VSB shall be 100 mA.

4.1.3 Input Power Rating

The supply is rated for an input power of 397 Watts at -43V (for reference only).

4.1.4 Input Protection

4.1.4.1 Inrush Current

Maximum inrush current during the application of the -48V input shall not exceed 10A during all power on conditions. The inrush circuit must perform correctly for the case where a power supply module is momentarily removed from a live socket and then quickly re-installed (hot-plugged).

4.1.4.2 Input Over-current

The power supply module shall be protected from excess input current by a suitable electronic fuse. This fuse is required to isolate the module from the input bus under abnormal operating conditions within 100µs. Abnormal operating conditions include internal module failure and external -48V input under-voltage. The electronic fuse must sustain all inrush and operating currents, but open on catastrophic failure of the module.

In the case of internal module failure, the power supply module shall isolate itself from the -48V bus and latch off until the -48V input bus is cycled.

In case of continuous under-voltage on the -48V input bus, the power supply module shall isolate itself from the bus. The module shall automatically reconnect to the bus as soon as the short has been cleared.

If a short occurs on the -48V input bus that is caused by some other external device connected to the bus, then the module shall immediately isolate itself from the input bus so that its bulk input capacitor is not discharged by the input short. The module shall automatically reconnect to the bus as soon as the short has been cleared.

4.1.4.3 Brownout, Under Voltage

The power supply shall contain protection circuitry such that the application of an input voltage below the minimum specified in Section 4.1.1 shall not cause damage to the power supply module nor cause failure of any input fuse. In the event of shutdown due to extended brownout, the power supply shall automatically restart once the DC input is restored to the limits defined in Section 4.1.1.

4.1.4.4 Catastrophic Failure Protection

The primary circuit design and the components specified in the same shall be such that, should a component failure occur, the power supply shall not exhibit the following:

a. Flame
b. Excessive smoke
c. Charred PCB
d. Fused PCB Conductor

4.1.5 Hot-Plug Sequencing

Hot-plugging is the process of inserting or extracting a power supply module from a host system while the host system is powered and operating. During this process, all remaining power supply modules must continue to operate normally and the output voltages at the host system interface must remain within the limits specified in Section 4.2.

The host may contain from 1 to 4 power supply modules. Hot-plugging can occur when the system is operating under either static or dynamic conditions. The power supply module shall be designed to allow connection into and removal from a host system without removing power. During any phase of insertion, start-up, shutdown, or removal, the power supply module shall not cause any other like modules in the system to exceed their specifications. The power supply module shall not be damaged during any phase of insertion or removal while input power is applied.

The ENABLE signals from the host system may or may not be asserted when the power supply module is hot-plugged into the host.

All converter outputs shall have an isolating device to isolate the power supply module from the host system during a power supply failure or during a hot-plug operation. The isolating device must be located within the power supply module. The device can be an “ORing” Diode or the functional equivalent.

4.1.6 Efficiency

The power supply efficiency shall be greater than 82%, when measured at full rated load -43V DC input, and with remote sense connected at the output connector.

4.1.7 Isolation Requirements

The module secondary output returns (GND) shall be isolated from the -48V input primary return and meet a minimum 500V breakdown voltage. The module will meet the following conditions.

DC: 10M Ohms of isolation at 500V DC
AC: f=1KHz to 100KHz: > 500 Ohms of isolation
f=100KHz to 1 MHz: > 50 Ohms of isolation.

4.1.8 Hold-UP Time

If two or more power supply modules are operating in parallel and one module experiences a primary failure, then the electronic fuse (or other protection) in the failed module shall isolate the failed module from the -48V input bus. If such a failure causes the -48V input bus to sag, all the remaining power supply modules must have enough hold-up time such that the healthy modules continue to deliver full rated output power to the load until the input bus recovers.
The hold time shall be 200µsec. minimum from the time input is removed till any output reaching out of regulation level.

4.2 OUTPUT

4.2.1 Voltage

Voltage Regulation Limit On Outputs - The four (5) output channels, when measured at the remote sense pins on the host side of the output connector, shall be within the range shown in Table 1.

TABLE 1
OUTPUT VOLTAGE REGULATION LIMITS

Channel Name	Nominal Output (Volts)	Regulation Limit (Volts)
+3.3V	+3.3	+ 3.20 to +3.40
+5V	+5.1	+4.75 to +5.25
+12V	+12.25	+11.4 to +12.6
-12V	-12.0	-13.2 to –10.8
3.3Vaux.	3.3	+3.17 to +3.650

Regulation limit shall include any input, load, transient load and temperature conditions specified herein. This limit includes output ripple and noise and set point tolerance.

4.2.2 Current

The module shall have the following minimum and maximum output currents under static operating conditions:

TABLE 2
MINIMUM AND MAXIMUM OUTPUT CURRENTS

Voltage channel	Min Load Current (A)	Full Load Current (A)
+3.3V	0.0	50.0
+5.0V	0.0	30.0
+12.0V	0.0	15.0
-12.0V	0.0	2.0
3.3Vaux.	0.0	5.0

Note 1) The total continuous and surge load power shall be limited to that specified in Section 4.2.9.

Note 2) The combined 3.3V and 5V output shall not exceed 180 Watts.

The module shall operate in a no load condition. When the module is subsequently loaded, it must begin to regulate and source current without triggering failures or causing control signals to malfunction.

4.2.3 Load Transient Response (Step Load)

All outputs must maintain regulation during specified load transients with the remote sense signals connected at the output connector pins on the host system side of the connector pair.

4.2.3.1 3.3V Transient Response

For a step load change of 10A, the slew rate of the transient load step shall be at least 1 A/µs. For a step load change of 50A, the slew rate of the transient load step shall be at least 0.5 A/µs. The +3.3V output voltage shall be measured at the converter output pins on the host side of the output connector. The output voltage must remain within the voltage range shown in Section 4.2.1. The transient response shall be measured over a 0 to 100 MHz frequency band, and at ambient temperatures between 0°C and 50°C.

4.2.3.2 5 V Transient Response

For a step load change of 10 A, the slew rate of the transient load step shall be at least 1 A/µs. For a step load change of 30A, the slew rate of the transient load step shall be at least 0.5 A/µs. The +5V output voltage shall be measured at the converter output pins on the host side of the output connector. The output voltage must remain within the voltage range specified in Section 4.2.1. The transient response shall be measured over a 0 to 100 MHz frequency band, and at ambient temperatures between 0°C and 50°C.

4.2.3.3 12 V Transient Response

For a step load change of 5 A, the slew rate of the transient load step shall be at least 1 A/µs. For a step load change of 15A, the slew rate of the transient load step shall be at least 0.5 A/µs. The +12V output voltage shall be measured at the converter output pins on the host side of the output connector. The output voltage must remain within the voltage range specified in Section 4.2.1.

4.2.3.4 Transient Cross-Regulation

At nominal DC input line voltage, any single converter output shall be subjected to the transient loads described in Section 4.2.3, while all the other converter outputs are within their respective static load ranges as defined in Section 4.2.2. Under these conditions, all outputs shall remain within the transient regulation limits as defined in Section 4.2.1.

4.2.4 Output Ripple/Noise

Maximum allowable peak-to-peak ripple and noise (as measured at the output connector on any output channel) shall be a maximum of 30mV for the +3.3V and 3.3Vaux. channels, a maximum of 50mV for the +5V channel, and a maximum of 120mV for the +12V and –12V channels. The ripple and noise shall be measured over a 20Hz to 100MHz frequency band. A resistive load (non-electronic) shall be used for this measurement. Each output shall be by-passed to return by a 10uF tantalum capacitor with an ESR less than 100 mΩ in parallel with a 0.47µF ceramic capacitor, at the point of load. The load cable shall be 12" of twisted wire capable of carrying the rated current.

4.2.5 Remote Sense

The +3.3V, +5V, +12V outputs shall have provisions for remote sense of the voltage at the load. Each channel shall be capable of compensating for up to 200 mV of drop in both the output and return legs. In the event of an open sense line, these outputs shall not initiate an over-voltage fault. A faulty module shall not load down the remote sense lines and cause errors on the voltage sense of the remaining modules. The remote sense line resistance shall not exceed 10 Ohm. Two pins (one each for Sense+ and Sense-) shall be allocated on the output connector for each of the three module outputs.

4.2.6 Stability

The power supply shall be unconditionally stable while operating within its normal operating specification and including load capacitance ranges as follows:

TABLE 3
CAPACITIVE LOADING

Output Channel	Minimum	Maximum
+3.3V	0	15000µF
+5V	0	10000µF
+12V	0	10000µF
3.3Vaux.	0	4700µF

4.2.7 By-Pass

The output return shall be connected to the chassis by a high frequency capacitor with a tested withstand voltage of 50V DC minimum.

4.2.8 Overshoot

There shall be no voltage overshoot outside of regulation limits on any channel during startup or shutdown. During startup or shutdown, the output voltage on any channel shall be a monotonically increasing or decreasing function once outside of the regulation window.

4.2.9 Maximum Output Power

The power supply module shall be capable of continuously supplying, when installed in the end use system, 325W combined output power from all outputs under all specified conditions.

4.2.10 Output Protection

The power supply module shall automatically shutdown under any fault condition as described below:

4.2.10.1 Over-voltage (OVP)

The power supply module shall be provided with over-voltage protection such that under any single component failure, no output channel shall exceed the upper limit of the voltage ranges specified below:

TABLE 4
OVP LIMITS OF OUTPUT CHANNELS

Channel	Trip Voltage (Vtrip)
+3.3V	3.7 to 4.3V
+5V	5.5 to 6.3V
+12V	12.9 to 14.2V
3.3aux.	3.7 to 4.3V

The over-voltage trip point may be set anywhere within the limits defined in Table 4. Over-voltage trip on any output (as defined in Table 4) shall open the input electronic fuse or cause all three outputs of the module to power down and latch off. The over-voltage protection circuit must protect against the following conditions:

- Open feedback/sense line
- Shorted output MOSFETs
- Faulty reference voltage in the control circuit or driver failure

Once an over-voltage has occurred, the main outputs shall remain disabled until the ENABLE signal is toggled, or the input power is cycled. No variation of input voltage or output current shall be allowed to falsely trigger the OVP circuit.

4.2.10.2 Output Over-current

The power supply shall limit the maximum steady state output currents to the following values:

TABLE 5
OVER CURRENT LIMITS OF OUTPUT CHANNELS

Channel	Maximum output Current
+3.3V	130% above Load level (Section 4.2.2)
+5V	130% above Load level (Section 4.2.2)
+12V	130% above Load level (Section 4.2.2)
3.3Vaux.	130% above Load level (Section 4.2.2)

The output over-current threshold for each of the three output channels shall be set between 110% and 130% of maximum rated output current. An over-current occurrence on any output channel must exist for at least 150mS before the over-current circuit shall be allowed to trip. The over-current circuit must trip within 500mS after a continuous over-current condition has occurred. Over-current trip on any output channel shall cause all three outputs of the module to power down and latch off. The ENABLE signal must be toggled or the input power must be cycled to restore operation.

The power supply module must be able to power-on into an overload without damage or overstress to the circuitry.

A short circuit to any output for an indefinite period of time shall not result in damage to the power supply module. The module shall be protected such that a short between outputs or from any output to return shall not result in a fire hazard or shock hazard. √

4.2.10.3 Over-temperature(OTP)

The power supply module shall be protected such that attempted operation with an inlet air temperature greater than that specified in Section 5.1 shall not result in damage to the power supply. If the module is to be shut down to accomplish this protection, the minimum inlet air temperature to trigger the inhibit shall be 60°C at 200 linear feet per minute (LFM) of airflow.

In the event of fan failure or airflow restriction, the power supply module shall protect itself such that semiconductor junction temperatures are not allowed to exceed the manufacturer's absolute maximum ratings and reinforced insulation does not exceed EN 60 950 (IEC 950) thermal limits.

Whenever the module exceeds its maximum safe operating temperature, it shall shut down and latch off to protect itself from over-temperature of its components,
An over-temperature trip shall cause all three outputs of the module to power down and latch off.
Once an over-temperature has occurred, all outputs shall remain disabled until the ENABLE signals are toggled, or input power is cycled.

4.2.11 Power-On Time

4.2.11.1 Output Regulation Delay

All outputs shall be in regulation within 10mS to 100mS after valid input power has been applied for the case where the ENABLE signals are already asserted. For the case where the ENABLE signals are asserted after application of input voltage, the output voltage s shall be within its specified range within 10 to 20mS from the time the each ENABLE signal is asserted. The timing diagrams are shown in Figures 1 and 2.

FIGURE 1
DC-DC CONVERTER OUTPUT TIMING: INPUT VOLTAGE CONTROLLED

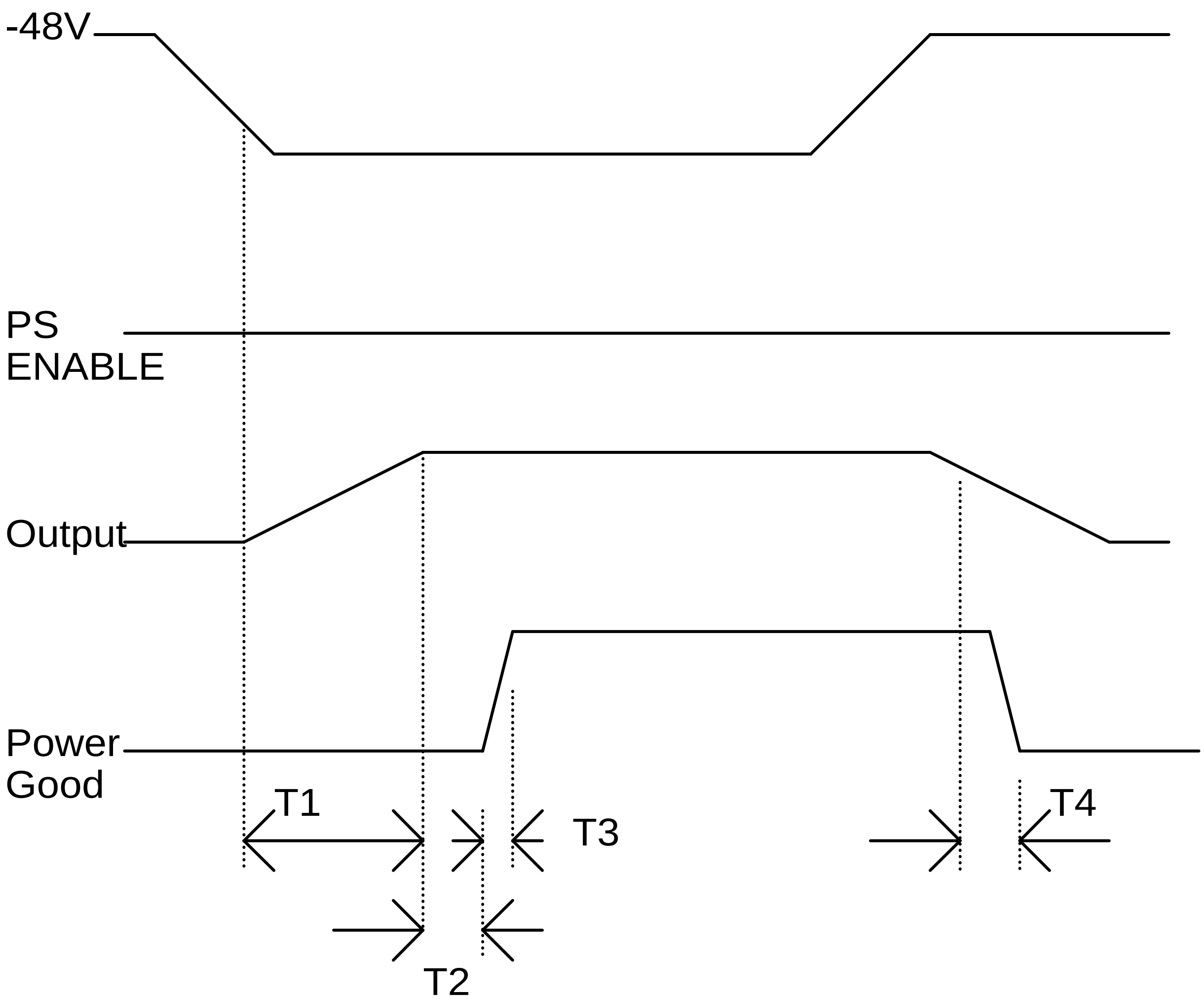


TABLE 6
POWER-ON TIMING PARAMETERS – INPUT VOLTAGE CONTROLLED

POWER	MINIMUM	MAXIMUM
T1	5 ms	100 ms
T2	0	5 ms
T3	0	10 µs
T4	0	20 µs

FIGURE 2
DC-DC CONVERTER OUTPUT TIMING: ENABLE CONTROLLED

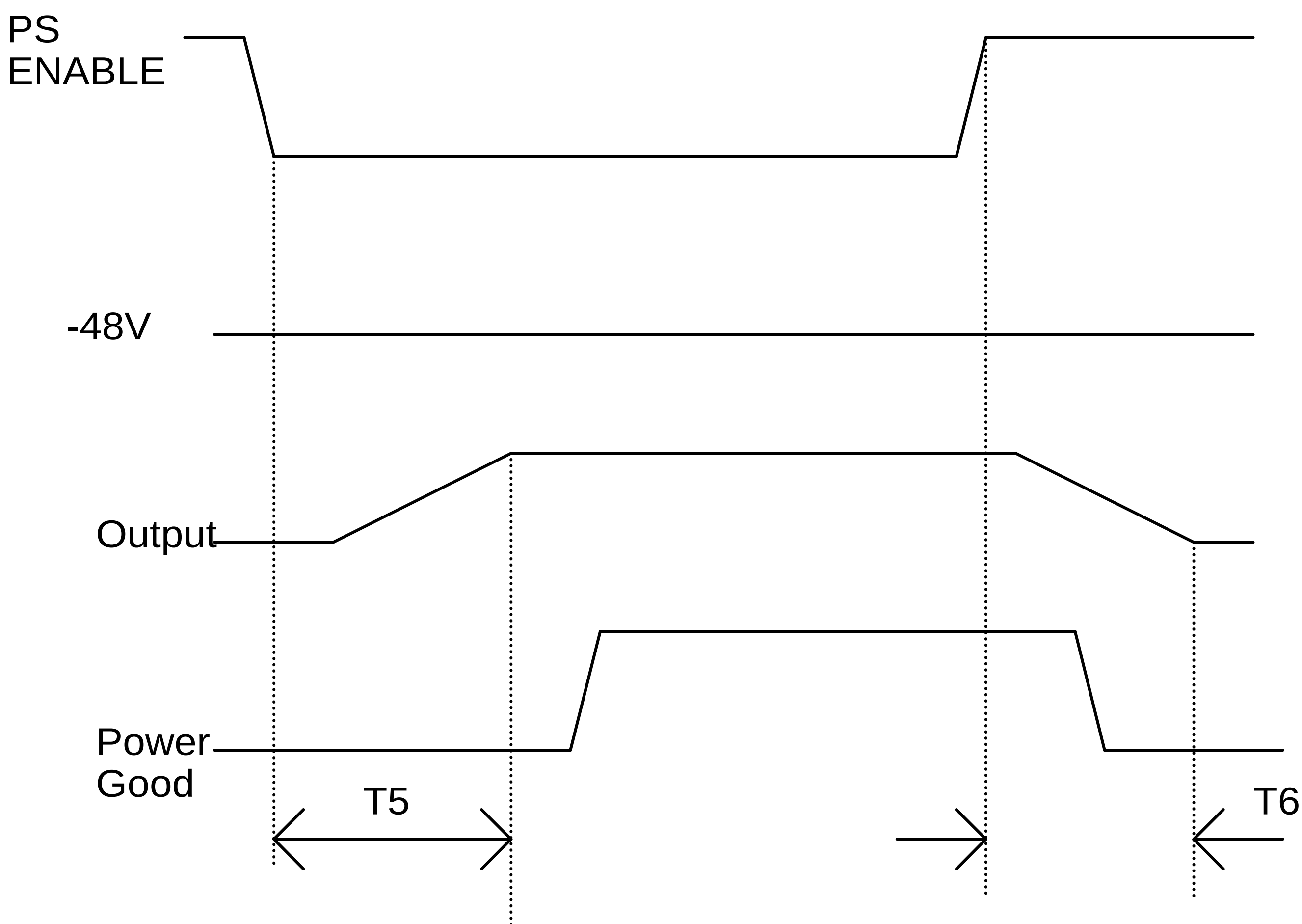


TABLE 7
POWER ON TIMING PARAMETERS – OUTPUT ENABLE CONTROLLED

	Minimum	**Maximum**
T5	10 ms	20 ms
T6	5 ms	300 ms

Note: PS shall meet T2,T3,T4 requirements(per table 6) in addition to T5, T6 for Enable controlled power on/off.

4.2.11.2 Power-On Sequencing

3.3Vaux. output and other internal house keeping voltages shall come up as soon as input power is applied to the power supply. These outputs shall decay later than main output voltages upon removal of input power.

There shall be two ENABLE signals (5V/12V Enable and 3.3V Enable) in this power supply. Each ENABLE signal sequence shall follow given timing requirements in Figure 2. If both Enables are pre-asserted and the power supply is powered on by applying input voltage, 3.3V output shall not exceed 5.1V output at any time and the max. differential between 5V and 3.3V shall be 2V.

4.2.11.3 Non-Latching Power-on Delay

In the case of non-latching shut down (such as might be caused by input brownout, etc), the power supply module is required to automatically restart. There shall be sufficient start-up delay to ensure that all module circuitry is in a defined and stable state.

4.2.12 Power-Off Decay

The +3.3, +5.0, and +12.0V outputs will decay to <300mV within 300 msec after the ENABLE signals are de-asserted and within 1 sec. after the input power is removed.

4.2.13 Enable Signal (ENABLE)

The +5V, and +12V converters shall have a common ENABLE signal labeled 5V/12V ENABLE_. The 3.3V converter shall have an independent enable labeled 3.3V ENABLE_. The host shall utilize the ENABLE signals to turn-on and turn-off the power supply module. The outputs of the module shall become operational when the ENABLE signal is below 0.8V and disabled when this signal is above 1.7V. The module shall not load these signals with more than 1mA. The ENABLE signal is referenced to output voltage return (GND). Two single pins on the output connector has been allocated for these signals.

4.2.14 Power Good (PWR_GOOD)

5V and 12V outputs shall have a common Power Good signal labeled 5V/12V POWER GOOD. This signal shall be logic high when both 5V and 12V outputs are in regulation, and it shall be active low when any of the two outputs are out of regulation.

3.3V output shall have an independent Power Good signal labeled 3.3V POWER GOOD. This signal shall be logic high when both 5V and 12V outputs are in regulation, and it shall be active low when any of the two outputs are out of regulation.

Each PWR_GOOD signal shall be controlled by an open collector device consistent with TTL DC specifications, and should maintain less than 0.4V while sinking up to 5mA. Each PWR_GOOD signal shall be pulled high through a pull-up resistor located externally. This signal must transition high to the open (> 100K) state within 5mS after the output stabilizes in the range specified. Signal rise and fall times must be 20µS or faster. The signal must be in the low impedance state (to secondary GND) whenever the output voltage goes outside of its specified limits.

4.2.15 Module Present (MOD_PRESENT_)

The MOD_PRESENT_ signal is provided so that the host system can sense the presence of a power supply module (without respect to the operational status). A mechanically shortened pin on the module output connector is grounded on the module side to pull the PRESENT signal from the host to DC ground. When the power supply module is not present, the

MOD_PRESENT# signal on the host side will be pulled to a logic high through a pull-up resistor located on the host system board. The MOD_PRESENT# signal is active low.

4.2.16 Module Ready Signal

This is an internal signal to the power supply which is used for monitoring functions utilizing the micro controller.

This signal shall be asserted logic high when 3.3Vaux. output is in regulation and other housekeeping circuits are powered up and functioning as expected upon application of input power to the module. Assertion of this signal to high state would mean that the module is ready and waiting for ENABLE signals to be asserted logic low for powering up the main outputs.

4.2.17 Output Current Signal

THE +3.3V, +5V, +12V CONVERTERS SHALL EACH HAVE THEIR OWN SIGNAL TO REPORT OUTPUT CURRENT. A TOTAL OF THREE PINS ON THE OUTPUT CONNECTOR ARE ALLOCATED FOR THIS PURPOSE. THE POWER SUPPLY MODULE SHALL PROVIDE A MEANS OF MEASURING THE OUTPUT CURRENT FOR EACH OUTPUT CHANNEL FROM A MINIMUM OF 10% TO 100% OF FULL LOAD CURRENT FOR THE 5V AND 12V OUTPUTS AND A MINIMUM OF 30% TO 100% OF FULL LOAD FOR THE 3.3V OUTPUT CHANNEL UNDER NORMAL OPERATING CONDITIONS. AN UNINTENTIONAL SHORT FROM THIS SIGNAL TO GROUND SHOULD NOT EFFECT THE DC-DC CONVERTER OPERATION. THE RANGE OF VOLTAGE AT THE CONNECTOR PIN SHALL BE LIMITED FROM 0.0 TO 4.0V. THE OUTPUT CURRENT FOR +3.3V IS SPECIFIED IN FIGURE 3. THE OUTPUT CURRENTS FOR +5V AND +12V ARE SPECIFIED IN

FIGURE 4 AND

Figure 5.

Output Current Signal Characteristics:

The output current signals described in Section 4.2.17 are also the input signals to the micro-controller. The output current signals shall be defined by the following transfer function:

$I = (m * V) + Io$

WHERE ' I ' IS THE MEASURED OUTPUT CURRENT, 'M' IS THE SCALING FACTOR (GAIN), ' IO ' IS THE OFFSET AND ' V ' IS THE CURRENT SENSE CIRCUIT OUTPUT VOLTAGE (SEE FIGURE 3,

FIGURE 4, AND

Figure 5).

The function described above is an equation of a straight line. The following restrictions are placed on the terms:

V = 4V @ I = 1.2 * (full scale output current)
Io ≤ 0.1 * (full scale output current)

The average gain and offset of the transfer function are defined as the values arrived at when two points, taken at half scale output current and full scale output current respectively, are used to solve for a simultaneous solution. One more restriction on the output transfer function addresses the “straightness” of the line without introducing higher order terms:

The gain and offset values for the transfer function of the output current sense circuit, calculated using any two points between ten percent of full scale and full scale output current values, shall be within one percent of the average gain and offset values defined earlier.

FIGURE 3
OUTPUT CURRENT SIGNAL FOR 3.3 VOLT CHANNEL(REFERENCE GRAPH,SCALED FOR 65A FULL LOAD CURRENT)

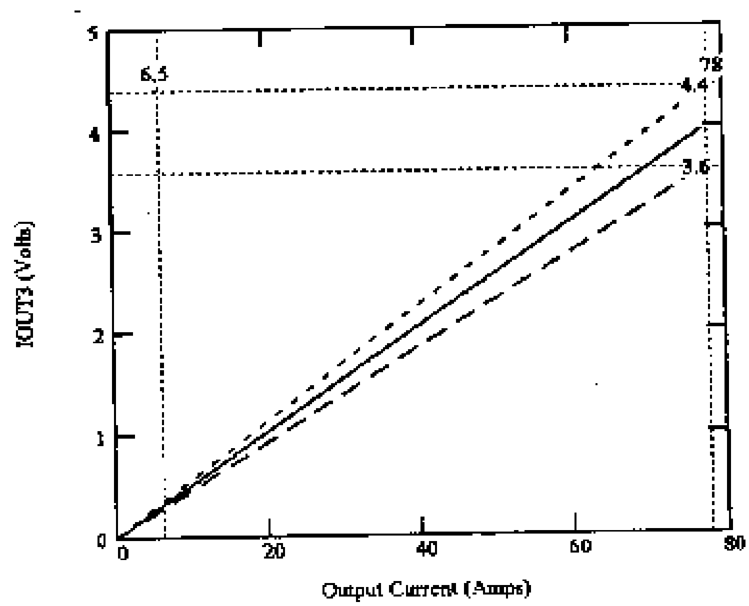


FIGURE 4
OUTPUT CURRENT SIGNAL FOR 5 VOLT CHANNEL(REFERENCE GRAPH, SCALED FOR 25A FULL LOAD CURRENT)

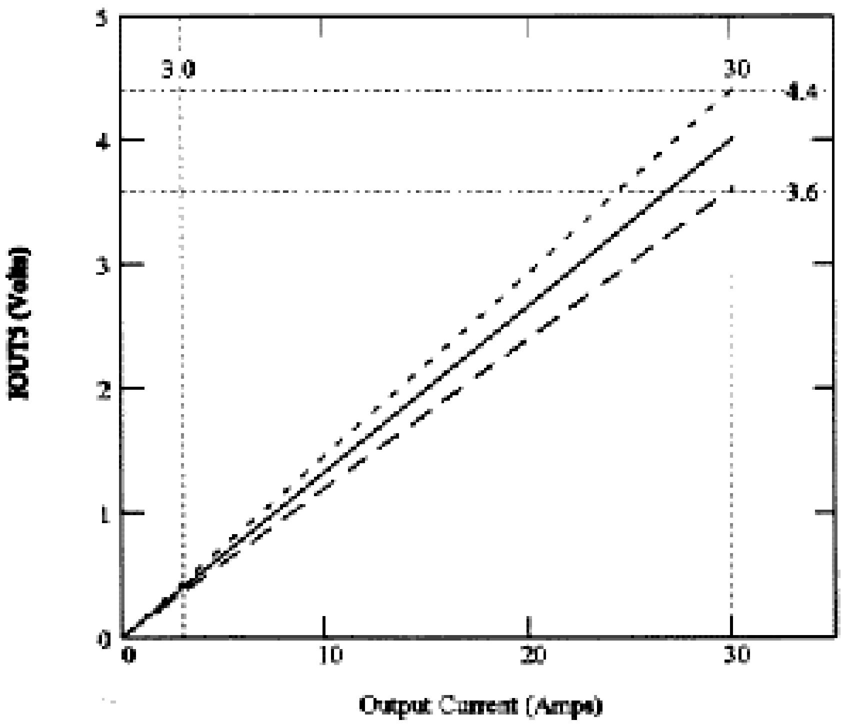
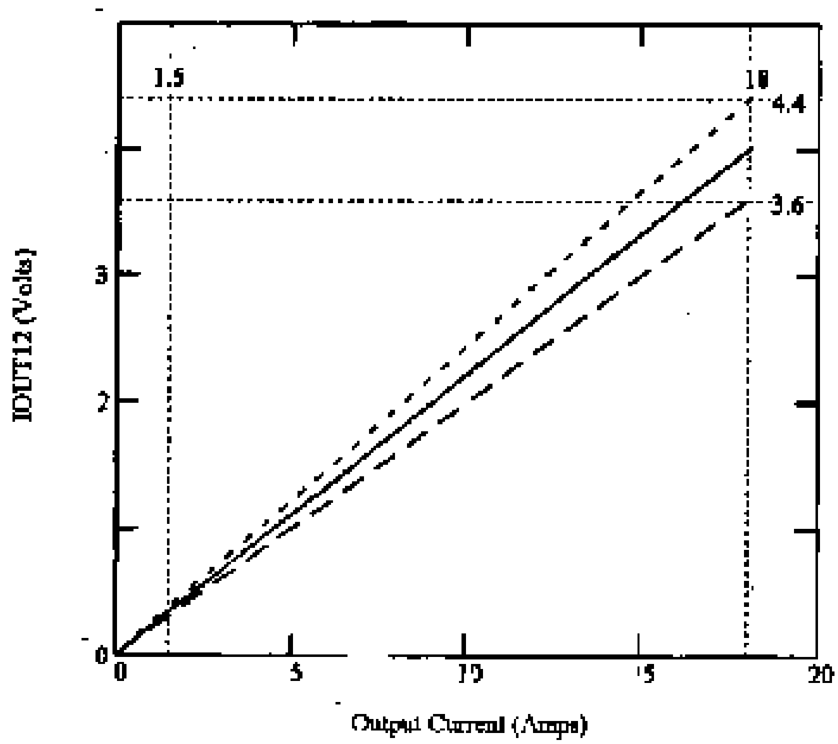


FIGURE 5
OUTPUT CURRENT SIGNAL FOR 12 VOLT CHANNEL



4.3 CURRENT SHARING

The 3.3Vaux. output of each module shall have passive current share characteristics amongst multiple modules. The main outputs of the each converter shall be designed to support current sharing. The pin designated Ishare for each output channel is intended to permit from two to five power supply modules from the same vendor to balance the total load current between them. The power supply module shall provide a means of balancing output currents on the +3.3V, +5V, and +12V channels within the limits specified in the following table:

TABLE 8
CURRENT SHARING LIMITS

Output Channel	Maximum Current Share Difference (ΔI)
+3.3V	6A
+5 V	2A
+12 V	1A

As an example, if three modules in the same host system are supplying a total system 3.3V load current of 90A, then any single module must supply between 27A and 33A of that total current. The difference between any two output currents (of the same channel) of modules shall be within the limits specified in Table 8. This shall apply for a system load current from minimum load (ICC1, 100mA) to full load current (ICC2) under normal operating conditions (see Table 9).

Load Share (Ishare) signal Characteristics:

The power supply modules load share by using a single load Ishare bus signal connected between the power supplies for the same output channel. If current sharing is disabled by shorting the Ishare bus to ground, then each module must continue to operate within ±20% of the full load current of a single module. A pin on the output connector for each channel is allocated to interface with the other power supply modules in the system. The current sharing bus specification is defined in Figure 6, Figure 7, Figure 8, and Table 9. The failure of any power supply module shall not affect the load sharing or output voltages of the other supplies still operating. The power supplies must be able to load share with up to 100mV of drop between the grounds of the different power supply outputs. Each power supply load share line must sink no more than 0.5mA from the load share bus. Each power supply load share line shall be capable of sourcing 4.0mA to the load share bus.

FIGURE 6
3.3 VOLT ISHARE BUS OPERATION(REFERENCE GRAPH, SCALED TO 65A FULL LOAD CURRENT)

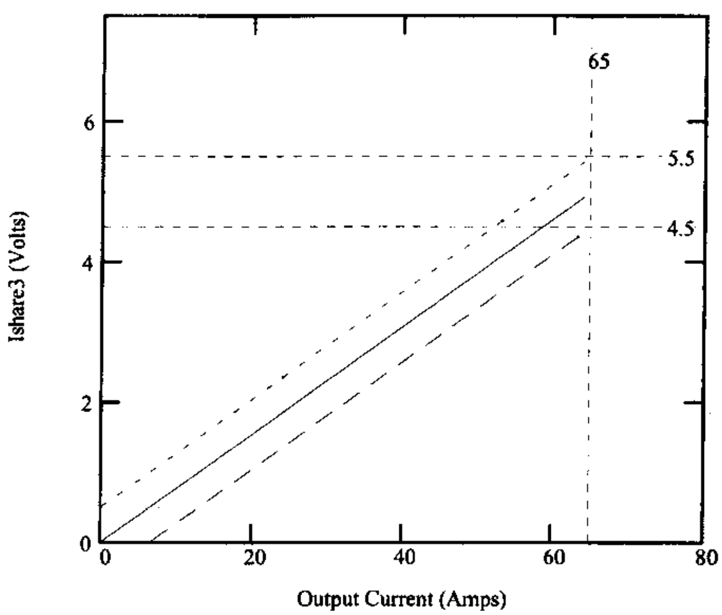
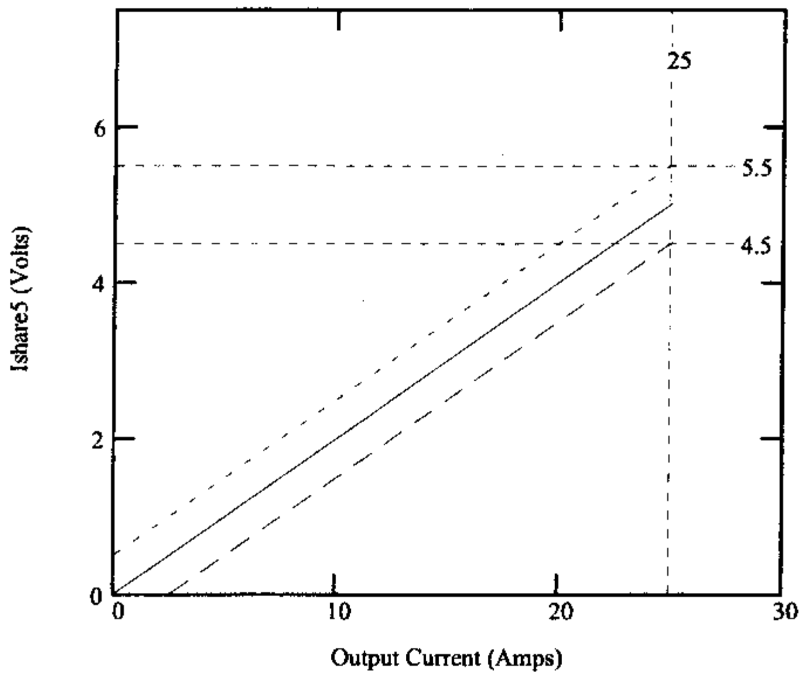


FIGURE 7
5.0 VOLT ISHARE BUS OPERATION (REFERENCE GRAPH, SCALED TO 25A FULL LOAD CURRENT)



	SIZE	DRAWING NO.			REV
COMPAQ	A	XXXXXX			X0.1
	DRAWN		SCALE 1/1	SHEET 27 OF 75	

FIGURE 8
12.0 VOLT ISHARE BUS OPERATION

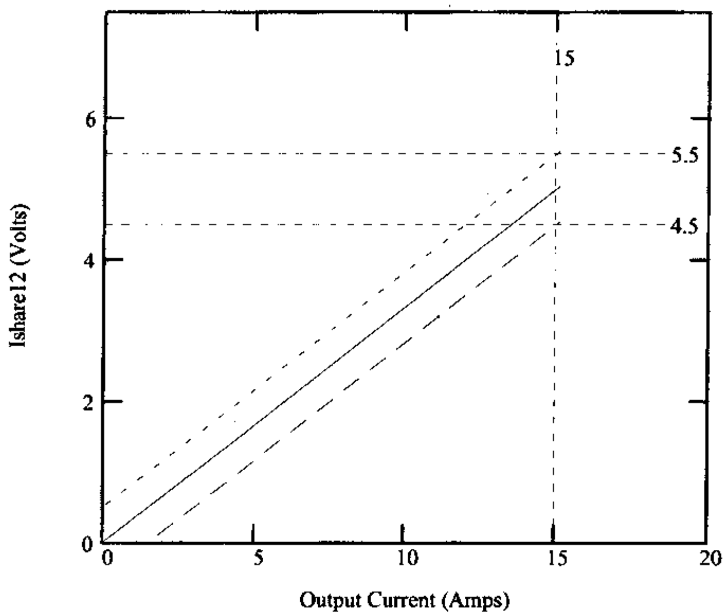


TABLE 9
LOAD SHARE BUS SPECIFICATIONS

	+3.3V	**+5V**	**+12V**
ICC1	100mA	100mA	100mA
ICC2	50A	30A	15A

4.4 MONITORING FUNCTIONS

4.4.1 Visual Indicators

The module shall have two LED indicators, one green and one amber, located on the opposite face of card edge gold fingers, location of the LEDs is left up to vendor's discretion. The operation of the LEDs are defined in Sections 4.5.1.4.1, 4.5.1.4.2, and Table 12.

The amber LED can be driven by an external source as well. Pin D1 on the output connector has been allocated for this purpose.

4.4.2 Monitor Circuit

The power supply module shall contain a monitor circuit including a micro-controller. The monitor circuit shall be used primarily to communicate power supply status to the host system via LEDs and a System Management Bus implemented via the PHILIPS I^2C bus specification. The functionality and implementation of the monitor circuit are specified in detail in Section 4.5.

4.5 MONITOR CIRCUIT

The power supply module utilizes a micro-controller, EEPROM, and associated circuitry primarily to monitor the module's operating status and to report power supply status to the host computer. Bi-directional communication with the host computer takes place via an I^2C bus. Each module connected to the host I^2C bus shall respond to its own unique base address determined from the value of its three address pins. A module's EEPROM address is determined by an offset of 0xA0 added to the value of its base address. A module's micro-controller is accessed by a second address determined by an offset of 0X30 added to the value of its base address. The power supply monitor circuit shall operate as an I^2C slave device only. The mapping and contents of the EEPROM appear in Appendix A and Appendix B at the end of this document.

The monitor circuit provides the following functionality:

- It controls the operation of the green and amber status LEDs
  It reports module operating status, inlet air temperature, output currents, and faults to the host computer via the I^2C bus

4.5.1 Monitor Circuit Hardware

The power supply module monitor circuit includes an NEC 78F9136A micro-controller, a 24C03 EEPROM, and other control circuitry. All circuit components shall operate at + 5V. The +5V shall be derived from external +5VSB coming into the module through the output connector (pin C5). The +5VSB voltage can vary from +4.75V to +5.25V.

4.5.1.1 Initialization Delay

When DC power is initially applied to the power supply, the FRU (EEPROM) and the micro-controller reporting functions will not be available to the system I^2C bus for a period of 200mS. During this time the micro-controller is loading it's calibration tables from the EERPOM, and any commands from the host will be ignored. After this period expires, the host system has access via the I^2C bus to both devices.

4.5.1.2 Power Supply Addresses

As many as four different power supplies can reside on the I^2C bus. Each module can have any of the addresses as indicated in the following table:

TABLE 10
MICRO-CONTROLLER AND EEPROM ADDRESSES

A1	A0	Address	
		EEPROM	Micro-controller
Low	Low	0xA0	0x30
Low	High	0xA2	0x32
High	Low	0xA4	0x34
High	High	0xA6	0x36

4.5.1.3 Signal Inputs to the Monitor Circuit

Inputs to the monitor circuit are provided by other hardware components that already exist elsewhere in the module.

4.5.1.3.1 <u>Module Output Currents</u>

The monitor circuit shall report output current for each output channel to the host system. The monitor circuit must measure and report output current from a minimum of 10% to 100% of full load current for the 5V and 12V output channels, and a minimum of 20% to 100% of full load for the 3.3V output channel. The output current shall be reported with the following resolution and accuracy:

TABLE 11
MONITOR CIRCUIT OUTPUT CURRENT ACCURACY

Output	Resolution	Accuracy
3.3V	250 mA	±2% of full load current value
5V	170 mA	±2% of full load current value
12V	80 mA	±2% of full load current value

Other circuits in the power supply module must provide analog signals representing output current to the monitor circuit inputs. To achieve the specified output reporting accuracy, calibration constants may be stored in the EEPROM during manufacturing final test (see Section 4.5.4.1). The output current shall be reported along with the minimum usable output current. The minimum usable output current will be a value determined during the manufacturing calibration process. This will be the value of output current below which electrical noise causes the measurement to become inaccurate and no longer useful.

4.5.1.3.2 Module Inlet Air Temperature

The power supply monitor circuit shall report the inlet air temperature of the power supply module to the host system. The temperature span should be from 20°C to 100°C with a 1°C resolution. The temperature shall be reported with at least 5% accuracy over the range from 35°C to 75°C.

4.5.1.3.3 Protection Signals

An over-voltage event on any module output shall set the over-voltage status bit in the micro-controller Control Status Register to high.

An over-current event on any module output shall set the over-current status bit in the micro-controller Control Status Register to high.

4.5.1.3.4 Other Inputs

In order to provide all monitoring functions, certain other input signals to the monitor circuit are required.

The ORed combination of the +3.3 PWR_GOOD, +5/+12V PWR_GOOD signals must be provided as a logic input to the monitor circuit.

The OTP signal must be provided as a logic input to the monitor circuit.

The ANDed combination of 3.3V ENABLE_, 5V/12V ENABLE_ signals must be provided as a logic input to the monitor circuit.

The over-voltage and over-current signals must be provided as logic inputs to the monitor circuit.

Module Ready signal must be provided as a logic input to the monitor circuit.

4.5.1.4 Signal Outputs From the Monitor Circuit

The monitor circuit provides both hardware and digital data outputs. This section specifies the hardware outputs.

4.5.1.4.1 Green Status LED

The micro-controller shall control the status of the green LED. The micro-controller controls the green LED through an open drain output. The green LED is connected through an internal pull-up resistor to external +5VSB.

The green LED shall blink about once per second (50% duty cycle) when the module is ready, but the output channels are not enabled. The green LED shall glow continuously when the 'ENABLE' signal and all three 'PWR_GOOD' (power good) signals are high (see Table 12).

4.5.1.4.2 Amber Status LED

The micro-controller controls the amber LED through an open drain output. The amber LED is connected through an internal pull-up resistor to external +5VSB.

The amber LED shall momentarily glow solid by default every time the module is plugged into a back plane which supplies external 5VSB. The LED shall turn off as soon as the internal housekeeping voltages are up, 3.3V aux. Power is good and READY# is asserted low.

If the PS fails to power up it's internal housekeeping circuits and 3.3V aux. For any reason, the LED shall continue to light solid Amber until the condition is corrected.

The amber LED shall glow continuously whenever any fault occurs that requires the module to be replaced. The amber LED shall blink about once per second (50% duty cycle) whenever, the module shuts down and latches off due to an over-current (OC) trip on any output channel (see Table 12).

If 48V is applied at the module input, the READY# is low, ENABLE is low, but PWR_GOOD never goes high, then the power supply module is considered to be bad and the amber LED should be lit.

If the power supply is operating normally, and the hardware over temperature (OTP) is triggered, it must be assumed that the module is defective, even though it might not be. The module should latch off and the amber LED should be lit.

If the power supply is operating normally and the PWR_GOOD signal falls low due to an output voltage that has gone too low or gone away, then the module is considered to be bad and the amber LED should be lit.

If the power supply is operating normally and the PWR_GOOD signal falls low due to an output voltage that has suddenly gone too high, it will not be clear at first which module is defective. The bus voltage will momentarily go too high, and the PWR_GOOD on all modules will momentarily go low. But is assumed that the voltage on the failing module will keep right on rising until it finally triggers its over voltage threshold (OVP). Then that module will latch off and shut down. After that, the PWR_GOOD on the remaining modules should go high again. The amber LED on the defective module should be lit.

The amber LED shall glow continuously whenever both calibration tables stored in the EEPROM are bad.

TABLE 12
LED TRUTH TABLE

SIGNALS							**LEDs**		**Remarks**
EN	PG	OC	READY#	CAL. TABLE	OTP	OVP	Green	Amber	
H	X	X	L	Good	L	L	Flash	Off	No ENABLE Signal
L	H	L	L	Good	L	L	Solid	Off	Operational
L	L	L	L	Good	L	L	Off	Solid	No Power Good signal
X	X	X	X	Bad	X	X	Off	Solid	Cal. table Bad
L	X	H	L	Good	L	L	Solid	Flash	Over-Current
L	X	X	L	Good	H	L	Off	Solid	Over-temp
L	X	X	L	Good	L	H	Off	Solid	Over-voltage
X	X	X	X	X	X	X	Off	Solid	Dead Module

NOTE:

X – Don’t care; L- Low; H - High

4.5.1.5 Connector Signals

Six pins on the module output connector are allocated to power and operate the I^2C EEPROM and micro-controller. These are Serial Clock (SCL), Serial Data (SDA), A0 and A1 address lines, and +5VSB (to power the device). These signals are all referenced to output return.

The peak-to-peak noise on the clock (SCL), data (SDA), and address pins A0 and A1 of the I^2C bus at the module output connector shall be a maximum of 500 mV. The noise shall be measured over a 20 Hz to 25 MHz frequency band at maximum or worst case load condition. The measurement shall take place at the pins on the mated side (system board side) of the output connector pair. The measurement is to be referenced to the power supply module output return. The measurement is to be made on the SCL, SDA, and the three address lines of the I^2C bus with 3.3K pull-up resistors to micro-controller Vcc and a 20 pF ceramic capacitor to the ground.

4.5.1.6 Programming Connector

The monitor circuit shall include an eight-pin programming header. This is not accessible to the customer. The connector pin-out is as follows:

TABLE 13
PROGRAMMING CONNECTOR PIN-OUT

PIN NO.	NAME	FUNCTION
1	VPP	Input VPP
2	P2.0	Input/output port 2.0
3	P2.1	Input/output port 2.1
4	P2.2	Input/output port 2.2
5	VDD	Input VDD
6	VSS	Ground VSS
7	P0.3	Input/output port 0.3
8	RESET	Reset input

The connector to be used is can be a CAROL P/N CL2002WRO-8P, a JOWLE P/N A2002WR2-8P, a JST S8B-PH-K, or the equivalent. The orientation of this connector should be such that pin 1 will be closest to the key of the connector.

4.5.2 Monitor Circuit Data Reporting

Power supply status information is stored in the Control Status Register inside the micro-controller. Digitized analog values (i.e. output current) are stored in the micro-controller output buffer (RAM). The EEPROM contains FRU (Field Replaceable Unit) data and two identical copies of the calibration table. A number of commands are available to read and write data from these devices (see Section 4.5.3).

4.5.2.1 Power Supply Control Status Register

The host system can read the data from the micro-controller Control Status Register using the RCSR command (see Section 4.5.3.2). All power supply status monitoring is done via this register. A detailed explanation of the monitoring functions is given below:

TABLE 14
POWER SUPPLY CONTROL STATUS REGISTER DESCRIPTION

Control Status Register							
BIT 7	*BIT 6*	*BIT 5*	*BIT 4*	*BIT 3*	*BIT 2*	*BIT 1*	*BIT 0*
ENA_STAT	BAD_CAL	PROG TEMP	OV_TRIP	Reserved	OC_TRIP	FAULT	OT_TRIP
R	R	R	R	R	R	R	R

- ENA_STAT: This bit shall be set to high when one of the two module ENABLE signals are asserted low.
- BAD_CAL: This bit will be set high if the check sum test of both calibration table(s) fail.
- PROG TEMP: This bit will be set high when the inlet temperature reading rises above the programmed Temperature Warning Level and the power supply outputs are not disabled.
- OV_TRIP: This bit will be set high whenever the module latches off due to over-voltage.
- RESERVED: This bit is reserved.
- OC_TRIP: Over current trip status. This bit is set high when the power supply output has latched off due to an over-current event.
- FAULT: This bit will be set high when the power supply outputs have been disabled due to a fault condition.

OT_TRIP: Over temperature trip status. This bit will be set high when the power supply outputs have been disabled due to a hardware over temperature trip.

4.5.2.1.1 Enable – Bit 7

In the Control Status Register, bit seven (ENA_STAT) shall be set high when the module ENABLE signal is asserted high (see Table 14). The host should never write to this bit.

4.5.2.1.2 Bad calibration – Bit 6

The EEPROM shall contain two copies of the calibration table. The calibration table consists of calibration data loaded into the EEPROM during the manufacturing process (see Appendix A and Appendix B). In the micro-controller Control Status Register, bit six is the bad calibration bit (see Table 14). Under normal operating conditions, this bit in the Control Status Register shall be low. This bit shall be set high if the checksum test of both calibration tables stored in EEPROM fails. The host should never write to this bit. In the event that both calibration tables are bad, the module is considered to be bad and the amber LED should be turned on. When this bit is set, the analog sensor data returned in response to RASD command (see Section 4.5.3.3) should all be zeros.

4.5.2.1.3 Over-Temperature operating condition – Bit 5

Bit five in the Control Status Register is the programmed temperature bit. Under normal operating conditions, this bit in the status register shall be low. This bit shall be set high if the module inlet air temperature rises above the programmed Temperature Warning Level, and none of the module output voltages are disabled.

The micro-controller shall set this bit back to low when the inlet air temperature falls below the programmed Temperature Warning Level by the number of ºC specified by the programmed Temperature Hysterisis. The Temperature Warning Level and the Temperature Hysterisis are programmable. The default values hard coded in the firmware are 50º C and 5º C respectively.

4.5.2.1.4 Over-Voltage – Bit 4

Bit four in the Control Status Register is the over-voltage bit. Under normal operating conditions, this bit in the status register shall be low. This bit shall be set high if the module latches off due to an over-voltage condition.

When an over-voltage fault latches the module off, the power supply Control Status Register will hold the failure status information until the module enable signal is re-enabled after having been disabled for at least 100mS.

4.5.2.1.5 Reserved – Bit 3

Bit 3 is reserved.

4.5.2.1.6 Over-Current – Bit 2

Bit two in the Control Status Register is the over-current bit. Under normal operating conditions, this bit in the status register shall be low. This bit shall be set high if the module latches off due to an over-current condition.

When an over-current fault latches the module off, the power supply status register will hold the failure status information until the module enable signal is re-enabled after having been disabled for at least 100mS.

4.5.2.1.7 Fault – Bit 1

Bit one in the Control Status Register is the Fault bit. Under normal operating conditions, this bit in the status register shall be low. This bit shall be set high if any of the power supply outputs are disabled for any reason. The host should never write to this bit. When this bit is set, the reported output current on all channels should be zero.

4.5.2.1.8 OTP shutdown – Bit 0

Bit zero in the Control Status Register is the temperature deadly bit. Under normal operating conditions, this bit in the status register shall be low. This bit shall be set high whenever the power supply outputs have been disabled due to a hardware over temperature trip (OTP).

When a temperature deadly fault latches the module off, the power supply status register will hold the failure status information until the module enable signal is re-enabled after having been disabled for at least 100mS.

4.5.2.2 FRU Table

The FRU (Field Replaceable Unit) data format shall be compliant with the Intel IPMI V1.0 specification. The EEPROM device to be used will be the 24C03 device or equivalent. Such device will have at least one hundred and twenty eight bytes of write- protected memory area. The write protected area of the EEPROM device will only be accessible for write operations when the module is placed in "test" mode via the STM command (see Section 4.5.3.4).

The FRU table is attached as an appendix at the end of this specification.

4.5.2.3 Analog Data Buffer

The analog data read back from the power supply analog data buffer is provided in the smallest unit of available resolution.

4.5.2.3.1 Power Supply Output Current

The module utilizes the micro-controller to report accurate output current values for all output channels to the host. The module output current signals shown in Figure 3,

Figure 4, and

Figure 5 are also input signals to the micro-controller. The output current is represented to the micro-controller as a DC level provided by the power supply interface. The micro-controller will convert the DC level to current readings in milliamps for each channel. This is done through the micro-controller's internal ADC converter and using the gain and offset calibration values written to the EEPROM during manufacture. Gain and offset values are written into the EEPROM calibration table as a three byte variable. As part of the power supply calibration, the minimum usable current reading is also measured and stored in the EEPROM as a three byte value. The minimum usable current is the value of the current at which the percentage of error of the measured output current exceeds 20% of the actual output current.

Output current shall be reported in milliamps as a three-byte value.

4.5.2.3.2 Power Supply Temperature

An analog signal (below 4.4V) proportional to the inlet air temperature shall be provided at the input port of the micro-controller (see Section 4.5.1.3.2). The power supply inlet air temperature measurement is provided as a linear DC level from the power supply interface. The micro-controller will convert the DC level to a temperature reading in degrees Celsius through its internal ADC converter and using the gain and offset calibration values written to the EEPROM during manufacture. Power supply inlet air temperature shall be reported in degrees Celsius.

4.5.3 Commands

Each power supply on the I^2C bus shall respond to its own address. There are 14 (fourteen) commands that the power supply will respond to. The first ten are as follows:

Command 01: SCR (Set_Control_Register)- 0x01
Command 02: RCSR (Read_Control_Status_Register)- 0x02
Command 03: RASD (Read_Analog_Sensor_Data)- 0x03
Command 04: STM (Set Test Mode)- 0x04
Command 05: FDC (Firmware Debug) - 0x05
Command 06: FRNC (Firmware Revision Number) –0x06
Command 07: SyTM (System Test Mode) –0x07
Command 08: STDF (System Test Data Format) –0x08
Command 13: STWL – Set Temperature Warning Level Command – 0x0D
Command 14: RTWL – Read Temperature Warning Level Command – 0x0E

Additionally, other commands needed for test and manufacturing purposes can be added. It is suggested that these commands be gated by a command that sets the module in a "test" mode.

Command 09: RFR (Read From RAM) - 0x09
Command 10: RSFR (Read SFR) - 0x0A
Command 11: WTR (Write To RAM) –0x0B
Command 12: WSFR (Write to SFR) – 0x0C

The interval between two consecutive I2C commands to the power supply shall be at least 50mS to insure proper monitoring functionality.

Commands and requests for data shall follow the formats described in the following sections:

4.5.3.1 SCR – Set Control Register Command

The module does not use the SCR command.

Power Supply Address
Set Control Register - Command (01)
Control Register Value
Control Register Value
LSByte of the sum of previous two bytes

4.5.3.2 RCSR – Read Control Status Register Command

Reading data from the power supply micro-controller is similar to reading from the EEPROM except that the read command takes the place of the EEPROM read offset value in the command transaction. The module shall execute the command through I^2C in the following sequence:

Power Supply Address
Read Control Status Register - Command(02)
Power Supply Address+1

Read First Byte (nack)

4.5.3.3 RASD – Read Analog Sensor Data Command

The host system can read the analog data from the micro-controller output buffer in the following two sequences:

4.5.3.3.1 Single Byte Read

Power Supply Address
Read Analog Sensor Data Command - Command (03)
Power Supply Address+1
Read First Byte (Nck)
Power Supply Address+1
Read Second Byte (Nck)
. . .
. . .
Read Byte N (Nck)
Power Supply Address+1
Read Last Byte (Nack)

4.5.3.3.2 Multi-byte Read Format

Power Supply Address
Read Analog Sensor Data Command - Command (03)
Power Supply Address+1
Read First Byte (ack)
Read Next Byte (ack)
Read Next Byte (ack)
……………..
Read Last Byte (nack)

4.5.3.3.3 Analog Buffer Data Format

In response to a RASD command, the analog data read from the power supply shall be in the format listed below:

3.3v Actual Output Current LSB (milliAmps)
3.3v Actual Output Current (milliAmps)
3.3v Actual Output Current MSB (milliAmps)
3.3v Maximum Output Current LSB (milliAmps)
3.3v Maximum Output Current (milliAmps)
3.3v Maximum Output Current MSB (milliAmps)
3.3v Minimum Usable Output Current LSB (milliAmps)
3.3v Minimum Usable Output Current (milliAmps)
3.3v Minimum Usable Output Current MSB (milliAmps)
5v Actual Output Current LSB (milliAmps)
5v Actual Output Current (milliAmps)
5v Actual Output Current MSB (milliAmps)
5v Maximum Output Current LSB (milliAmps)
5v Maximum Output Current (milliAmps)
5v Maximum Output Current MSB (milliAmps)
5v Minimum Usable Output Current LSB (milliAmps)
5v Minimum Usable Output Current (milliAmps)
5v Minimum Usable Output Current MSB(milliAmps)
12v Actual Output Current LSB (milliAmps)
12v Actual Output Current (milliAmps)
12v Actual Output Current MSB (milliAmps)
12v Maximum Output Current LSB (milliAmps)
12v Maximum Output Current (milliAmps)
12v Maximum Output Current MSB (milliAmps)
12v Minimum Usable Output Current LSB (milliAmps)
12v Minimum Usable Output Current (milliAmps)
12v Minimum Usable Output Current MSB (milliAmps)
Inlet air Temperature (Degrees Celsius)
Programmed Temperature Hysterisis (Degrees Celsius)
Programmed Temperature Warning Level (Degrees Celsius)
ADC Update Status (1 = Updated Data; 0 = Old Data)

4.5.3.4 STM – Set Test Mode Command

This command will set the module in test mode. In this mode of operation, the EEPROM write protection is disabled and the test commands (commands 9 through 12) are enabled. A 1(one) will enable the test mode; a 0(zero) will disable it. This command can only be executed when the power supply output enable signal is not asserted. The power supply will simply ignore this command if the output enable signal is asserted. The module shall execute the command through I2C in the following sequence:

Power Supply Address
Set Test Mode Command - Command (04)
Control Register Value (1) or (0)
Control Register Value (1) or (0)
LSByte of the sum of previous two bytes

4.5.3.5 FDC – Firmware Debug Command

The Firmware Debug Command returns the Status, Internal Flags and Port Pin Status of the micro-controller. This command will be used to debug the firmware only. The Firmware Debug Command will respond to the following two formats:

4.5.3.5.1 Single-byte Read Format

Power Supply Address
Firmware Debug Command - Command(05)
Power Supply Address+1
Read First Byte (Nck)
Power Supply Address+1
Read Second Byte (Nck)
. . .
. . .
Read Byte N (Nck)
Power Supply Address+1
Read Last Byte (Nack)

4.5.3.5.2 Multi-byte Read Format

Power Supply Address
Firmware Debug Command - Command(05)
Power Supply Address+1
Read First Byte (Ack)
Read Byte N (Ack)
Read Last Byte (Nack)

4.5.3.5.3 Firmware Debug Command Data Format

The data format of the Firmware Debug Command Read will be as follows:

Status Register
EEPROM Error Flag
ADC Flag
System Test Flag
Port 0
Port 1
Port 2
Port 5

4.5.3.6 FRNC - Firmware Revision Number Command

The firmware revision number will be hard coded into the firmware itself. This command will return the revision number of the firmware. The Firmware Revision Number Command will respond to the following two formats:

4.5.3.6.1 Single-byte Read Format

Power Supply Address
Firmware Revision Number Command - Command (06)
Power Supply Address+1
Read First Byte (Nck)
Power Supply Address+1
Read Second Byte (Nck)

4.5.3.6.2 Multi-byte Read Format

Power Supply Address
Firmware Revision Number Command - Command (06)
Power Supply Address+1
Read First Byte (Ack)
Read Last Byte (Nack)

4.5.3.6.3 Firmware Revision Number Data Format

The data format of the Firmware Revision Number Command Read shall be as follows:

Major Revision Number
Minor Revision Number

4.5.3.7 SyTM - System Test Mode Command

The System Test Mode Command will force the power supply to send data in a format specified by the System Test Data Format Command (command #8). This command will toggle the power supply in and out of System Test Mode. This command must be immediately followed by the System Test Data Format Command (command #8) in order for the power supply to get into the System Test Mode. The format of this command shall be as follows:

Power Supply Address
System Test Mode Command - Command (07)
System Test Mode Command - Command (07)
System Test Mode Command - Command (07)
LSB of the Sum of Previous two bytes

NOTE:

This command is repeated three (3) times to insure that entry into this mode is deliberate.

4.5.3.8 STDF - System Test Data Format Command

The System Test Data Format command will specify the format of the data that will be returned by the power supply in response to ADC data request (Command #3) if it is in System Test Mode. This command is invalid if the power supply is not in System Test Mode and will be ignored by the power supply. The format of this command shall be as follows:

Power Supply Address
System Test Data Format Command - Command (08)
System Test Data Format
System Test Data Format
LSB of the Sum of Previous two bytes

System Test Data Format: The data format of this command will be as follows:

System Test Data Format	Format of Data Returned in response to Command (03)
0	Default Format (Processed ADC data)
1	Raw ADC Reading
2	All Zero's
3	All One's
4	Alternate Zero's and One's
Remaining Values	Reserved

4.5.3.9 STWL – Set Temperature Warning Level Command

This command overwrites the default values of the temperature warning level and the temperature hysterisis that are loaded at power up. The micro-controller shall set the over temperature bit and pull the temperature warning signal to low (GND potential) when the inlet air temperature exceeds the Programmed Temperature Warning Level set by this command. It will clear the over temperature bit and release the temperature warning signal when the inlet air temperature falls below the programmed Temperature Warning Level by the number of ºC specified by the programmed Temperature Hysterisis. The default values of the Temperature Warning Level and the Temperature Hysterisis hard coded in the firmware are 50º C and 5º C respectively.

The format of this command shall be as follows:

Power Supply Address
Power Supply Set Temp - Command (13)
Prog. Temp Limit
Temp Limit Hysterisis
LSByte of the SUM of the prev. three bytes

To verify the data integrity, the micro-controller shall calculate the sum of the second, third and fourth bytes received from the host, and then compare the result to the checksum sent by the host.

4.5.3.10 RTWL – Read Temperature Warning Level Command

The RTWL command allows the host to read the over-temperature warning threshold value. The command sequence is shown below:

Power Supply Address
Power Supply Read Temp. - Command (14)
Power Supply Address+1
Read Prog_temp_level (ack)
Read Prog_temp_hys (nack)

4.5.3.11 RFR – Read From RAM Command

The RFR command is used for test and development purposes. This command will allow the contents of any RAM location to be examined. The format of this command shall be as follows:

Power Supply Address
Read From RAM Command – Command (9)
Ram Offset
Power Supply Address+1
Read RAM contents (nack)

4.5.3.12 RSFR – Read From Special Function Register Command

The RSFR command is used for test and development purposes. This command will allow the contents of any SFR to be examined. The format of this command shall be as follows:

Power Supply Address
Read SFR Command - Command (10)
SFR (Lsbyte)
SFR (Msbyte)
Power Supply Address+1
Read SFR contents (nack)

4.5.3.13 WTR – Write To RAM Command

The RFR command is used for test and development purposes. This command will allow the contents of any RAM location to be modified. The format of this command shall be as follows:

Power Supply Address
Write To RAM Command - Command (11)
Ram Offset
RAM contents (nack)
RAM contents (nack)
Chksum of prev three bytes

4.5.3.14 WSFR – Write To Special Function Register Command

The RSFR command is used for test and development purposes. This command will allow the contents of any SFR to be modified. The format of this command shall be as follows:

Power Supply Address
Write To SFR Command - Command (12)
SFR (Lsbyte)
SFR (Msbyte)
SFR DATA
Chksum of prev. three bytes

4.5.4 Power Supply Calibration

Calibration of the power supply analog measurements will be made during manufacturing final test. For each analog input channel there will be A0 and A1 terms that will be used as coefficients in a first order linear equation, along with the raw A/D reading, to calculate the normalized data reported when the supply is queried.

4.5.4.1 Output Current Calibration

THE OUTPUT CURRENT SIGNALS SHOWN IN FIGURE 3,

FIGURE 4, AND

Figure 5 are also the input signals to the micro-controller. For output current calibration, the test system shall record the A/D readings at 50% and 100% of the converter full-scale output current rating. This is repeated for each converter output. Using these two readings the test system will calculate the "GAIN" (A1 coefficient in milliamps/bit) and the "OFFSET" (A0 coefficient in milliamps). The A0 and A1 coefficients will be stored in the power supply calibration table in the EEPROM. These two values will be used in the equation: Current = A1* A/D rdg. + A0 to convert the A/D readings into milliamps to be stored in the micro-controller output buffer.

4.5.4.2 Temperature Calibration

An analog signal (below 4.4V) proportional to the inlet air temperature shall be provided at the input port of the micro-controller. Temperature calibration coefficients will be derived from component specifications and circuit design parameters. It is assumed that the temperature sensors to be used are standard 10K NTC thermistors. Linearization of the temperature transfer function over the normal operating range is desirable.

4.5.4.3 Calibration Table Corruption

In the event that the calibration table stored in EEPROM is corrupted, the interpretation of the A/D data representing output current, input line voltage, and temperature is no longer possible. Power supply and operating status information is still available. Two separate copies of the calibration table shall be placed in the EEPROM, each with it's own check sum.

4.5.5 <u>Self Test</u>

Part of the initialization procedure for the micro-controller should include a test of the RAM, and if possible, the A/D converter.

5. ENVIRONMENTAL REQUIREMENTS

5.1 TEMPERATURE

5.1.1 Operating

0°C to 50°C at full load at 100 LFM. Temperature to be derated 1°C for every 1000 feet above sea level.

5.1.2 Non-Operating

-40°C to 70°C with a maximum rate of change of 20°C/hour.

5.2 HUMIDITY

The unit shall be able to withstand 5 to 95% relative humidity, 38.7°C maximum wet bulb temperature, non-condensing.

5.3 ALTITUDE

5.3.1 Operating

10,000 feet above sea level. Temperature to be derated 1°C for every 1000 feet above sea level.

5.3.2 Non-Operating

30,000 feet above sea level.

5.4 MECHANICAL SHOCK

5.4.1 Fixturing

For the shock testing of powers supplies that do not have their own subassembly enclosure the power supply board shall be attached by its normal mounting means to a rigid fixture capable of transmitting the shock conditions specified below. The fixture shall not inhibit any elastic or permanent deformation of the board that may occur during the shock tests. For power supplies contained in their own subassembly enclosure the power supply subassembly may be rigidly clamped directly to the shock machine working surface; however, if the integrity of the power supply enclosure is to be part of the evaluation the power supply subassembly shall be attached by its normal mounting means to a rigid fixture capable of transmitting the shock conditions specified below.

5.4.2 Operating

Half sine wave shock - 40 G, 2 ms duration, half sine wave shock in each direction of three mutually perpendicular axes. There shall be one shock input in each direction of three mutually perpendicular axes for a total of six shock inputs.

5.4.3 Non-Operating

Half sine wave shock - 140 G, 2 ms duration, half sine wave shock in each direction of three mutually perpendicular axes. There shall be one shock input in each direction of three mutually perpendicular axes for a total of six shock inputs.

Square wave shock - 80 G, 180 in/sec velocity change, square wave shock in each direction of three mutually perpendicular axes. There shall be one shock input in each direction of three mutually perpendicular axes for a total of six shock inputs.

5.5 VIBRATION

5.5.1 Fixturing

For the vibration testing of power supplies that do not have their own subassembly enclosure the power supply board shall be attached by its normal mounting means to a rigid fixture capable of transmitting the vibration conditions specified below. The fixture shall not inhibit any elastic or permanent deformation of the board that may occur during the vibration tests. For the power supplies contained in their own subassembly enclosure, the power supply subassembly may be rigidly clamped directly to the vibration shaker; however, if the integrity of the power supply enclosure is to be part of the evaluation the power supply subassembly shall be attached by its normal mounting means to a rigid fixture capable of transmitting the vibration conditions specified below.

5.5.2 Operating

Random Vibration - 0.002 G^2/Hz, 10 to 500 Hz, nominal 1.0 Grms in each of three mutually perpendicular axes. The test duration shall be one hour/axis for a total test duration of three hours.

5.5.3 Non-Operating

Random Vibration - 0.008 G^2/Hz, 10 to 500 Hz, nominal 2.0 Grms in each of three mutually perpendicular axes. The test duration shall be one hour/axis for a total test duration of three hours.

5.6 PACKAGED VIBRATION AND SHOCK

5.6.1 Unitized Load (Bulk) Shipping Container

The bulk shipping container must meet the requirements defined in Compaq Document 137114.

5.6.2 Individual Finished Product Shipping Container

The individual finished product shipping container must meet the requirements defined in Compaq Document 109291.

5.7 ELECTROSTATIC DISCHARGE (ESD)

The power supply shall withstand the following ESD conditions at any point on the power supply enclosure when tested per Compaq P/N 106244-001, "Procedure, Test Electrostatic Discharge":

A) 15 kV with no abnormal operation
B) 25 kV with no damage to power supply
C) Transients as defined in IEC 801-2, Level 4

The storage capacitance shall be 150pF and the discharge resistance shall be 330 ohms. The power supply shall meet all discharge requirements for the CE Mark designation.

6. AGENCY APPPROVALS

6.1 REGULATOR PRODUCT IDENTIFICATION: SERIES TBD

The power supply module shall be certified under the Compaq Brand using product identifier TBD. This number shall be used on all certification documents as the “Model” or “Type”. The Series number should appear on the Regulatory Nameplate Label. All direct references to the manufacturer’s name shall be removed from the product and labels. Identification of the manufacturer shall be accomplished by use of appropriate File and License numbers. The process of Co-Licensing shall not be used to accomplish this effort.

6.2 PRODUCT SAFETY REQUIREMENTS AND APPROVALS

The power supply module shall be approved/licensed/certified as specified below. Copies of ALL approval licenses for the power supply module shall be provided to the Product Safety Group as part of the final COMPAQ power supply module qualification. The installed power supply module shall pass all applicable safety tests at these ratings. Besides the required outside Regulatory qualification for the Compaq end product with the power supply module, the Compaq Product Safety Group reserves the right to conduct all applicable component level Safety tests and evaluations on the power supply module. Samples and information from the OEM Supplier will be requested in order to support this evaluation.

EN60 950 (IEC 950): The OEM DC-DC Converter Assembly shall comply with all applicable requirements of EN 60 950, and IEC 950 2nd Edition (1991) including Amendment 1, 2, 3, and 4. The power supply module shall also comply with the applicable requirements of each of the IEC based 950 based national or regional standards identified below.

ACCESSIBLE VOLTAGE LEVELS: The output voltage of the power supply module shall be within the limits for Safety Extra Low Voltage (SELV) circuits as described in Clause 2.3 of EN60 950, Second Edition. If Non-SELV voltages are present in the circuitry, these points shall be insulated and/or separated from other circuits and user/service person contact in accordance with all applicable requirements in EN60 950, Second Edition.

CB SCHEME CERTIFICATION: The manufacturer of the power supply module shall obtain a CB Test Certificate and CB Test Report from a National Certification Body. The Certificate and Report shall be valid for and state conformity with EN 60950 and IEC 950 2nd Edition (1991) including Amendment 1, 2, 3, and 4. The report should also include an evaluation of all the country specific deviations (not just the Group deviations). The CB Test Certificate shall contain Compaq's trademark/name Compaq authorized Series number.

UL APPROVAL: The power supply module shall be a Recognized Component by Underwriters Laboratories Inc. in accordance with UL 1950, 3rd Edition. The nameplate shall include the Supplier's UL Recognition mark, the Supplier's UL file number (EXXXXXX) and any other required factory identification. All output channels shall be SELV for external interconnection and operator accessibility.

6.3 EMC REQUIREMENTS AND APPROVALS

The information contained in this section was the criteria and approvals anticipated at the time of release of this document. This information may not be current. It is recommended that for current information, the Compaq EMC Services group be contacted.

Based upon the intended marketing and use of the product, the product shall comply with:

C.I.S.P.R. REQUIREMENTS: All administrative and performance requirements for C.I.S.P.R. Publication 22 Class B. Radiated emission testing shall be performed at 10 meters. Conducted emission testing shall be performed at a line voltage of 110 and 230 volts. This device, when tested as part of a system defined by Compaq Computer Corporation, shall not increase the emissive level of that system to a level greater than 3 dB below the class B limits. Testing shall be performed using Compaq Computer Corporation labeled/manufactured peripherals**.**

AUSTRALIAN ACA APPROVAL: All administrative and performance requirements for ACA AS/NZS 3548, class B in accordance with the Electromagnetic Compatibility Framework Information for Suppliers document, July 1995 and URL: http://www.aca.gov.au/standards/emc/emc.htm . The product label shall contain the C-Tick logo and the manufacturer’s Supplier Code.

TAIWAN BSMI APPROVAL: All administrative and performance requirements for the BSMI Taiwan "Commodity EMC Regulation" in accordance with Chinese National Standard (CNS) 13438 (CISPR 22), class A and URL: http://www.bsmi.gov.tw/english/emc/e_emc_hp.htm . The product label shall contain the BSMI ID number and warning statement.

All EMC testing/submissions shall be performed using the most recent operating systems software appropriate for the product (e.g., Windows 2000), COMPAQ COMPUTER CORPORATION labeled/manufactured peripherals, the defined test systems (contact EMC Services), and a continuous scrolling 'H' pattern.

6.4 CE MARK REQUIREMENTS

The power supply module shall comply with all of the performance requirements for placing the CE Marking on the product in accordance with the CE Marking Directive (93/68/EEC), the EMC Directive [89/336/EEC] with its amendments, and the Low Voltage Directive [73/23/EEC] with its amendments. Specifically, the product shall comply with the following requirements and associated test parameters when tested as part of a system defined by COMPAQ COMPUTER CORPORATION:

•	**<u>Electrical Product Safety requirements</u>**	**EN 60950**
•	**<u>EMC emissions compliance requirements</u>**	**EN 55022:1998 (CISPR 22 -Class B at 10 meters)**
•	**<u>Harmonic distortion compliance requirements</u>**	**EN 61000-3-2**
•	**<u>Immunity compliance requirements</u>**	**EN 55024 consisting of:**
⇒	**IEC 61000-4-2: 1995 Electrostatic Discharge**	**[4kV contact, 8kV air discharge]**
⇒	**IEC 61000-4-3: 1995 RF Fields**	**[3V/m; 80 - 1000 MHz; 80% modulated at distance of 3 meters]**
⇒	**IEC 61000-4-4: 1995 Elec. Fast Transients**	**[± 1kV on AC power port for 1 minute;±0.5kV on signal/control lines]**
⇒	**IEC 61000-4-5: 1995 Surge**	**[± 1kV line to line/±2kV line to earth on AC power port; ±0.5kV for outdoor cables]**
⇒	**IEC 61000-4-6:1996 Conducted RF**	**[3V; 0.15-80MHz; 80% modulated]**
⇒	**IEC 61000-4-8; 1993 Magnetic field**	**[50Hz; 1A/m]**
⇒	**IEC 61000-4-11:1994 Voltage variations**	**[>95% dip, 0.5 period; 30% dip, 25 periods;>95% reduction, 250 periods]**

For the purposes of compliance with EN 55024, the product when tested with the intended COMPAQ system, shall not cause a halt of the operation of software applications operating on the COMPAQ. Voltages and currents shall remain within the specified parameters contained elsewhere in this document. Test setups shall be in accordance with EN 55022, namely complete systems with all ports appropriately terminated into a peripheral.

- **The manufacturer shall place the “CE" marking on the product.**
- **<u>Manufacturer’s Declaration of Conformity</u> - A DofC accompanied by a complete Technical Data file containing all associated Test Reports shall be provided to the Compaq EMC Services and Product Safety groups prior to first revenueable product shipment.**

6.5 AGENCY ACCEPTANCE TESTING

Acceptance testing will be performed by COMPAQ COMPUTER CORPORATION. Test samples for acceptance testing will be retained by COMPAQ COMPUTER CORPORATION.

Copies of all submissions documents and resulting approvals will be supplied to COMPAQ COMPUTER CORPORATION' Product Safety and EMC Services representatives prior to first revenueable product shipment.

6.6 AGENCY COMPONENT REQUIREMENTS

6.6.1 PRINTED WIRING BOARDS

All printed wiring boards shall be Underwriter Laboratories Inc. Recognized Component rated 94V-1 or less flammable and shall be so marked. The maximum board surface temperature shall not exceed its UL temperature rating under any normal operating condition (130°C). Use of solder build-up on traces as a method of increasing current/energy capacity shall be approved by each of the Agencies identified in Section 6.

6.6.2 WIRING

All internal and external wiring shall be UL Recognized Component Appliance Wiring Material (AVLV2), and CSA Certified "Appliance Wiring Material" (AWM). Primary circuit wire shall be minimum rated 300V, 105°C, while the secondary SELV shall be rated at min. 30V, 80°C.

6.6.3 HOT PLUG CONNECTORS

Because the power supply module is intended for hot plugging (disconnecting under load), the connector must be approved/tested for this at the max. rated load of the supply. This fact must be noted in the agency test report (e.g. conditions of acceptability).

6.6.4 APPROVED VENDOR LIST

The OEM's Approved Vendor List (AVL) of Critical Components shall be sent to COMPAQ Computer Safety Group prior to approval.

6.6.5 DC LINE FUSE

The incoming -48 V dc line shall be fused with appropriate safety fuse.

6.7 MARKINGS

The OEM power supply module nameplate label (s) shall have the following markings:

A) Compaq Computer Corporation
B) Series #ESP106 (see Section 6.1)
C) Compaq's Part Number/ Spares Part Number
D) Date Code
E) All Required AGENCY MARKINGS (See Sections 6.2–6.4)
F) Country of Manufacture
G) Electrical Rating: Output rating, Input rating in Volts and Amps

NOTE:

The OEM's logo/marking shall not appear on the power supply module.

7. RELIABILITY

7.1 DEMONSTRATED MEAN TIME BETWEEN FAILURES

The power supply shall have a demonstrated MTBF of greater than one (1) million hours of continuous operation at 50°C air at a velocity of 100 LFM directed along the connector axis. The module is expected to be in operation continuously for 62000 hours.

"Given a one million hour MTBF, no more than 0.2% of the modules will be allowed to fail for every 2000 hour increment within the first 62000 hours of operation".

7.1.1 Input Voltage

-48V DC

7.1.2 Output Load

Rated full load.

7.1.3 Ambient Temperature

50°C inlet air.

7.2 LIFE EXPECTANCY

The power supply shall have a field failure rate of less than 1% per 10,000 hrs within the first 40,000 hours of operation. The calculation shall be made in accordance with Military Specification MIL-217E.

7.3 SEMICONDUCTOR TEMPERATURE

Maximum semiconductor junction temperature shall not exceed 125°C or vendor's maximum rating, whichever is less, under any specified operating condition.

8. COMPONENT REQUIREMENTS

8.1 PRINTED WIRING BOARDS

8.1.1 Design and Fabrication of PCBs

The power supply printed circuit board shall meet Compaq Document 101045-001.

The PCB layout and design shall meet Compaq Document 106663-001 and if applicable Compaq Document 106217-001.

8.1.2 Solder Mask

Solder mask shall be provided on all primary and secondary traces with spacing less than 2 mm.

8.2 WIRING

All internal and external wiring shall be rated minimum 105 degrees C and U.L. Recognized Component Appliance Wiring Material (AVLV2), and CSA certified "Appliance Wiring Material" (AWM). Wire shall be rated minimum 300V.

8.3 COMPONENT QUALIFICATION

All components shall be qualified to mutually agreed upon specifications as to their acceptability.

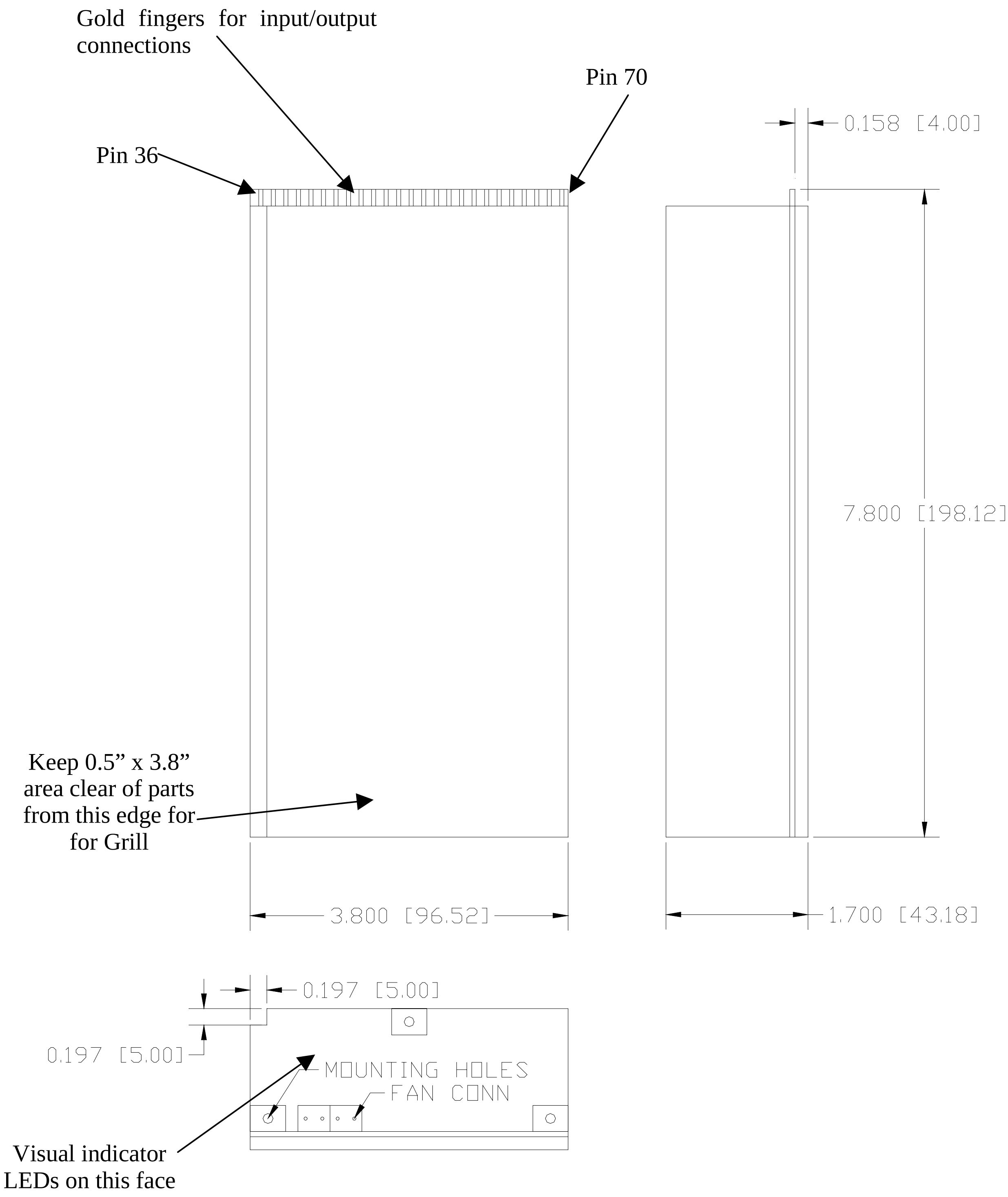
9. MECHANICAL

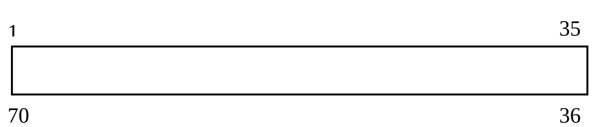
The mechanical design of the power supply module shall meet the requirements as defined in the following paragraphs.

9.1 MECHANICAL CONFIGURATION

The physical dimensions of the power supply module are shown in Figure 9 below:

FIGURE 9
GENERAL VIEW OF THE POWER SUPPLY MODULE





Mating Connector Top View

COMPAQ	SIZE A	DRAWING NO. XXXXXX		REV X0.1
	DRAWN	SCALE 1/1	SHEET 57 OF 77	

9.2 MATERIALS

All polymeric parts within the enclosure shall be molded from Underwriters Laboratories, Inc. "Recognized" QMFZ2 polymeric material minimally rated 94V-2.

9.3 WEIGHT

The weight of the power supply module shall be less than less than or equal to 2.0 pounds (approx).

9.4 SIZE

Approx. 7.8(L) x 3.8(W) x 1.7(H) inches, including an input and output connector pins.

10. CONNECTORS

10.1 INPUT AND OUTPUT POWER CONNECTOR

The power supply module input/output connector shall be 70 pins (35 rows on each side) gold plated fingers to mate with AMP p/n – 1489782-X.

10.2 MODULE CONNECTOR ASSIGNMENT AND FUNCTION

The power supply mating connector has 70 pins in 2 rows of 35 pins each. Pin assignments are defined in Table 15.

Table15 – MATING CONNECOTR PIN ASSIGNMENT

PIN #	Connection	PIN #	Connection
1	0V Input	70	-48V Input
2	0V Input	69	-48V Input
3	0V Input	68	-48V Input
4	BLANK(No pin)	67	BLANK(No pin)
5	3.3V(Aux.)	66	-12V
6	3.3V(Aux.)	65	A1(address bit)
7	A0 (address bit)	64	3.3V I-share
8	I^2C data	63	5.1V I-share
9	I^2C Clock	62	12.25V I-share
10	5V/12V Enable_	61	5V/12V Power Good
11	3.3V Enable_	60	3.3V Power Good
12	12V	59	12V RS+
13	12V	58	12V
14	5.1V RS+	57	5.1V
15	5.1V	56	5.1V
16	5.1V	55	5.1V
17	5.1V	54	5.1V
18	3.3V RS+	53	5VSB(external supply)
19	Output RTN	52	Module Present_
20	Output RTN	51	Output RTN
21	Output RTN	50	Output RTN
22	Output RTN	49	Output RTN
23	Output RTN	48	Output RTN
24	Output RTN	47	Output RTN
25	Output RTN	46	Output RTN
26	Output RTN	45	Output RTN
27	Output RTN	44	Output RTN
28	Output RTN	43	Output RTN
29	3.3V	42	3.3V
30	3.3V	41	3.3V
31	3.3V	40	3.3V
32	3.3V	39	3.3V
33	3.3V	38	3.3V
34	3.3V	37	3.3V
35	3.3V	36	3.3V

10.3 PRODUCT SAFETY LABEL

The product safety label must contain all the information listed in Section 7.7. The label shall be placed on the base side of the power supply sheet metal. The label can be the same as the insulator/label previously described, or it can be a separate label that is applied on top of the label/insulator. If a separate safety label is applied on top of the insulator/label, the total thickness of the two labels cannot exceed 0.015 inches. The label material and construction shall be a recognized component in the Underwriters Laboratories marking and labeling system, and in accordance with Underwriters Laboratories standard for safety, “marking and labeling systems,” suitable for the maximum power supply module case temperature and the surface material.

10.4 COMMODITY TRACKING LABEL

Compaq requires that a commodity-tracking label be applied to the power supply. The requirements for this label are described in Compaq specification 185411. The label shall include a unique sequence identifier (serial number). The label dimensions shall be 2.5 inches long by 1.75 inches tall. The label shall be applied on top of the label/insulator. When applied on top of the insulator/label, the total thickness of the two labels cannot exceed 0.015 inches.

10.5 CODE REVISION LABEL

Compaq requires that a code revision label be applied to the power supply. This information can be printed on the commodity-tracking label if desired, or it can be a separate label. If it is a separate label, it should be placed near the commodity-tracking label. The code revision label shall indicate the revision number of the firmware that is programmed into the micro-controller. When applied on top of the insulator/label, the total thickness of the two labels cannot exceed 0.015 inches.

10.6 HOT SURFACE WARNING LABEL

Compaq requires that a hot surface warning label be applied to the power supply module. This is to warn the customer and service personnel that the power supply surface may be hot and to use caution during hot plug or service events.

The label dimensions shall be 2.0 inches long by 1.0 inches wide. The label shall be placed in the center of the sheet metal on the top of the power supply. The label material and construction shall be a recognized component in the Underwriters Laboratories marking and labeling system, and in accordance with Underwriters Laboratories standard for safety, “marking and labeling systems,” suitable for the maximum power supply module case temperature and the surface material.

The label shall have a yellow background with black letters/symbols on it.

11. QUALITY ASSURANCE AND RELIABILITY PROVISIONS

11.1 RESPONSIBILITY FOR QUALITY

Unless otherwise specified in the contract or purchase order, the supplier shall be responsible for the quality of the part as it is delivered to Compaq. The supplier shall be responsible for having controlled processes to ensure product is in total compliance with this specification.

11.2 SUPPLIER PROCESS CHANGE NOTICE

Compaq shall be notified of all process changes as specified within Compaq Document 114971.

11.3 SDP HANDBOOK

Compaq utilizes the Supplier Development Process Handbook (SDP) as a tool for continuous material improvements and supplier development. As needed, supplier agrees to support improvement tools such as surveys, gauge capability studies, and correlation as described in the SDP handbook (handbook copies may be obtained from Compaq Supplier Quality Engineering).

11.4 PACKAGING AND LABELING

Packing shall be sufficient to protect the product against loss or damage during shipment from the manufacturer to the destination. The shipping, packaging, and labeling shall meet the requirements of Compaq Document 109893. Compaq Document 137063 defines the preferred shipping label requirements.

The method of shipment shall be agreed upon between sender and recipient. The product shall be clearly identified and packed according to prevailing regulations. It is the responsibility of the shipper to take all reasonable precautions to ensure the product arrives undamaged and on time.

11.5 PALLETIZATION AND SHIPPING

A 42” x 48” pallet will be used. A 40” x 48” pallet will be used for Europe. Palletization, labeling and shipping requirements shall be in accordance with Compaq Documents 106128, 109893, and 137063.

12. **APPENDIX A – NVRAM SPECIFICATION (FOR REFERENCE, SOME LOCATION VALUES MAY CHANGE PER NEW REQUIREMENTS)**

NVRAM PAGE 2 CONTENTS

OFFSET (BYTES)	VALUE (DECIMAL)	DEFINITION (REMARKS)
0 to 7		**Common Header, 8 bytes**
0 to 7	001	Format Version Number
	023	Internal Use Area Offset
	001	Chassis Info Area Offset
	000	Board Info Area Offset
	005	Product Info Area Offset
	012	Multi Record Area Offset
	000	PAD (reserved) Default value is 0.
	214	Zero Check Sum (256 – (Sum of bytes 0 to 6))
8 to 39		**Computer/Chassis Info Area, 32 Bytes** This area will be filled by the Mfg. Diag. or by the OS if used
8	001	**Format Version Number**
9	004	**Chassis Info Area Length**
10	000	**Chassis Type** Default value is 0.
11	202	**Chassis Part Number** Type/Length 0CAH (if used) = Type "ASCII+LATIN1" 10 Bytes.
12 to 21	000	**Chassis Part Number** Default value is 0.
	000	
	000	
	000	
	000	
	000	
	000	
	000	
	000	
	000	
22	207	**Chassis Serial Number** Type/Length 0CFH (if used) = Type "ASCII+LATIN1" 15 Bytes.
23 to 37	000	**Chassis Serial Number** Default value is 0.
	000	
	000	
	000	
	000	
	000	
	000	
	000	
	000	
	000	
	000	
	000	
	000	
	000	
	000	
38	193	**End Tag** (0C1H if used)
39	XXX	**CHKSUM** (Zero CHKSUM if used)

NVRAM PAGE 2 CONTENTS

OFFSET (BYTES)	**VALUE** (DECIMAL)	**DEFINITION** (REMARKS)
40 to 95		**Product Information Area, 56 bytes**
40	001	**Format Version Number**
41	007	**Product Info Area Length** in multiples of 8 Bytes
42	025	**Language** (English)
43	197	**Manufacturer Name** Type/Length (0C5H) = Type “ASCII+LATIN1” 5 Bytes.
44 to 48	065	Manufacturer Name 5 byte sequence “ASTEC” In Decimal = 065, 083, 084, 069, 067 In Hex = 41H, 53H, 54H, 45H, 43H
	083	
	084	
	069	
	067	
49	203	**Product Name** Type/Length (0CBH) = Type “ASCII+LATIN1” 11 Bytes.
50 to 60	065	11 Byte sequence Product Name “AA21090 ” In Decimal = 056, 065, 050, 049, 048, 057, 048, 032, 032, 032, 032 In Hex = 41H, 41H, 32H, 31H, 30H, 39H, 30H, 20H, 20H, 20H, 20H
	065	
	050	
	049	
	048	
	057	
	048	
	032	
	032	
	032	
	032	
61	202	**Part/Model Number** Type/Length (0CAH) = Type “ASCII+LATIN1” 10 Bytes.
62 to 71	049	Specified 10-Byte Sequence “158677-001” In Decimal = 049, 053, 056, 054, 055, 055, 045, 048, 048, 049 In Hex = 31H, 35H, 38H, 36H, 37H, 37H, 2DH, 30H, 30H, 31H
	053	
	056	
	054	
	055	
	055	
	045	
	048	
	048	
	049	
72	194	**Product Version Number** (Compaq Auto Rev. Number) Type/Length (0C2H) = Type “ASCII+LATIN1” 2 Bytes.
73 to 74	048	Specified 2-Byte Sequence Production level start at “01” In Decimal = 048, 049 In Hex = 30H, 31H
	049	
75	206	**Product Serial Number** Type/Length (0CEH) = Type “ASCII+LATIN1” 14 Bytes.
76	053	**Commodity Code,** “5” for Power Supply In Decimal = 053 In Hex = 35H
77 to 80	051	**AAAA: Assembly Code,** “3497” In Decimal = 051, 052, 057, 055 In Hex = 33H, 34H, 39H, 37H
	052	
	057	
	055	

NVRAM PAGE 2 CONTENTS

OFFSET (BYTES)	VALUE (DECIMAL)	DEFINITION (REMARKS)
81 to 82	048	**RR: Revision Level,** Specified 2-Byte Sequence Production level start at "0A" In Decimal = 048, 065 In Hex = 30H, 41H
	065	
83 to 84	057	**SS: Supplier Site of Mfg.,** "95" In Decimal = 057, 053 In Hex = 39H, 35H
	053	
85 to 86	XXX	**WW: Week/Year of Mfg.** 2 Byte Sequence for week Code
	XXX	
87 to 89	XXX	**Unique Sequence Identifier** Specified 3 Bytes Sequence for Serial Number
	XXX	
	XXX	
90	000	**Asset Tag** Default Value is 0
91	193	**End Tag** In Decimal: 193 In Hex: 0C1H
92 to 94	000	**Reserved** Default Value is 0
	000	
	000	
95	XXX	**Zero Check Sum** (256 – (Sum of bytes 80 to 134))
96 to 214		**Multi Record Area, 119 Bytes**
96 to 100		**Power Supply Record Header**
96 to 100	000	Record type = 00 for Power supply
	002	End of List /Record Format Version Number
	024	Record Length of Power Supply Record
	154	Record CHECKSUM of Power Supply Record (Zero CHECKSUM)
	076	Header CHECKSUM of Power Supply Record Header (Zero CHECKSUM)
101 to 124		**Power Supply Record**
101 to 102	139	**Overall Capacity of the Power Supply**, 395W = 018BH 2 Bytes Sequence In Decimal = 139, 001 In Hex = 8BH, 01H
	001	
103 to 104	038	**Peak VA,** 500W = 0226H 2 Bytes Sequence In Decimal = 038, 002 In Hex = 26H, 02H
	002	
105	028	**Inrush Current**, 028A In Decimal = 028 In Hex = 1CH
106	001	**Inrush Interval**, 001ms In Decimal = 001 In Hex = 01H
107 to 108	224	**Low End Input Voltage Range 1(10mV),** 43.2V= 10E0H 2 Bytes Sequence In Decimal = 224, 016 In Hex = E0H, 10H
	016	

NVRAM PAGE 2 CONTENTS

OFFSET (BYTES)	VALUE (DECIMAL)	DEFINITION (REMARKS)
109 to 110	160 020	**High End Input Voltage Range 1(10mV),** 52.8V= 14A0H 2 Bytes Sequence In Decimal = 160, 020 In Hex = A0H, 14H
111 to 112	000 000	**Low End Input Voltage Range 1(10mV), Not Applicable** 2 Bytes Sequence In Decimal = 000, 000 In Hex = 00H, 00H
113 to 114	000 000	**High End Input Voltage Range 1(10mV), Not Applicable** 2 Bytes Sequence In Decimal = 000, 000 In Hex = 00H, 00H
115	000	**Low End Input Frequency Range, Not Applicable for DC Input**
116	000	**Low End Input Frequency Range, Not Applicable for DC Input**
117	000	**AC Dropout Tolerance in ms, Not Applicable**
118	008	**Binary Flags**, 1 indicates function supported and a 0 indicates function not supported. Bits 7-5: RESERVED, WRITE AS 000B Bit 4: Tachometer Pulses Per Rotation / Predictive Fail Polarity BIT = 0 Bit 3: Hot Swap / Redundancy Support BIT = 1 Bit 2: Autoswitch Support BIT = 0 Bit 1: Power Factor Correction Support BIT = 0 Bit 0: Predictive Fall Support BIT = 0
119 to 120	000 000	**Peak Wattage Capacity and Holdup Time**, Not specified Bits 15-12: Holdup Time in Seconds 00 = 00H Bits 11- 0: Peak Capacity in Watts 00 = 00H 2 Bytes sequence: In Decimal: 000,000 In Hex: 00H, 00H
121 to 123	018 215 000	**Combined Wattage, 215W combined for 3.3V and 5V** Byte 1: 018 = 12H Bits 7-4: Voltage 1 = Channel 1 indicating 5V Bits 3-0: Voltage 2 = Channel 2 indicating 3.3 V Byte 2 and Byte 3: Total Combined Wattage (LSB First) = 215W = 00D7H 3 Bytes Sequence In Decimal = 018, 215, 000 In Hex = 12H, D7H, 00H
124	000	**Predictive Fail Tachometer Lower Threshold,** Not Applicable. Predictive Failure is not Supported.
125 to 129		**12V DC Output Record Header**
125 to 129	001	Record type = 01 for DC Output Record
	002	End of List /Record Format Version Number for 3.3V DC Output Record
	013	Record Length of 3.3V DC Output Record
	154	Record CHECKSUM of 3.3V DC Output Record (Zero CHECKSUM)
	086	Header CHECKSUM of 3.3V DC Output Record Header (Zero CHECKSUM)
130 to 142		**12V Output Record**
130	000	**Output Information,** 000 =00H Bit 7: Standby Information Bits 6-4: Reserved, Write as 000B Bits 3-0: Output Number 0 = 000B
131 to 132	176	**Nominal Voltage (10mV),** 1200 = 04B0H 2 Bytes Sequence

NVRAM PAGE 2 CONTENTS

OFFSET (BYTES)	VALUE (DECIMAL)	DEFINITION (REMARKS)
	004	In Decimal: 176, 004 In Hex: B0H, 04H
133 to 134	116 004	**Maximum Negative Voltage Deviation (10mV),** 1140 = 0474H 2 Bytes Sequence In Decimal: 116, 004 In Hex: 74H, 04H
135 to 136	236 004	**Maximum Positive Voltage Deviation (10mV),** 1260 = 04ECH 2 Bytes Sequence In Decimal: 236, 004 In Hex: ECH, 04H
137 to 138	120 000	**Ripple and Noise pk-pk 10Hz to 30 MHz (mV),** 120 = 0078H 2 Bytes Sequence In Decimal: 120, 000 In Hex: 78H, 00H
139 to 140	000 000	**Minimum Current Draw (mA),** 00mA = 0000H 2 Bytes Sequence In Decimal: 000, 000 In Hex: 00H, 00H
141 to 142	152 058	**Maximum Current Draw (mA),** 15000 = 3A98H 2 Bytes Sequence In Decimal: 152, 058 In Hex: 98H, 3AH
143 to 147		**5V DC Output Record Header**
143 to 147	001	Record type = 01 for DC Output Record
	002	End of List /Record Format Version Number for 5V DC Output Record
	013	Record Length of 5V DC Output Record
	228	Record CHECKSUM of 5V DC Output Record (Zero CHECKSUM)
	012	Header CHECKSUM of 5V DC Output Record Header (Zero CHECKSUM)
148 to 160		**5V DC Output Record**
148	001	**Output Information,** 001 =01H Bit 7: Standby Information Bits 6-4: Reserved, Write as 000B Bits 3-0: Output Number 1 = 001B
149 to 150	244 001	**Nominal Voltage (10mV),** 500 = 01F4H 2 Bytes Sequence In Decimal: 244, 001 In Hex: F4H, 01H
151 to 152	229 001	**Maximum Negative Voltage Deviation (10mV),** 485 = 01E5H 2 Bytes Sequence In Decimal: 229, 001 In Hex: 0E5H, 01H
153 to 154	003 002	**Maximum Positive Voltage Deviation (10mV),** 515 = 0203H 2 Bytes Sequence In Decimal: 003, 002 In Hex: 03H, 02H
155 to 156	050 000	**Ripple and Noise pk-pk 10Hz to 30 MHz (mV),** 50 = 0032H 2 Bytes Sequence In Decimal: 050, 000 In Hex: 32H, 00H
157 to 158	000	**Minimum Current Draw (mA),** 00 = 0000H 2 Bytes Sequence

NVRAM PAGE 2 CONTENTS

OFFSET (BYTES)	**VALUE** (DECIMAL)	**DEFINITION** (REMARKS)
159 to 160	000	In Decimal: 000, 000 In Hex: 00H, 00H
	168	**Maximum Current Draw (mA),** 25000 = 61A8H 2 Bytes Sequence
	097	In Decimal: 168, 097 In Hex: A8H, 61H
161 to 165		**3.3V DC Output Record Header**
161 to 165	001	Record type = 01 for DC Output Record
	130	End of List /Record Format Version Number for 12V DC Output Record
	013	Record Length of 12V DC Output Record
	013	Record CHECKSUM of 12V DC Output Record (Zero CHECKSUM)
	099	Header CHECKSUM of 12V DC Output Record Header (Zero CHECKSUM)
166 to 178		**3.3V DC Output Record**
166	002	**Output Information,** 002 =02H Bit 7: Standby Information Bits 6-4: Reserved, Write as 000B Bits 3-0: Output Number 2 = 010B
167 to 168	074	**Nominal Voltage (10mV),** 330 = 014AH 2 Bytes Sequence
	001	In Decimal: 074, 001 In Hex: 4AH, 01H
169 to 170	062	**Maximum Negative Voltage Deviation (10mV),** 318 = 013EH 2 Bytes Sequence
	001	In Decimal: 062, 001 In Hex: 3EH, 01H
171 to 172	089	**Maximum Positive Voltage Deviation (10mV),** 345 = 0159H 2 Bytes Sequence
	001	In Decimal: 089, 001 In Hex: 59H, 01H
173 to 174	040	**Ripple and Noise pk-pk 10Hz to 30 MHz (mV),** 40 = 0028H 2 Bytes Sequence
	000	In Decimal: 040, 000 In Hex: 28H, 00H
175 to 176	000	**Minimum Current Draw (mA),** 00mA = 0000H 2 Bytes Sequence
	000	In Decimal: 000, 000 In Hex: 00H, 00H
177 to 178	232	**Maximum Current Draw (mA),** 65000 = FDE8H 2 Bytes Sequence
	253	In Decimal: 232, 253 In Hex: E8H, FDH
179 to 183		**Reserved Area, 5 Bytes**
179 to 183	000	**Reserved** Default Value is 0
	000	
	000	
	000	
	000	
184 to 255		**Internal Use Area, 119 Bytes**
184	001	Format version number = 1

NVRAM PAGE 2 CONTENTS

OFFSET (BYTES)	**VALUE** (DECIMAL)	**DEFINITION** (REMARKS)
185 to 216		**CALIBRATION TABLE (CAL Table 1)**
185	009	Length of the Internal use area in multiples of 8 bytes. (48H/ 8H = 09H)
186	025	Length of the CALIBRATION Table 25 Bytes = 19H
187	XXX	3.3V Offset LSB in mA Negative values are represented in 2's complement
188	XXX	3.3V Offset MSB in mA Negative values are represented in 2's complement
189	XXX	3.3V Gain LSB in mA/BIT
190	XXX	3.3V Gain MSB in mA/BIT
191	XXX	5V Offset LSB in mA Negative values are represented in 2's complement
192	XXX	5V Offset MSB in mA Negative values are represented in 2's complement
193	XXX	5V Gain LSB in mA/BIT
194	XXX	5V Gain MSB in mA/BIT
195	XXX	12V Offset LSB in mA Negative values are represented in 2's complement
196	XXX	12V Offset MSB in mA Negative values are represented in 2's complement
197	XXX	12V Gain LSB in mA/BIT
198	XXX	12V Gain MSB in mA/BIT
199	XXX	Temp1 Offset LSB in Degree C
200	XXX	Temp1 Offset MSB in Degree C
201	XXX	Temp1 Gain LSB in Degree C/BIT
202	XXX	Temp1 Gain MSB in Degree C/BIT
203	XXX	3.3V Minimum Usable Current LSB in mA
204	XXX	3.3V Minimum Usable Current Byte #2 in mA
205	XXX	3.3V Minimum Usable Current MSB in mA
206	XXX	5V Minimum Usable Current LSB in mA
207	XXX	5V Minimum Usable Current Byte #2 in mA
208	XXX	5V Minimum Usable Current MSB in mA
209	XXX	12V Minimum Usable Current LSB in mA
210	XXX	12V Minimum Usable Current Byte #2 in mA
211	XXX	12V Minimum Usable Current MSB in mA
212	XXX	CHKSUM LSB (Sum of the CAL TABLE Data Only) NOT a zero CHKSUM
213	XXX	CHKSUM MSB
214 to 216	000 000 000	Reserved Default Value is 0
217	XXX	Calibration Station Number
218	XXX	Calibration Week Code
219	XXX	Calibration Week Code
220 to 250		**BACKUP CALIBRATION TABLE (CAL Table 2)**
220	025	Length of the CALIBRATION Table 25 Bytes = 19H
221	XXX	3.3V Offset LSB in mA Negative values are represented in 2's complement
222	XXX	3.3V Offset MSB in mA Negative values are represented in 2's complement
223	XXX	3.3V Gain LSB in mA/BIT
224	XXX	3.3V Gain MSB in mA/BIT

NVRAM PAGE 2 CONTENTS

OFFSET (BYTES)	**VALUE** (DECIMAL)	**DEFINITION** (REMARKS)
225	XXX	5V Offset LSB in mA Negative values are represented in 2's complement
226	XXX	5V Offset MSB in mA Negative values are represented in 2's complement
227	XXX	5V Gain LSB in mA/BIT
228	XXX	5V Gain MSB in mA/BIT
229	XXX	12V Offset LSB in mA Negative values are represented in 2's complement
230	XXX	12V Offset MSB in mA Negative values are represented in 2's complement
231	XXX	12V Gain LSB in mA/BIT
232	XXX	12V Gain MSB in mA/BIT
233	XXX	Temp1 Offset LSB in Degree C
234	XXX	Temp1 Offset MSB in Degree C
235	XXX	Temp1 Gain LSB in Degree C/BIT
236	XXX	Temp1 Gain MSB in Degree C/BIT
237	XXX	3.3V Minimum Usable Current LSB in mA
238	XXX	3.3V Minimum Usable Current Byte #2 in mA
239	XXX	3.3V Minimum Usable Current MSB in mA
240	XXX	5V Minimum Usable Current LSB in mA
241	XXX	5V Minimum Usable Current Byte #2 in mA
242	XXX	5V Minimum Usable Current MSB in mA
243	XXX	12V Minimum Usable Current LSB in mA
244	XXX	12V Minimum Usable Current Byte #2 in mA
245	XXX	12V Minimum Usable Current MSB in mA
246	XXX	CHKSUM LSB (Sum of the CAL TABLE Data Only) NOT a zero CHKSUM
247	XXX	CHKSUM MSB
248 to 250	000	Reserved Default Value is 0
	000	
	000	
251	193	No More Field Marker
252 to 254	000	Reserved Default Value is 0
	000	
	000	
255	XXX	Zero CHECKSUM of Internal Use Area.

13. APPENDIX B – FRU EEPROM MAP(FOR REFERENCE, SOME VALUES MAY CHANGE)

ITEM	ADDRESS	BYTE VALUE	DESCRIPTION	BLOCK TITLE
1	0000H	01H	FORMAT VERSION NUMBER	COMMON HEADER
2	0001H	17H	INTERNAL USE AREA OFFSET	
3	0002H	01H	CHASSIS INFO AREA OFFSET	
4	0003H	00H	BOARD AREA OFFSET	
5	0004H	05H	PRODUCT INFO AREA OFFSET	
6	0005H	0CH	MULTI RECORD AREA OFFSET	
7	0006H	00H	PAD (ALWAYS ZERO)	
8	0007H	#NAME?	ZERO CHECK SUM (100H-(TOTAL BYTES))	
1	0008H	01H	Format version number = 0 to reflect that this area is not used.	CHASSIS INFO AREA
2	0009H	04H	Chassis Info Area Length (In multiples of 8 Bytes) 32Bytes are allocated (20Bytes/8 = 04H)	
3	000AH	XXH	Chassis type	
4	000BH	CAH	Chassis Part Number Type/Length - CAH (10 Bytes are allocated for Part Number)	
5	000CH	XXH	Chassis Part Number Bytes	
6	000DH	XXH	Chassis Part Number Bytes	
7	000EH	XXH	Chassis Part Number Bytes	
8	000FH	XXH	Chassis Part Number Bytes	
9	0010H	XXH	Chassis Part Number Bytes	
10	0011H	XXH	Chassis Part Number Bytes	
11	0012H	XXH	Chassis Part Number Bytes	
12	0013H	XXH	Chassis Part Number Bytes	
13	0014H	XXH	Chassis Part Number Bytes	
14	0015H	XXH	Chassis Part Number Bytes	
15	0016H	CFH	Chassis Serial Number Type/Length - D7H (15 Bytes are allocated for Serial Number)	
16	0017H	XXH	Chassis Serial Number Bytes	
17	0018H	XXH	Chassis Serial Number Bytes	
18	0019H	XXH	Chassis Serial Number Bytes	
19	001AH	XXH	Chassis Serial Number Bytes	
20	001BH	XXH	Chassis Serial Number Bytes	
21	001CH	XXH	Chassis Serial Number Bytes	
22	001DH	XXH	Chassis Serial Number Bytes	
23	001EH	XXH	Chassis Serial Number Bytes	
24	001FH	XXH	Chassis Serial Number Bytes	
25	0020H	XXH	Chassis Serial Number Bytes	

ITEM	ADDRESS	BYTE VALUE	DESCRIPTION	BLOCK TITLE
26	0021H	XXH	Chassis Serial Number Bytes	
27	0022H	XXH	Chassis Serial Number Bytes	
28	0023H	XXH	Chassis Serial Number Bytes	
29	0024H	XXH	Chassis Serial Number Bytes	
30	0025H	XXH	Chassis Serial Number Bytes	
31	0026H	C1H	NO MORE FIELDS MARKER	
32	0027H	XXH	ZERO CHECK SUM	
1	0028H	01H	PRODUCT AREA FORMAT VERSION : 01 = 01H	PRODUCT INFORMATION AREA
2	0029H	07H	PRODUCT AREA LENGTH (In multiple of 8 Bytes) : (56Bytes / 8)= 07 = 07H	
3	002AH	19H	LANGUAGE : ENGLISH = 25 = 19H	
4	002BH	C5H	MANUFACTURES NAME LENGTH : 05 = 05H	
5	002CH	41H	"A" = 41H	
6	002DH	53H	"S" = 53H	
7	002EH	54H	"T" = 54H	
8	002FH	45H	"E" = 45H	
9	0030H	43H	"C" = 43H	
10	0031H	CBH	PRODUCT NAME LENGTH: 11 = 0BH	
11	0032H	41H	"A" = 41H	
12	0033H	41H	"A" = 41H	
13	0034H	32H	"2" = 32H	
14	0035H	31H	"1" = 31H	
15	0036H	30H	"0" = 30H	
16	0037H	39H	"9" = 39H	
17	0038H	30H	"0" = 30H	
18	0039H	20H	" " = 20H	
19	003AH	20H	" " = 20H	
20	003BH	20H	" " = 20H	
21	003CH	20H	" " = 20H	
22	003DH	CAH	PART / MODEL NO. LENGTH: 10 = 0AH	
23	003EH	31H	Part Number = 1	
24	003FH	35H	Part Number = 5	
25	0040H	38H	Part Number = 8	
26	0041H	36H	Part Number = 6	
27	0042H	37H	Part Number = 7	
28	0043H	37H	Part Number = 7	
29	0044H	2DH	Part Number = -	

ITEM	ADDRESS	BYTE VALUE	DESCRIPTION	BLOCK TITLE
30	0045H	30H	Part Number = 0	
31	0046H	30H	Part Number = 0	
32	0047H	31H	Part Number = 1	
33	0048H	C2H	PRODUCT VERSION NO. LENGTH: 02 = 02H	
34	0049H	30H	0	Compaq Product AutoRev. 01 Upon Release
35	004AH	31H	1	
36	004BH	CEH	PRODUCT SERIAL NO. LENGTH: 14 = 0EH	
37	004CH	35H	Commodity Code: Power Supply = "5" = 53 = 35H	COMMODITY CODE
38	004DH	33H	3	
39	004EH	34H	4	
40	004FH	39H	9	
41	0050H	37H	7	AAAA: ASSEMBLY CODE
42	0051H	30H	0	
43	0052H	41H	A (When Released)	RR: REVISION LEVEL
44	0053H	39H	9	
45	0054H	35H	5	SS: SUPPLIER/SITE OF MFG
46	0055H	XXH	WEEK: Code provided by Compaq Procurement	
47	0056H	XXH	WEEK: Code provided by Compaq Procurement	WW: WEEK/YEAR OF MFG
48	0057H	XXH	Unique Sequence Identifire (Variable)	
49	0058H	XXH	Unique Sequence Identifire (Variable)	
50	0059H	XXH	Unique Sequence Identifire (Variable)	UNIQUE SEQUENCE IDENTIFIER
51	005AH	00H	ASSET TAG	
52	005BH	C1H	NO MORE FIELDS MARKER	
53	005CH	00H	Remaining Unused space - 00H	
54	005DH	00H	Remaining Unused space - 00H	
55	005EH	00H	Remaining Unused space - 00H	
56	005FH	XX	ZERO CHECK SUM	
1	0060H	00H	RECORD TYPE ID: POWER SUPPLY INFORMATIOM = 00 = 00H	MULTI - RECORD HEADER
2	0061H	02H	7:7 - END OF LIST = 0b, 6:4 - RESERVED = 000b, 3:0 - RECORD FORMAT VERSION = 0001b	POWER SUPPLY INFORMATION
3	0062H	18H	RECORD LENGTH OF MULTIRECORD : 24 = 18H	
4	0063H	#NAME?	RECORD CHECKSUM (Zero Checksum)	
5	0064H	#NAME?	HEADER CHECKSUM (Zero Checksum)	
1	0065H	8BH	15:12 - RESERVED = 000B, 11:0 - OVERALL CAPACITY (WATTS) 395W = 018BH	MULTI - RECORD HEADER
2	0066H	01H		POWER SUPPLY INFORMATION

ITEM	ADDRESS	BYTE VALUE	DESCRIPTION	BLOCK TITLE
3	0067H	26H	PEAK VA: 550W = 0226H (LSB FIRST)	
4	0068H	02H		
5	0069H	1CH	INRUSH CURRENT: 28Amp = 1CH	
6	006AH	01H	INRUSH INTERVAL in ms: 1ms = 01H	
7	006BH	E0H	LOW END INPUT VOLTAGE RANGE 1: 43.2V = 10E0H	
8	006CH	10H		
9	006DH	A0H	HIGH END INPUT VOLTAGE RANGE 1: 52.8V = 14A0H	
10	006EH	14H		
11	006FH	00H	LOW END INPUT VOLTAGE RANGE 2: NOT USED = 00H	
12	0070H	00H		
13	0071H	00H	HIGH END INPUT VOLTAGE RANGE 2: NOT USED = 00H	
14	0072H	00H		
15	0073H	00H	LOW END INPUT FREQUENCY RANGE: NOT USED = 00H	
16	0074H	00H	HIGH END INPUT FREQUENCY RANGE : NOT USED = 00H	
17	0075H	00H	A / C DROPOUT TOLERANCE IN mS : 0mS = 0H	
			7:5 - RESERVED: 000b	
			4:4 - TACHOMETER PULSES PER ROTATION / PREDICTIVE FALL POLARITY (2 PULSE PER ROTATION = 1b, ONE PULSE PER ROTATION = 0b) OR (SIGNAL ASSERTED (1) INDICATES FAILURE = 0b, SIGNAL DEASSERTED(0) INDICATES FAILURE = 1b): BIT = 0	DON'T CARE
			3:3 - HOT SWAP / REDUNDANCY SUPPORT: BIT = 1	SUPPORTED
			2:2 - AUTOSWITCH SUPPORT: BIT = 0	NOT SUPPORTED
			1:1 - POWER FACTOR CORRECTION SUPPORT: BIT = 0	NOT SUPPORTED
18	0076H	08H	0:0 - PREDICTIVE FALL SUPPORT: BIT = 0	NOT SUPPORTED
19	0077H	00H	15:12 - HOLD UP TIME IN SECONDS: NOT SPECIFIED = 00 = 00H, 11:0 - PEAK CAPACITY (WATTS): NOT SPECIFIED = 00 = 00H (LSB FIRST)	
20	0078H	00H		
21	0079H	12H	7:4 - VOLTAGE 1: (5V Ch. Number) = 01H, 3:0 - VOLTAGE 2: (3.3V Ch. Number) = 02H	
22	007AH	D7H	BYTE 2: 3 TOTAL COMBINED WATTAGE: 215W = 00D7H	COMBINED WATTAGE Byte1 - Voltage Byte 2:3 - Total Combined Wattage
23	007BH	00H		
24	007CH	00H	PREDICTIVE FALL TACHPMETER LOWER THRESHOLD = 00H	NOT SUPPORTED

ITEM	ADDRESS	BYTE VALUE	DESCRIPTION	BLOCK TITLE
1	007DH	01H	RECORD TYPE ID: DC OUTPUT = 01 = 01H	MULTIRECORD
2	007EH	02H	7:7 - END OF LIST = 0b, 6:4 - RESERVED = 000b, 3:0 - RECORD FORMAT VERSION = 0010b	HEADER
3	007FH	0DH	RECORD LENGTH OF MULTIRECORD : 13 = 0DH	DC Output +12V
4	0080H	#NAME?	RECORD CHECKSUM (Zero Checksum)	
5	0081H	#NAME?	HEADER CHECKSUM (Zero Checksum)	
1	0082H	00H	7:7 - STANDBY = 0b, 6:4 - RESERVED = 000b , 3:0 - OUTPUT NUMBER = 0000b	+12V Data
2	0083H	B0H	NOMINAL VOLTAGE (10mV) 1200 = 04B0H	
3	0084H	04H		
4	0085H	74H	MAXIMUM NEGATIVE VOLTAGE DEVIATION (10mV): 1140 = 0474H	
5	0086H	04H		
6	0087H	ECH	MAXIMUM POSITIVE VOLTAGE DEVIATION (10mV): 1260 = 04ECH	
7	0088H	04H		
8	0089H	78H	RIPPLE AND NOISE PK-PK 10Hz TO 30MHz (mV) : 120mV = 0078H	
9	008AH	00H		
10	008BH	00H	MINIMUM CURRENT DRAW(mV): 00mA = 00H	
11	008CH	00H		
12	008DH	98H	MAXIMUM CURRENT DRAW(mV): 15000mA = 3A98H	
13	008EH	3AH		MULTIRECORD
1	008FH	01H	RECORD TYPE ID : DC OUTPUT = 01 = 01H	
2	0090H	02H	7:7 - END OF LIST = 0b, 6:4 - RESERVED = 000b, 3:0 - RECORD FORMAT VERSION = 0010b	HEADER
3	0091H	0DH	RECORD LENGTH OF MULTIRECORD: 13 = 0DH	DC Output +5V
4	0092H	#NAME?	RECORD CHECKSUM (Zero Checksum)	
5	0093H	#NAME?	HEADER CHECKSUM (Zero Checksum)	
1	0094H	01H	7:7 - STANDBY = 0b, 6:4 - RESERVED = 000b , 3:0 - OUTPUT NUMBER = 0001b	+5V Data
2	0095H	F4H	NOMINAL VOLTAGE (10mV) : 500 = 01F4H	
3	0096H	01H		
4	0097H	E5H	MAXIMUM NEGATIVE VOLTAGE DEVIATION (10mV): 485 = 01E5H	
5	0098H	01H		
6	0099H	03H	MAXIMUM POSITIVE VOLTAGE DEVIATION (10mV): 515 = 0203H	
7	009AH	02H		
8	009BH	32H	RIPPLE AND NOISE PK-PK 10Hz TO 30MHz (mV): 50mV = 0032H	
9	009CH	00H		
10	009DH	00H	MINIMUM CURRENT DRAW (mA): 00mA = 00H	

ITEM	ADDRESS	BYTE VALUE	DESCRIPTION	BLOCK TITLE
11	009EH	00H		
12	009FH	A8H	MAXIMUM CURRENT DRAW (mA): 25000mA = 61A8H	
13	00A0H	61H		
1	00A1H	01H	RECORD TYPE ID: DC OUTPUT = 01 = 01H	MULTI - RECORD
2	00A2H	82H	7:7 - END OF LIST = 1b, 6:4 - RESERVED = 000b, 3:0 - RECORD FORMAT VERSION = 0010b	HEADER
3	00A3H	0DH	RECORD LENGTH OF MULTIRECORD : 13 = 0DH	DC Output +3.3V
4	00A4H	#NAME?	RECORD CHECKSUM (Zero Checksum)	
5	00A5H	#NAME?	HEADER CHECKSUM (Zero Checksum)	
1	00A6H	02H	7:7 - STANDBY = 0b, 6:4 - RESERVED = 000b , 3:0 - OUTPUT NUMBER = 0010b	+3.3V Data
2	00A7H	4AH	NOMINAL VOLTAGE (10mV) 330 = 014AH	
3	00A8H	01H		
4	00A9H	3EH	MAXIMUM NEGATIVE VOLTAGE DEVIATION (10mV) 318 = 013EH	
5	00AAH	01H		
6	00ABH	59H	MAXIMUM POSITIVE VOLTAGE DEVIATION (10mV) 345 = 0159H	
7	00ACH	01H		
8	00ADH	28H	RIPPLE AND NOISE PK-PK 10Hz TO 30MHz (mV) 40mV = 0028H	
9	00AEH	00H		
10	00AFH	00H	MINIMUM CURRENT DRAW (mA) 00mA = 00H	
11	00B0H	00H		
12	00B1H	E8H	MAXIMUM CURRENT DRAW (mA) 65000mA = 0FDE8H	
13	00B2H	FDH		
1	00B3H	00H	Reserved	
2	00B4H	00H	Reserved	
3	00B5H	00H	Reserved	
4	00B6H	00H	Reserved	
5	00B7H	00H	Reserved	
1	00B8H	01H	Format version number = 1	INTERNAL USE AREA
2	00B9H	09H	Length of the Internal use area in multiples of 8 bytes. (48H/ 8H = 09H)	72 Bytes have been allocated to this area .
3	00BAH	19H	Length of the CALIBRATION Table 25 Bytes = 19H	Power Supply Calibration Table
4	00BBH	XXH	3.3V Offset LSB (mA) (Negative values are represented in 2's complement)	
5	00BCH	XXH	3.3V Offset MSB (mA) (Negative values are represented in 2's complement)	
6	00BDH	XXH	3.3V Gain LSB (mA/BIT)	
7	00BEH	XXH	3.3V Gain MSB (mA/BIT)	

ITEM	ADDRESS	BYTE VALUE	DESCRIPTION	BLOCK TITLE
8	00BFH	XXH	5V Offset LSB (mA) (Negative values are represented in 2's complement)	
9	00C0H	XXH	5V Offset MSB (mA) (Negative values are represented in 2's complement)	
10	00C1H	XXH	5V Gain LSB (mA/BIT)	
11	00C2H	XXH	5V Gain MSB (mA/BIT)	
12	00C3H	XXH	12V Offset LSB (mA) (Negative values are represented in 2's complement)	
13	00C4H	XXH	12V Offset MSB (mA) (Negative values are represented in 2's complement)	
14	00C5H	XXH	12V Gain LSB (mA/BIT)	
15	00C6H	XXH	12V Gain MSB (mA/BIT)	
16	00C7H	XXH	Temp1 Offset LSB (Degree C)	
17	00C8H	XXH	Temp1 Offset MSB (Degree C)	
18	00C9H	XXH	Temp1 Gain LSB (Degree C/BIT)	
19	00CAH	XXH	Temp1 Gain MSB (Degree C/BIT)	
20	00CBH	XXH	3.3V Minimum Usable Current LSB (mA)	
21	00CCH	XXH	3.3V Minimum Usable Current Byte #2 (mA)	
22	00CDH	XXH	3.3V Minimum Usable Current MSB (mA)	
23	00CEH	XXH	5V Minimum Usable Current LSB (mA)	
24	00CFH	XXH	5V Minimum Usable Current Byte #2 (mA)	
25	00D0H	XXH	5V Minimum Usable Current MSB (mA)	
26	00D1H	XXH	12V Minimum Usable Current LSB (mA)	
27	00D2H	XXH	12V Minimum Usable Current Byte #2 (mA)	
28	00D3H	XXH	12V Minimum Usable Current MSB (mA)	
29	00D4H	XXH	CHKSUM LSB (Sum of the CAL TABLE Data Only) NOT a zero CHKSUM	
30	00D5H	XXH	CHKSUM MSB	
31	00D6H	00H	Reserved - 00H	
32	00D7H	00H	Reserved - 00H	
33	00D8H	00H	Reserved - 00H	
34	00D9H	XXH	Calibration Station Number	
35	00DAH	XXH	Calibration Week Code	
36	00DBH	XXH	Calibration Week Code	
37	00DCH	19H	Length of the BackUp CALIBRATION Table 25 Bytes = 19H	(BACKUP CALIBRATION TABLE)
38	00DDH	XXH	3.3V Offset LSB (mA)	
39	00DEH	XXH	3.3V Offset MSB (mA)	

ITEM	ADDRESS	BYTE VALUE	DESCRIPTION	BLOCK TITLE
40	00DFH	XXH	3.3V Gain LSB (mA/BIT)	
41	00E0H	XXH	3.3V Gain MSB (mA/BIT)	
42	00E1H	XXH	5V Offset LSB (mA)	
43	00E2H	XXH	5V Offset MSB (mA)	
44	00E3H	XXH	5V Gain LSB (mA/BIT)	
45	00E4H	XXH	5V Gain MSB (mA/BIT)	
46	00E5H	XXH	12V Offset LSB (mA)	
47	00E6H	XXH	12V Offset MSB (mA)	
48	00E7H	XXH	12V Gain LSB (mA/BIT)	
49	00E8H	XXH	12V Gain MSB (mA/BIT)	
50	00E9H	XXH	Temp1 Offset LSB (Degree C)	
51	00EAH	XXH	Temp1 Offset MSB (Degree C)	
52	00EBH	XXH	Temp1 Gain LSB (Degree C/BIT)	
53	00ECH	XXH	Temp1 Gain MSB (Degree C/BIT)	
54	00EDH	XXH	3.3V Minimum Usable Current LSB (mA)	
55	00EEH	XXH	3.3V Minimum Usable Current Byte #2 (mA)	
56	00EFH	XXH	3.3V Minimum Usable Current MSB (mA)	
57	00F0H	XXH	5V Minimum Usable Current LSB (mA)	
58	00F1H	XXH	5V Minimum Usable Current Byte #2 (mA)	
59	00F2H	XXH	5V Minimum Usable Current MSB (mA)	
60	00F3H	XXH	12V Minimum Usable Current LSB (mA)	
61	00F4H	XXH	12V Minimum Usable Current Byte #2 (mA)	
62	00F5H	XXH	12V Minimum Usable Current MSB (mA)	
63	00F6H	XXH	CHKSUM LSB (Sum of the CAL TABLE Data Only) NOT a zero CHKSUM	
64	00F7H	XXH	CHKSUM MSB	
65	00F8H	00H	Reserved - 00H	
66	00F9H	00H	Reserved - 00H	
67	00FAH	00H	Reserved - 00H	
68	00FBH	C1H	NO MORE FIELDS MARKER	
69	00FCH	00H	Reserved - 00H	
70	00FDH	00H	Reserved - 00H	
71	00FEH	00H	Reserved - 00H	
72	00FFH	XXH	ZERO CHECK SUM	

[CR1]

PART No.:	**158677**		
PROJECT CODE:	11265		
PROCUREMENT ENGINEER:	SONNY TRAN OR MICHAEL MATHEIDAS	**EXT:**	
COG ENGINEER:	HAROLD SELOFF	**EXT:**	
SPEC WRITER:	M. LUNA	**EXT:**	8-4950
RECEIVED INPUT:	05/04/01		

ARTWORK:

TO DRAFTING	FROM DRAFTING	DRAFTER
		Figs. In softcopy input from COG

DRAFT/REV	SENT TO ENG	REC'D FROM ENG	DATE LAST WORKED	SW
A				**ML**