An Improved Full-Bridge Zero-Voltage Switching PWM Converter Using a Two-Inductor Rectifier

Nasser H. Kutkut, *Student Member, IEEE,* Deepakraj M. Divan, *Senior Member, IEEE,* and Randal W. Gascoigne, *Member, IEEE*

Abstract— **An improved full-bridge ZVS PWM using a two-inductor rectifier dc/dc converter is presented in this paper. For this improved topology, the main devices are switched on under zero-voltage (ZVS) conditions using the energy stored in the secondary filter inductors. In addition, it utilizes the low leakage inductance of a coaxial winding transformer to reset the currents in the rectifier diodes and eliminate the secondary voltage spike. The two-inductor rectifier has only one diode conduction drop in addition to frequency doubling in the output capacitor. The secondary filter size in the proposed topology is rather small. The advantages of the new topology include a wide loa d range with ZVS, no lost duty cycle due to diode recovery, no secondary voltage spikes, in addition to high power density and high efficiency.**

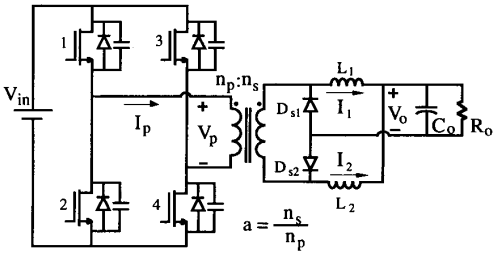

Fig. 1. Full-bridge ZVS PWM converter with two-inductor rectifier.

I. Introduction

MOST of the dc/dc converters in use today are derived from the three basic single quadrant topologies: buck, boost, and buck-boost converters. At high power levels, the full-bridge (buck-derived) dc/dc converter with isolation on the intermediate high frequency ac link is the preferred topology. The main advantages of this topology include constant frequency operation, which allows optimum design of the magnetic filter components, PWM control, minimum VA stresses, and good control range and controllability. However, the increase in device switching losses as the frequency increases and the high-voltage stress induced by the parasitic inductances following diode reverse recovery are major drawbacks of this topology.

Various soft switching schemes (ZVS and ZCS) have been proposed to improve the performance of hard switching converters. A pseudoresonant dc/dc converter proposed by Patterson *et al.* [1] demonstrates the possibility of achieving conventional PWM control with resonant switching. Yet, reverse recovery of output diodes causes large voltage spikes and hence, a snubber circuit is needed. Another topology that achieves PWM control with resonant switching is the full-bridge ZVS (FB-ZVS) PWM converter [2]. In this topology, the transformer leakage and magnetizing inductances in addition to the MOSFET capacitance are effectively utilized to achieve ZVS. The load range can be extended by properly sizing the leakage inductance of the transformer. One drawback of this topology is that secondary voltage spikes are generated and there is a lost duty cycle caused by output diodes reverse recovery.

Most topologies, unless dependent on multiresonant conversion, or using active elements on both sides of the converter, are subject to diode recovery problems. In the FB-ZVS PWM converter described above, secondary voltage spikes are generated due to the interaction between the transformer leakage inductance and the output diode capacitance following diode reverse recovery. This problem can get worse if the leakage inductance is made larger. On the other hand, reducing the size of the leakage inductance results in reducing the ZVS range and higher di/dt, which in turns results in higher secondary voltage spikes.

In this paper, an improved converter topology is proposed. It is basically a full-bridge topology with a two- inductor rectifier, as shown in Fig. 1. The two-inductor rectifier circuit was first reported in [3]. The output voltage is controlled using phase shift control. For this topology, ZVS is achieved using the energy stored in the output filter inductors instead of the leakage inductance energy. In fact, the transformer leakage inductance is reduced drastically to allow output diode commutation prior to switching the primary voltage to the other rail. This, in turn, results in elimination of secondary voltage spikes.

The need for a transformer with very low and controllable leakage inductance makes the coaxial winding transformer (CWT) the preferred structure [4], [5]. Due to its coaxial structure, the leakage inductance can be controlled and made very small.

This paper presents a complete steady-state analysis of the proposed topology and an assessment of the various losses

Paper IPCSD 94-52, approved by the Industrial Power Converter Committee of the IEEE Industry Applications Society for presentation at the 1993 IAS Annual Meeting. This work was supported by the NASA Lewis Research Center, Cleveland, OH. Manuscript released for publication June 25, 1994.

The authors are with the Department of Electrical and Computer Engineering, University of Wisconsin, Madison, WI 53706 USA.

IEEE Log Number 9405309.

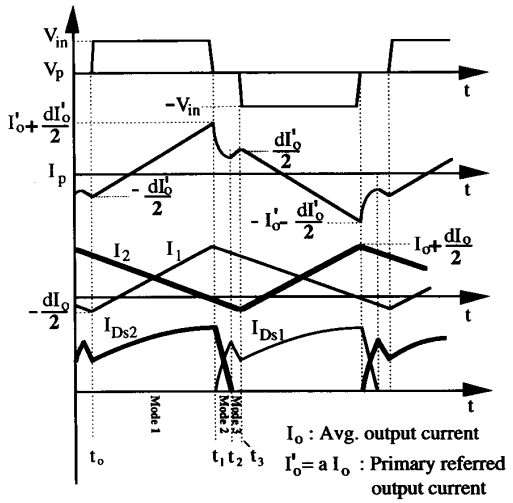

Fig. 2. Typical voltage and current waveforms of the converter.

in the circuit. Simulation and experimental results of a 2 kW prototype converter built in the lab will be included.

II. Analysis

A. Principle of Operation

As shown in Fig. 1, the converter is basically a full-bridge PWM converter with a two-inductor rectifier circuit. The converter is operated in a mode that provides zero voltage turn-on for the main devices. This can be achieved by introducing a phase shift between the switches in the right leg (leading leg) and those in the left leg (lagging leg). In addition, the phase shift will determine the duty cycle of the converter. The current and voltage wave forms of the circuit are shown in Fig. 2.

In contrast with the FB-ZVS PWM converter described earlier, ZVS for the proposed topology is achieved using the energy stored in the secondary filter inductors to discharge the output capacitance of the MOSFET's before turning them on. As mentioned earlier, a low leakage inductance is required for this topology.

With Q1 and Q4 conducting at t_o, the primary voltage will be$+V_{\text{in}}$ with diode Ds1 off and diode Ds2 conducting. When Q4 is turned off at t_1, the energy stored in the secondary filter inductor L_1 charges the output capacitance of Q4 and discharges the output capacitance of Q3 causing diode D3 to conduct. After D3 starts conducting, Q3 can be turned on under ZVS. Since the energy available for achieving ZVS for the leading leg is the output filter energy, ZVS can be achieved even at light loads.

In order to ensure ZVS for Q3, a dead time is needed between the turn off of Q4 and the turn-on of Q3 to ensure that D3 conducts prior to the turn on of Q3. The required dead time, Δt_1, can be computed using

$$I_{p1}\,\Delta t_1 = 2C_{\text{eff}}V_{\text{in}} \tag{1}$$

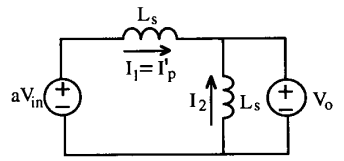

Fig. 3. Equivalent circuit for mode I.

where C_{eff} is the effective drain to source MOSFET capacitance and I_{p1} is the value of the primary current at t_1.

While Q1 and D3 are conducting, the primary current decays in a fashion similar to an R–L circuit with a time constant $\tau_p = L_{lp}/r_p$, where the L_{lp} is the primary referred leakage inductance while r_p is the device-on resistance in addition to the transformer resistance. As the primary current decays, the current in diode Ds1 ramps up while the current in Ds2 ramps down at the same rate. If the current I_2 becomes negative during this mode and the time constant τ_p is very small, the secondary diodes will commutate, where Ds2 turns off and Ds1 takes over. This is shown in Fig. 2, where Ds2 turns off and Ds1 takes over at t_2. As a result, the primary current will be the reflected secondary filter current I_2. When Q1 is turned off at a later time t_3, the energy available to charge and discharge the output capacitance of Q1 and Q2, respectively, is again the energy stored in the secondary filter L_2. The delay time needed between the turn off of Q1 and the turn on of Q2, Δt_2, is computed using a similar formula as in (1), namely,

$$I_{p2}\,\Delta t_2 = 2C_{\text{eff}}V_{\text{in}} \tag{2}$$

where I_{p2} is the primary current at t_2. Note here that since the secondary diodes commutate prior to switching the primary voltage to the negative rail, no duty cycle is lost and no voltage spike will occur on the secondary side of the transformer.

B. Steady-State Analysis

The analysis of this converter is divided into three distinct circuit modes. Note that the secondary filter inductances, L_1 and L_2, are assumed to be the same and will be referred to as L_s. These circuit modes are categorized as follows:

$$\text{Mode I: } t_o < t < t_1, \quad \text{where } t_1 = DT_s/2.$$

In the primary, Q1 and Q4 are conducting while in the secondary, Ds2 is conducting. The equivalent circuit is shown in Fig. 3. The governing equations during this mode are as follows:

$$I_1(t) = I_{1o} + \frac{aV_{\text{in}} - V_o}{L_s}t \tag{3}$$

$$I_2(t) = I_{2o} - \frac{V_o}{L_s}t \tag{4}$$

$$I_p(t) = aI_1(t) \tag{5}$$

where a is the secondary to primary turns ratio. This mode terminates when transistor Q4 is turned off.

$$\text{Mode II: } t_1 < t < t_2, \quad \text{where } t_2 \le T_s/2.$$

This mode is initiated by turning off Q4 where Q1 and D3 are conducting in the primary circuit. In the secondary circuit,

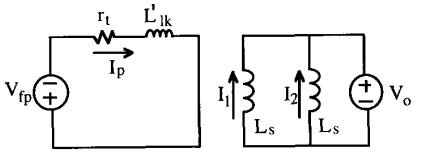

Fig. 4. Equivalent circuit for mode II.

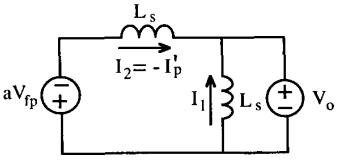

Fig. 5. Equivalent circuit for mode III.

the output current freewheels in both Ds1 and Ds2, hence, both diodes are conducting. The equivalent circuit is shown in Fig. 4.

The governing equations for this mode are

$$I_1(t) = I_1\left(\frac{DT_s}{2}\right) - \frac{V_o}{L_s}\left(t - \frac{DT_s}{2}\right) \tag{6}$$

$$I_2(t) = I_2\left(\frac{DT_s}{2}\right) - \frac{V_o}{L_s}\left(t - \frac{DT_s}{2}\right) \tag{7}$$

$$I_p(t) = -\frac{V_{fp}}{r_t} + \left[\frac{V_{fp}}{r_t} + I_p\left(\frac{DT_s}{2}\right)\right] e^{-(t-DT_s/2)/\tau} \tag{8}$$

$$\tau = \frac{L'_{lk}}{r_t} \tag{9}$$

$$r_t = r_{\text{mosfet}} + r_{xfmr} \tag{10}$$

where D is the duty ratio defined over half a cycle, f_s is the switching frequency, L'_{lk} is the primary referred leakage inductance, r_t is the equivalent primary circuit resistance, τ_p is the time constant of the primary current decay, and V_{fp} is the forward voltage drop of the primary diodes.

Mode III: $t_2 < t < t_3$, where $t_3 = T_s/2$.

This mode is very similar to mode II, where Q1 and D3 are conducting in the primary circuit. It is initiated by the turn-off of Ds2 in the secondary circuit when the secondary diodes commutate. The equivalent circuit is shown in Fig. 5.

The governing equations for this mode are

$$I_1(t) = I_1\left(\frac{DT_s}{2}\right) - \frac{V_o}{L_s}\left(t - \frac{DT_s}{2}\right) \tag{11}$$

$$I_2(t) = I_2\left(\frac{DT_s}{2}\right) - \frac{V_o}{L_s}\left(t - \frac{DT_s}{2}\right) \tag{12}$$

$$I_p(t) = -aI_2(t) \tag{13}$$

Note here that the currents I_1 and I_2 are the same as in mode II, while the diode Ds1 will have the full-load current. In addition, the diode forward drop is small in comparison with the output voltage, and hence, it was neglected. This mode terminates when Q1 is turned off where the energy stored in the secondary filter L_2 will charge/discharge the output capacitances of Q1/Q2 in a linear fashion.

In the steady state, and since $L_1 = L_2 = L_s$, the currents I_1 andI_2 will be symmetrical over half a cycle. Using this condition, the output voltage V_o is computed as

$$V_o = \frac{aDV_{\text{in}}}{2}. \tag{14}$$

Since the average output current$I_o = I_{1,\text{avg}} + I_{2,\text{avg}}$, the initial value of I_1 and I_2 can be computed. Hence,

$$I_{1o} = \frac{I_o}{2} - \frac{aD(2-D)V_{\text{in}}}{8f_sL_s}. \tag{15}$$

At the end of mode III, Q1 turns off and diodes D2 and D3 in the primary circuit will be conducting while diode Ds1 in the secondary will be conducting. During this mode, Q2 and Q3 can be turned on under ZVS. When the primary current goes negative, Q2 and Q3, in the primary circuit, will take over. Due to symmetry, the negative half cycle will be the same as the positive one.

In order to simplify the analysis, the initial current I_{1o} will be written as

$$I_{1o} = -\frac{dI_o}{2} \tag{16}$$

where d is defined as the secondary current undershoot ratio. The value of d defines the initial current I_{1o} as a fraction of the average output current I_o. The negative sign in (16) is used to indicate that the initial current I_{1o} is negative for positive values of d. In fact, this condition is essential in order to achieve secondary diodes' commutation with zero voltage and to eliminate secondary voltage spikes due to diode reverse recovery. For a given value of d, the required secondary inductance can be computed via

$$L_s = \frac{aD(2-D)V_{\text{in}}}{4f_s(1+d)I_o}. \tag{17}$$

Hence, given the rating of the converter, the operating frequency, and full-load duty cycle, the required L_s can be computed.

III. ZVS Range

As discussed earlier, it was shown that the transistors in the right leg are always turned on under ZVS conditions since the energy available to charge/discharge the MOSFET's output capacitance is the energy stored in the leakage inductance in addition to the energy stored in the secondary output filter L_1. The latter energy is available due to the fact that when Q4 is turned-off, the secondary diodes do not freewheel the output current until the primary voltage has fallen to zero. Hence ZVS for the right leg is achieved even at light load conditions.

For the left leg transistors, it was stated that in order to achieve ZVS in a similar manner to that of the right leg, the secondary filter current I_2 need be negative at the instant when Q4 is turned-off. This condition is equivalent to constraining d in (16) to be a positive value. In addition, the decay rate of the

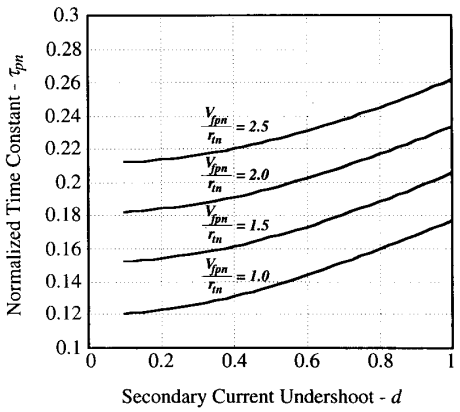

Fig. 6. Normalized time constant of the primary circuit for different V_{fpn}/r_{tn} with $D = 0.67$ and $a = 3$.

primary current during mode II needs to be very rapid in order for the secondary diodes to commutate. This can be achieved if the time constant τ_p is very small compared with the time spent in mode II. Once the secondary diodes commutate, the primary current will be the reflected secondary filter current, I_2'.

The above discussion can be rephrased mathematically as

$$I_p(t_2) = -aI_2\left(\frac{DT_s}{2}\right) = \frac{adI_o}{2} \tag{18}$$

where $t_1 = DT_s/2 \le t_2 \le t_3 = T_s/2$. In the limit, if t_2 equals $T_s/2$, (18) can be solved for τ_p as

$$\frac{1}{\tau_p} \ge \frac{2f_s}{1-D}\ln\left(1 + \frac{aI_o}{\frac{V_{fp}}{r_t} + \frac{adI_o}{2}}\right). \tag{19}$$

Equation (19) gives the value of τ_p required to achieve ZVS. Hence, by solving (19) for L_{lk},

$$L_{lk} = a^2 r_t \tau_p \tag{20}$$

where r_t is defined in (10). In summary, (18) and (19) specify the conditions that are required to achieve ZVS for the left leg.

Equation (19) can be normalized using the input voltage, the output currentand the switching frequency as base values. Fig. 6 shows the normalized time constant (τ_{pn}) as a function of the secondary current undershoot ratio d for different values of V_{fpn}/r_{tn}. These curves were obtained with a duty cycle D of 0.67 and a turns ratio, a, of 3.

As shown in Fig. 6, the normalized time constant increases with increasing d and V_{fpn}/r_{tn}. Notice here that the leakage reactance required in the primary circuit can be found using (20) for a given set of base values. In fact, the value of the leakage reactance required in the primary circuit for this topology is typically low. Normally, this value cannot be achieved using conventional winding transformers. On the other hand, coaxial winding transformers can achieve low values of leakage inductances due to their unique characteristics of confined and easily controlled leakage flux.

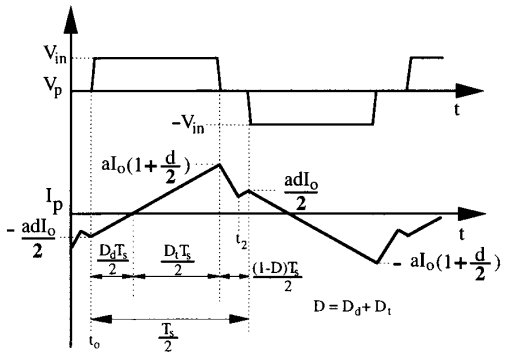

Fig. 7. Primary voltage and current waveforms for loss analysis.

IV. Loss Analysis

A. Conduction Losses

In this section, the conduction losses of the converter, which are the main loss components, will be evaluated. For MOSFET's, conduction losses can be computed via

$$P_{\text{con}} = I_{\text{rms}}^2 r_{ds} \tag{21}$$

where r_{ds} is the on-resistance of the MOSFET. Hence, the MOSFET's rms currents need to be evaluated first. In order to simplify the analysis, the primary current in mode II is assumed to decay in a linear fashion. This is shown in Fig. 7.

Referring to Fig. 7, consider the case where t_2 equals to $T_s/2$,the devices rms currents are computed to be

$$I_{Q1,\,2-\text{rms}} = aI_o\sqrt{\frac{D_t(2+d)^2}{24} + \frac{(1-D)}{8}\left[\frac{1}{3} + (1+d)^2\right]} \tag{22}$$

$$I_{Q3,\,4-\text{rms}} = aI_o\sqrt{\frac{D_t(2+d)^2}{24}} \tag{23}$$

where $D_tT_s/2$ is the conduction time of transistors Q3 and Q4. D_t can be computed by referring to Fig. 7 as

$$D_t = \frac{2+d}{2(1+d)}D. \tag{24}$$

Hence, the conduction losses of the MOSFET's are,

$$P_{Q-\text{con}} = 2(I_{Q1,\,2-\text{rms}}^2 + I_{Q3,\,4-\text{rms}}^2)r_{ds}. \tag{25}$$

For the primary and secondary diodes, the conduction losses are computed by

$$P_{D-\text{con}} = I_{\text{avg}}V_f \tag{26}$$

where I_{avg} is the average current in the diode and V_f is the forward voltage drop across the diode. The average currents of the primary diodes were computed to be

$$I_{D1,\,2-\text{avg}} = aI_o\left(\frac{dD_t}{8}\right) \tag{27}$$

$$I_{D3,\,4-\text{avg}} = aI_o\left(\frac{2(1-D)(1+d) + dD_t}{8}\right). \tag{28}$$

Hence, the primary diodes conduction losses are

$$P_{dp-\text{con}} = 2(I_{D1,\,2-\text{avg}} + I_{D3,\,4-\text{avg}})V_{fp} \tag{29}$$

where D_t is computed using (24).

For the secondary diodes, the average current in each diode and the totalconduction losses are given below:

$$I_{Ds1,\,2-\text{avg}} = \frac{I_o}{2} \tag{30}$$

$$P_{ds-\text{con}} = I_o V_{fs}. \tag{31}$$

Finally, the total devices' conduction losses are given by,

$$P_{\text{con-total}} = P_{Q-\text{con}} + P_{dp-\text{con}} + P_{ds-\text{con}}. \tag{32}$$

B. Switching Losses

Since this converter achieves ZVS for both legs over a wide load range, the turn-on losses for the transistors are zero if the conditions stated in Section III are met.

Turn-off losses in MOSFET's are very small due to their fast switching characteristics and the presence of parasitic capacitance across the output junction, C_{ds}, which will control the dv/dt across the device. The output capacitance has a nonlinear nature, where it is inversely proportional to the square root of the voltage.

These losses are very small and can be computed using

$$P_{Q-sw} = f_s t_f (aI_o)^2 \frac{\left(\frac{d}{2}\right)^2 + \left(1+\frac{d}{2}\right)^2}{16 C_{\text{mosfet}}} \tag{33}$$

where t_f is the fall time of the MOSFET. By adding up (32) and (33), the total normalized losses are,

$$P_{\text{loss-total}} = P_{\text{con-total}} + P_{Q-sw}. \tag{34}$$

Hence, the efficiency can be computed by

$$\text{Efficiency} = 1 - P_{\text{loss-total-norm}} \tag{35}$$

where $P_{\text{loss-total-norm}}$ is the normalized total loss.

V. Design Curves

Using the equations derived in the preceding section, the design curves for a 10 kW converter can be obtained. The specifications of the proposed converter are 150 V input, 150 V output voltages with 20 kHz switching frequency.

For the proposed converter, the on-resistance of the MOSFET's is assumed to be 20 mΩ with 2 V forward drop for the primary and the secondary diodes. For the isolation transformer, a minimum of 1:2 turns ratio is required to obtain a 150 V output voltage since the proposed topology has an inherent 2:1 voltage ratio. The equivalent resistance of a coaxial winding transformer designed for such an application is calculated to be on the order of 1 mΩ.

Using the above data, the effect of leakage inductance on the different design parameters is shown in Fig. 8.

Fig. 8(a) shows the effect of the leakage inductance on the secondary current undershoot ratio d needed to ensure ZVS for all devices. For low values of leakage inductance (less than 150 nH), a minimum value of d equals to 0.1 is assumed

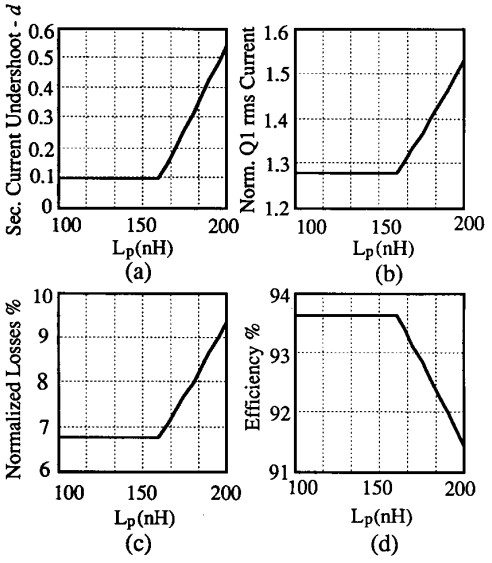

Fig. 8. Design curves for the proposed converter (10 kW) ($V_B = V_{\text{in}}$, $I_B = I_o$, $f_s = 20$ kHz, $a = 3$).

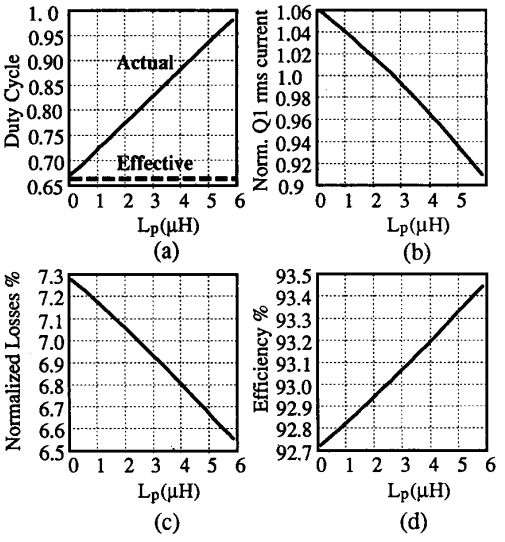

Fig. 9. Design curves of a conventional 10 kW FB-PWM converter ($V_B = V_{\text{in}}$, $I_B = I_o$, $f_s = 20$ kHz, $a = 1.5$).

in the above analysis. As the leakage inductance increases, the required value of d becomes larger. This results in higher rms device currents, higher conduction loss, and hence, lower efficiency, as shown in Fig. 8(b), (c), and (d), respectively. On the other hand, increasing d results in a wider ZVS range for the MOSFET's. As a result, the design of d is a compromise between the higher losses and wider ZVS range. Note here that the value of d specifies the size of the secondary filters as given by (17).

Unlike the FB-PWM ZVS converter, the required leakage inductance is rather small due to the fact that the secondary filter energy is used to achieve ZVS for the main devices

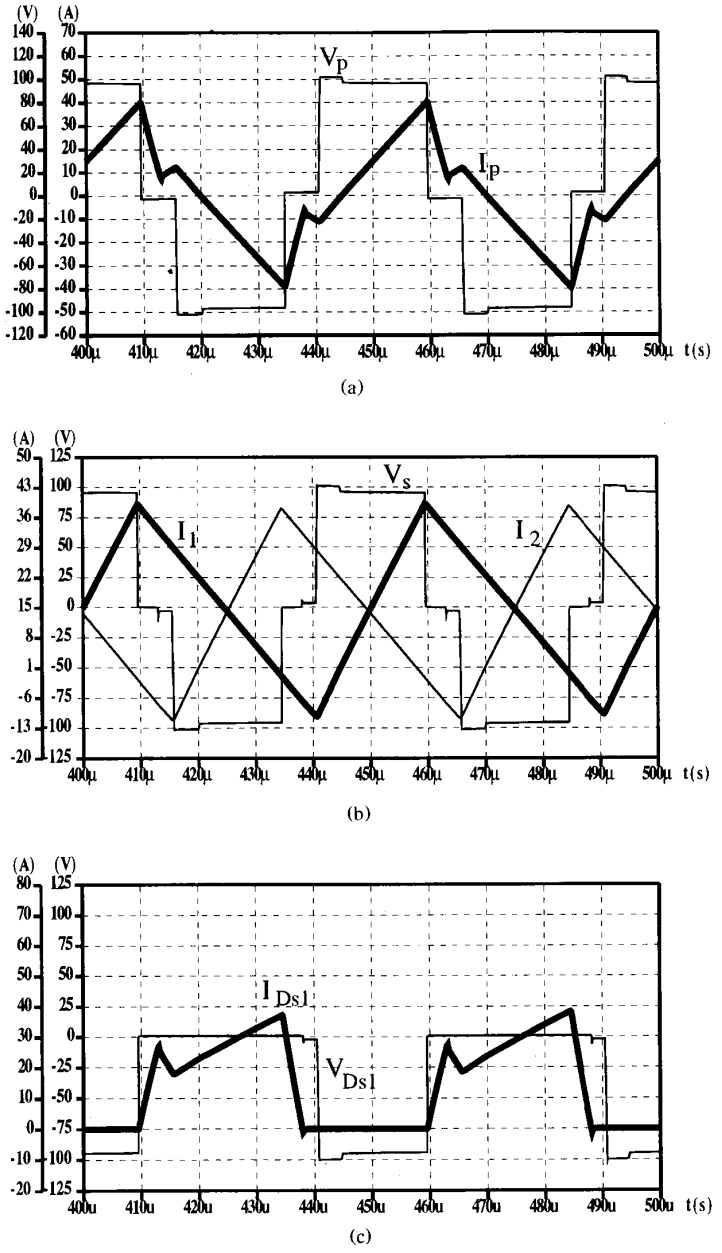

Fig. 10. Simulation results (at 1 kW). (a) Primary voltage and current. (b) Secondary voltage and secondary filter currents. (c) Secondary diode currents.

instead of the leakage energy. Such low values of leakage inductances cannot be realized easily using conventional winding transformers. On the other hand, coaxial transformers can realize low leakages due to their unique structure of confined leakage flux.

VI. A Comparison with a Conventional Full-Bridge PWM ZVS Converter

In this section, a comparison between the proposed converter and the full-bridge PWM ZVS converter is presented. For the FB-PWM ZVS converter, the leakage and magnetizing inductances of the transformer, in addition to the parasitic capacitance of the MOSFET's, are used to achieve ZVS. Phase shift control is also used here to achieve ZVS.

In the FB-PWM ZVS converter, the MOSFET's in the leading leg of the primary bridge always switch under ZVS conditions even at light load. This is due to the fact that the energy available to charge/discharge the output capacitances of the MOSFET's is the energy stored in the leakage inductance of the transformer, in addition to the energy stored in the output

filter inductance. For the lagging leg MOSFET's, the energy available to charge/discharge the output capacitances of the MOSFET's is the energy stored in the leakage inductance of the transformer only. Hence, under a certain load condition, ZVS is lost. It was shown by Sabate [6] that by sizing the leakage inductance of the transformer, the ZVS range of the converter can be extended.

In order to carry out a comparison between the conventional full-bridge PWM converter and the improved topology, the effect of the leakage inductance on the different design parameters will be investigated and compared with the results obtained in the preceding section. The 10 kW converter specifications proposed earlier will also be used for this comparison. Note here that the required transformer turns ratio to obtain the same output voltage is 2:3.

By carrying out a similar analysis to that of Section IV, the effect of leakage inductance on the design of a 10 kW conventional FB-PWM converter is shown in Fig. 9.

Fig. 9(a) shows the effect of leakage inductance on the actual duty cycle of the converter. As the leakage inductance increases, the time required for the secondary diodes to commutate becomes longer and hence the lost duty cycle becomes higher. In addition, a voltage spike on the secondary side occurs after the commutation of the secondary diodes due to the reverse recovery of these diodes. Hence, a snubber circuit is needed to limit this voltage spike. Such a snubber circuit consumes almost 1–2% of the output power [6], [7]. For the above analysis, a 1% loss is assumed to be consumed by such a snubber circuit.

The effect of the leakage inductance on the normalized Q1 rms current, the total normalized losses, in addition to the efficiency of the converter, is shown in Fig. 9(b), (c), and (d), respectively. Unlike the improved topology, increasing the leakage inductance results in reduced rms currents, reduced losses, and hence, higher efficiency. However, for values of d less than 0.3, the efficiency of the improved topology is higher than that of the conventional FB PWM converter.

VII. Simulation Results

Simulation results for a 2 kW converter were obtained using SABER. The converter specifications are 150 V input, 48 V output voltage with 20 kHz switching frequency. Detailed device and diode models were used in simulations (Lauritzen diode model with reverse recovery [8], IGBT's library models, coaxial transformer model, and so on). Fig. 10(a) shows the primary voltage and current. The characteristics of the primary current, where it picks up the secondary filter current before the primary voltage is switched to the other rail, are clearly seen. Fig. 10(b) shows the secondary voltage and filter currents. Note that since the secondary currents have considerably higher ripple, the value of the secondary filters needed are rather small. Fig. 10(c) shows the current and voltage wave forms of one of the secondary diodes. Again, here it is clear that the secondary diodes commutate under zero voltage before the primary voltage is switched to the other rail; hence, no secondary voltage spike occurs when the primary voltage changes polarity.

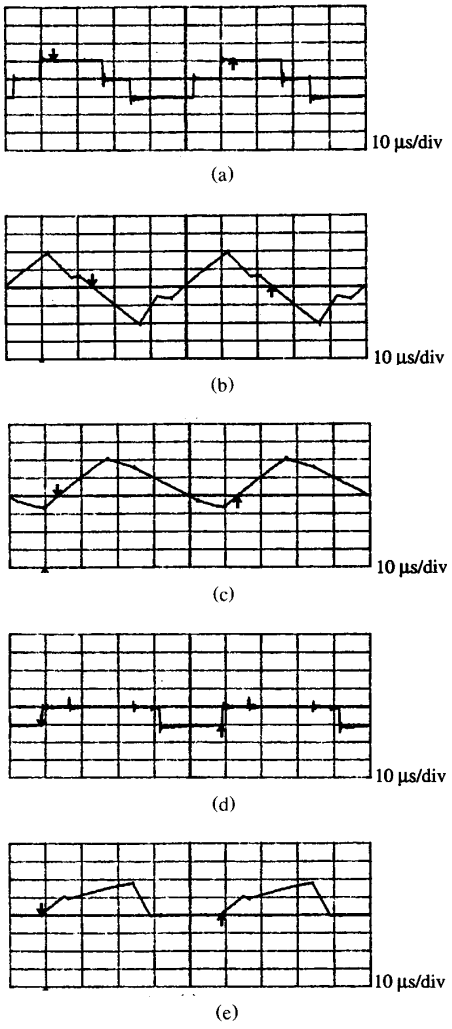

Fig. 11. Experimental results (at 1 kW). (a) Primary voltage (100 V/div). (b) Primary current (20 A/div). (c) Secondary filter current I_1 (20 A/div). (d) Secondary diode voltage (100 V/div). (e) Secondary diode current (20 A/div).

VIII. Experimental Verification

A 2 kW prototype converter was built in the lab to verify the operation of the proposed converter. The converter specifications are the same as those used in the simulations above. IGBT's were used instead of MOSFET's since they were readily available in the lab. The device ratings were 600 V/100 A. For the secondary diodes, 600 V/30 A devices were used. A 1:1 coaxial winding transformer was designed where the leakage inductance was estimated to be on the order of 250 nH. The required secondary filter inductors for a value of d of 0.3 was 30 μH. A phase shift control board was used to provide the required gating signals.

Fig. 11 shows the resultant waveforms for a 1 kW output power. It is clear that the experimental results verify the simulations shown earlier.

The experimental test data obtained were as follows:

$$V_{\text{in}} = 125 \text{ V} \qquad I_{\text{in}} = 16.5 \text{ A} \qquad P_{\text{in}} = 2063 \text{ W}$$

$$V_o = 45.9 \text{ V} \qquad I_o = 40.5 \text{ A} \qquad P_o = 1859 \text{ W}$$

$$\text{Efficiency} = 90.1\%.$$

By carrying out loss calculations, as shown earlier in Section III, the primary device losses were found to be 108 W, while the secondary diodes' losses were computed to be 80 W, a total loss of 188 W. An additional 1% loss is expected for the transformer. This seems to match the obtained experimental data were the losses are about 203 W. In fact, the performance of the converter can be improved substantially by using MOSFET's with low on resistance for the primary devices, while using Schottky diodes on the secondary side.

IX. Conclusions

An improved dc/dc converter topology was presented in this paper. Detailed analyses were conducted with both simulation and experimental results presented. The advantages of the proposed topology include the following.

- Fixed frequency operation with PWM control and minimum VA ratings.
- ZVS for the main devices is achieved using the energy stored in the secondary filter inductors.
- Wide load range with ZVS.
- Utilizes the low leakage inductance of a coaxial winding transformer to achieve soft switching for the secondary diodes.
- No lost duty cycle since the secondary diodes commutate under zero voltage.
- No voltage spike in the secondary circuit due to the soft switching of the secondary diodes.
- Utilizes the circuit parasitic elements effectively.

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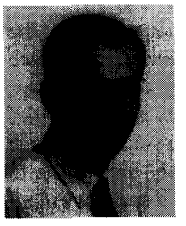

Nasser H. Kutkut (SM'89) received the B.Sc. degree in electrical engineering with honors from Jordan University of Science & Technology, Irbid, Jordan, in 1989, and the M.Sc. degree from the University of Illinois at Chicago in 1990.

Since 1990, he has been working toward the Ph.D. degree at the University of Wisconsin–Madison. His areas of interest are in power electronic converter circuits, high-frequency transformers and magnetics, in addition to electrical machines.

Mr. Kutkut is a member of the IEEE Industry Applications Society and the IEEE Power Electronics Society.

Deepakraj M. Divan (S'78–M'78–S'82–M'83–SM'91), for a photograph and biography, please see page 34 of this issue.

Randal Gascoigne (M'90), for a photograph and biography, please see page 118 of this issue.