ASSOCIATION CONNECTING
ELECTRONICS INDUSTRIES®

IPC-6013A

Amendment 1

Qualification and Performance Specification for Flexible Printed Boards

IPC-6013A
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January 2005

A standard developed by IPC

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- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feedback system on use and problems for future improvement

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- Contain anything that cannot be defended with data

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Qualification and Performance Specification for Flexible Printed Boards

Global Replacement for Dimensional Values

Convert all micrometer (µm) dimensions to millimeter (mm) dimensions. Convert all corresponding micro-inch [µin] dimensions to inch dimensions [in] and limit the accuracy to no more than 5 digits to the right of the decimal point.

Table 1-1 Final Finish, Surface Plating and Coating Thickness Requirements

Replace dimensional values in table as follows (excluding GWB-1 and Immersion Gold which cannot be expressed in inches in less than 6 digits to the right of the decimal point):

Code	Finish	Class 1	Class 2	Class 3
Final Finish				
S	**Solder Coating** over Bare Copper	Coverage and Solderable[5]	Coverage and Solderable[5]	Coverage and Solderable[5]
T	**Electrodeposited Tin-Lead** (fused) (min.)	Coverage and Solderable[5]	Coverage and Solderable[5]	Coverage and Solderable[5]
X	Either Type S or T	As indicated by code		
TLU	**Electrodeposited Tin-Lead Unfused** (min)	0.008 mm [0.00031 in]	0.008 mm [0.00031 in]	0.008 mm [0.00031 in]
G	**Gold Electroplate** (min.) for flexible printed wiring edge connectors and areas not intended to be soldered	0.0008 mm [0.00003 in]	0.0008 mm [0.00003 in]	0.0013 mm [0.00005 in]
GS	**Gold Electroplate** (max.) for areas intending to be soldered	0.0008 mm [0.00003 in]	0.0008 mm [0.00003 in]	0.0008 mm [0.00003 in]
GWB-1	**Gold Electroplate** for areas to be wire bonded (ultrasonic) (min)	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]	0.05 µm [1.97 µin]
GWB-2	**Gold Electroplate** for areas to be wire bonded (thermosonic) (min)	0.0003 mm [0.00001 in]]	0.0003 mm [0.00001 in]]	0.0008 mm [0.00003 in]
N	**Nickel - Electroplate** for Edge Board Connectors (min)	0.002 mm [0.00008 in]	0.0025 mm [0.00010 in]	0.0025 mm [0.00010 in]
NB	**Nickel - Electroplate** as a Barrier to Copper-Tin Diffusion[1] (min)	0.001 mm [0.00004 in]	0.0013 mm [0.00005 in]	0.0013 mm [0.00005 in]
OSP	**Organic Solderability Preservative**	Solderable	Solderable	Solderable
ENIG	**Electroless Nickel**	0.003 mm [0.00012 in] (min)	0.003 mm [0.00012 in] (min)	0.003 mm [0.00012 in] (min)
	Immersion Gold	0.05 µm [1.97 µin] (min)	0.05 µm [1.97 µin] (min)	0.05 µm [1.97 µin] (min)
IS	**Immersion Silver**	Solderable	Solderable	Solderable
IT	**Immersion Tin**	Solderable	Solderable	Solderable
C	**Bare Copper**	As indicated in Table 3-10 and/or 3-11		
Surface and Hole Plating				
Copper [2] (Min. Average)		**Holes**		
	Type 2	0.012 mm [0.00047 in]	0.012 mm [0.00047 in]	0.012 mm [0.00047 in]
	Type 3, 4 ≥ 6 layers	0.025 mm [0.00098 in]	0.025 mm [0.00098 in]	0.025 mm [0.00098 in]
	Type 3, 4 > 6 layers	0.035 mm [0.00138 in]	0.035 mm [0.00138 in]	0.035 mm [0.00138 in]
Copper (Min. Thin Areas[3])				
	Type 2	0.010 mm [0.00039 in]	0.010 mm [0.00039 in]	0.010 mm [0.00039 in]
	Type 3, 4 ≤ 6 layers	0.020 mm [0.00079 in]	0.020 mm [0.00079 in]	0.020 mm [0.00079 in]

Code	Finish	Class 1	Class 2	Class 3
	Type 3, 4 > 6 layers	0.030 mm [0.00118 in]	0.030 mm [0.00118 in]	0.030 mm [0.00118 in]]
Copper (Via Structure[4])		**Blind Vias [4]**		
	(min. average)	0.020 mm [0.00079 in]	0.020 mm [0.00079 in]	0.025 mm [0.00098 in]
	(min. at thin area)	0.018 mm [0.00071 in]	0.018 mm [0.00071 in]	0.020 mm [0.00079 in]
Copper (Via Structure[4])		**Buried Vias**		
	(min. average)	0.013 mm [0.00051 in]	0.015 mm [0.00059 in]	0.015 mm [0.00059 in]
	(min. at thin area)	0.011 mm [0.00043 in]	0.013 mm [0.00051 in]	0.013 mm [0.00051 in]

[1] Nickel plating used under the tin-lead or solder coating for high temperature operating environments act as a barrier to prevent the formation of copper-tin compounds.
[2] Copper plating (1.2.5.2) thickness applies to surface and hole walls.
[3] For Class 3 boards having a drilled hole diameter <0.35 mm [0.0138 in] and having an aspect ratio >3.5:1, the minimum thin area copper plating in the hole **shall** be 0.025 mm [0.00098 in].
[4] Low Aspect Ratio Blind Vias refer to blind vias produced using a controlled depth mechanism (e.g., laser, mechanical, plasma or photo defined). All performance characteristics for plated holes, as defined in this document, **shall** be met.
[5] See also 3.3.5.

2 APPLICABLE DOCUMENTS

Replace IPC-7711, Rework of Electronic Assemblies as follows:

IPC-7711/21A Rework and Repair Guide

3.2.6.2 Electrodeposited Copper

Replace 50 µm - 100 µm [1969 µin - 3937 µin] as follows:

0.05 mm - 0.10 mm [0.00197 in - 0.00394 in]

3.3.1.2 Edges, Flexible Section

Replace 2nd sentence as follows:

Tears **shall not** be allowed in Type 1 or Type 2 flexible printed wiring or within the flexible sections of Type 3 or Type 4.

3.3.2 Construction Imperfections - Rigid

Replace subsection title with "Construction Imperfections"

3.3.2.6 Scratches, Dents and Tool Marks

Replace as follows:

Scratches, dents and tool marks are acceptable, provided they do not expose conductors or disrupt fibers greater than allowed in 3.3.2.4 and 3.3.2.5 and do not reduce the dielectric spacing below the minimum specified. Dents or tool marks that cause delamination, changes physical size of the conductor, or reduces conductor width or spacing **shall** be rejectable.

3.3.2.10 Coverfilm Separations

Replace item c as follows:

There **shall** be no coverfilm nonlamination along the outer edges or covercoat openings of the coverfilm that reduces the seal below minimum edge to conductor spacing.

3.3.2.11.1 Covercoat Coverage

Replace micrometer and micro-inch values in subparagraph e., item a) as follows:

a) On surface mount lands, misregistration **shall not** cause encroachment of the covercoat over the land area greater than 0.050 mm [0.00197 in] for a pitch ≥1.25 mm [0.04921 in]. Encroachment **shall not** exceed 0.025 mm [0.00098 in] for a pitch ≤1.25 mm [0.04921 in], and encroachment may occur on adjacent sides, but not on opposite sides of a surface mount land.

3.4.2 Etched Annular Ring and Breakout (Internal)

Move to 3.7.10, Etched Annular Ring and Breakout (Internal)

3.4.3 becomes 3.4.2 and 3.4.4 becomes 3.4.3 as a result of this transfer. Likewise, the following figure changes take effect:

Figure 3-4 becomes Figure 3-15.

Figure 3-5 through Figure 3-15 become Figure 3-4 through Figure 3-14.

Table 3-5 Minimum Etch Annular Ring

Replace all instances of 50 µm [0.0020 in] with 0.050 mm [0.0020 in]

Replace 150 µm [0.00591 in] with 0.15 mm [0.00591 in]

Internal Plated-through Holes, Class 3, replace as follows:

The minimum internal annular ring[2] **shall** be 0.025 mm [0.00098 in].

Add footnote 2 following Table 3-5 as follows:

2. See 3.7.10 regarding annular ring requirements for functional and nonfunctional lands.

Table 3-6 Allowable Squeeze-Out of Coverlayer Adhesive and Ooze-Out of Covercoat

Replace both instances of 70 µm with 0.070 mm [0.00276 in]

3.7 Structural Integrity

Add the following sentence to the end of the 2nd paragraph:

Refer to IPC-2221 for appropriate coupon design of blind and buried vias for plated hole evaluation.

3.7.1 Thermal Stress Testing

Replace 2nd paragraph as follows:

Following stress, test coupons or production boards **shall** be microsectioned. Microsectioning **shall** be accomplished per IPC-TM-650, Method 2.1.1, or 2.1.1.2 on test coupons or production boards. Evaluation of all applicable holes and vias, including blind and buried, for all such structures found on the finished printed board **shall** be inspected in the vertical cross section in accordance with Table 4-3. The grinding and polishing accuracy of the microsection **shall** be such that the viewing area of each of the holes is within 10% of the drilled diameter of the hole.

3.7.5 Etchback (Type 3 and Type 4 Only)

Replace first sentence as follows:

When specified on the procurement documentation, flexible printed wiring **shall** be etched back for the lateral removal of adhesive, resin and/or glass fibers from the drilled hole wall prior to plating.

Replace 0.003 mm [0.000118 in] with 0.003 mm [0.00012 in] in second sentence

Append at the end of Note as follows:

Adhesiveless constructions exhibit minimal etchback at the flexible dielectric to metal interface.

Table 3-9 Plated-Through Hole Integrity After Stress

Change table title as follows:

Table 3-9 Plated Hole Integrity After Stress

Replace "Wicking" as follows:

Property	Class 1	Class 2	Class 3
Wicking (maximum copper plating penetration including 0.08 mm [0.00315 in] etchback allowance)	0.205 mm [0.00807 in], provided the additional microsection criteria of 3.7.8.1 are met	0.18 mm [0.00709 in], provided the additional microsection criteria of 3.7.8.1 are met	0.16 mm [0.00630 in], provided the additional microsection criteria of 3.7.8.1 are met
Wicking (maximum copper plating penetration including 0.05 mm [0.0020 in] smear removal allowance)	0.175 mm [0.00689 in], provided the additional microsection criteria of 3.7.8.1 are met	0.15 mm [0.00591 in], provided the additional microsection criteria of 3.7.8.1 are met	0.13 mm [0.00512 in], provided the additional microsection criteria of 3.7.8.1 are met

Replace "Plating Separation" as follows:

Plating Separation	Allowed at knee, maximum length 0.125 mm [0.00492 in]	None Allowed

3.7.8 Plating Integrity

Add new section 3.7.8.1 for wicking as follows:

3.7.8.1 Wicking (Copper Plating) When Etchback is specified on the master drawing, the maximum copper plating penetration, when measured from the edge of the drilled hole, **shall not** exceed the values in Table 3-9, which is the sum of copper wicking and etchback allowances (see Figure 3-12), or **shall not** violate the minimum conductor spacing below the minimum requirements in 3.5.2. See also 3.7.10.2 regarding minimum conductor spacing.

When Etchback is not specified on the master drawing (smear removal only), the maximum copper plating penetration, when measured from the edge of the drilled hole, **shall not** exceed the values in Table 3-9, which is the sum of copper wicking and smear removal allowances (see Figure 3-13), or **shall not** violate the minimum conductor spacing below the minimum requirements in 3.5.2).

3.7.10 Annular Ring (Internal)

Replace as follows:

3.7.10 Etched Annular Ring and Breakout (Internal)

Internal annular ring **shall** be measured by microsection to verify conformance to Table 3-5 as shown in Figure 3-15.

Note: The board design may have nonfunctional lands of varying sizes for conductor routing spacing constraints. The functional lands **shall** meet the minimum annular ring requirement. Non-functional lands which are less than the functional land diameter are not required to meet the minimum annular ring requirement.

Measurements for internal annular ring are from the inside of the drilled hole to the edge of the internal land as shown in Figure 3-15. Negative etchback is evaluated per 3.7.7 and Figure 3-14. External pads of vias produced as sequentially laminated structures may be evaluated inprocess prior to additional lamination(s) (see 3.4.2). When sequentially produced vias are evaluated in-process their compliance **shall** be documented. Lands not associated with a sequential via structure **shall** be evaluated as internal annular ring at microsection. Microsection analysis is performed per 3.7.2 (see Figures 3-5 and 3-6). Unless prohibited by the customer, the employment of filleting or ''tear drops'' to create additional land area at the conductor junction **shall** be acceptable for Class 1 and 2 and in accordance with general requirements for lands with holes detailed in IPC-2221. Employment of filleting or ''tear drops'' in Class 3 product **shall** be as agreed upon between user and supplier.

Note: Consideration should be given to how the microsection cut is ''clocked,'' or rotated. Misregistration can occur randomly as opposed to orthogonally and therefore an orthogonal cut will not guarantee that a microsection view will portray hole breakout, if it exists. See Figures 3-16 and 3-17 for an example of how breakout may or may not be detected within a microsection based on the rotation.

Add new section 3.7.10.1 for internal registration assessment for Class 2 product as follows:

3.7.10.1 Internal Registration Assessment (Class 2) For Class 2 boards, if internal annular ring breakout is detected in the vertical cross section, but the degree of breakout cannot be determined, internal registration may be assessed by nondestructive techniques other than microsection, such as, special patterns, probes, and/or software, which are configured to provide information on the interpolated annular ring remaining and pattern skew. Techniques include, but are not limited to the following:

- The optional F coupon.
- Custom designed electrically testable coupons.
- Radiographic (x-ray) techniques.
- Horizontal microsection.
- CAD/CAM data analysis as correlated to pattern skew by layer.

Note: Microsectioning or statistical sampling **shall** be used to verify correlation of the approved technique, and a calibration standard established for the specific technique employed.

Add new 3.7.10.2 for breakout conditions as follows:

3.7.10.2 Breakout (Internal) Conditions If misregistration to the point of breakout is detected in vertical microsections, the concerns are that:

1. The conductor width minimum may be compromised at the land junction and,
2. There is insufficient electrical spacing.

Note: Electrical spacing may be further compromised due to the combined copper plating penetration of both etchback and wicking.

The extent and direction of misregistration **shall** be determined. Actual boards or appropriate test coupons **shall** then be tested to determine compliance. This may be accomplished by the techniques listed in 3.7.10.

Figure 3-12 Negative Etchback

Replace metric and inch dimensions as follows:

Class 1 - 0.025 mm [0.00098 in]
Class 2 - 0.025 mm [0.00098 in]
Class 3 - 0.013 mm [0.00051 in]

Figure 3-13 Etchback Depth Allowance

Renumber as Figure 3-12 and replace as follows:

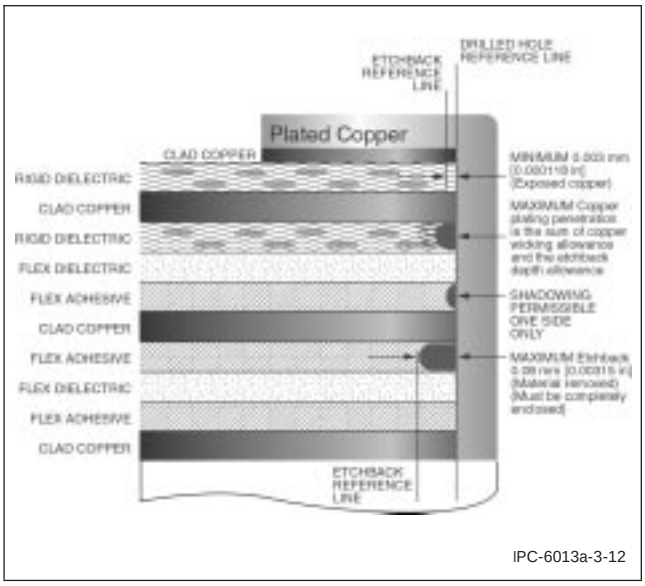

Figure 3-12 Etchback Depth Allowance

Figure 3-14 Smear Removal Allowance

Renumber as Figure 3-13 and replace as follows:

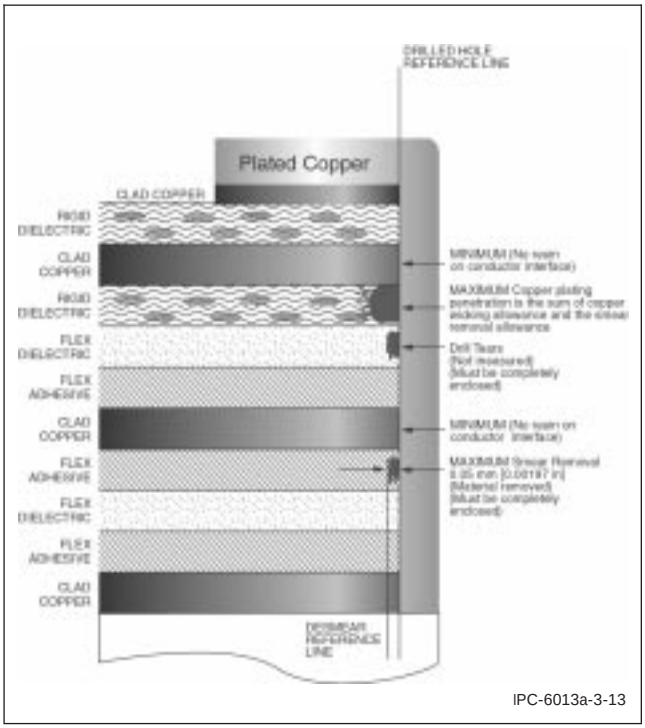

Figure 3-13 Smear Removal Allowance

Add new Figure 3-16:

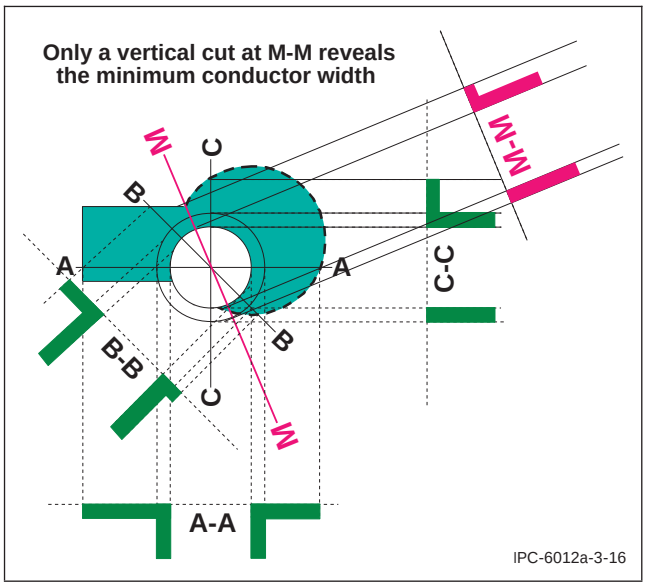

Figure 3-16 Microsection Rotations for Breakout Detection

Add new Figure 3-17:

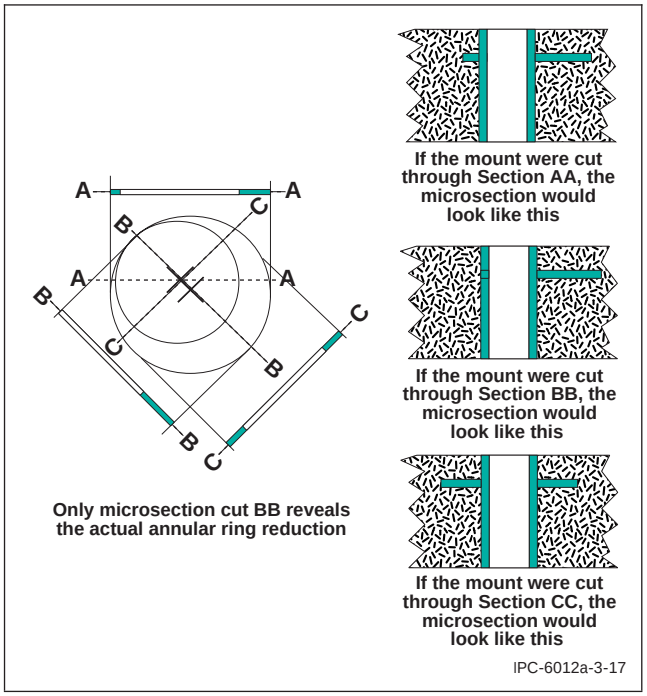

Figure 3-17 Comparison of Microsection Rotations

Table 3-10 Conductor Thickness after Processing

Rename and replace table as follows:

Table 3-10 Internal Layer Foil Thickness after Processing

Weight	Absolute Cu Min. (IPC-4562 less 10% reduction) (mm) [in]	Maximum Variable Processing Allowance Reduction* (mm) [in]	Minimum Final Finish after Processing (mm) [in]
1/8 oz. [0.0051]	0.0046 [0.00018]	0.0015 [0.00006]	0.0031 [0.00012]
1/4 oz. [0.0085]	0.0070 [0.00030]	0.0015 [0.00006]	0.0062 [0.00024]
3/8 oz. [0.012]	0.0108 [0.00043]	0.0015 [0.00006]	0.0093 [0.00037]
1/2 oz. [0.0171]	0.0154 [0.00061]	0.0040 [0.00016]	0.0114 [0.00045]
1 oz. [0.0343]	0.0309 [0.00122]	0.0060 [0.00024]	0.0249 [0.00098]
2 oz. [0.0686]	0.0617 [0.00243]	0.0060 [0.00024]	0.0557 [0.00219]
3 oz. [0.1029]	0.0926 [0.00365]	0.0060 [0.00024]	0.0866 [0.00341]
4 oz. [0.1372]	0.1235 [0.00486]	0.0060 [0.00024]	0.1175 [0.00463]
Above 4 oz. [0.1372]	IPC-4562 value less 10% reduction	0.0060 [0.00024]	0.0060 [0.00024] below minimum thickness of calculated 10% reduction of foil thickness in IPC-4562

* Process allowance reduction does not allow for rework processes for weights below 1/2 oz. For 1/2 oz. and above, the process allowance reduction allows for one rework process.

Table 3-11 External Conductor Thickness after Plating

Replace table as follows:

Table 3-11 External Conductor Thickness after Plating

Weight[1]	Absolute Cu Min. (IPC-4562 less 10% reduction) (mm) [in]	Plus minimum plating for Class 1 and 2 (0.020 mm) [0.00079 in][2]	Plus minimum plating for Class 3 (0.025 mm) [0.00098 in][2]	Maximum Variable Processing Allowance Reduction[3] (mm) [in]	Minimum Surface Conductor Thickness after Processing (mm) [in]	
					Class 1 & 2	Class 3
1/8 oz.	0.0046 [0.00018]	0.0246 [0.00097]	0.0296 [0.00117]	0.0015 [0.00006]	0.0231 [0.00091]	0.0281 [0.00111]
1/4 oz.	0.0070 [0.00030]	0.0277 [0.00109]	0.0327 [0.00129]	0.0015 [0.00006]	0.0262 [0.00103]	0.0312 [0.00123]
3/8 oz.	0.0108 [0.00043]	0.0308 [0.00121]	0.0358 [0.00141]	0.0015 [0.00006]	0.0293 [0.00115]	0.0343 [0.00135]
1/2 oz.	0.0154 [0.00061]	0.0354 [0.00139]	0.0404 [0.00159]	0.0020 [0.00008]	0.0334 [0.00132]	0.0384 [0.00151]
1 oz.	0.0309 [0.00122]	0.0509 [0.00200]	0.0559 [0.00220]	0.0030 [0.00012]	0.0479 [0.00189]	0.0529 [0.00208]
2 oz.	0.0617 [0.00243]	0.0817 [0.00322]	0.0867 [0.00341]	0.0030 [0.00012]	0.0787 [0.00310]	0.0837 [0.00320]
3 oz.	0.0926 [0.00365]	0.1126 [0.00443]	0.1176 [0.00463]	0.0040 [0.00016]	0.1086 [0.00428]	0.1136 [0.00447]
4 oz.	0.1235 [0.00486]	0.1435 [0.00565]	0.1485 [0.00585]	0.0040 [0.00016]	0.1395 [0.00549]	0.1445 [0.00569]

1. Starting foil weight of design requirement per procurement documentation.
2. Process allowance reduction does not allow for rework processes for weights below 1/2 oz. For 1/2 oz. and above, the process allowance reduction allows for one rework process.
3. Reference: Min. Cu Plating Thickness
   Class 1 = 2 (0.020 mm) [0.00079 in] Class 2 = 2 (0.020 mm) [0.00079 in] Class 3 = (0.025 mm) [0.00098 in]

3.9.2.2 Isolation (Circuit Shorts)

Replace last sentence in 2nd paragraph as follows:

When automated test equipment is used, the minimum applied voltage **shall** be the maximum rated voltage of the flexible printed wiring. When not specified, the default value of 40 volts **shall** be used.

4.1 Qualification

Add the following 3rd sentence to the paragraph:

Qualification should include those applicable tests as referenced in Tables 4-3 and 4-4.

Table 4-3 Acceptance Testing and Frequency

Replace Dimensional Requirements as follows:

Dimensional Requirements							
Dimensional: Flexible Printed Wiring	3.4	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Board
Hole Size and Hole Pattern Accuracy	3.4.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Board
Etched Annular Ring (External)	3.4.2	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Board
Solderable Annular Ring (External)	3.4.2.1	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Board
Bow and Twist (Individual Board or Stiffener Portion Only)	3.4.3	X		Sample (6.5)	Sample (4.0)	Sample (4.0)	Per Board

Replace Structural Integrity After Stress Types 3-4 (Microsection) as follows:

Structural Integrity After Stress Types 3-4 (Microsection)[6]							
Laminated Integrity	3.7.3 3.7.4		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel
Etchback (Type 3 and Type 4 Only)	3.7.5 3.7.6 3.7.7		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel
Plating Integrity	3.7.8		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel
Plating Voids	3.7.9		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel
Annular Ring (Internal)	3.7.10		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Twice per panel, opposite corners 3,5
Plating/Coating Thickness	3.7.11		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel
Minimum Layer/Copper Foil Thickness	3.7.12		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel
Minimum Surface Conductor Thickness	3.7.13		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel
Metal Cores	3.7.14		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel
Dielectric Thickness	3.7.15		A and B or A/B	Sample (2.5)	Sample (1.5)	Sample (1.0)	Per panel

Replace Structural Integrity After Stress Type 2 (Microsection) as follows:

Structural Integrity After Stress Type 2 (Microsection)[6]							
Laminate Integrity (Flexible)	3.7.3		A or B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Plating Integrity	3.7.8		A or B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Plating Voids	3.7.9		A or B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Plating/Coating Thickness	3.7.11		A or B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Minimum Surface Conductor Thickness	3.7.13		A or B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel
Dielectric Thickness	3.7.15		A or B or A/B	Sample (6.5)	Sample (4.0)	Sample (2.5)	Per panel

Add footnote 3 following Table 4-3:

3. For class 2 product, the degree of breakout following evaluation of vertical cross sections may be assessed by methods other than horizontal microsection.

Add footnote 5 following Table 4-3:

5. The A and B or 2 A/B test coupons **shall** be taken from opposite corners of the manufacturing panel and in opposing axes (one in the ''x'' axis and the other in the ''y'' axis).

Add footnote 6 following Table 4-3:

6. All via structures **shall** be represented in the thermally stressed evaluations.

Table 4-4 Quality Conformance Testing

Replace as follows:

Inspection	Requirement and Method Section	Test Coupon		Test Frequency		
		Type 1, 5	Type 2 - 4	Class 1	Class 2	Class 3
Rework Simulation	3.8		B or A/B	As required	Two coupons per QTR	Two coupons per month
Bond Strength (Unsupported Lands)	3.6.3	B or A/B	As required	As required	Two coupons per QTR	Two coupons per month
Bond Strength (Stiffener)	3.6.4	Board	Board	As required	As required	As required
Dielectric Withstanding Voltage	3.9.1	E	E	As required	Two coupons per QTR	Two coupons per month
Moisture and Insulation Resistance	3.10.1	E	E	Maintain electrical function	Two coupons per QTR	Two coupons per month

5.2 Superceded Specifications

Replace as follows:

This specification supersedes and replaces IPC-6013A, IPC-FC-250 and IPC-RF-245.