Power Factor Correction With Flyback Converter Employing Charge Control[1]

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Abstract -- **In this paper, charge control concept is applied to a flyback converter for the purpose of power factor correction (PFC). Using charge control, a flyback converter can operate in continuous conduction-mode (CCM) with unity power factor. The simplicity of the flyback circuit is maintained and the power handling capacity is increased. The properties of charge control related to flyback PFC application are studied. The design guidelines are presented. A 200 W prototype circuit was built, and the experiment results show good prospects of application.**

I. INTRODUCTION

Due to the ever-increasing requirement for improved power quality, The use of power factor correction (PFC) circuit for off line power supplies have been dramatically increased. A variety of circuit topologies and control methods have been developed for the PFC application [1, 2, 3, 4]. Although both boost and flyback converters are capable for PFC applications, the boost converter finds more usage than the flyback converter, partly because the existing control methods make it easier to control the average inductor current than the average switch current.

For low power applications, the flyback converter is more attractive than the boost converter because of its simplicity. It provides the isolation, start-up, and short-circuit protection by a single switch. Also, the line voltage is not necessarily lower than the output voltage, as in the boost converter case. The main difficulty in flyback PFC circuits is the control of the average input current when it operates in continuous-conduction mode (CCM). When flyback converter operates in discontinuous-conduction mode (DCM), a unity power factor can be achieved by using a simple constant on-time control [5]. But the DCM operation significantly increases the conduction loss and the current stress on the switch. It also increases the size and weight of the EMI filter.

Charge control [6] can control the average switch current of any PWM converter operating in CCM. By employing charge control, a flyback converter operating in CCM can achieve a unity power factor. An attempt to control a flyback converter operating in CCM as a PFC circuit can also be found in [7]. The control method discussed is basically the same as charge control. The simulation results given by [7] reveal that this control can achieve a very high power factor. But the problems of this control, such as subharmonic oscillation and its relation with line current distortion, are not discussed. No experiment results are given in [7]. The idea of controlling the input charge of the flyback converter to achieve PFC can also be found in [8], where instead of using a capacitor as the low-frequency energy storage element, the silicon-iron inductor is used to store the low-frequency energy. This method has little practical use.

Subharmonic oscillation exists in charge control and is line and load dependent [6]. It can be eliminated by adding an external ramp. But adding an external ramp introduces line current distortion. Hence there exists a trade-off between subharmonic oscillation and line current distortion.

This paper studies the properties of charge control related to the flyback PFC application. A flyback PFC circuit operating in CCM was designed and built. The experiment results, which include line current waveform, measured efficiency, and power factor are also given in this paper.

II. PROPERTIES OF CHARGE CONTROL

In this section, the properties of charge control, especially those related to PFC applications, are reviewed. The circuit diagram and key waveforms of a flyback converter employing charge control are shown in Fig. 1. The main switch, S1, turns on at the beginning of each switching cycle, and

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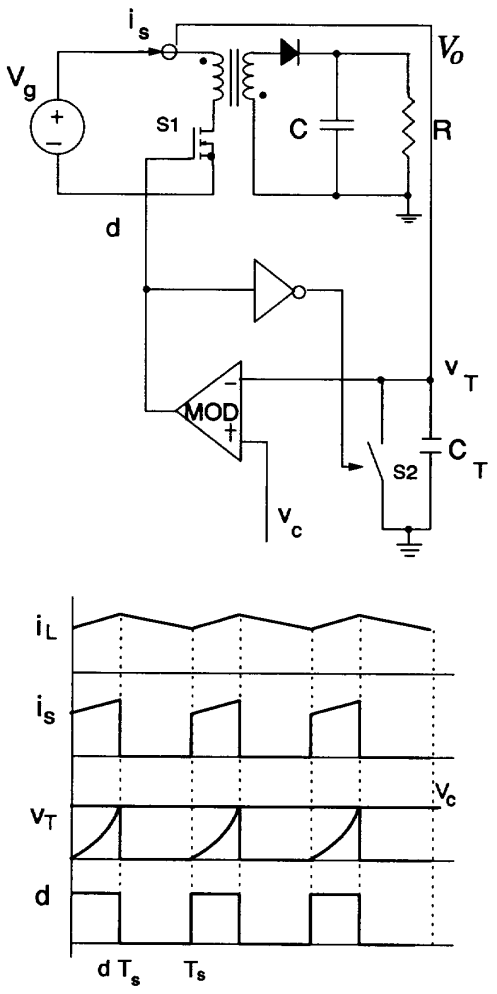

Figure 1. Charge Control Scheme and Key Waveforms: (a) A flyback converter with charge control. (b) Key waveforms of charge control. Voltage, v_T, is proportional to average input current of the flyback converter.

switch S2 turns off at the same time. The switch current, i_s, is sensed and charged to capacitor C_T. When v_T, the voltage across capacitor C_T, reaches control voltage, v_c, S1 turns off, and S2 turns on to discharge C_T. Voltage v_T represents the total charge of the switch current in one switching cycle. For constant frequency operation, it is proportional to the average value of the switch current.

As stated previously, subharmonic oscillation in charge control is line and load dependent. For a PFC circuit, the line voltage varies from zero to its

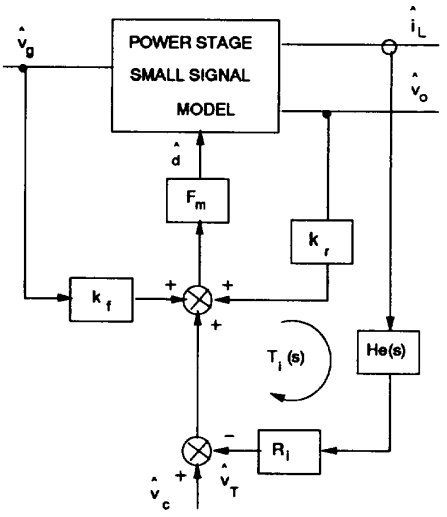

Figure 2. Small-Signal Model of PWM Converter with Charge Control: The power stage of the PWM converter can be replaced by any existing small-signal model. F_m, R_i and $H_e(s)$ are independent of converter topologies.

peak value during one line cycle. Hence subharmonic oscillation cannot be avoided if no external ramp is added to the system. To study the unstable problem, the current loop gain of flyback converter with charge control needs to be analyzed. The small-signal model of PWM converter with charge control is shown in Fig. 2. From Fig. 2 the current loop gain of PWM converter with charge control is as follows:

$$T_i(s) = F_m R_i G_{id}(s) H_e(s). \quad (1)$$

where F_m, R_i, and $H_e(s)$ are modulator gain, current gain, and sampling gain of charge control [6], respectively. $G_{id}(s)$ is the power stage duty cycle-to-inductor current transfer function. In PFC case, $G_{id}(s)$ varies during the line cycle since the input voltage of the converter is the rectified line voltage. $G_{id}(s)$ can be determined by using quasi-static approach [9], i.e., the line voltage is assumed constant within each switching cycle. The derived $G_{id}(s)$ is a function of line voltage. For a flyback converter, the low-frequency portion of $G_{id}(s)$ varies with the line voltage. However, the high-frequency portion of it is independent of line voltage. Since the low-frequency portion does not affect the stability of the current loop, a similar approach as in [10] is taken here to obtain a simplified duty cycle-to-inductor current gain $G^s_{id}(s)$, which is accurate at high frequency for a flyback converter:

$$G^s_{id}(s) = \frac{V_o}{DsL}. \quad (2)$$

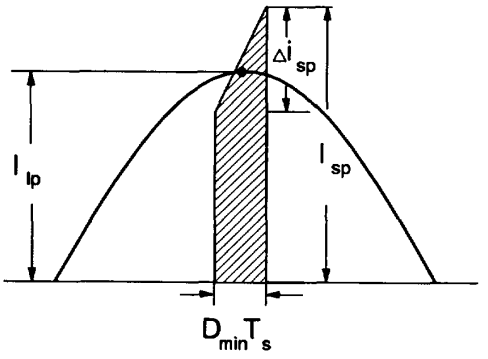

Figure 4. The Relationship Between Peak Line Current and Switch Current: The average switch current in one switching cycle (the shadowed area divided by T_s) equals the instantaneous line current at the time the switching cycle occurs.

$$V_{DS} = V_{lp,\,max} + NV_o, \tag{10}$$

and

$$V_D = V_o + \frac{V_{lp,\,max}}{N}, \tag{11}$$

where V_{DS} is the drain-to-source voltage stress, and V_D is the voltage stress of the rectifier diode. For the given line and output voltage, N is selected to be 2 so that a Schottky diode can be used.

After the turns ratio N is determined, the minimum duty cycle can be determined as follows:

$$D_{min} = \frac{V_o}{V_o + \dfrac{V_{lp,\,max}}{N}}. \tag{12}$$

Figure 4 relates the peak line current with the peak switch current and inductance L. Since the peak line current occurs at the time when the duty cycle reaches its minimum:

$$I_{lp} = \frac{1}{T_s}\int_0^{D_{min}T_s} i_s dt, \tag{13}$$

where I_{lp} is the peak line current. For a constant output power, the maximum peak line current occurs when the line voltage is at its minimum value. From power balance:

$$I_{lp,max} = \frac{\sqrt{2}\,P_o}{V_{lrms,\,min}\,\eta}, \tag{14}$$

where $I_{lp,\,max}$ is the maximum peak line current, $V_{lrms,\,min}$ is the minimum line rms voltage, P_o is the output power, and η is the efficiency. If η equals 0.85, $I_{lp,\,max} = 3.9A$.

To determine parameters L and $I_{sp,\,max}$, another equation is needed in addition to Eq. (13). To obtain this equation, assume:

$$\Delta i_{sp,\,max} = \frac{1}{3} I_{sp,\,max}, \tag{15}$$

where

$$\Delta i_{sp,\,max} = \frac{V_{lp,\,min}}{L} D_{min} T_s. \tag{16}$$

From Eqs. (13) and (15), L and $I_{sp,\,max}$ can be obtained:

$$I_{sp,\,max} = \frac{6}{5}\frac{I_{lp,\,max}}{D_{min}}, \tag{17}$$

$$L = \frac{5}{2}\frac{V_{lp,\,min} D_{min}^2 T_s}{I_{lp,\,max}}. \tag{18}$$

For given N, line range, and output power:

$I_{sp,\,max} = 11.7A$,

$L = 273\mu H$.

As discussed in the previous section, subharmonic oscillation cannot be avoided over the entire line cycle if no external ramp is added, and adding an external ramp introduces line current distortion. Though the dc off-set can partially solve this distortion problem when the converter operates at full load [10], it complicates circuit design (adding an external ramp as well as dc off-set). It is known from previous discussions that subharmonic oscillation occurs only in the time duration where the peak switch current is small, and large magnetizing inductance will reduce this duration. Hence in the practical design the inductor is selected about two times larger than the value given by Eq. (18), and no external ramp is added to the system. The experiment results show that subharmonic oscillation exists only in a very small duration near the line zero crossing. It has no effect on the system behaviors.

To close the voltage loop, the small-signal characteristics of the voltage loop of flyback PFC need to be studied. The average small-signal model derived for the boost PFC circuit [11] is also valid for the flyback case, since the derivation does not relate to converter topologies. It can be seen from [11] that the control-to-output voltage transfer function of the PFC circuit with resistance is as follows:

The modulator gain of charge control with external ramp added is as follows [6]:

$$F_m = \frac{D}{(I_L(DT_s) + S'_e C_T)R_i}, \quad (3)$$

where $I_L(DT_s)$ is the peak inductor current,

$$S'_e = S_e - S_L, \quad (4)$$

and S_e is the external ramp slope. S_L is the slope of the scaled line reference, which varies from positive to negative during half of the line cycle [10].

The expression of $H_e(s)$ for charge control can also be found from [6]:

$$H_e(s) = 1 + \frac{s}{\omega_n Q_n} + \frac{s^2}{\omega_n^2}, \quad (5)$$

where

$$\omega_n = \frac{\pi}{T_s}, \quad (6)$$

$$Q_n = -\frac{2}{\pi}. \quad (7)$$

From Eqs. (1), (2), (3), and (5), the current loop gain of the flyback converter with charge control is obtained:

$$T_i(s) = \frac{K_I}{s}\left(1 + \frac{s}{\omega_n Q_n} + \frac{s^2}{\omega_n^2}\right), \quad (8)$$

where

$$K_I = \frac{V_o}{(I_L(DT_s) + S'_e C_T)L}. \quad (9)$$

It can be seen from Eq. (8) that the current loop gain is formed by two parts, an integration and a pair of right-half-plane zeros centered at half of the switching frequency. A set of current loop gain of charge control is shown in Fig. 3, with integrator gain, K_I, as the running parameter. It can be seen from Eq. (9) that a small $I_L(DT_s)$ produces large K_I, which results in a small or even negative phase margin of the current loop. This phenomenon indicates that subharmonic oscillation can be seen near the line voltage zero crossing region, where the peak switch current is smaller. On the other hand, adding an external ramp (increasing S'_e) or increasing the magnetizing inductance, L, will reduce K_I and increase the phase margin of the current loop.

Line current distortion will occur when an external ramp is added. If there is no external ramp, the line current follows line reference exactly. When an external ramp is added, the line current follows the line reference, subtracting $S_e DT_s$. The distortion is more severe near the line voltage zero crossing, since in that region the line current is comparable to or even smaller than $S_e DT_s$. There exists a trade-off between the line current distortion and the subharmonic oscillation range. Reducing the oscillation range increases line current distortion.

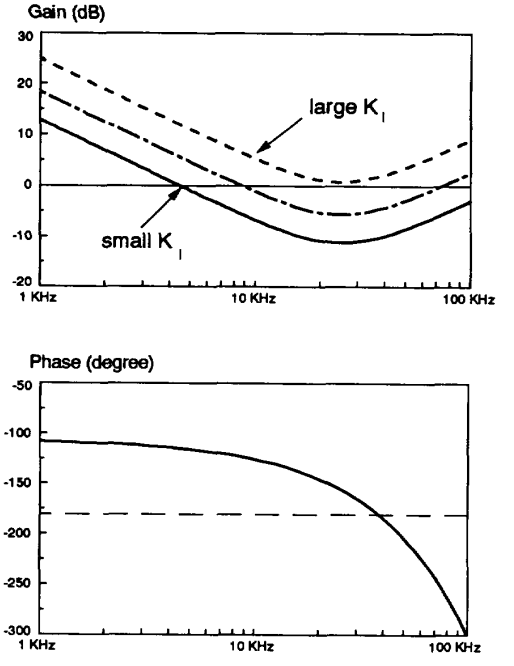

Figure 3. Simplified Current Loop Gain of Flyback PFC with Charge Control: The gain characteristics increase as integrator gain, K_I, decreases, while the phase characteristics remain the same.

III. HARDWARE IMPLEMENTATION

A 200 W flyback converter with charge control was built. The line voltage range is 85 to 140 V, output voltage is 40 V, and switching frequency is 45 kHz. The main task of the power stage design is the design of the flyback transformer. Selecting bulk capacitor is similar to that for boost PFC circuits and is not described here.

In order to design a flyback transformer, the turns ratio, N, the magnetizing inductance, L, and the maximum peak switch current, $i_{sp,max}$ (which equals peak inductor current in PWM converters), need to be determined according to given parameters and line/load conditions. The turns ratio is determined by the maximum voltage stresses on the main switch and the rectifier diode:

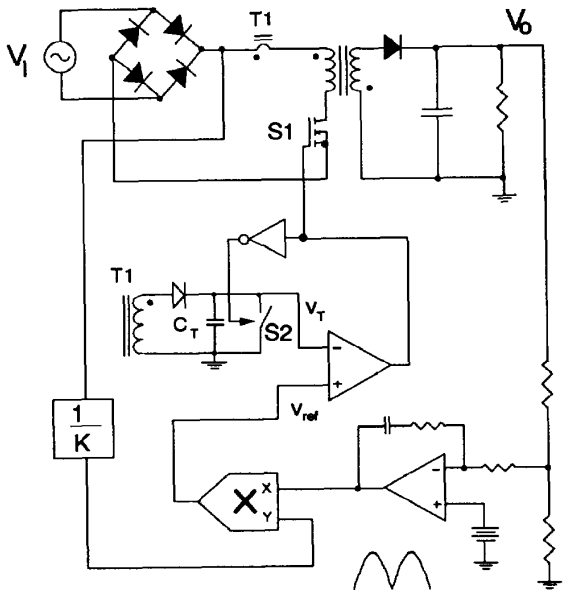

Figure 5. Power Stage and Control Circuit of Flyback PFC with Charge Control: S1 turns on at the beginning of the switching cycle. The switch current, i_s, is sensed by current transformer T1 and used to charge C_T. When v_T reaches v_{ref}, S1 turns off, and S2 turns on to discharge C_T.

$$G_{vc}(s) = \frac{V_i}{kM} \frac{R_L}{2(1 + \frac{CR_L}{2} s)}, \qquad (19)$$

where k is the line reference scaling factor, M is the conversion ratio of the converter, R_L is the load resistance, and C is the output filter capacitance. An integral-lead network provides the optimum voltage loop compensation. The zero of the compensator should be placed at the same frequency as the pole in Eq. (19).

The flyback PFC with control circuit is shown in Fig. 5. A scaled line reference is generated by line voltage and control voltage derived from the voltage feedback loop. The input charge is compared to the reference to generate PWM control. The value of C_T determines the height of voltage v_T, and it should not exceed the comparator saturation voltage.

The rectified line voltage and the line current of the experimental circuit are shown in Fig. 6. The efficiency versus output power characteristics are

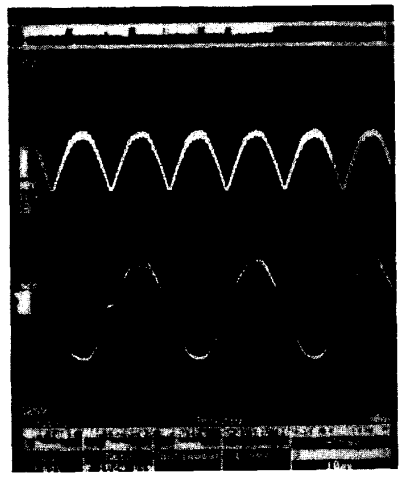

Figure 6. Oscillograms of the Rectified Line Voltage and the Line Current Waveforms: The upper curve is the rectified line voltage, and the lower curve is the line current.

shown in Fig. 7. The efficiency is above 0.87 from half load to full load at high line condition. The power factor is also measured using an ac power analyzer (Voltech PM1000). It is 0.992 at half load and 0.995 at full load.

IV. SUMMARY

In this paper, the application of charge control to a flyback converter for the purpose of PFC is studied. The flyback PFC circuit has the following advantages: 1) the power stage circuit is very simple; 2) the output voltage can be higher or lower than input voltage; and 3) isolation, start up and short-circuit protection problems are solved. The trade-off between the subharmonic oscillation region and line current distortion is also studied. The external ramp canbe avoided. By properly increasing the magnetizing inductance, the subharmonic oscillation can be limited to a very small region, and no line current distortion will be introduced.

The built flyback PFC circuit almost achieves unity power factor (0.995). Due to its simplicity in both power stage and control circuit, this circuit will find applications in the future.

The limitation of the flyback PFC is the output power level. When the output power increases, both voltage and current stresses increase. The

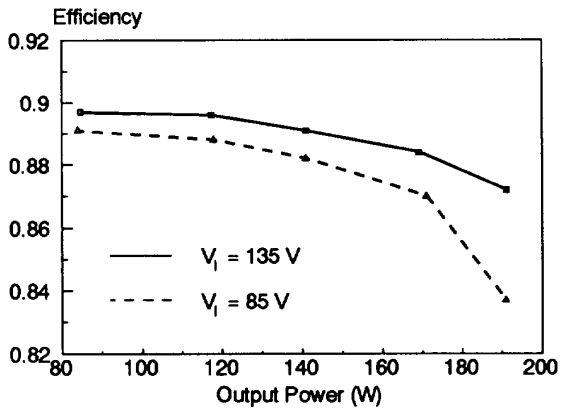

Figure 7. Efficiency Characteristics of Flyback PFC versus Line Voltage and Output Power: The solid line represents the efficiency at high line, and the dotted line represents the efficiency at low line.

leakage energy also increases, which in turn dramatically increases the voltage stress on the switch. It turns out that recovering or dissipating this energy is the key issue of a high output power and high efficiency flyback PFC circuit. Several techniques which can increase the output power of flyback PFC are under studying. By using active clamp technique, a single flyback can output 300 W power while has a 90 percent efficiency at low line. By interleaving two or more power stages, large output power can be achieved and the input current ripple is reduced in the same time.

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