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LM5109

100V, 1A Half Bridge Gate Driver

The LM5109 is a low cost high voltage gate driver, designed to drive both the high side and the low side N-Channel MOSFETs in a synchronous buck or a half bridge configuration. The floating high-side driver is capable of working with rail voltages up to 100V. The outputs are independently controlled with TTL compatible input thresholds. A robust level shifter technology operates at high speed while consuming low power and providing clean level transitions from the control input logic to the high side gate driver. Under-voltage lockout is provided on both the low side and the high side power rails. The device is available in the SOIC - 8 packages.

Features

- Drives high side and low side N-Channel MOSFET
- Independent TTL compatible inputs
- Bootstrap supply voltage to 118V DC
- Fast propagation times (25nsec typical)
- Drives 1000pF loads with tbd ns rise and fall times
- Excellent propagation delay matching (3nsec typical)
- Supply rail under-voltage lockout
- Low power consumption

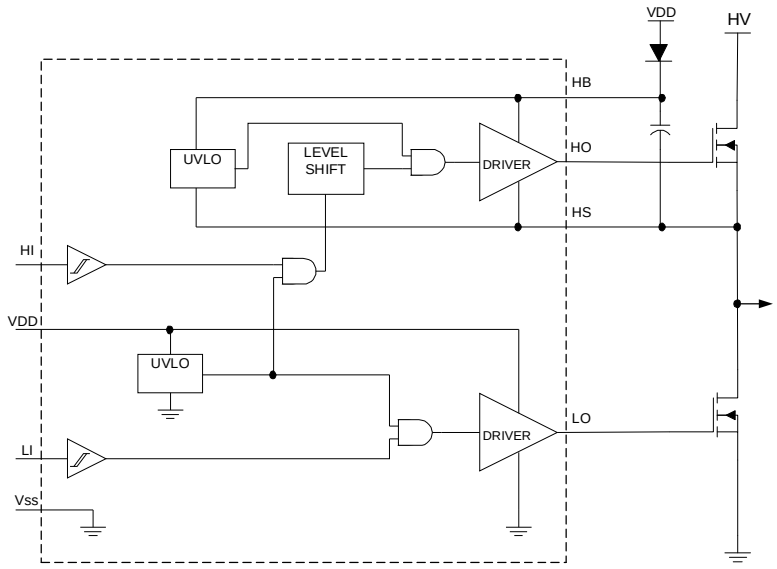
Typical Applications

- Current Fed push-pull power converters
- Half Bridge & Full Bridge power converters
- Solid state motor drives
- Two switch forward power converters

Package

- SOIC – 8

Simplified Block Diagram



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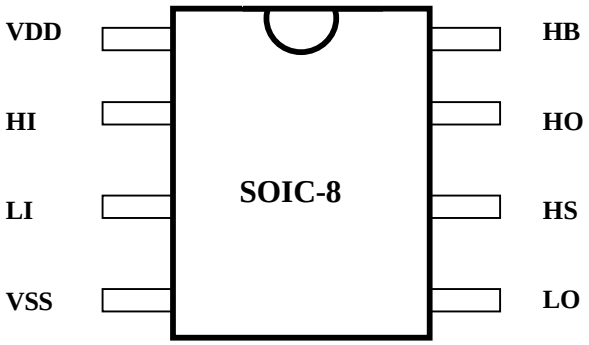
Connection Diagrams



Ordering Information

Ordering Number	Package Type	NSC Package Drawing	Supplied As
LM5109 M	SOIC 8	M08A	Shipped in anti static rails
LM5109 MX	SOIC 8	M08A	2500 shipped in Tape &Reel

Pin Descriptions

NAME		DESCRIPTION	APPLICATION INFORMATION
1	VDD	Positive ground referenced supply	Locally decouple to Vss using low ESR/ESL capacitor, placed as close to IC as possible.
2	HI	High side control input	The HI input is compatible with TTL input thresholds. If unused, the HI input should be tied to VDD or VSS and not left open.
3	LI	Low side control input	The LI input is compatible with TTL input thresholds. If unused, the LI input should be tied to VDD or VSS and not left open.
4	VSS	Ground reference	All signals are referenced to this ground.
5	LO	Low side gate driver output	Connect to low side N-MOS gate.
6	HS	High side source connection	Connect to bootstrap capacitor negative. Connect to the source of the high side NMOS device.
7	HO	High side gate driver output	Connect to high side NMOS gate.
8	HB	High side gate driver positive supply rail.	Connect positive side of bootstrap capacitor to this pin. Connect negative side of bootstrap capacitor to HS. Bootstrap capacitor should be placed as close to IC as possible.

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Absolute Maximum Ratings (note 1)

If Military /Aerospace specified devices are required, please contact the National Semiconductor Sales Office / Distributors for availability and specifications.

V_{DD} to V_{SS}	0.3 to 18V
V_{HB} to V_{HS}	-0.3 to 18V
LI or HI Inputs to V_{SS}	-0.3 to V_{DD}+ 0.3V
LOto V_{SS}	-0.3 to V_{DD}+ 0.3V
Voltage on HO	V_{HS} – 0.3 to V_{HB} + 0.3
V_{HS} to V_{SS}	-1 to 100V
V_{HB} to V_{SS}	118V
Junction Temperature	-40 to +150°C
Storage Temperature Range	-55 to +150°C
ESD Rating HBM (note2)	1KV

Recommended Operating Conditions

V_{DD}	**+7.5V** to +14V
HS	-1V to 100V
HB	V_{HS} + 8V to V_{HS} + 14V
HS Slew Rate	<50V/ns
Junction Temperature	-40 to +125°C

ELECTRICAL CHARACTERISTICS:

Specifications in standard typeface are for T_J = +25°C, and those in **boldface** apply over the full **operating temperature range** T_J = -40 to 125°C**,**
Unless otherwise specified V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO. (note 4)

PARAMETERS	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENTS						
V_{DD} Quiescent Current	I_{DD}	LI = HI = OV	-	0.3	**0.6**	mA
V_{DD} Operating Current	I_{DDO}	f = 500kHz	-	1.5	**3**	mA
Total HB Quiescent Current	I_{HB}	LI = HI = OV	-	0.06	**0.2**	mA
Total HB Operating Current	I_{HBO}	f = 500kHz	-	1.0	**3**	mA
HB to V_{SS} Current, Quiescent	I_{HBS}	V_{HS} = V_{HB} = 100V	-	0.1	**10**	µA
HB to V_{SS} Current, Operating	I_{HBSO}	f = 500kHZ	-	0.5		mA
INPUT PINS						
Low Level Input Voltage Threshold	V_{IL}		**0.8**	1.8	-	V
High Level Input Voltage Threshold	V_{IH}		-	1.8	**2.2**	V
Input Pulldown Resistance	R_I		**100**	180	**500**	kΩ
THERMAL RESISTANCE						
Junction to Ambient (note5)	θJA	SOIC-8		200		°C/W
		LLP-8 (note3)		40		

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Unless otherwise specified V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, No Load on LO or HO.(continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UNDER VOLTAGE PROTECTION						
V_{DD} Rising Threshold	V_{DDR}		**6.0**	6.9	**7.4**	V
V_{DD} threshold Hysteresis	V_{DDH}		-	0.5	-	V
HB Rising Threshold	V_{HBR}		**5.7**	6.6	**7.1**	V
HB Threshold Hysteresis	V_{HBH}		-	0.4	-	V
LO GATE DRIVER						
Low-Level Output Voltage	V_{OLL}	I_{LO} = 100mA	-	0.28	**0.6**	V
High-Level Output Voltage	V_{OHL}	I_{LO} = -100mA, V_{OHL} = V_{DD} -V_{LO}	-	0.45	**0.9**	V
Peak Pullup Current	I_{OHL}	V_{LO} =0V	-	1	-	A
Peak Pulldown Current	I_{OLL}	V_{LO} = 12V	-	1	-	A
HO GATE DRIVER						
Low Level Output Voltage	V_{OLH}	I_{HO} = 100mA	-	0.28	**0.6**	V
High Level Output Voltage	V_{OHH}	I_{HO} = -100mA, V_{OHH} = V_{HB} –V_{HO}	-	0.45	**0.9**	V
Peak Pullup Current	I_{OHH}	V_{HO} = 0V	-	1	-	A
Peak Pulldown Current	I_{OLH}	V_{HO} = 12V	-	1	-	A

SWITCHING CHARACTERISTICS:

Lower Turn-Off Propagation Delay (LI Falling to LO Falling)	t_{LPHL}		-	27	**56**	ns
Upper Turn-Off Propagation Delay (HI Falling to HO Falling)	t_{HPHL}		-	27	**56**	ns
Lower Turn-On Propagation Delay (LI Rising to LO Rising)	t_{LPLH}		-	29	**56**	ns
Upper Turn-On Propagation Delay (HI Rising to HO Rising)	t_{HPLH}		-	29	**56**	ns
Delay Matching: Lower Turn-On and Upper Turn-Off	t_{MON}		-	2	10	ns
Delay Matching: Lower Turn-Off and Upper Turn-On	t_{MOFF}		-	2	10	ns
Either Output Rise/Fall Time	t_{RC}, t_{FC}	C_L=1000pF	-	20	-	ns
Minimum Input Pulse Width that Changes the Output	t_{PW}			-	50	ns

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Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating ratings are conditions under which operation of the device is guaranteed. Operating limits do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristic tables.

Note 2: The human body model is a 100pF capacitor through a 1.5kΩ resistor into each pin. Pin 6 , Pin7 and Pin 8 are rated at 500V.

Note 3: Four layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. Five times body length of Cu trace on PCB top. 50mm x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.

Note 4: Minimum and Maximum limits are 100% production tested at 25°C. Limits over operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL)

Note 5: The θ_{JA} is not a given constant for the package and depends on the printed circuit board design and the operating conditions.

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