UNITRODE

# bq2050

## Lithium Ion Power Gauge™ IC

## Features

- Conservative and repeatable measurement of available capacity in Lithium Ion rechargeable batteries
- Designed for battery pack integration
  - 120µA typical operating current
  - Small size enables implementations in as little as ½ square inch of PCB
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- 16-pin narrow SOIC

## General Description

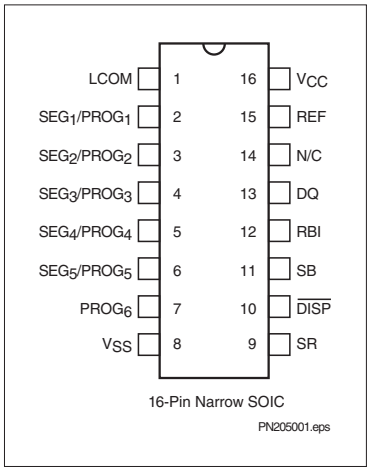
The bq2050 Lithium Ion Power Gauge™ IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery capacity. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available capacity information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

Nominal available capacity may be directly indicated using a five-segment LED display. These segments are used to graphically indicate available capacity. The bq2050 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2050 outputs battery information in response to external commands over the serial link.

The bq2050 may operate directly from one cell ($V_{BAT}$ > 3V). With the REF output and an external transistor, a simple, inexpensive regulator can be built for systems with more than one series cell.

Internal registers include available capacity, temperature, scaled available energy, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2050 power gauge data registers.

## Pin Connections




16-Pin Narrow SOIC

PN205001.eps

## Pin Names

| | | | |
|---|---|---|---|
| LCOM | LED common output | REF | Voltage reference output |
| $SEG_1/PROG_1$ | LED segment 1/ program 1 input | N/C | No connect |
| $SEG_2/PROG_2$ | LED segment 2/ program 2 input | DQ | Serial communications input/output |
| $SEG_3/PROG_3$ | LED segment 3/ program 3 input | RBI | Register backup input |
| $SEG_4/PROG_4$ | LED segment 4/ program 4 input | SB | Battery sense input |
| $SEG_5/PROG_5$ | LED segment 5/ program 5 input | $\overline{DISP}$ | Display control input |
| $PROG_6$ | Program 6 input | SR | Sense resistor input |
| | | $V_{CC}$ | 3.0–6.5V |
| | | $V_{SS}$ | System ground |

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## Pin Descriptions

**LCOM** **LED common output**

Open-drain output switches $V_{CC}$ to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

**$SEG_1$–$SEG_5$** **LED display segment outputs (dual function with $PROG_1$–$PROG_6$)**

Each output may activate an LED to sink the current sourced from LCOM.

**$PROG_1$–$PROG_2$** **Programmed full count selection inputs (dual function with $SEG_1$–$SEG_2$)**

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

**$PROG_3$–$PROG_4$** **Power gauge rate selection inputs (dual function with $SEG_3$–$SEG_4$)**

These three-level input pins define the scale factor described in Table 2.

**$PROG_5$** **Self-discharge rate selection (dual function with $SEG_5$)**

This three-level input pin defines the selfdischarge and battery compensation factors as shown in Table 1.

**$PROG_6$** **Capacity initialization selection**

This three-level pin defines the battery state of charge at reset as shown in Table 1.

**N/C** **No connect**

**SR** **Sense resistor input**

The voltage drop ($V_{SR}$) across the sense resistor $R_S$ is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied between the negative terminal of the battery and the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, $V_{SRO}$, as seen by the bq2050 is $V_{SR} + V_{OS}$ .

**$\overline{DISP}$** **Display control input**

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to $V_{CC}$ allows $PROG_X$ to connect directly to $V_{CC}$ or $V_{SS}$ instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during charge. $\overline{DISP}$ low activates the display. See Table 1.

**SB** **Secondary battery input**

This input monitors the battery cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, and battery removed.

**RBI** **Register backup input**

This pin is used to provide backup potential to the bq2050 registers during periods when $V_{CC} \leq 3V$. A storage capacitor or a battery can be connected to RBI.

**DQ** **Serial I/O pin**

This is an open-drain bidirectional pin.

**REF** **Voltage reference output for regulator**

REF provides a voltage reference output for an optional micro-regulator.

**$V_{CC}$** **Supply voltage input**

**$V_{SS}$** **Ground**

# Functional Description

## General Operation

The bq2050 determines battery capacity by monitoring the amount of current input to or removed from a rechargeable battery. The bq2050 measures discharge and charge currents, measures battery voltage, estimates self-discharge, monitors the battery for low battery voltage thresholds, and compensates for temperature and charge/discharge rates. The current measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The estimate of scaled available energy is made using the remaining average battery voltage during the discharge cycle and the remaining nominal available charge. The scaled available energy measurement is corrected for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2050 using the LED display capability as a charge-state indicator. The bq2050 is configured to display capacity in relative display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. A push-button display feature is available for momentarily enabling the LED display.

The bq2050 monitors the charge and discharge currents as a voltage across a sense resistor (see $R_S$ in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.

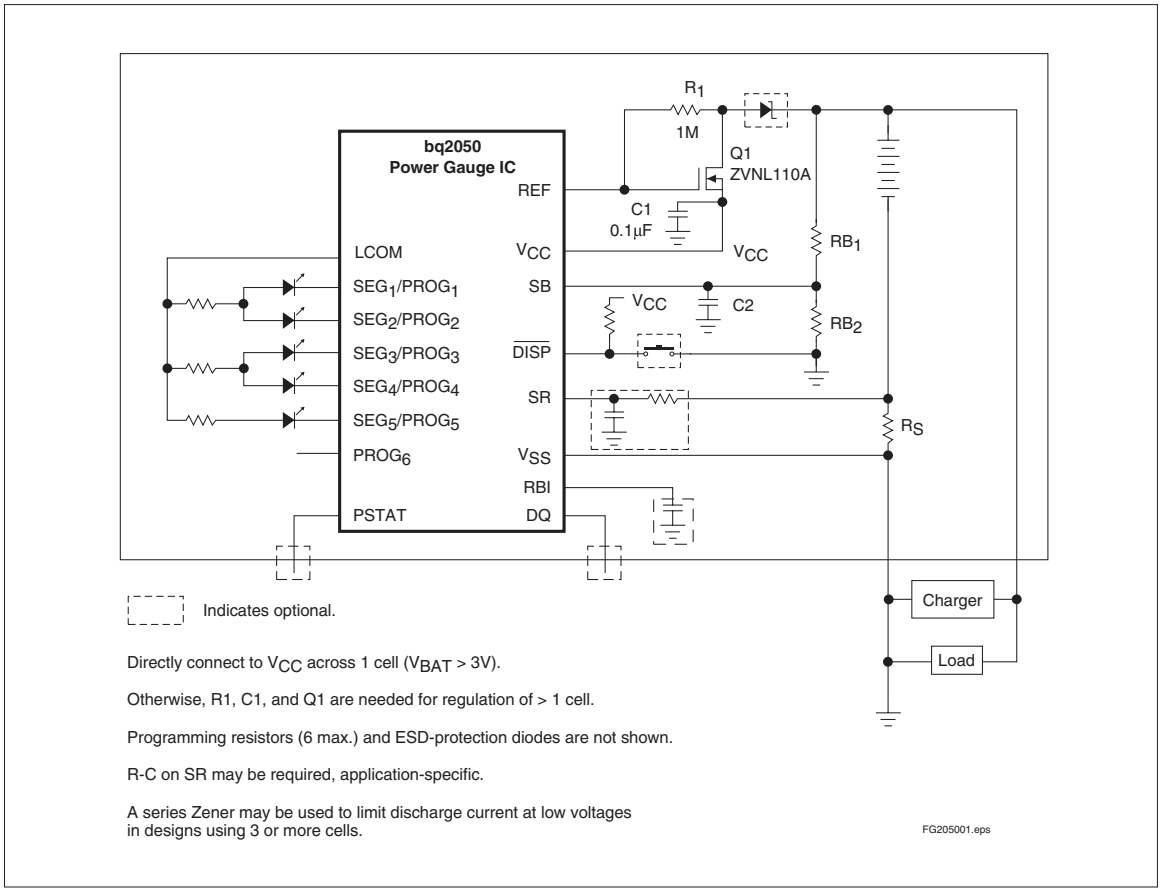



**Figure 1. Battery Pack Application Diagram—LED Display**

### Voltage Thresholds

In conjunction with monitoring $V_{SR}$ for charge/discharge currents, the bq2050 monitors the battery potential through the SB pin. The voltage is determined through a resistor-divider network per the following equation:

$$\frac{RB1}{RB2} = 2N - 1$$

where N is the number of cells, RB1 is connected to the positive battery terminal, and RB2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV). EDV threshold levels are used to determine when the battery has reached an "empty" state.

Two EDV thresholds for the bq2050 are programmable with the default values fixed at:

EDV1 (early warning) = 1.52V

EDVF (empty) = 1.47V

If $V_{SB}$ is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of $V_{SB}$, until the next valid charge. The $V_{SB}$ value is also available over the serial port.

During discharge and charge, the bq2050 monitors $V_{SR}$ for various thresholds used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if the discharge rate is greater than 2C (typical) and resumes ½ second after the rate falls below 2C.

### RBI Input

The RBI input pin is intended to be used with a storage capacitor or external supply to provide backup potential to the internal bq2050 registers when $V_{CC}$ drops below 3.0V. $V_{CC}$ is output on RBI when $V_{CC}$ is above 3.0V. A diode is required to isolate the external supply.

### Reset

The bq2050 can be reset either by removing $V_{CC}$ and grounding the RBI pin for 15 seconds or by writing 0x80 to register 0x39.

### Temperature

The bq2050 internally determines the temperature in 10°C steps centered from approximately -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown in the following table:

| TMP (hex) | Temperature Range |
|---|---|
| 0x | < -30°C |
| 1x | -30°C to -20°C |
| 2x | -20°C to -10°C |
| 3x | -10°C to 0°C |
| 4x | 0°C to 10°C |
| 5x | 10°C to 20°C |
| 6x | 20°C to 30°C |
| 7x | 30°C to 40°C |
| 8x | 40°C to 50°C |
| 9x | 50°C to 60°C |
| Ax | 60°C to 70°C |
| Bx | 70°C to 80°C |
| Cx | > 80°C |

## Layout Considerations

The bq2050 measures the voltage differential between the SR and $V_{SS}$ pins. $V_{OS}$ (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (C1 and C2) should be placed as close as possible to the $V_{CC}$ and SB pins, respectively, and their paths to $V_{SS}$ should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for $V_{CC}$.
- The sense resistor capacitor should be placed as close as possible to the SR pin.
- The sense resistor ($R_S$) should be as close as possible to the bq2050.

## Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2050. The bq2050 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Capacity (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2050 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. **Last Measured Discharge (LMD) or learned battery capacity:**

   LMD is the last measured discharge capacity of the battery. On initialization (application of $V_{CC}$ or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

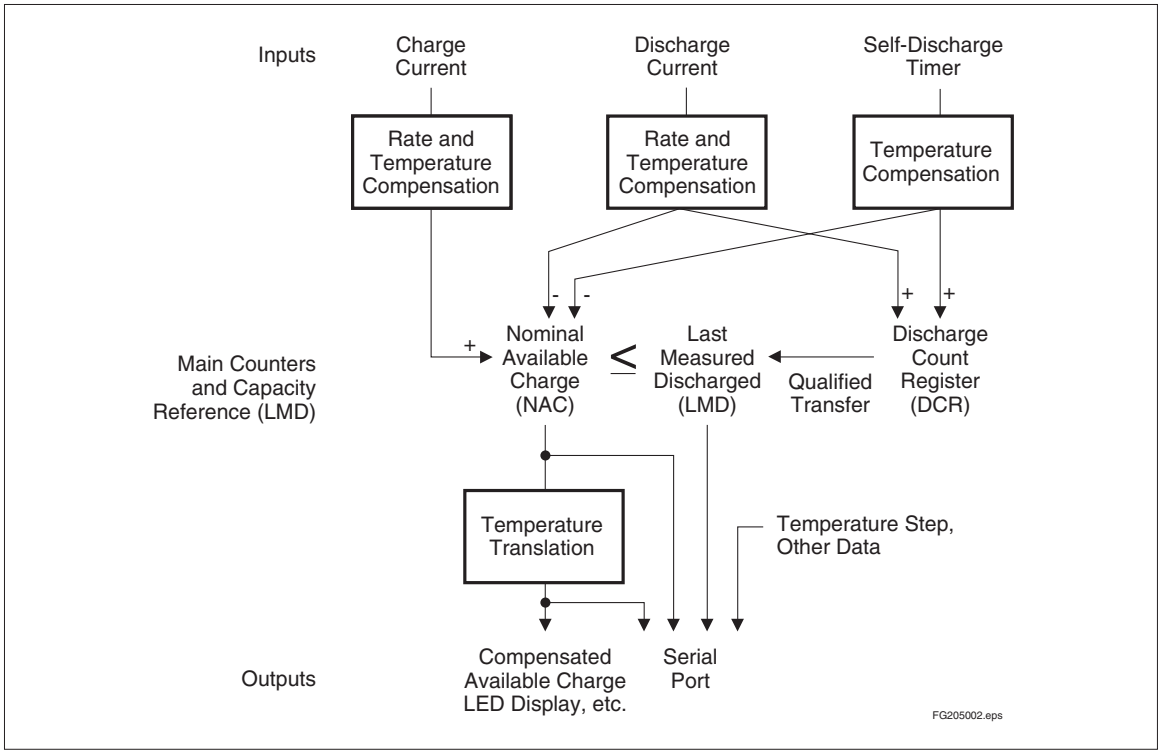



**Figure 2. Operational Overview**

**2. Programmed Full Count (PFC) or initial battery capacity:**

The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The bq2050 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) ∗ sense resistor (Ω) =

PFC (mVh)

Selecting a PFC slightly less than the rated capacity provides a conservative capacity reference until the bq2050 "learns" a new capacity reference.

***Example: Selecting a PFC Value***

Given:

Sense resistor = 0.05Ω
Number of cells = 2
Capacity = 1000mAh, Li-Ion battery, coke-anode
Current range = 50mA to 1A
Relative display mode
Serial port only
Self-discharge = $^{NAC}/_{512}$ per day @ 25°C
Voltage drop over sense resistor = 2.5mV to 50mV
Nominal discharge voltage = 3.6V

Therefore:

1000mAh ∗ 0.05Ω = 50mVh

**Table 1. bq2050 Programming**

| Pin Connection | $PROG_5$ Compensation/ Self-Discharge | $PROG_6$ NAC on Reset | $\overline{DISP}$ Display State |
|---|---|---|---|
| H | Table 4/Disabled | PFC | LEDs disabled |
| Z | Table 4/ $^{NAC}/_{512}$ | 0 | LEDs on when charging |
| L | Table 3/ $^{NAC}/_{512}$ | 0 | LEDs on for 4 sec. |

**Note:** $PROG_5$ and $PROG_6$ states are independent.

**Table 2. bq2050 Programmed Full Count mVh Selections**

| $PROG_x$ | | Programmed Full Count (PFC) | $PROG_4$ = L | | | $PROG_4$ = Z | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 2 | | PROG3 = H | PROG3 = Z | PROG3 = L | PROG3 = H | PROG3 = Z | PROG3 = L | |
| - | - | - | SCALE = 1/80 | SCALE = 1/160 | SCALE = 1/320 | SCALE = 1/640 | SCALE = 1/1280 | SCALE = 1/2560 | mVh/ count |
| H | H | 49152 | 614 | 307 | 154 | 76.8 | 38.4 | 19.2 | mVh |
| H | Z | 45056 | 563 | 282 | 141 | 70.4 | 35.2 | 17.6 | mVh |
| H | L | 40960 | 512 | 256 | 128 | 64.0 | 32.0 | 16.0 | mVh |
| Z | H | 36864 | 461 | 230 | 115 | 57.6 | 28.8 | 14.4 | mVh |
| Z | Z | 33792 | 422 | 211 | 106 | 53.0 | 26.4 | 13.2 | mVh |
| Z | L | 30720 | 384 | 192 | 96.0 | 48.0 | 24.0 | 12.0 | mVh |
| L | H | 27648 | 346 | 173 | 86.4 | 43.2 | 21.6 | 10.8 | mVh |
| L | Z | 25600 | 320 | 160 | 80.0 | 40.0 | 20.0 | 10.0 | mVh |
| L | L | 22528 | 282 | 141 | 70.4 | 35.2 | 17.6 | 8.8 | mVh |
| VSR equivalent to 2 counts/sec. (nom.) | | | 90 | 45 | 22.5 | 11.25 | 5.6 | 2.8 | mV |

Select:

PFC = 30720 counts or 48mVh
$PROG_1$ = float
$PROG_2$ = low
$PROG_3$ = high
$PROG_4$ = float
$PROG_5$ = float
$PROG_6$ = float

The initial full battery capacity is 48mVh (960mAh) until the bq2050 "learns" a new capacity with a qualified discharge from full to EDV1.

**3. Nominal Available Capacity (NAC):**

NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV1. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

**4. Discharge Count Register (DCR):**

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to $V_{EDV1}$ if:

No valid charge initiations (charges greater than 256 NAC counts, where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1 detected.

The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).

The temperature is ≥ 0°C when the EDV1 level is reached during discharge.

The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

**5. Scaled Available Energy (SAE):**

SAE is useful in determining the available energy within the battery, and may provide a more useful capacity reference in battery chemistries with sloped voltage profiles during discharge. SAE may be converted to a mWh value using the following formula:

$$E(mWh) = (SAEH * 256 + SAEL) * \frac{2.4 * SCALE * (R_{B1} + R_{B2})}{R_S * R_{B2}}$$

where $R_{B1}$, $R_{B2}$ and $R_S$ are resistor values in ohms. SCALE is the selected scale from Table 2. SAEH and SAEL are digital values read via DQ.

**6. Compensated Available Capacity (CAC)**

CAC counts similar to NAC, but contains the available capacity compensated for discharge rate and temperature.

### Charge Counting

Charge activity is detected based on a positive voltage on the $V_{SR}$ input. If charge activity is detected, the bq2050 increments NAC at a rate proportional to $V_{SR}$ and, if enabled, activates an LED display. Charge actions increment the NAC after compensation for temperature.

The bq2050 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until $V_{SRO}$ ($V_{SR} + V_{OS}$) falls below $V_{SRQ}$. $V_{SRQ}$ is 210µV, and is described in the Digital Magnitude Filter section.

### Discharge Counting

Discharge activity is detected based on a negative voltage on the $V_{SR}$ input. All discharge counts where $V_{SRO} < V_{SRD}$ cause the NAC register to decrement and the DCR to increment. $V_{SRD}$ is -200µV, and is described in the Digital Magnitude Filter section.

### Self-Discharge Estimation

The bq2050 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal $\frac{1}{512} * NAC$ per day or disabled. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

## Count Compensations

### Discharge Compensation

Corrections for the rate of discharge, temperature, and anode type are made by adjusting an internal compensation factor. This factor is based on the measured rate of discharge of the battery. Tables 3A and 3B outline the correction factor typically used for graphite anode Li-Ion batteries, and Tables 4A and 4B outline the factors typically used for coke anode Li-Ion batteries. The compensation factor is applied to CAC and is based on discharge rate and temperature.

### Table 3A. Graphite Anode

| Approximate Discharge Rate | Discharge Compensation Factor | Efficiency |
|---|---|---|
| < 0.5C | 1.00 | 100% |
| ≥ 0.5C | 1.05 | 95% |

### Table 3B. Graphite Anode

| Temperature | Temperature Compensation Factor | Efficiency |
|---|---|---|
| ≥ 10°C | 1.00 | 100% |
| 0°C to 10°C | 1.10 | 90% |
| -10°C to 0°C | 1.35 | 74% |
| ≤ -10°C | 2.50 | 40% |

### Table 4A. Coke Anode

| Approximate Discharge Rate | Discharge Compensation Factor | Efficiency |
|---|---|---|
| <0.5C | 1.00 | 100% |
| ≥ 0.5C | 1.15 | 86% |

### Table 4B. Coke Anode

| Temperature | Temperature Compensation Factor | Efficiency |
|---|---|---|
| ≥ 10°C | 1.00 | 100% |
| 0°C to 10°C | 1.25 | 80% |
| -10°C to 0°C | 2.00 | 50% |
| ≤ -10°C | 8.00 | 12% |

## Charge Compensation

The bq2050 applies the following temperature compensation to NAC during charge:

| Temperature | Temperature Compensation Factor | Efficiency |
|---|---|---|
| < 10°C | 0.95 | 95% |
| ≥ 10°C | 1.00 | 100% |

This compensation applies to both types of Li-Ion cells.

## Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $\frac{1}{512} * NAC$ per day. This is the rate for a battery within the 20°C–30°C temperature range. This rate varies across 8 ranges from < 10°C to > 70°C, changing with each higher temperature (approximately 10°C). See Table 5 below:

### Table 5. Self-Discharge Compensation

| Temperature Range | Typical Rate $PROG_5$ = Z or L |
|---|---|
| < 10°C | $NAC/2048$ |
| 10–20°C | $NAC/1024$ |
| 20–30°C | $NAC/512$ |
| 30–40°C | $NAC/256$ |
| 40–50°C | $NAC/128$ |
| 50–60°C | $NAC/64$ |
| 60–70°C | $NAC/32$ |
| > 70°C | $NAC/16$ |

Self-discharge may be disabled by connecting $PROG_5$ = H.

## Digital Magnitude Filter

The bq2050 has a digital filter to eliminate charge and discharge counting below a set threshold. The bq2050 setting is 200µV for $V_{SRD}$ and 210µV for $V_{SRQ}$.

**Table 6. bq2050 Current-Sensing Errors**

| Symbol | Parameter | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|
| INL | Integrated non-linearity error | ± 2 | ± 4 | % | Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V. |
| INR | Integrated non-repeatability error | ± 1 | ± 2 | % | Measurement repeatability given similar operating conditions. |

# Error Summary

## Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated (see the DCR description on page 7). The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description) and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

## Current-Sensing Error

Table 5 illustrates the current-sensing error as a function of $V_{SRO}$. A digital filter eliminates charge and discharge counts to the NAC register when $V_{SRO}$ is between $V_{SRQ}$ and $V_{SRD}$.

# Communicating With the bq2050

The bq2050 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2050 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2050 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2050. The command directs the bq2050 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2050 may be sampled using the pulse-width capture timers available on some microcontrollers.

If a communication error occurs, e.g. $t_{CYCB}$ > 6ms, the bq2050 should be sent a BREAK to reinitiate the serial interface. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, $t_B$ or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, $t_{BR}$. The bq2050 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2050 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, $t_{DSU}$, after the negative edge used to start communication. The data should be held for a period, $t_{DV}$, to allow the host or bq2050 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, $t_{SSU}$, after the negative edge used to start communication. The final logic-high state should be held until a period, $t_{SV}$, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2050 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2050 NAC register.

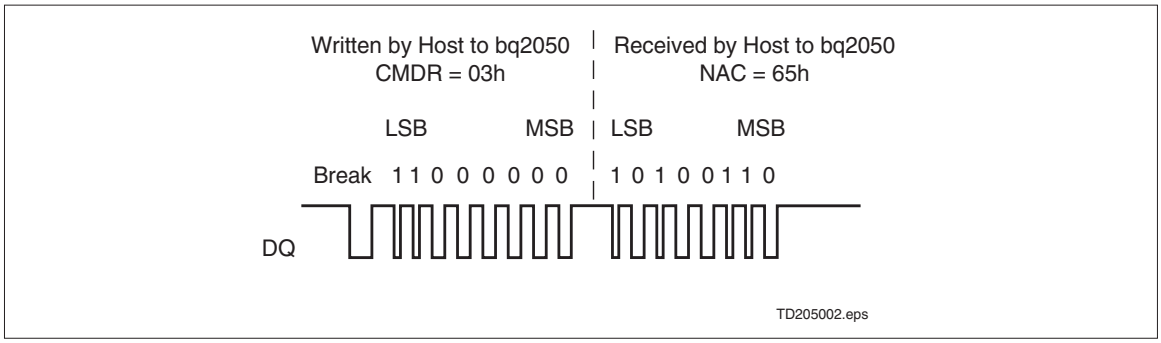



**Figure 3. Typical Communication With the bq2050**

## bq2050 Registers

The bq2050 command and status registers are listed in Table 7 and described below.

### Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2050. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

The W/$\overline{R}$ values are:

| CMDR Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| W/$\overline{R}$ | - | - | - | - | - | - | - |

Where W/$\overline{R}$ is:

0 The bq2050 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

| CMDR Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 (LSB) |

### Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2050 flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A $V_{SRO}$ of less than $V_{SRQ}$ or discharge activity clears CHGS.

The CHGS values are:

| FLGS1 Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHGS | - | - | - | - | - | - | - |

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the bq2050 is reset either by application of $V_{CC}$ or by a serial port command. BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are:

| FLGS1 Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | BRP | - | - | - | - | - | - |

Where BRP is:

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 bq2050 is reset

## Table 7. bq2050 Command and Status Registers

| Symbol | Register Name | Loc. (hex) | Read/ Write | Control Field | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | 7(MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0(LSB) |
| CMDR | Command register | 00h | Write | W/$\overline{R}$ | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 |
| FLGS1 | Primary status flags register | 01h | Read | CHGS | BRP | n/u | CI | VDQ | n/u | EDV1 | EDVF |
| TMP | Temperature register | 02h | Read | TMP3 | TMP2 | TMP1 | TMP0 | GG3 | GG2 | GG1 | GG0 |
| NACH | Nominal available capacity high byte register | 03h | R/W | NACH7 | NACH6 | NACH5 | NACH4 | NACH3 | NACH2 | NACH1 | NACH0 |
| NACL | Nominal available capacity low byte register | 17h | Read | NACL7 | NACL6 | NACL5 | NACL4 | NACL3 | NACL2 | NACL1 | NACL0 |
| BATID | Battery identification register | 04h | R/W | BATID7 | BATID6 | BATID5 | BATID4 | BATID3 | BATID2 | BATID1 | BATID0 |
| LMD | Last measured discharge register | 05h | R/W | LMD7 | LMD6 | LMD5 | LMD4 | LMD3 | LMD2 | LMD1 | LMD0 |
| FLGS2 | Secondary status flags register | 06h | Read | n/u | DR2 | DR1 | DR0 | n/u | n/u | n/u | OVLD |
| PPD | Program pin pull-down register | 07h | Read | n/u | n/u | PPD6 | PPD5 | PPD4 | PPD3 | PPD2 | PPD1 |
| PPU | Program pin pull-up register | 08h | Read | n/u | n/u | PPU6 | PPU5 | PPU4 | PPU3 | PPU2 | PPU1 |
| CPI | Capacity inaccurate count register | 09h | Read | CPI7 | CPI6 | CPI5 | CPI4 | CPI3 | CPI2 | CPI1 | CPI0 |
| VSB | Battery voltage register | 0Bh | Read | VSB7 | VSB6 | VSB5 | VSB4 | VSB3 | VSB2 | VSB1 | VSB0 |
| VTS | End-of-discharge threshold select register | 0Ch | R/W | VTS7 | VTS6 | VTS5 | VTS4 | VTS3 | VTS2 | VTS1 | VTS0 |
| CACH | Compensated available capacity high byte register | 0Dh | Read | CACH7 | CACH6 | CACH5 | CACH4 | CACH3 | CACH2 | CACH1 | CACH0 |
| CACL | Compensated available capacity low byte register | 0Eh | Read | CACL7 | CACL6 | CACL5 | CACL4 | CACL3 | CACL2 | CACL1 | CACL0 |
| SAEH | Scaled available energy high byte register | 0Fh | Read | SAEH7 | SAEH6 | SAEH5 | SAEH4 | SAEH3 | SAEH2 | SAEH1 | SAEH0 |
| SAEL | Scaled available energy low byte register | 10h | Read | SAEL7 | SAEL6 | SAEL5 | SAEL4 | SAEL3 | SAEL2 | SAEL1 | SAEL0 |
| RST | Reset register | 39h | Write | RST | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Note:** n/u = not used

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2050 is reset. The flag is cleared after an LMD update.

The CI values are:

| FLGS1 Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | CI | - | - | - | - |

Where CI is:

0 When LMD is updated with a valid full discharge

1 After the 64th valid charge action with no LMD updates or the bq2050 is reset

The ***valid discharge*** flag (VDQ) is asserted when the bq2050 is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

| FLGS1 Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | VDQ | - | - | - |

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The ***first end-of-discharge warning*** flag (EDV1) warns the user that the battery is almost empty. The first segment pin, $SEG_1$, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected. The EDV1 threshold is externally controlled via the VTS register (see Voltage Threshold Register on this page).

The EDV1 values are:

| FLGS1 Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | EDV1 | - |

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$ providing that the discharge rate is < 2C

The ***final end-of-discharge warning*** flag (EDVF) flag is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EDVF threshold is set 50mV below the EDV1 threshold.

The EDVF values are:

| FLGS1 Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | - | EDVF |

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq (V_{TS}$ - 50mV)

1 $V_{SB} < (V_{TS}$ - 50mV) providing the discharge rate is < 2C

## Temperature Register (TMP)

The read-only TMP register (address=02h) contains the battery temperature.

| TMP Temperature Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TMP4 | TMP3 | TMP2 | TMP1 | - | - | - | - |

The bq2050 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient. The temperature register contents may be translated as shown in Table 7.

The bq2050 calculates the gas gauge bits, GG3-GG0 as a function of CACH and LMD. The results of the calculation give available capacity in $1/16$ increments from 0 to $15/16$.

**Table 7. Temperature Register**

| TMP3 | TMP2 | TMP1 | TMP0 | Temperature |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | T < -30°C |
| 0 | 0 | 0 | 1 | -30°C < T < -20°C |
| 0 | 0 | 1 | 0 | -20°C < T < -10°C |
| 0 | 0 | 1 | 1 | -10°C < T < 0°C |
| 0 | 1 | 0 | 0 | 0°C < T < 10°C |
| 0 | 1 | 0 | 1 | 10°C < T < 20°C |
| 0 | 1 | 1 | 0 | 20°C < T < 30°C |
| 0 | 1 | 1 | 1 | 30°C < T < 40°C |
| 1 | 0 | 0 | 0 | 40°C < T < 50°C |
| 1 | 0 | 0 | 1 | 50°C < T < 60°C |
| 1 | 0 | 1 | 0 | 60°C < T < 70°C |
| 1 | 0 | 1 | 1 | 70°C < T < 80°C |
| 1 | 1 | 0 | 0 | T > 80°C |

| TMPGG Gas Gauge Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | GG3 | GG2 | GG1 | GG0 |

## Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging register for the bq2050. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC. NACH and NACL are set to 0 during a bq2050 reset.

Writi*ng to the NAC registers affects the available charge counts and, therefore, affects the bq2050 gas gauge operation. Do not write the NAC registers to a value greater than LMD.*

## Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as $V_{CC}$ is greater than 2V. The contents of BATID have no effect on the operation of the bq2050. There is no default setting for this register.

## Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2050 uses as a measured full reference. The bq2050 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2050 updates the capacity of the battery. LMD is set to PFC during a bq2050 reset.

## Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2050 flags.

| FLGS2 Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | DR2 | DR1 | DR0 | - | - | - | |

The ***discharge rate*** flags, DR2–0, are bits 6–4.

| DR2 | DR1 | DR0 | Discharge Rate |
|---|---|---|---|
| 0 | 0 | 0 | DRATE < 0.5C |
| 0 | 0 | 1 | 0.5C ≤ DRATE < 2C |
| 0 | 1 | 0 | DRATE ≥ 2C (OVLD = 1) |

They are used to determine the current discharge regime as follows:

| FLGS2 Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | - | - | - | - | - | OVLD |

The ***overload*** flag (OVLD) is asserted when a discharge rate in excess of 2C is detected. OVLD remains asserted as long as the condition persists and is cleared 0.5 seconds after the rate drops below 2C. The overload condition is used to stop sampling of the battery terminal characteristics for end-of-discharge determination.

## Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2050. The segment drivers, $SEG_{1–6}$, have a corresponding PPD register location, $PPD_{1–6}$. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if $SEG_1$ and $SEG_4$ have pull-down resistors, the contents of PPD are xx001001.

## Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2050. The segment drivers, $SEG_{1–6}$, have a corresponding PPU register location, $PPU_{1–6}$. A given location is set if a pull-up resistor has been detected on its corresponding segment

driver. For example, if $SEG_3$ and $SEG_6$ have pull-up resistors, the contents of PPU are xx100100.

| PPD/PPU Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| - | - | $PPU_6$ | $PPU_5$ | $PPU_4$ | $PPU_3$ | $PPU_2$ | $PPU_1$ |
| - | - | $PPD_6$ | $PPD_5$ | $PPD_4$ | $PPD_3$ | $PPD_2$ | $PPD_1$ |

## Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2050 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 ∗ LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 ∗ LMC. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

## Battery Voltage Register (VSB)

The read-only battery voltage register is used to read the single-cell battery voltage on the SB pin. The VSB register (address = 0Bh) is updated approximately once per second with the present value of the battery voltage. $V_{SB}$ = 2.4V ∗ (VSB/256).

| VSB Register Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VSB7 | VSB6 | VSB5 | VSB4 | VSB3 | VSB2 | VSB1 | VSB0 |

## Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register (address = 0Ch). The read/write VTS register sets the EDV1 trip point. EDVF is set 50mV below EDV1. The default value in the VTS register is A2h, representing EDV1 = 1.52V and EDVF = 1.47V. EDV1 = 2.4V ∗ (VTS/256).

| VTS Register Bits | | | | | | | |
|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VTS7 | VTS6 | VTS5 | VTS4 | VTS3 | VTS2 | VTS1 | VTS0 |

## Compensated Available Charge Registers (CACH/CACL)

The read-only CACH high-byte register (address = 0Dh) and the read-only CACL low-byte register (address = 0Eh) represent the available charge compensated for discharge rate and temperature. CACH and CACL use piece-wise corrections as outlined in Tables 3A, 3B, 4A, and 4B, and will vary as conditions change. The NAC and LMD registers are not affected by the discharge rate and temperature.

## Scaled Available Energy Registers (SAEH/SAEL)

The read-only SAEH high-byte register (address = 0Fh) and the read only SAEL low-byte register (address = 10h) are used to scale battery voltage and CAC to a value which can be translated to watt-hours remaining under the present conditions. SAEL and SAEH may be converted to mWh using the formula on page 7.

## Reset Register (RST)

The reset register (address = 39h) enables a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2050 reset is performed. *Setting any bit other than the most-significant bit of the RST register is* ***not allowed*** *and results in improper operation of the bq2050.*

Resetting the bq2050 sets the following:

- LMD = PFC
- CPI, VDQ, NACH, and NACL = 0
- CI and BRP = 1

**Note:** Self-discharge is disabled when $PROG_5$ = H.

# Display

The bq2050 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to $V_{CC}$ or $V_{SS}$ for a program high or program low, respectively.

The bq2050 displays the battery charge state in relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does

not affect the NAC register. The temperature adjustments are detailed in the CACH and CACL register descriptions.

When $\overline{DISP}$ is tied to $V_{CC}$, the $SEG_{1–5}$ outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2050 detects a charge in progress $V_{SRO} > V_{SRQ}$ . When pulled low, the segment outputs become active for a period of four seconds, ± 0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

$SEG_1$ blinks at a 4Hz rate whenever $V_{SB}$ has been detected to be below $V_{EDV1}$ (EDV1 = 1), indicating a low-battery condition. $V_{SB}$ below $V_{EDVF}$ (EDVF = 1) disables the display output.

## Microregulator

The bq2050 can operate directly from one cell. A micropower source for the bq2050 can be inexpensively built using the FET and an external resistor to accommodate a greater number of cells; see Figure 1.

## Absolute Maximum Ratings

| Symbol | Parameter | Minimum | Maximum | Unit | Notes |
|---|---|---|---|---|---|
| $V_{CC}$ | Relative to $V_{SS}$ | -0.3 | 7.0 | V | |
| All other pins | Relative to $V_{SS}$ | -0.3 | 7.0 | V | |
| REF | Relative to $V_{SS}$ | -0.3 | 8.5 | V | Current limited by R1 (see Figure 1) |
| $V_{SR}$ | Relative to $V_{SS}$ | -0.3 | 7.0 | V | Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2050 application note for details). |
| $T_{OPR}$ | Operating temperature | 0 | 70 | °C | Commercial |
| | | | | | |

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

## DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{EDVF}$ | Final empty warning | 1.44 | 1.47 | 1.50 | V | SB |
| $V_{EDV1}$ | First empty warning | 1.49 | 1.52 | 1.55 | V | SB |
| $V_{SRO}$ | SR sense range | -300 | - | 2000 | mV | SR, $V_{SR} + V_{OS}$ |
| $V_{SRQ}$ | Valid charge | 210 | - | - | µV | $V_{SR} + V_{OS}$ (see note) |
| $V_{SRD}$ | Valid discharge | - | - | -200 | µV | $V_{SR} + V_{OS}$ (see note) |
| $V_{MCV}$ | Maximum single-cell voltage | 2.20 | 2.25 | 2.30 | V | SB |

**Note:** $V_{OS}$ is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See “Layout Considerations.”

## DC Electrical Characteristics ($T_A = T_{OPR}$)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Notes |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 3.0 | 4.25 | 6.5 | V | $V_{CC}$ excursion from < 2.0V to ≥ 3.0V initializes the unit. |
| $V_{OS}$ | Offset referred to $V_{SR}$ | - | ±50 | ±150 | µV | $\overline{DISP}$ = $V_{CC}$ |
| $V_{REF}$ | Reference at 25°C | 5.7 | 6.0 | 6.3 | V | $I_{REF}$ = 5µA |
| | Reference at -40°C to +85°C | 4.5 | - | 7.5 | V | $I_{REF}$ = 5µA |
| $R_{REF}$ | Reference input impedance | 2.0 | 5.0 | - | MΩ | $V_{REF}$ = 3V |
| $I_{CC}$ | Normal operation | - | 90 | 135 | µA | $V_{CC}$ = 3.0V, DQ = 0 |
| | | - | 120 | 180 | µA | $V_{CC}$ = 4.25V, DQ = 0 |
| | | - | 170 | 250 | µA | $V_{CC}$ = 6.5V, DQ = 0 |
| $V_{SB}$ | Battery input | 0 | - | $V_{CC}$ | V | |
| $R_{SBmax}$ | SB input impedance | 10 | - | - | MΩ | 0 < $V_{SB}$ < $V_{CC}$ |
| $I_{DISP}$ | $\overline{DISP}$ input leakage | - | - | 5 | µA | $V_{DISP}$ = $V_{SS}$ |
| $I_{LCOM}$ | LCOM input leakage | -0.2 | - | 0.2 | µA | $\overline{DISP}$ = $V_{CC}$ |
| $I_{RBI}$ | RBI data retention current | - | - | 100 | nA | $V_{RBI}$ > $V_{CC}$ < 3V |
| $R_{DQ}$ | Internal pulldown | 500 | - | - | KΩ | |
| $V_{SR}$ | Sense resistor input | -0.3 | - | 2.0 | V | $V_{SR}$ < $V_{SS}$ = discharge; $V_{SR}$ > $V_{SS}$ = charge |
| $R_{SR}$ | SR input impedance | 10 | - | - | MΩ | -200mV < $V_{SR}$ < $V_{CC}$ |
| $V_{IH}$ | Logic input high | $V_{CC}$ - 0.2 | - | - | V | $PROG_1$–$PROG_6$ |
| $V_{IL}$ | Logic input low | - | - | $V_{SS}$ + 0.2 | V | $PROG_1$–$PROG_6$ |
| $V_{IZ}$ | Logic input Z | float | - | float | V | $PROG_1$–$PROG_6$ |
| $V_{OLSL}$ | $SEG_X$ output low, low $V_{CC}$ | - | 0.1 | - | V | $V_{CC}$ = 3V, $I_{OLS}$ ≤ 1.75mA $SEG_1$–$SEG_5$ |
| $V_{OLSH}$ | $SEG_X$ output low, high $V_{CC}$ | - | 0.4 | - | V | $V_{CC}$ = 6.5V, $I_{OLS}$ ≤ 11.0mA $SEG_1$–$SEG_5$ |
| $V_{OHLCL}$ | LCOM output high, low $V_{CC}$ | $V_{CC}$ - 0.3 | - | - | V | $V_{CC}$ = 3V, $I_{OHLCOM}$ = -5.25mA |
| $V_{OHLCH}$ | LCOM output high, high $V_{CC}$ | $V_{CC}$ - 0.6 | - | - | V | $V_{CC}$ = 6.5V, $I_{OHLCOM}$ = -33.0mA |
| $I_{IH}$ | $PROG_{1-6}$ input high current | - | 1.2 | - | µA | $V_{PROG}$ = $V_{CC}$/2 |
| $I_{IL}$ | $PROG_{1-6}$ input low current | - | 1.2 | - | µA | $V_{PROG}$ = $V_{CC}$/2 |
| $I_{OHLCOM}$ | LCOM source current | -33 | - | - | mA | At $V_{OHLCH}$ = $V_{CC}$ - 0.6V |
| $I_{OLS}$ | $SEG_{1-5}$ sink current | - | - | 11.0 | mA | At $V_{OLSH}$ = 0.4V |
| $I_{OL}$ | Open-drain sink current | - | - | 5.0 | mA | At $V_{OL}$ = $V_{SS}$ + 0.3V DQ |
| $V_{OL}$ | Open-drain output low | - | - | 0.5 | V | $I_{OL}$ ≤ 5mA, DQ |
| $V_{IHDQ}$ | DQ input high | 2.5 | - | - | V | DQ |
| $V_{ILDQ}$ | DQ input low | - | - | 0.8 | V | DQ |
| $R_{PROG}$ | Soft pull-up or pull-down resistor value (for programming) | - | - | 200 | KΩ | $PROG_1$–$PROG_6$ |
| $R_{FLOAT}$ | Float state external impedance | - | 5 | - | MΩ | $PROG_1$–$PROG_6$ |

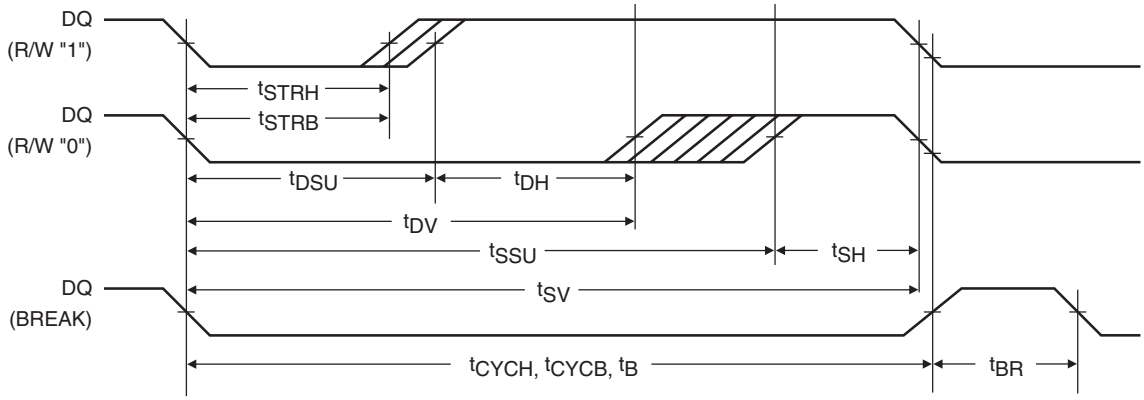
**Note:** All voltages relative to $V_{SS}$.

## Serial Communication Timing Specification ($T_A = T_{OPR}$)

| Symbol | Parameter | Minimum | Typical | Maximum | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{CYCH}$ | Cycle time, host to bq2050 | 3 | - | - | ms | See note |
| $t_{CYCB}$ | Cycle time, bq2050 to host | 3 | - | 6 | ms | |
| $t_{STRH}$ | Start hold, host to bq2050 | 5 | - | - | ns | |
| $t_{STRB}$ | Start hold, bq2050 to host | 500 | - | - | µs | |
| $t_{DSU}$ | Data setup | - | - | 750 | µs | |
| $t_{DH}$ | Data hold | 750 | - | - | µs | |
| $t_{DV}$ | Data valid | 1.50 | - | - | ms | |
| $t_{SSU}$ | Stop setup | - | - | 2.25 | ms | |
| $t_{SH}$ | Stop hold | 700 | - | - | µs | |
| $t_{SV}$ | Stop valid | 2.95 | - | - | ms | |
| $t_B$ | Break | 3 | - | - | ms | |
| $t_{BR}$ | Break recovery | 1 | - | - | ms | |

**Notes:** The open-drain DQ pin should be pulled to at least $V_{CC}$ by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

## Serial Communication Timing

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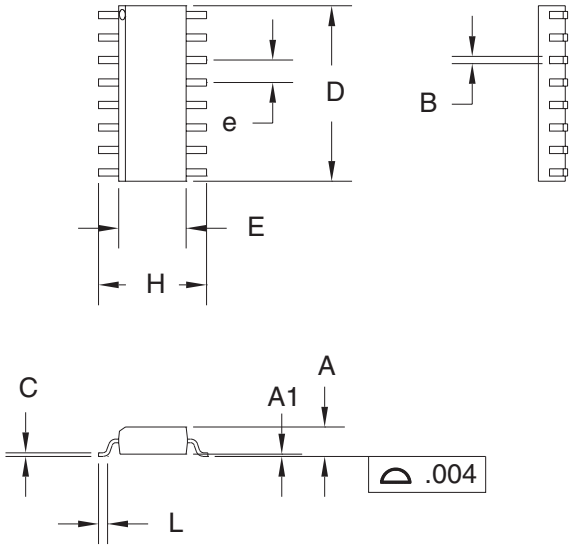
## 16-Pin SOIC Narrow (SN)




### 16-Pin SN (0.150" SOIC)

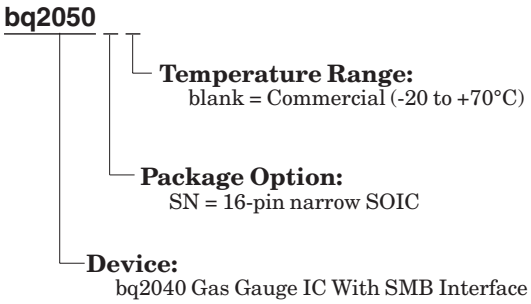
| Dimension | Inches | | Millimeters | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| A | 0.060 | 0.070 | 1.52 | 1.78 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.013 | 0.020 | 0.33 | 0.51 |
| C | 0.007 | 0.010 | 0.18 | 0.25 |
| D | 0.385 | 0.400 | 9.78 | 10.16 |
| E | 0.150 | 0.160 | 3.81 | 4.06 |
| e | 0.045 | 0.055 | 1.14 | 1.40 |
| H | 0.225 | 0.245 | 5.72 | 6.22 |
| L | 0.015 | 0.035 | 0.38 | 0.89 |

## Data Sheet Revision History

| Change No. | Page No. | Description | Nature of Change | |
|---|---|---|---|---|
| 1 | 4 | Changed reset procedure | Was:<br>Is: | Reset by issuing command over serial port<br>Reset by removing $V_{CC}$ and grounding RBI for 15 s. |
| 1 | 11, 14 | Deleted reset register | | |
| 2 | 16 | Changed values | $V_{EDVF}$:<br><br>$V_{EDV1}$: | Min. was 1.45; Max. was 1.49<br>Min. now is 1.44; Max. now is 1.50<br>Min. was 1.50; Min. now is 1.49 |
| 2 | 17 | Changed values | $V_{CC}$: | Min. was 2.5; Min. now is 3.0 |
| 2 | 4, 11, 13, 14 | Reinserted reset register | | |
| 2 | 9 | Maximum offset | $V_{OS}$: | Max. was 150<br>Max. now is 180 |

**Notes:** Change 1 = June 1995 B changes from Dec. 1994.
Change 2 = Sept. 1996 C changes from June 1995 B.

## Ordering Information

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