PWM CONTROLLED SRC WITH INDUCTIVE OUTPUT FILTER AT CONSTANT SWITCHING FREQUENCY†

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ABSTRACT

By using PWM control scheme in the series resonant converter with inductive output filter, we can operate the converter at a constant frequency. This converter has lower switching loss than the PWM converter and better control characteristics than the ordinary SRC. Since the peak current in the the present converter equals the load current, it has the lowest possible peak current stress among converters. In this paper, we present the analysis and the performance characteristics of the converter operating at a constant switching frequency. Computer simulation results will be given to confirm our analytical work.

I. INTRODUCTION

The conventional series resonant converter (SRC) [1] has relatively high component stress and poor control characteristics. The series resonant converter with inductive output filter using variable frequency control [2] introduced recently has better component stress and control characteristics than the conventional SRC. However, the variable frequency control scheme requires a relatively wide range of switching frequency for its output regulation and is undesirable in many applications. PWM and phase shift controlled SRCs operated at resonant frequency [3] has been presented recently. However, the component stresses in these converters are also relatively high.

In this paper, we present a series resonant converter with inductive output filter using PWM control at a constant switching frequency. The half-bridge and full-bridge configurations of the present converter are shown in Figs. 1 and 2, respectively. It can be shown from the converter circuits that the absolute value of the resonant inductor current i_l is clamped at the output current I_O, which assures that the present converter has low current stress. Our theoretical results will show that the converter also has good control characteristics.

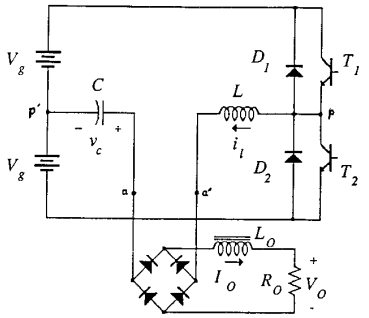

Fig. 1 Half-bridge circuit configuration of series resonant converter with inductive output filter.

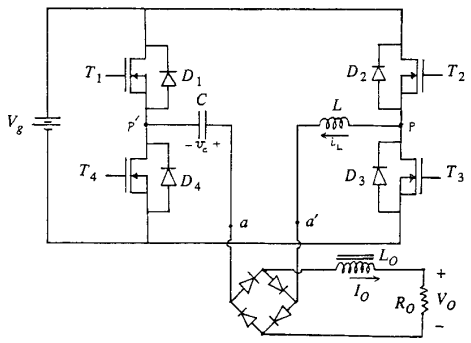

Fig. 2 Full-bridge circuit configuration of series resonant converter with inductive output filter.

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We use the state-plane approach in our analysis from which the design curves for the converter are derived. The design procedure as well as simulation results will be given to confirm our analytical work.

II. CONVERTER OPERATION

In the half-bridge configuration shown in Fig. 1, transistors T_1 and T_2 are driven by the waveforms shown in Fig. 3, indicating that the turn-on time interval for each transistor is directly proportional to the duty ratio d. In the full-bridge configuration shown in Fig. 2, transistors T_3 and T_4 are turned on and off at the same time as transistors T_1 and T_2, respectively, which are also driven by the same waveforms shown in Fig. 3. Thus, for the full-bridge configuration, we may refer the switching operation of transistors T_1 and T_2 onlv

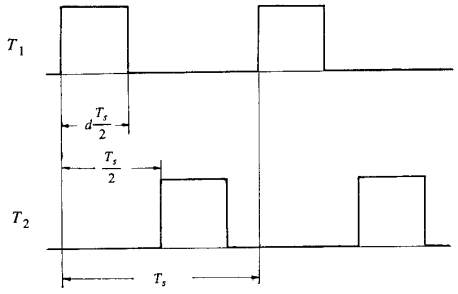

Fig. 3 Driving waveforms of transistors.

As described in the recent paper [2], the present converter may possess up to five topological circuit modes which are shown in Fig. 4. The steady state response of the converter can be represented by a closed trajectory in the normalized state-plane v_{nc}–i_{nl} in which all currents and voltages are normalized by V_g/Z_o and V_g, respectively, where $Z_o = \sqrt{L/C}$. In Figs. 1 and 2, we assume that L_O are large enough so that the output currents I_O can be considered constant. Hence, when $|i_l|$ is less than I_O, the rectifying diodes present a short circuit for i_l. The trajectory in the normalized state-plane will be a circular arc centered at +1 or -1 on the v_{nc}–axis, depending on whether the voltage across the tank circuit at terminals pp' is $+V_g$ or $-V_g$, respectively. Otherwise, the normalized inductor current i_{nl} will be clamped at either $+I_{no}$ or $-I_{no}$.

The state-plane trajectories of the converter can be classified into three operation modes I, II and III, depending on duty ratio d and the normalized output current I_{no}. The state-plane diagrams as well as the conducting switching devices and circuit modes for operation modes I, II and III are shown in Figs. 5 (a), (b) and (c), respectively. Since all state-plane diagrams are symmetrical with respect to the origin, only a half of a switching period will be used for the analysis.

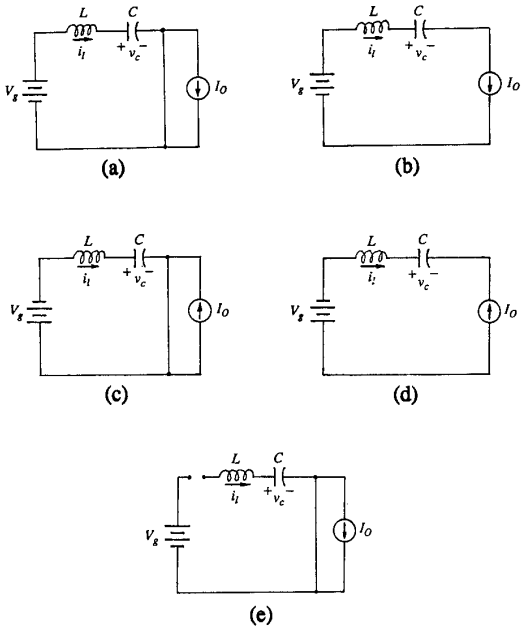

Fig. 4 Five topological circuit modes: (a) M_1, (b) M_2, (c) M_3, (d) M_4 and (e) M_5.

2.1 Operation Mode I

From the state-plane diagram given in Fig. 5 (a), we obtain the inductor current and the capacitor voltage waveforms which are given in Fig. 6. In this mode of operation, the cycle starts at t_0 when transistor T_1 is turned on at zero current. After t_0, the converter is in circuit mode M_1 and inductor current i_l increases sinusoidally until it reaches I_O at t_1. After t_1, the inductor current is clamped at a constant value, I_O, and capacitor C is linearly charged by this current. Thus, the normalized capacitor voltage v_{nc} after t_1 can be expressed by

$$v_{nc}(t) = v_{nc}(t_1) + \omega_o I_{no}(t-t_1) \quad (1)$$

where $\omega_o = 1/\sqrt{LC}$, and $v_{nc}(t_1)$ is the normalized capacitor voltage at t_1.

At t_2, transistor T_1 is turned off while $i_l = I_O$. After t_2, diode D_2 is forced to commutate the inductor current. The converter is in the circuit mode M_3 and remains there until i_l reaches zero at t_3 where $v_{nc}(t_3) \le 1$. When $v_{nc}(t_3) \le 1$, the converter is in the dead time interval which can be represented by circuit mode M_5. The converter operation for the first half of the cycle is completed when transistor T_2 is turned on at t_4. In order to satisfy the condition that

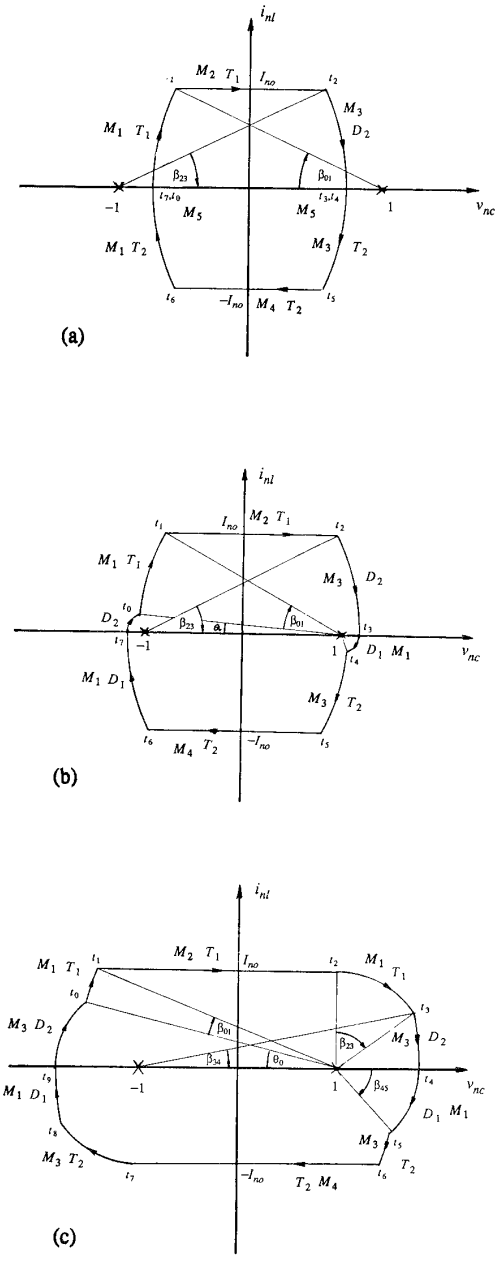

Fig. 5 State-plane diagrams of the converter for (a) operation mode I, (b) operation mode II and (c) operation mode III.

$v_{nc}(t_3) \leq 1$, the normalized capacitor voltage v_{nc} at the switching point t_2 must satisfy the following condition:

$$v_{nc}(t_2) = \sqrt{4 - I_{no}^2} - 1 \quad (2)$$

Since the state-plane diagram of this mode of operation is also symmetrical with respect to the i_{nl}-axis, the following relations must be satisfied:

$$v_{nc}(t_2) = -v_{nc}(t_1) \quad (3)$$

$$v_{nc}(t_3) = -v_{nc}(t_0) \quad (4)$$

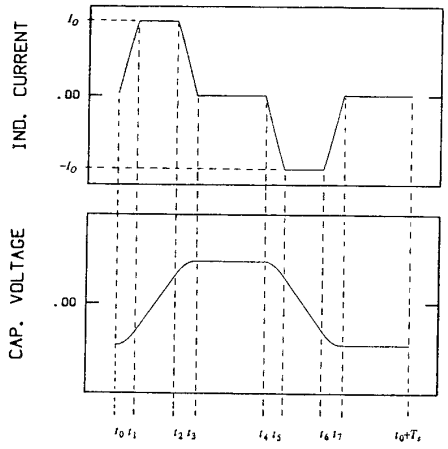

Fig. 6 Inductor current and capacitor voltage waveforms for operation mode I.

2.2 Operation Mode II

The state-plane diagram for this operation mode is shown in Fig. 5 (b). the inductor current and capacitor voltage waveforms can be obtained from this diagram and they are given in Fig. 7. The cycle starts at t_0 when transistor T_1 is turned on. The converter is in circuit mode M_1 and remains there until inductor current i_l reaches I_O at t_1. In circuit mode M_2, i_l is being clamped at I_O and the normalized capacitor voltage is expressed by

$$v_{nc}(t) = v_{nc}(t_1) + \omega_o I_{no}(t - t_1) \quad (5)$$

Similar to the operation mode I, transistor T_1 is turned off while the inductor current i_l is being clamped at I_O. The only difference is that when the inductor current reaches zero at t_3, the normalized capacitor voltage is greater than 1. Therefore, the range of $v_{nc}(t_2)$ for this operation mode is given by

$$\sqrt{4 - I_{no}^2} - 1 < v_{nc}(t_2) \leq 1 \quad (6)$$

Since $v_{nc} > 1$ at t_3, diode D_1 starts to conduct at this time and the converter goes back to the circuit mode M_1. The converter operation for the first half of the cycle is completed when transistor T_2 is turned on at t_4.

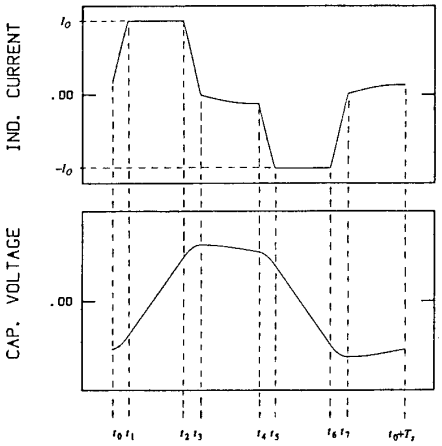

Fig. 7 Inductor current and capacitor voltage waveforms for operation mode II.

2.3 Operation Mode III

For this mode of operation, the state-plane diagram is shown in Fig. 5 (c) and the inductor current and capacitor voltage waveforms are given in Fig. 8. The converter operation from t_0 to t_3 are the same as that of the operation mode II, except that transistor T_1 is turned off at $v_{nc} > 1$ while the converter is in circuit mode M_1. Diode D_2 is forced to commutate the inductor current and the converter is in circuit mode M_3. In this mode of operation, v_{nc} is assumed to be greater than 1.0 when i_l equals zero. Therefore, D_1 starts to conduct at t_4. The converter operation is completed for the first half of the cycle when transistor T_2 is turned on at t_5.

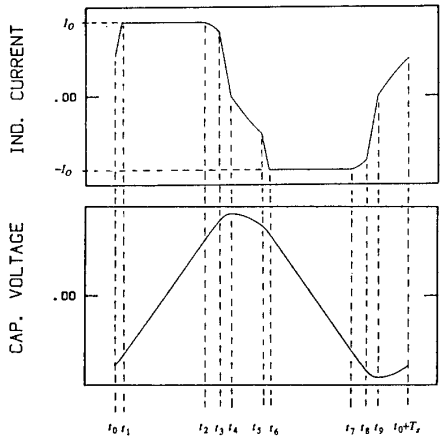

Fig. 8 Inductor current and capacitor voltage waveforms for operation mode III.

III. STEADY STATE ANALYSIS

The steady state voltage and current responses of the converter can be determined from the responses of its circuit modes. The transition currents and voltages between circuit modes uniquely determine the steady state current and voltage waveforms, which can be described by state-plane parameters such as $v_{nc}(t_0)$, $i_{nl}(t_0)$, $v_{nc}(t_1)$, $i_{nl}(t_1)$ . . . in the state-plane diagram. These state-plane parameters are functions of switching frequency, duty ratio, output current and converter gain.

In order to determine the control characteristics of the converter for given values of switching frequency and output current, converter gain m and duty ratio d have to be solved simultaneously from the state-plane parameters. In this section, we derive the relations among state-plane parameters and give the duty ratio as a function of these parameters for each mode of operation.

3.1 Operation Mode I

The time interval for each circuit mode over a half of a switching period can be expressed in terms of state-plane parameters. From the state-plane diagram shown in Fig. 5 (a), these time intervals can be expressed by

$$\omega_o(t_1-t_0) = \beta_{01} = \tan^{-1}\frac{I_{no}}{1-v_{nc}(t_1)} \tag{7}$$

$$\omega_o(t_2-t_1) = \frac{v_{nc}(t_2)-v_{nc}(t_1)}{I_{no}} \tag{8}$$

$$\omega_o(t_3-t_2) = \beta_{23} = \tan^{-1}\frac{I_{no}}{1+v_{nc}(t_2)} \tag{9}$$

Substituting Eq. (3) into Eqs. (7) and (8), we obtain the following equations:

$$\omega_o(t_1-t_0) = \tan^{-1}\frac{I_{no}}{1+v_{nc}(t_2)} \tag{10}$$

$$\omega_o(t_2-t_1) = \frac{2v_{nc}(t_2)}{I_{no}} \tag{11}$$

Since transistor T_1 is turned off at t_2, using Eqs. (10) and (11), the duty ratio d can be obtained from

$$d = \frac{t_2-t_0}{T_s/2} = \frac{f_{ns}}{\pi}\left[\tan^{-1}\frac{I_{no}}{1+v_{nc}(t_2)} + \frac{2v_{nc}(t_2)}{I_{no}}\right] \tag{12}$$

where $$f_{ns} = \frac{f_s}{f_o} = \frac{2\pi}{\omega_o T_s} \tag{13}$$

3.2 Operation Mode II

Using the state-plane diagram shown in Fig. 5(b), we can express the time interval for each circuit mode by

$$\omega_o(t_1-t_0) = \beta_{01} = \tan^{-1}\frac{I_{no}}{1-v_{nc}(t_1)} - \tan^{-1}\frac{i_{nl}(t_0)}{1-v_{nc}(t_0)} \quad (14)$$

$$\omega_o(t_2-t_1) = \frac{v_{nc}(t_2)-v_{nc}(t_1)}{I_{no}} \quad (15)$$

$$\omega_o(t_3-t_2) = \beta_{23} = \tan^{-1}\frac{I_{no}}{1+v_{nc}(t_2)} \quad (16)$$

$$\omega_o(t_4-t_3) = \beta_{34} \quad (17)$$

Adding Eqs. (14) to (17) together, we obtain the following equation:

$$\frac{\pi}{f_{ns}} = \tan^{-1}\frac{I_{no}}{1-v_{nc}(t_1)} - \tan^{-1}\frac{i_{nl}(t_0)}{1-v_{nc}(t_0)} + \beta_{34} + \frac{v_{nc}(t_2)-v_{nc}(t_1)}{I_{no}} + \tan^{-1}\frac{I_{no}}{1+v_{nc}(t_2)} \quad (18)$$

Since the state-plane diagram is symmetrical with respect to the origin, $i_{nl}(t_0)$ and $v_{nc}(t_0)$ can be expressed by

$$i_{nl}(t_0) = \left[\sqrt{I_{no}^2+[1+v_{nc}(t_2)]^2} - 2\right]\sin\beta_{34} \quad (19)$$

$$v_{nc}(t_0) = -1 - \left[\sqrt{I_{no}^2+[1+v_{nc}(t_2)]^2} - 2\right]\cos\beta_{34} \quad (20)$$

From the state-plane diagram, the value of $v_{nc}(t_1)$ can be determined by

$$v_{nc}(t_1) = 1 - \sqrt{i_{nl}^2(t_0) + [1-v_{nc}(t_0)]^2 - I_{no}^2} \quad (21)$$

Since f_{ns} is assumed to be specified, Eqs. (18) to (21) can be solved numerically once I_{no} and $v_{nc}(t_2)$ are given. The duty ratio d for this mode of operation is given by

$$d = \frac{f_{ns}}{\pi}\left[\tan^{-1}\frac{I_{no}}{1-v_{nc}(t_1)} - \tan^{-1}\frac{i_{nl}(t_0)}{1-v_{nc}(t_0)} + \frac{v_{nc}(t_2)-v_{nc}(t_1)}{I_{no}}\right] \quad (22)$$

3.3 Operation Mode III

The steady state responses of the converter in this mode of operation can be determined from the state-plane diagram shown in Fig. 5 (c). Adding each time interval over a half of a switching period, we obtain the following equation:

$$\frac{\pi}{f_{ns}} = \tan^{-1}\frac{I_{no}}{1-v_{nc}(t_1)} - \tan^{-1}\frac{i_{nl}(t_0)}{1-v_{nc}(t_0)} + \frac{1-v_{nc}(t_1)}{I_{no}} + \beta_{23} + \tan^{-1}\frac{i_{nl}(t_3)}{1+v_{nc}(t_3)} + \beta_{45} \quad (23)$$

Using the geometric properties of the state-plane diagram, we obtain the following equations:

$$i_{nl}(t_0) = \left[\sqrt{I_{no}^2\cos^2\beta_{23} + (2+I_{no}\sin\beta_{23})^2} - 2\right]\sin\beta_{45} \quad (24)$$

$$v_{nc}(t_0) = -1 - \left[\sqrt{I_{no}^2\cos^2\beta_{23} + (2+I_{no}\sin\beta_{23})^2} - 2\right]\cos\beta_{45} \quad (25)$$

$$v_{nc}(t_1) = 1 - \sqrt{i_{nl}^2(t_0) + [1-v_{nc}(t_0)]^2 - I_{no}^2} \quad (26)$$

Eqs. (23) to (26) can be numerically solved once I_{no}, β_{23} and f_{ns} are given. Analogous to the operation mode II, the duty ratio d can be expressed by

$$d = \frac{f_{ns}}{\pi}\left[\tan^{-1}\frac{I_{no}}{1-v_{nc}(t_1)} - \tan^{-1}\frac{i_{nl}(t_0)}{1-v_{nc}(t_0)} + \frac{1-v_{nc}(t_1)}{I_{no}} + \beta_{23}\right] \quad (27)$$

IV. PERFORMANCE CHARACTERISTICS

From the circuit configuration given in Fig. 1 or 2, the normalized output voltage V_{no}, which is equal to the converter gain, m, can be derived from the following equation:

$$V_{no} = m = \frac{2}{T_s}\int_{t_0}^{t_0+\frac{T_s}{2}} |v_{naa'}|\, dt \quad (28)$$

In all modes of operation, $v_{aa'}$ becomes non-zero only in time interval $[t_1,t_2]$ over the first half of the switching period. Therefore, Eq. (28) can be rewritten as

$$m = \frac{2}{T_s}\int_{t_1}^{t_2}(1-v_{nc})\, dt \quad (29)$$

Since the capacitor voltage is linearly charged by I_O during time interval $[t_1,t_2]$, we obtain the solution of Eq. (29) by

$$m = \frac{f_{ns}}{\pi I_{no}}\left[v_{nc}(t_2) - v_{nc}(t_1) - \frac{v_{nc}^2(t_2)-v_{nc}^2(t_1)}{2}\right] \quad (30)$$

Substituting $v_{nc}(t_1)$ from Eq. 3 into Eq. (30), we obtain

$$m = \frac{2f_{ns}v_{nc}(t_2)}{\pi I_{no}} \quad (31)$$

Using Eqs. (13) and (31), we can express converter gain m in terms of I_{no} and d, assuming that f_{ns} is given.

In the operation mode II, converter gain m can be derived numerically from Eqs. (17) to (21) and (30) in terms

of I_{no} and d for a given value of f_{ns}. Thus, the control characteristics for this mode of operation can be obtained.

In the operation mode III, the relation between converter gain m and duty ratio d can be derived numerically from Eqs. (23) to (27) once f_{ns} and I_{no} are given. Therefore, we can obtain the control characteristics of the converter for this mode of operation.

Combining the control characteristics for all three modes of operation, we can obtain the overall control characteristics of the present converter which are given in Figs. 9 and 10 for f_{ns} equal to 0.75 and 0.85, respectively. From these curves, we can see that the present converter requires a narraw range of duty ratios for a load change from I_{no} = 0.2 to I_{no} = 1.0. Besides the control characteristics, the normalized transistor current at a switching point for each load condition can be obtained in the similar fashion. The curves for these values are given in Figs. 11 and 12 for f_{ns} equal to 0.75 and 0.85, respectively. It can be seen from these figures that, unlike PWM converters, the transistors are turned off at currents equal to or less than the output current.

V. DESIGN EXAMPLE

In the converter design, the control characteristic curves shown in Fig. 9 or 10 can be used, depending on whether the value of 0.75 or 0.85, respectively, is selected for f_{ns}. In this design example, we choose f_{ns} = 0.75, so that the control characteristic curves shown in Fig. 9 will be used. The following specifications are given for the design:

Min/Max Input Voltage	120/160	*Volts*
Output Voltage	120	*Volts*
Min/Max Output Power	300/1500	*Watts*
Switching Frequency	100	*KHz*

Based on the above specifications, the minimum and maximum output currents are 2.5 and 12.5 Amperes, respectively. If the full-bridge configuration shown in Fig. 2 is used, the value of V_g is the same as that of the input voltage. From the design point of view, the minimum output voltage $V_{g,min}$ and the maximum output current $I_{O,max}$ represent the worst case condition for the converter design. For this condition, we select from Fig. 9 the maximum converter gain $m_{\max}$ = 0.8 and $I_{no,max}$ = 1.0. Since $m_{\max}$ and $V_{g,min}$ are given, the transformer ratio 1:n can be ontained from the following equation:

$$n = \frac{V_O}{m_{\max} V_{g,min}} \tag{32}$$

Substituting all parameters into Eq. (32), we have n equal to 1.25. The characteristic impedance Z_o of the tank circuit can be obtained by

$$Z_o = \frac{I_{no,max} V_{g,min}}{n\, I_{O,max}} \tag{33}$$

From the above equation, Z_o can be obtained and is equal to 7.68 Ω. Since f_{ns} = 0.75 and f_s = 100 KHz, the resonant frequency f_o equals 133.33 KHz. Knowing the values of Z_o and f_o, the values of inductor L and capacitor C can be calculated and are equal to 9.17 μH and 155.4 nF, respectively. From the maximum input voltage $V_{g,max}$, the minimum converter gain $m_{\min}$ is determined by

$$m_{\min} = \frac{V_O}{n\, V_{g,max}} \tag{34}$$

which is equal to 0.6.

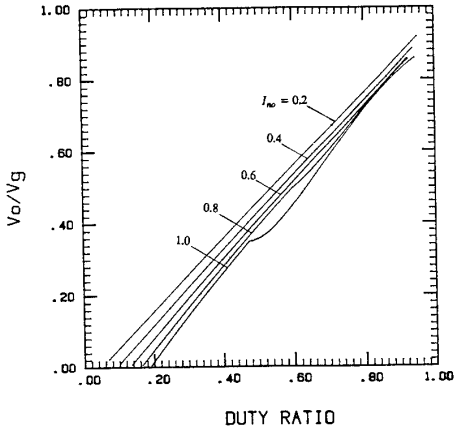

Fig. 9 Control characteristics of the converter for f_{ns} = 0.75.

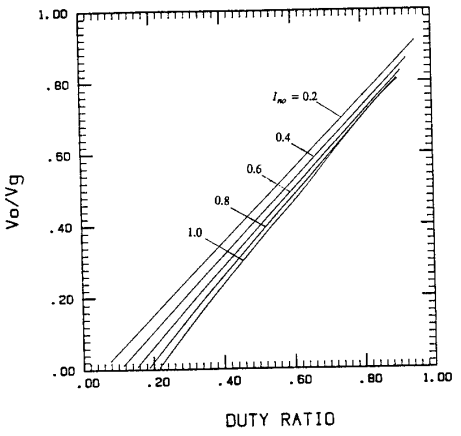

Fig. 10 Control characteristics of the converter for f_{ns} = 0.85.

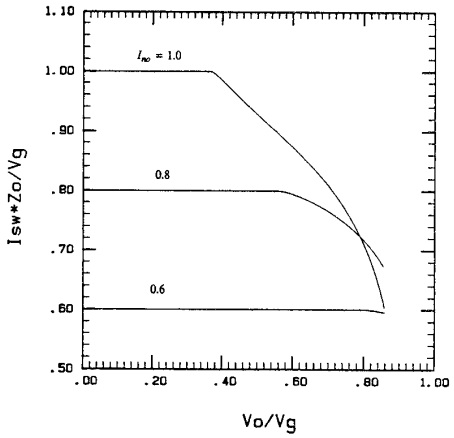

Fig. 11 Normalized currents at switching points for $f_{ns} = 0.75$.

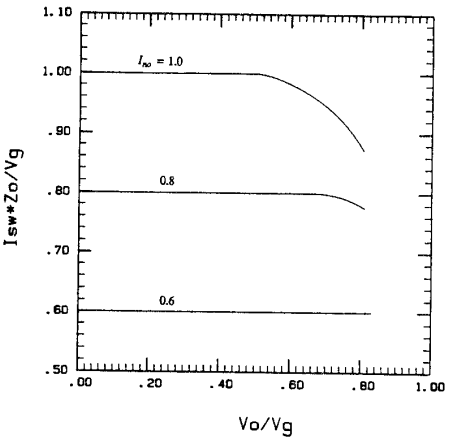

Fig. 12 Normalized currents at switching points for $f_{ns} = 0.85$.

To verify our theoretical work, we use PSPICE to simulate the converter circuit with circuit parameters given above. We have performed the simulations under four different conditions: $V_{g,min}$ and $I_{O,min}$; $V_{g,min}$ and $I_{O,max}$; $V_{g,max}$ and $I_{O,min}$; and $V_{g,max}$ and $I_{O,max}$. The results for these conditions are given in Figs. 13, 14, 15 and 16, respectively. It can be seen from these results that the inductor currents are clamped at nI_O, and the currents at turn-off switching points are less than or equal to nI_O. Thus, our theoretical work is confirmed by these results.

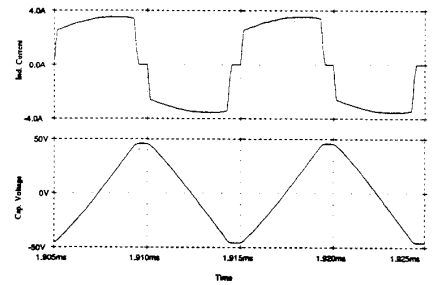

Fig. 13 Inductor current and capacitor voltage from PSPICE simulation at V_g = 120 *Volts* and I_O = 2.5 *Amperes*.

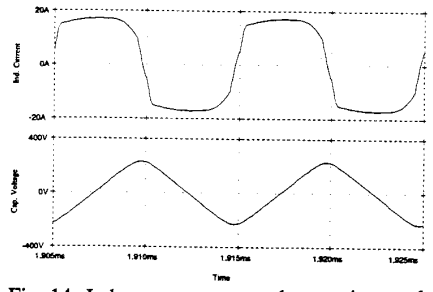

Fig. 14 Inductor current and capacitor voltage from PSPICE simulation at V_g = 120 *Volts* and I_O = 12.5 *Amperes*.

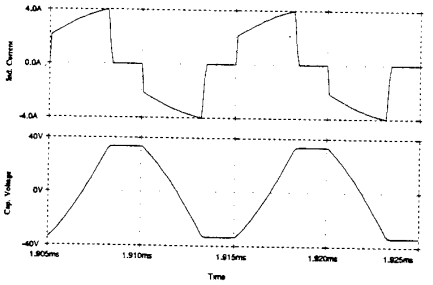

Fig. 15 Inductor current and capacitor voltage from PSPICE simulation at V_g = 160 *Volts* and I_O = 2.5 *Amperes*.

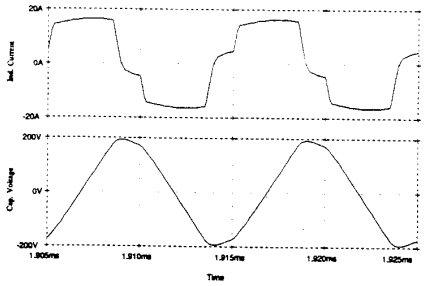

Fig. 16 Inductor current and capacitor voltage from PSPICE simulation at V_g = 160 *Volts* and I_O = 12.5 *Amperes*.

VI. CONCLUSION

For applications that require constant frequency operation, the present converter has an advantage over PWM converters in that the transistors are turned on and off at lower currents. Consequently, the present converter has lower switching losses than those of the PWM converters. In addition, the converter has the lowest possible peak current stress among converters. Besides the current stress advantage, we can see from the control characteristic curves shown in Figs. 9 and 10 that, for $m > 0.5$, this converter requires a narrower range of duty ratios than those in the conventional SRCs operating at a constant frequency [3] for the same range of load change.

References:

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