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Power Factor Correction Handbook

Power Factor Correction (PFC) Handbook

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Preface

Choices for the power factor correction solutions range from passive circuits to a variety of active circuits. Depending on the power level and other specifics of the application, the appropriate solution will differ. The advances in the discrete semiconductors in recent years, coupled with availability of lower priced control ICs, have made the active PFC solutions more appropriate in a wider range of applications. When evaluating the PFC solutions, it is important to evaluate them in the context of full system implementation cost and performance.

In this handbook, a number of different PFC approaches are evaluated for a 120 W (12 V, 10 A) application. By providing step−by−step design guidelines and system level comparisons, it is hoped that this effort will help the power electronics designers select the right approach for their application.

Chapter 1 provides a comprehensive overview of PFC circuits and details of operation and design considerations for commonly used PFC circuits.

Chapter 2 describes the methodology used for comparing different active PFC approaches for a given application (12 V, 10 A output). It also introduces the proposed approaches.

Chapter 3 contains the design guidelines, discussion and salient operational results for the two variations of the critical conduction mode topologies (constant output and follower boost versions).

Chapter 4 contains the design guidelines, discussion and salient operational results for the two continuous conduction mode topologies (traditional CCM boost and CCM isolated flyback).

Chapter 5 provides a detailed analysis of the results obtained from the four different implementations for the same applications. Comparative analyses and rankings are provided for the topologies for given criteria. It also includes guidelines for the designers based on the results described in the previous chapters.

Chapter 6 provides recommendations to meet FCC limits on line conducted EMI for the topologies presented in the previous chapters.

CHAPTER 1

Overview of Power Factor Correction Approaches

ABSTRACT

Power factor correction shapes the input current of off−line power supplies to maximize the real power available from the mains. Ideally, the electrical appliance should present a load that emulates a pure resistor, in which case the reactive power drawn by the device is zero. Inherent in this scenario is the freedom from input current harmonics. The current is a perfect replica of the input voltage (usually a sine wave) and is exactly in phase with it. In this case the current drawn from the mains is at a minimum for the real power required to perform the needed work, and this minimizes losses and costs associated not only with the distribution of the power, but also with the generation of the power and the capital equipment involved in the process. The freedom from harmonics also minimizes interference with other devices being powered from the same source.

Another reason to employ PFC in many of today's power supplies is to comply with regulatory requirements. Today, electrical equipment in Europe must comply with the European Norm EN61000−3−2. This requirement applies to most electrical appliances with input power of 75 W or greater, and it specifies the maximum amplitude of line−frequency harmonics up to and including the 39th harmonic. While this requirement is not yet in place in the US, power supply manufacturers attempting to sell products worldwide are designing for compliance with this requirement.

Definition

Power factor correction is simply defined as the ratio of real power to apparent power, or:

$$PF = \frac{\text{Real Power}}{\text{Apparent Power}}$$

where the real power is the average, over a cycle, of the instantaneous product of current and voltage, and the apparent power is the product of the rms value of current times the rms value of voltage. If both current and voltage are sinusoidal and in phase, the power factor is 1.0. If both are sinusoidal but not in phase, the power factor is the cosine of the phase angle. In elementary courses in electricity, this is sometimes taught as the definition of power factor, but it applies only in the special case, where both the current and voltage are pure sine waves. This occurs when the load is composed of resistive, capacitive and inductive elements and all are linear (invariant with current and voltage).

Switched−mode power supplies present a non−linear impedance to the mains, as a result of the input circuitry. The input circuit usually consists of a half−wave or full−wave rectifier followed by a storage capacitor. The capacitor maintains a voltage of approximately the peak voltage of the input sine wave until the next peak comes along to recharge it. In this case, current is drawn from the input only at the peaks of the input waveform, and this pulse of current must contain enough energy to sustain the load until the next peak. It does this by dumping a large charge into the capacitor during a short time, after which the capacitor slowly discharges the energy into the load until the cycle repeats. It is not unusual for the current pulse to be 10% to 20% of the cycle duration, meaning that the current during the pulse must be 5 to 10 times the average current in magnitude. Figure 1 illustrates this situation.

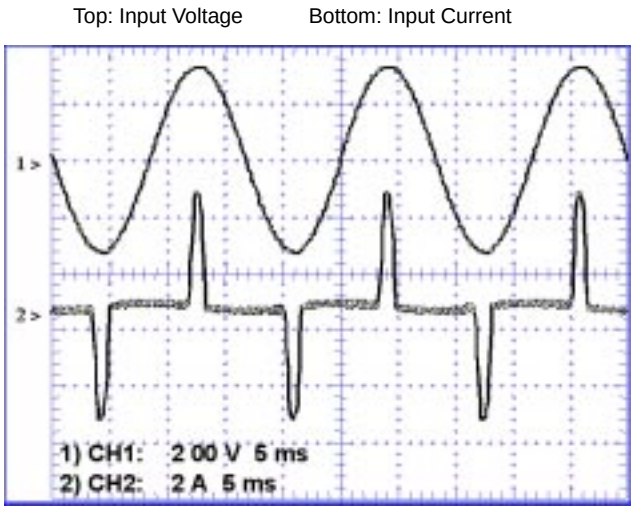


Figure 1. Input Characteristics of a Typical Switched−Mode Power Supply without PFC

Note that the current and voltage can be perfectly in phase, in spite of the severe distortion of the current waveform. Applying the "cosine of the phase angle" definition would lead to the erroneous conclusion that this power supply has a power factor of 1.0.

Figure 2 shows the harmonic content of the current waveform. The fundamental (in this case 60 Hz) is shown with a reference amplitude of 100%, and the higher harmonics are then given with their amplitudes shown as percentages of the fundamental amplitude. Note that the even harmonics are barely visible; this is a result of the symmetry of the waveform. If the waveform consisted of infinitesimally narrow and infinitely high pulses (known to mathematicians as "delta" functions) the spectrum would be flat, meaning that all harmonics would be of equal amplitude. Incidentally, the power factor of this power supply is approximately 0.6.

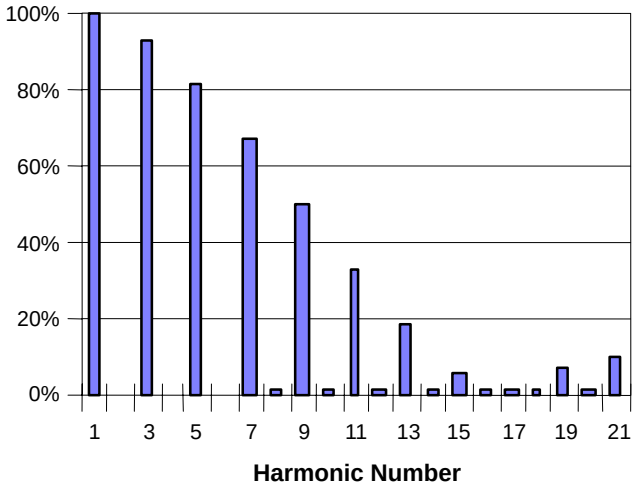
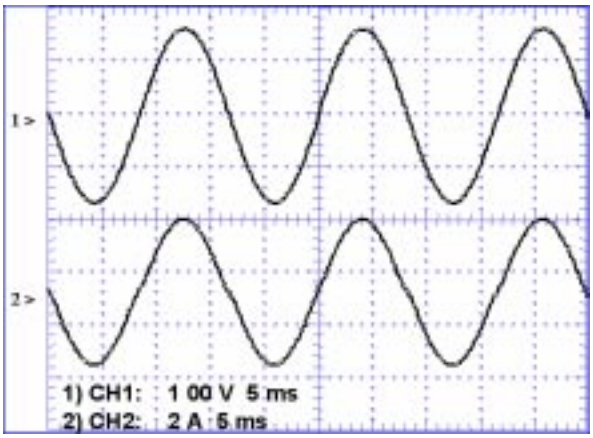


Figure 2. Harmonic Content of the Current Waveform in Figure 1

For reference, Figure 3 shows the input of a power supply with perfect power factor correction. It has a current waveform that mimics the voltage waveform, both in shape and in phase. Note that its input current harmonics are nearly zero.



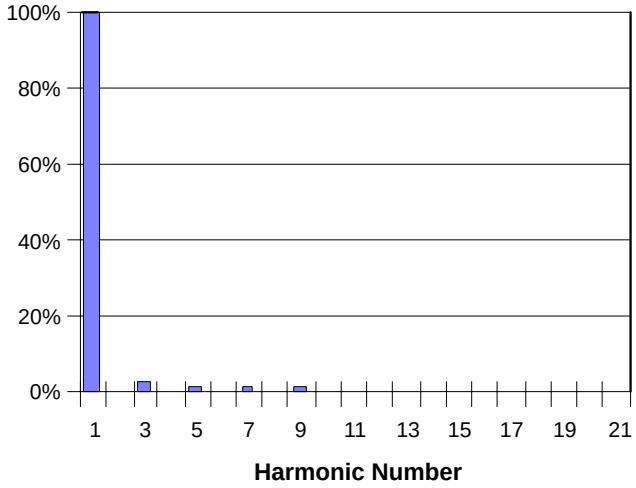


Figure 3. Input Characteristics of a Power Supply with Near−Perfect PFC

Power Factor Correction vs. Harmonic Reduction

It is clear from the previous illustrations that high power factor and low harmonics go hand−in−hand. There is not a direct correlation however, the following equations link total harmonic distortion to power factor.

$$THD(\%) = 100 * \sqrt{\frac{1}{Kd^2} - 1}$$

where Kd is the distortion factor and is equal to:

$$Kd = \frac{1}{\sqrt{1 + \left(\frac{THD(\%)}{100}\right)^2}}$$

Therefore, when the fundamental component of the input current is in phase with the input voltage, $K\theta = 1$ and:

$$PF = Kd * K\theta = Kd$$

As illustrated, a perfectly sinusoidal current could have a poor power factor, simply by having its phase not in line with the voltage.

Then:

$$PF = \frac{1}{\sqrt{1 + \left(\frac{THD(\%)}{100}\right)^2}}$$

A 10% THD corresponds then to a Power Factor approximately equal to 0.995.

It is clear that specifying limits for each of the harmonics will do a better job of controlling the “pollution” of the input current, both from the standpoint of minimizing the current and reducing interference with other equipment. So, while the process of shaping this input current is commonly called “power factor correction,” the measure of its success in the case of the international regulations is the harmonic content.

Types of Power Factor Correction

The input characteristics shown in Figure 3 were obtained with “active” power factor correction, using a switched−mode boost converter placed between the input rectifier and the storage capacitor, with the converter controlled by a relatively complex IC and its attendant

circuitry in a manner to shape the input current to match the input voltage waveform. This is the most popular type of PFC used in today's power supplies. It isn't the only type, however. There are no rules demanding that the PFC be accomplished by active circuits (transistors, ICs, etc.). Any method of getting the harmonics below the regulatory limits is fair game. It turns out that one inductor, placed in the same location as the active circuit, can do the job. An adequate inductor will reduce the peaks of the current and spread the current out in time well enough to reduce the harmonics enough to meet the regulations. This method has been used in some power supplies for desktop personal computers, where the size of the inductor (approximately a 50 mm^3) and its weight (due to its iron core and copper winding) are not objectionable. At power levels above the typical personal computer (250 W), the size and weight of the passive approach becomes unpopular. Figure 4 shows the input characteristics of three different 250 W PC power supplies, all with the current waveforms at the same scale factor.

Waveforms:
1. Input current with no PFC
2. Input current with passive PFC
3. Input current with active PFC
4. Input voltage

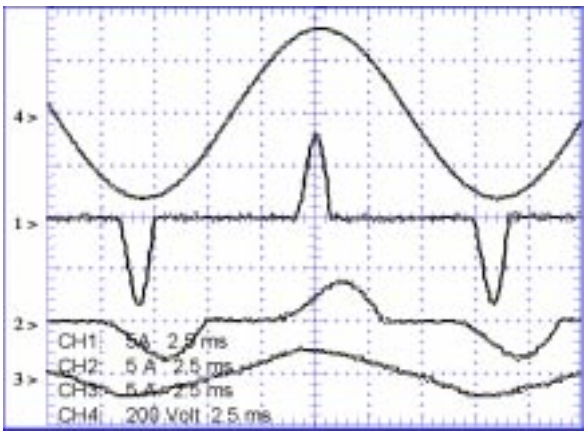


Figure 4. Input Characteristics of PC Power Supplies with Different PFC Types (None, Passive, and Active)

Input Line Harmonics Compared to EN1000−3−2

Figure 5 shows the input harmonics of three 250 W PC power supplies, along with the limits according to EN61000−3−2. These limits are for Class D devices, which include personal computers, televisions and monitors. The harmonic amplitudes are proportioned to the input power of these devices. In the case of other products not used in such high volume, the limits are fixed at the values corresponding to 600 W input. The performance of the passive PFC, as shown in this graph, just barely complies with the limit for the third harmonic (harmonic number 3).

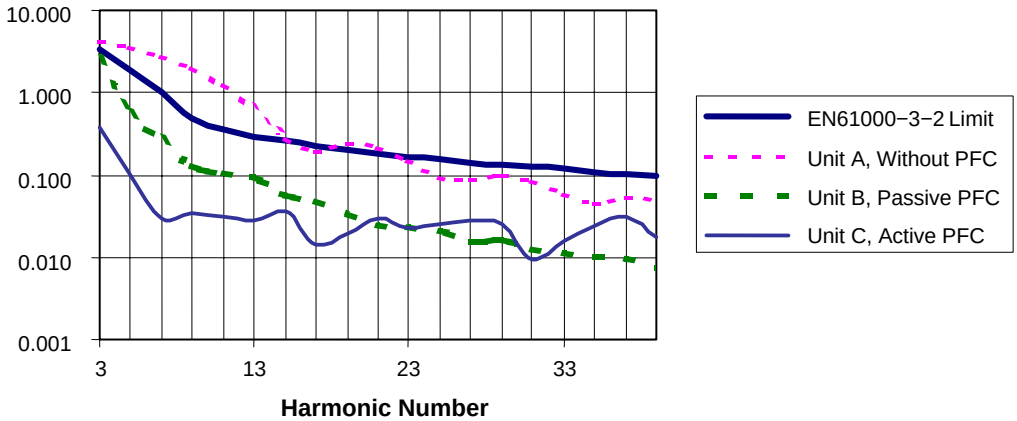


Figure 5. Input Harmonics of Three PC Power Supplies Relative to EN1000−3−2 Limits

Passive PFC

Figure 6 shows the input circuitry of the PC power supply with passive PFC. Note the line−voltage range switch connected to the center tap of the PFC inductor. In the 230 V position (switch open) both halves of the inductor winding are used and the rectifier functions as a full−wave bridge. In the 115 V position only the left half of the inductor and the left half of the rectifier bridge are used, placing the circuit in the half−wave doubler mode. As in the case of the full−wave rectifier with 230 Vac input, this produces 325 Vdc at the output of the rectifier. This 325 Vdc bus is of course unregulated and moves up and down with the input line voltage.

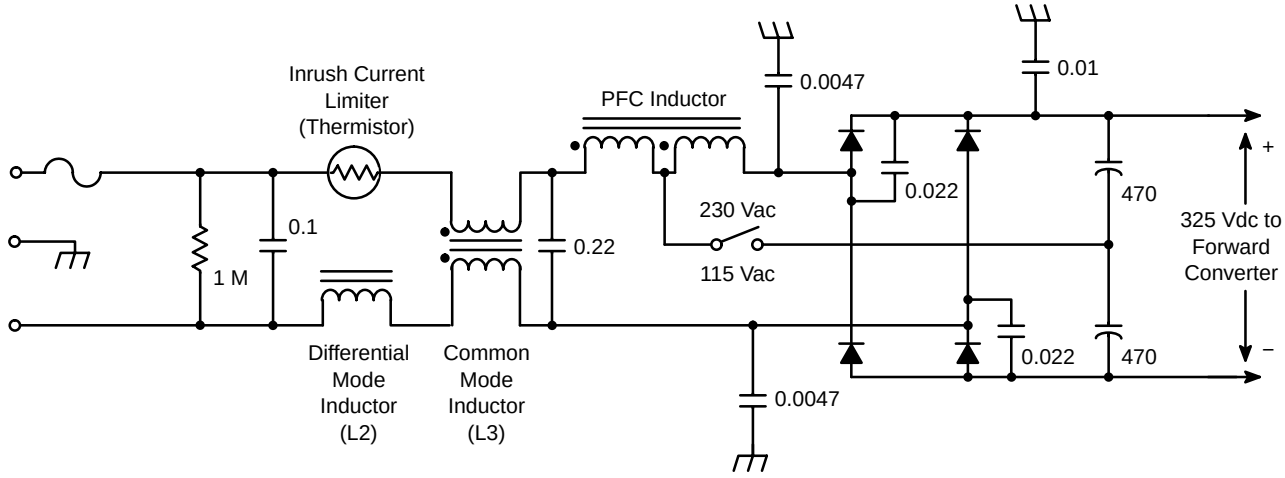


Figure 6. Passive PFC in a 250 W PC Power Supply

The passive PFC circuit suffers from a few disadvantages despite its inherent simplicity. First, the bulkiness of the inductor restricts its usability in many applications. Second, as mentioned above, for worldwide operation, a line−voltage range switch is required. Incorporation of the switch makes the appliance/system prone to operator errors if the switch selection is not properly made. Finally, the voltage rail not being regulated leads to a cost and efficiency penalty on the dc−dc converter that follows the PFC stage.

Critical Conduction Mode (CRM) Controllers

Critical Conduction Mode or Transitional Mode controllers are very popular for lighting and other lower power applications. These controllers are very simple to use as well as very inexpensive. A typical application circuit is shown in Figure 7.

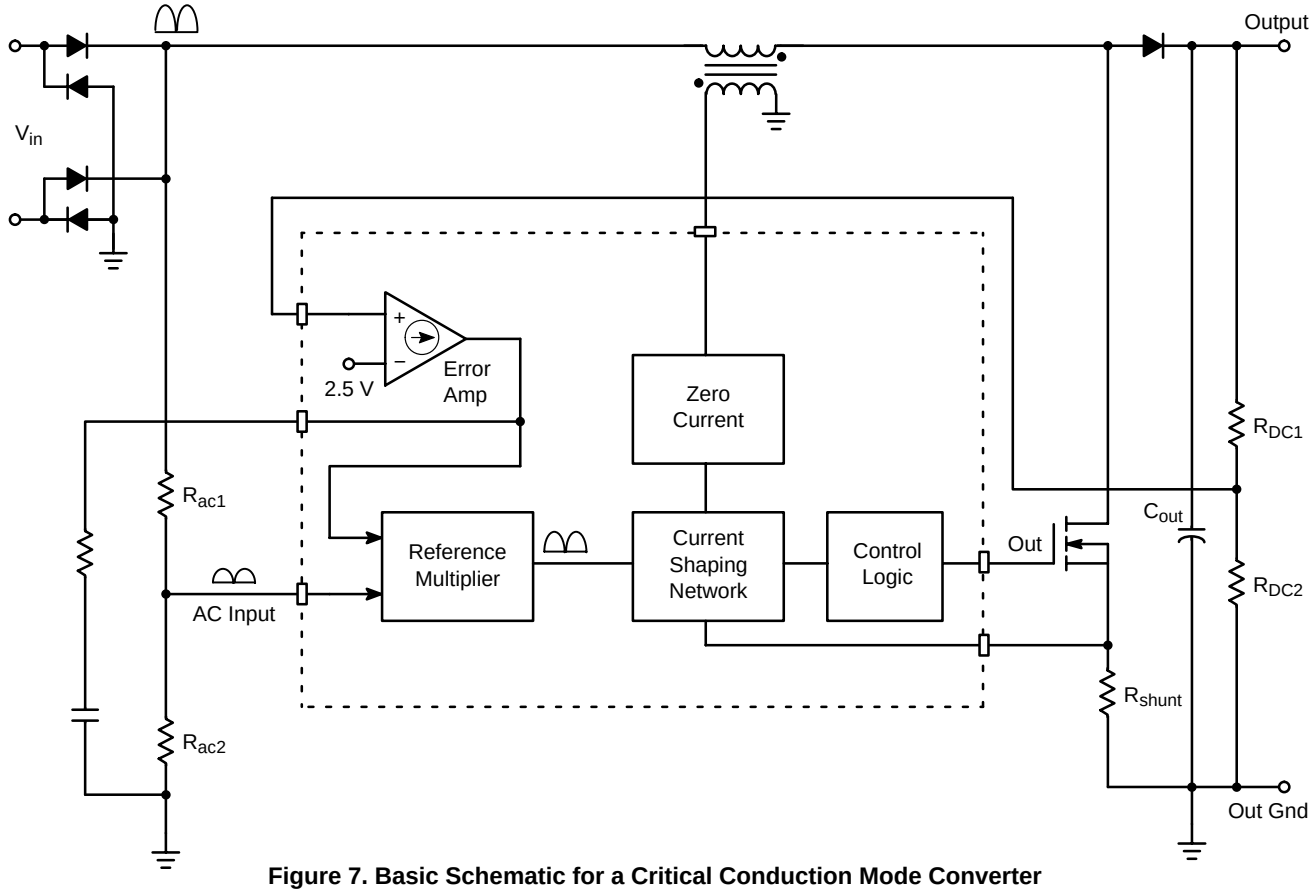


Figure 7. Basic Schematic for a Critical Conduction Mode Converter

The basic CRM PFC converter uses a control scheme similar to that shown above. An error amplifier with a low frequency pole provides an error signal into the reference multiplier. The other input to the multiplier is a scaled version of the input rectified ac line voltage. The multiplier output is the product of the near dc signal from the error amplifier and the full−wave rectified sine waveform at the ac input.

The signal out of the multiplier is also a full−wave rectified sine wave that is scaled by a gain factor (error signal), and is used as the reference for the input voltage. This amplitude of this signal is adjusted to maintain the proper average power to cause the output voltage to remain at its regulated value.

The current shaping network forces the current to follow the waveform out of the multiplier, although the line frequency current signal (after sensing) will be half of the amplitude of this reference. The current shaping network functions as follows:

In the waveforms of Figure 8, Vref is the signal out of the multiplier. This signal is fed into one input of a comparator, with the other input connected to the current waveform.

When the power switch turns on, the inductor current ramps up, until the signal across the shunt reaches the level of Vref. At that point, the comparator changes states and turns off the power switch. With the switch off, the current ramps down until it reaches zero. The zero current sense circuit measures the voltage across the inductor, which will fall to zero when the current reaches zero. At this point, the switch is turned on and the current again ramps up.

This control scheme is referred to as critical conduction and as the name implies, it keeps the inductor current at the borderline limit between continuous and discontinuous conduction. This is important, because the waveshape is always known, and therefore, the relationship between the average and peak current is also known. For a triangular waveform, the average is exactly one half of the peak. This means that the average current signal (Inductor current x Rsense) is at a level of one half of the reference voltage.

The frequency of this type of regulator varies with line and load variations. At high line and light load, the frequency is at a maximum, but it also varies throughout the line cycle.

Pros: Inexpensive chips. Simple to design. No turn−on switching losses. Boost diode selection not as critical.

Cons: Variable frequency. Potential EMI issue requiring an elaborate input filter.

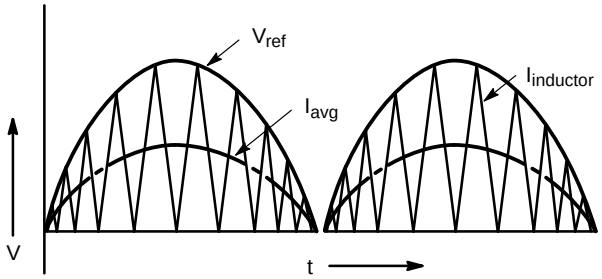


Figure 8. CRM Waveforms

Critical Conduction Without a Multiplier

A novel approach to the critical conduction mode controller is available in an ON Semiconductor chip, MC33260. This chip provides the same input−output function as the controllers described above. However, it accomplishes this without the use of a multiplier [1].

As explained in the previous section, the current waveform for a CRM controller ramps from zero to the reference signal and then slopes back down to zero. The reference signal is a scaled version of the rectified input voltage, and as such can be referred to as k x Vin, where k is a scaling constant from the ac voltage divider and multiplier in a classic circuit. Given this, and knowing the relation of the slope of the inductor with the input voltage, the following are true:

$$Ipk = k \cdot Vin(t) \quad \text{and} \quad Ipk = \Delta I = \frac{Vin(t)}{L} \cdot t_{on}$$

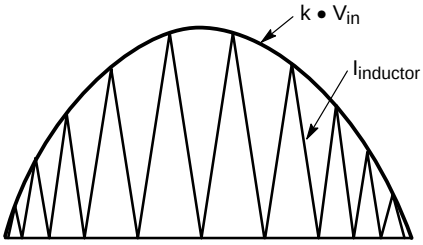


Figure 9. CRM Current Envelope

Equating the peak current for these two equations gives:

$$k \cdot Vin(t) = \frac{Vin(t)}{L} t_{on} \qquad \text{Therefore, } t_{on} = k \cdot L$$

This equation shows that t_{on} is a constant for a given reference signal (k x Vin). T_{off} will vary throughout the cycle, which is the cause of the variable frequency that is necessary for critical conduction. The fact that the on time is constant for a given line and load condition is the basis for this control circuit.

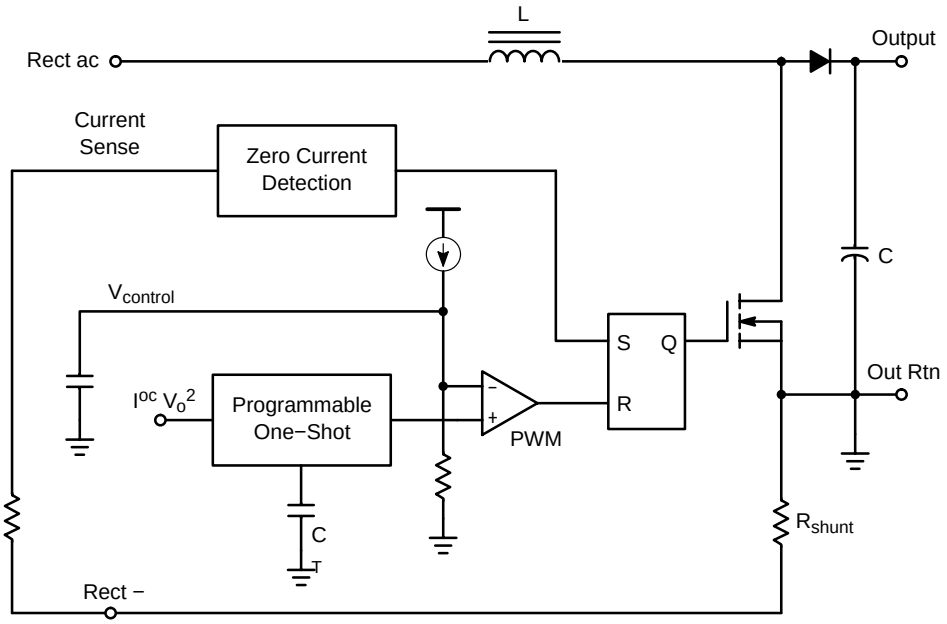


Figure 10. Simplified Schematic of CRM Controller without Multiplier

In the circuit of Figure 10, the programmable one−shot timer determines the on time for the power switch. When the on period is over, the PWM switches states and turn off the power switch. The zero current detector senses the inductor current, and when it reaches zero, the switch is turned on again. This creates somewhat different current waveforms but the same dc output as with the classic scheme, without the use of the multiplier.

Since a given value of on time is only valid for a given load and line condition, a low frequency error amplifier for the dc loop is connected to the one−shot. The error signal modifies the charging current and therefore, the on time of the control circuit so that regulation over a wide range of load and line conditions can be maintained.

Follower Boost

The MC33260 contains a number of other features including a circuit that will allow the output voltage to follow the input voltage. This is called follower boost operation. In the follower boost mode, the output voltage is regulated at a fixed level above the peak of the input voltage. In most cases, the output of the PFC converter is connected to a dc−dc converter. The dc−dc converter is generally capable of regulating over a wide range of input voltages, so a constant input voltage is not necessary.

Follower boost operation offers the advantages of a smaller and therefore less expensive inductor, and reduced on−time losses for the power MOSFET [2]. This is normally used in systems where the lowest possible system cost is the main objective.

Pros: Inexpensive chips. Simple to design. No turn−on switching losses. Can operate in follower boost mode. Smaller, cheaper inductor.

Cons: Variable frequency. Potential EMI issue requiring an elaborate input filter.

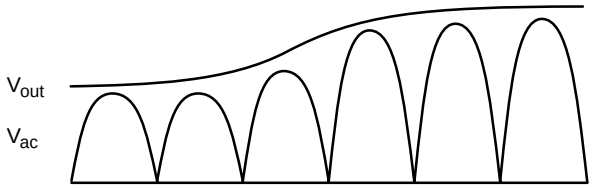


Figure 11. Follower Boost

Continuous Conduction Mode (CCM) Control

The Continuous conduction mode control has been widely used in a broad range of applications because it offers several benefits. The peak current stress is low, and that leads to lower losses in the switches and other components. Also, input ripple current is low and at constant frequency, making the filtering task much easier. The following attributes of the CCM operation need further consideration.

Vrms^2 Control

As is the case with almost all of the PFC controllers on the market, one essential element is a reference signal that is a scaled replica of the rectified input voltage, which is used as a reference for the circuit that shapes the current waveform. These chips all use a multiplier to accomplish this function; however, the multiplier system is more complex than a conventional two−input multiplier.

Figure 12 shows the classic approach to continuous−mode PFC. The boost converter is driven by an average current−mode pulse width modulator (PWM) that shapes the inductor current (the converter's input current) according to the current command signal, V_i. This signal, V_i, is a replica of the input voltage, V_{in}, scaled in magnitude by $V_{DIV} \bullet V_{DIV}$ results from dividing the voltage error signal by the square of the input voltage (filtered by C_f, so that it is simply a scaling factor proportional to the input amplitude).

It may seem unusual that the error signal is divided by the square of the input voltage magnitude. The purpose is to make the loop gain (and hence the transient response) independent of the input voltage. The voltage squared function in the denominator cancels with the magnitude of V_{SIN} and the transfer function of the PWM control (current slope in the inductor is proportional to the input voltage). The disadvantage of this scheme lies in the production variability of the multiplier. This makes it necessary to overdesign the power−handling components, to account for the worst−case power dissipation.

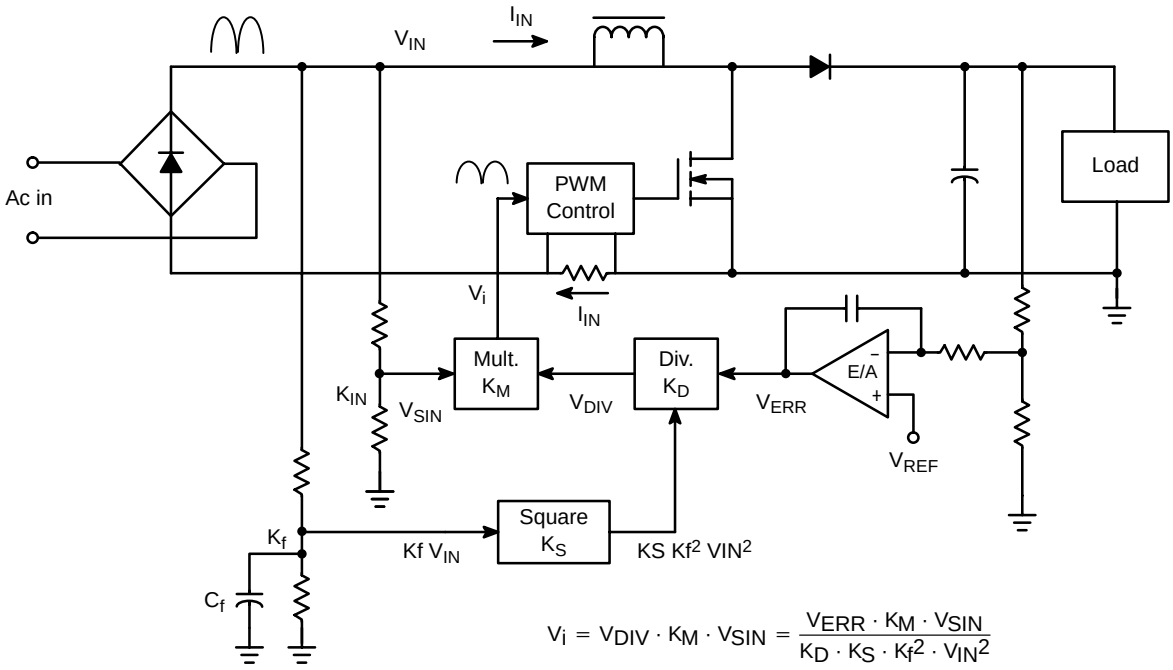


Figure 12. Block Diagram of the Classic PFC Circuit

Average Current Mode Control

The ac reference signal output from the multiplier (Vi) represents the waveshape, phase and scaling factor for the input current of the PFC converter in Figure 12. The job of the PWM control block is to make the average input current match the reference. To do this, a control system called average current mode control is implemented in these controllers [3], [4]. This scheme is illustrated in Figure 13.

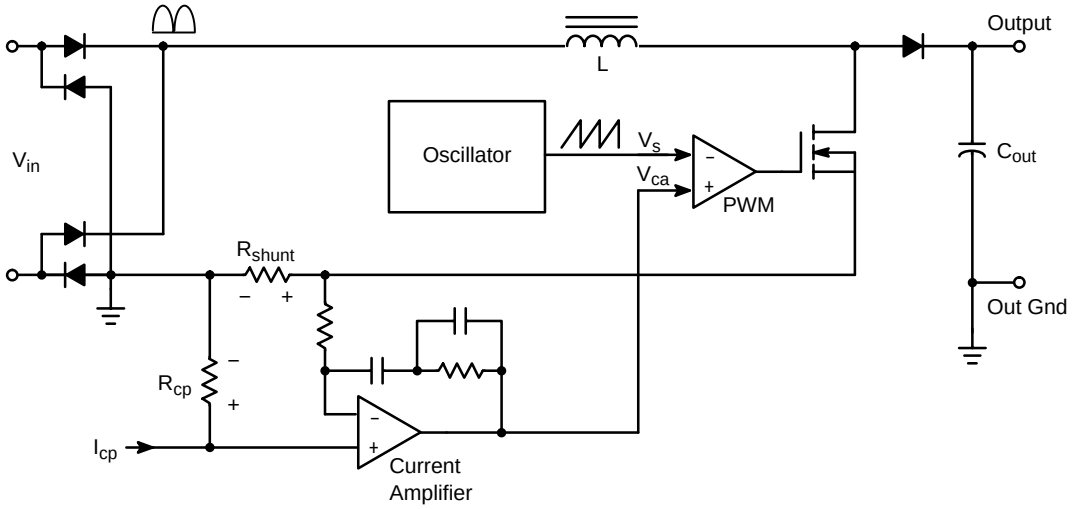


Figure 13. Diagram for Average Current Mode Control Circuit

Average current mode control employs a control circuit that regulates the average current (input or output) based on a control signal I_{cp}. For a PFC controller, I_{cp} is generated by the low frequency dc loop error amplifier. The current amplifier is both an integrator of the current signal and an error amplifier. It controls the waveshape regulation, while the I_{cp} signal controls the dc output voltage. The current I_{cp} develops a voltage across R_{cp}. For the current amplifier to remain in its linear state, its inputs must be equal. Therefore, the voltage dropped across R_{shunt} must equal the voltage across R_{cp}, since there can be no dc current in the input resistor to the non−inverting input of the current amplifier. The output of the current amplifier is a "low frequency" error signal based on the average current in the shunt, and the I_{cp} signal.

This signal is compared to a sawtooth waveform from an oscillator, as is the case with a voltage mode control circuit. The PWM comparator generates a duty cycle based on these two input signals.

Pros: Effective for power levels above 200 W. A "divide by V^{2}" circuit stabilizes loop bandwidth for input variations. Fixed frequency operation. Lower peak high−frequency current than other approaches.

Con: More expensive and complex than critical conduction circuits.

ON Semiconductor NCP1650 Family

ON Semiconductor has recently introduced a new line of highly integrated PFC controllers, with a novel control scheme [5]. This chip's control circuit uses elements from the critical conduction mode units, as well as an averaging circuit not used before in a power factor correction chip. The basic regulator circuit includes a variable ac reference, low frequency voltage regulation error amplifier and current shaping network.

This chip incorporates solutions to several problem that are associated with PFC controllers, including transient response, and multiplier accuracy. It also includes other features that reduce total parts count for the power converter [6].

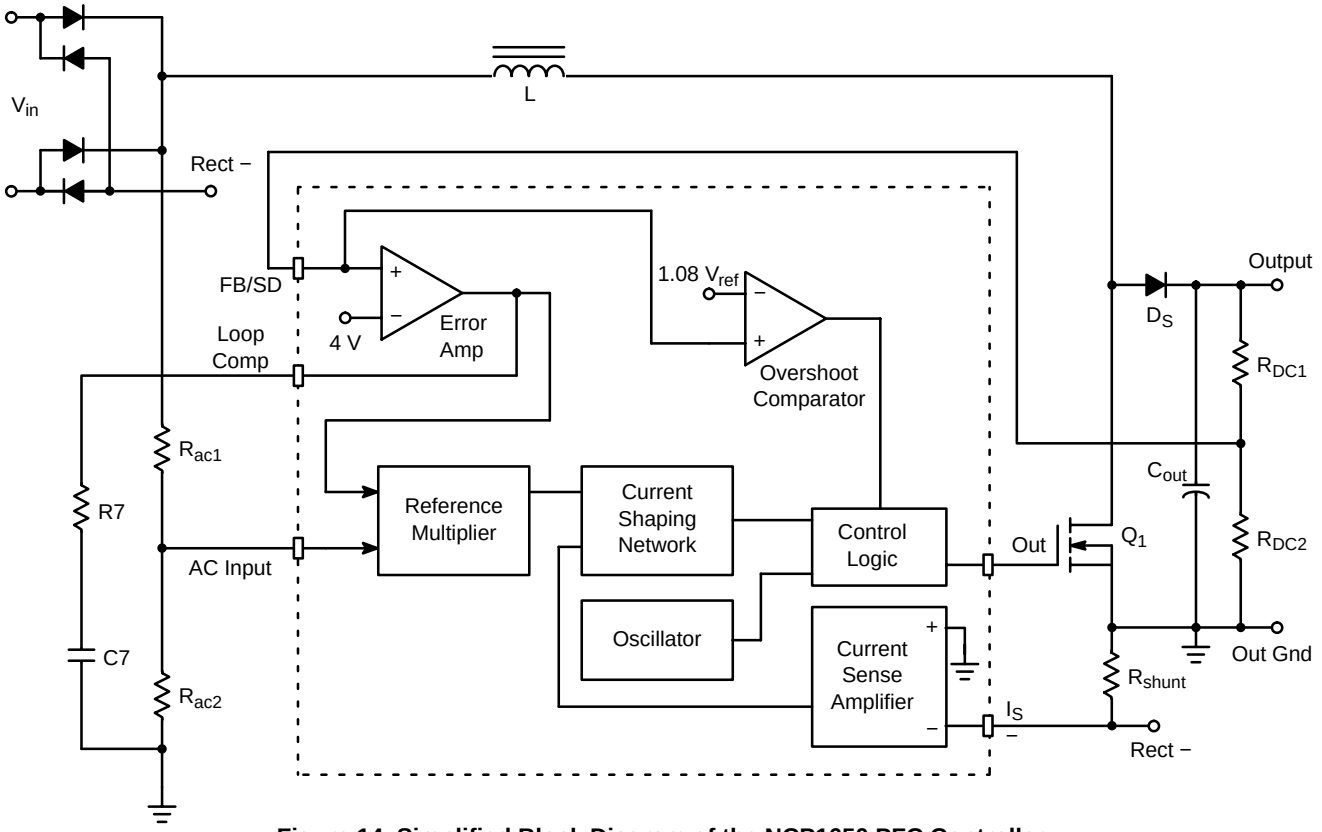


Figure 14. Simplified Block Diagram of the NCP1650 PFC Controller

PFC Loop

The error amplifier has a very low frequency pole associated with it, to provide for a typical overall loop bandwidth of 10 Hz. This signal drives one of the inputs to the reference multiplier. The other multiplier input is connected to the divided down, rectified ac line. The output of this multiplier is a full−wave rectified sine wave that is a scaled copy of the rectified input voltage. This ac reference provides the input signal to the current shaping network that will force the input current to be of the correct waveshape and magnitude for both good power factor and the proper output voltage. The current shaping network uses an average current mode control scheme. However, this circuit is quite different from anything currently available. This is illustrated in Figure 15.

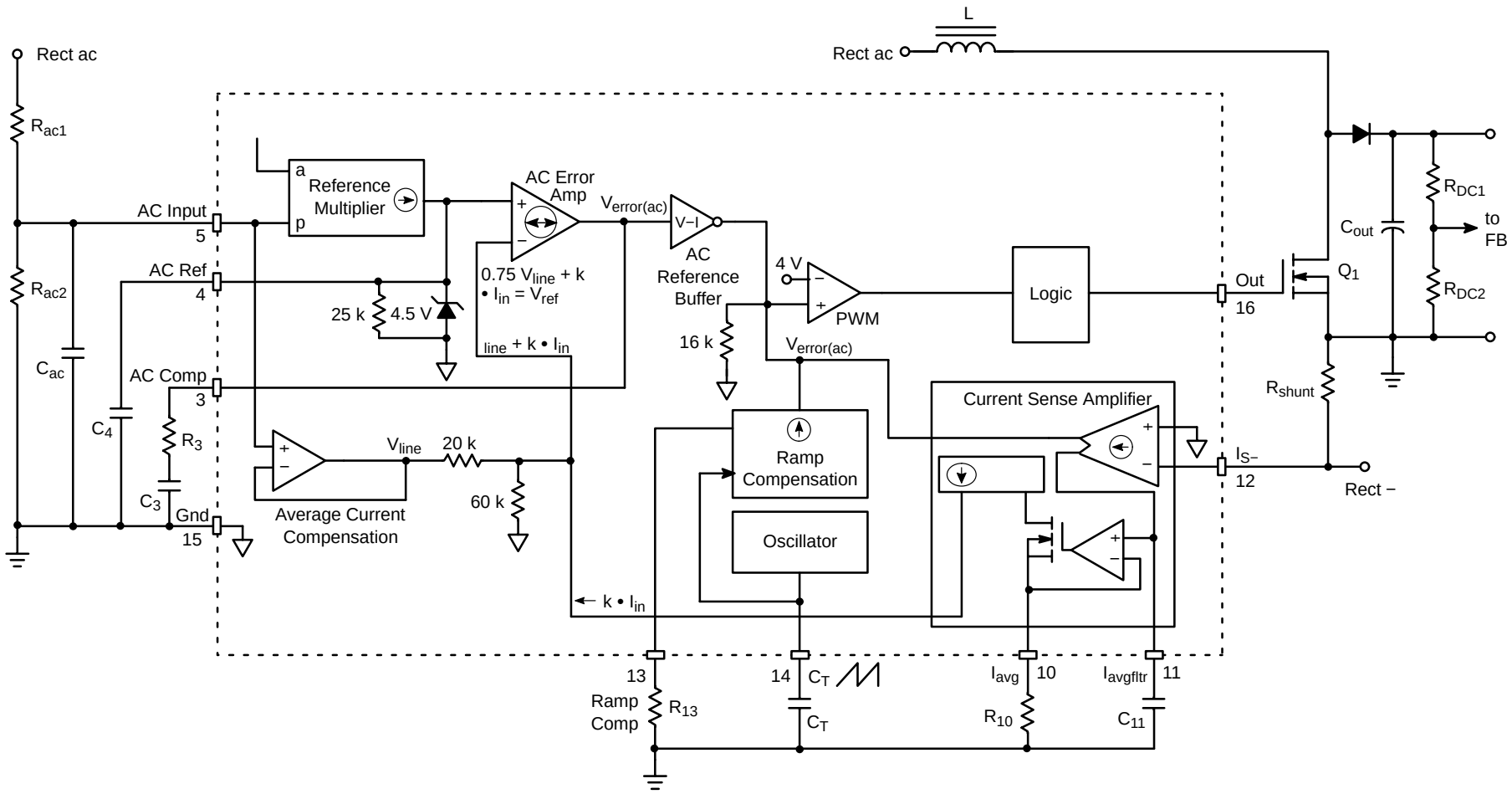


Figure 15. Current Shaping Circuit of the NCP1650 PFC Controller

Current Shaping Circuit

The current shaping network's primary function is to force the average value of the inductor current to follow the reference signal generated by the reference multiplier.

The switch current is converted to a voltage by means of a shunt resistor in series with the source of the MOSFET switch. The shunt resistor is connected from the source (ground) to the return lead of the input rectifiers. This manner of sensing current creates a negative voltage, which is not ideal for an IC, as there are issues with substrate injection if the voltage goes more than a few hundred millivolts below ground. On the other hand, this sense configuration allows both the switch and diode current to be sensed, which is the same as sensing the inductor current.

The current sense amplifier is a transconductance amplifier with two high frequency outputs. It inverts the current signal and feeds one output to a summing node at the input to the PWM. The other output feeds an averaging network on pin 11. This network has an adjustable pole formed by an external capacitor and an internal resistance. The average current is scaled by a buffer stage and summed with a scaled version of the ac input voltage, and is then fed into the input of the ac error amplifier.

The ac error amplifier is the key to maintaining a good input power factor. Since the inputs to this amplifier should be equal, and one is connected to the reference signal, the output of this amplifier must generate a signal that will force the inverting input to match. This means that the averaged switch current will be a good representation of the reference signal, since this is the signal that is applied to the inverting input.

The output of the ac error amplifier is compensated with a pole−zero network. This signal is fed into the inverting reference buffer. The circuit was designed in this manner so that the output of the ac error amplifier would be in a low state at zero output. This allows a convenient means of connecting an external soft−start circuit to the chip.

There are a total of four signals on the input to the PWM that comprise the information used to determine when the switch is turned off. The inverting input to this comparator is a 4.0 V reference. The non−inverting input sums the ac error signal out of the ac reference buffer, the ramp compensation signal and the instantaneous current. When the sum of the last three signals equals 4.0 V the PWM comparator switches, and the power switch is turned off.

Figure 16 illustrates the waveform that results from the summing of the current signal out of the current amplifier and the ramp compensation signal. Both of these signals are in the form of currents, which are summed by injecting them into the same 16 kΩ resistor at the input to the PWM. The third signal is that of the ac error amp buffer. The result of these signals is shown in the bottom waveform in Figure 17.

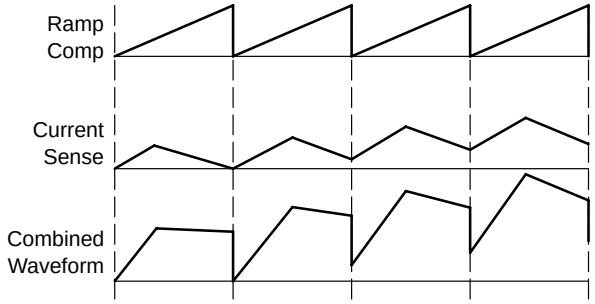


Figure 16. Summed Waveforms

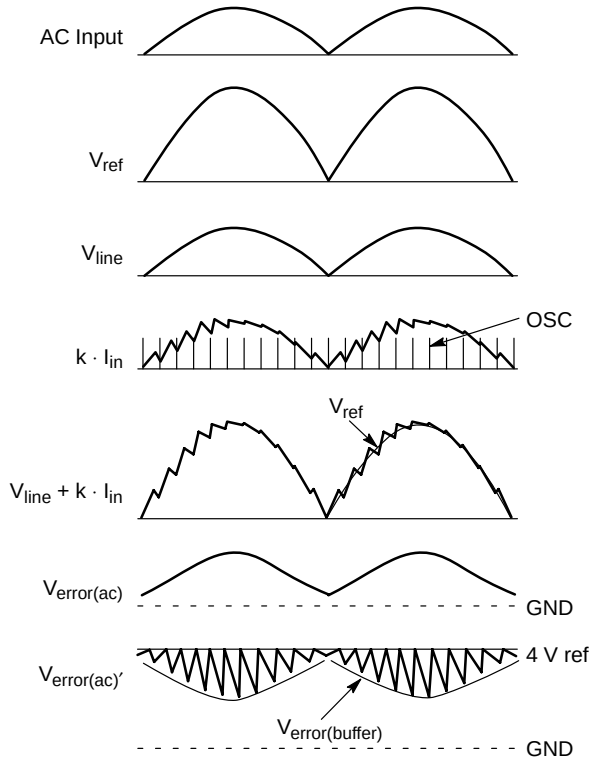


Figure 17. Waveshaping Circuit Waveforms

OTHER FEATURES

Transient Response

As with all PFC units, the voltage error amplifier must be compensated with a very low frequency pole. This assures a good power factor, but doesn't allow for fast transient response. In order to respond quickly to line or load transients the error amplifier in this chip includes a threshold−sensitive gain boost circuit.

In normal operation, the inputs are balanced. However, during a transient event there will be a voltage differential across the inputs. If this differential exceeds a predetermined

level, the output will transition into a high gain mode and quickly adjust the regulation loop until it is close to being in balance. At that point, the amplifier will return to its normal gain and finish bringing the output voltage to its nominal value.

Figure 18 shows the operation of the voltage loop error amplifier. During a load dump, the output voltage of the PFC unit would go high as the loop tried to respond to the new control conditions. As the feedback voltage increases from its nominal voltage of 4.0 V, the output current of the transconductance amplifier increases until it reaches its maximum level of 20 μA. This corresponds to an input voltage of 4.20 V. At this point, it cannot increase further.

When the input voltage reaches 4.24 V, the upper boost circuit is activated. This circuit dumps an additional 250 μA (a factor of 12 greater than the normal output current) into the amplifier's compensation circuit. When the input voltage is reduced to less than 4.24 V, the upper boost circuit is deactivated, and the amplifier resumes operation at its normal gain level.

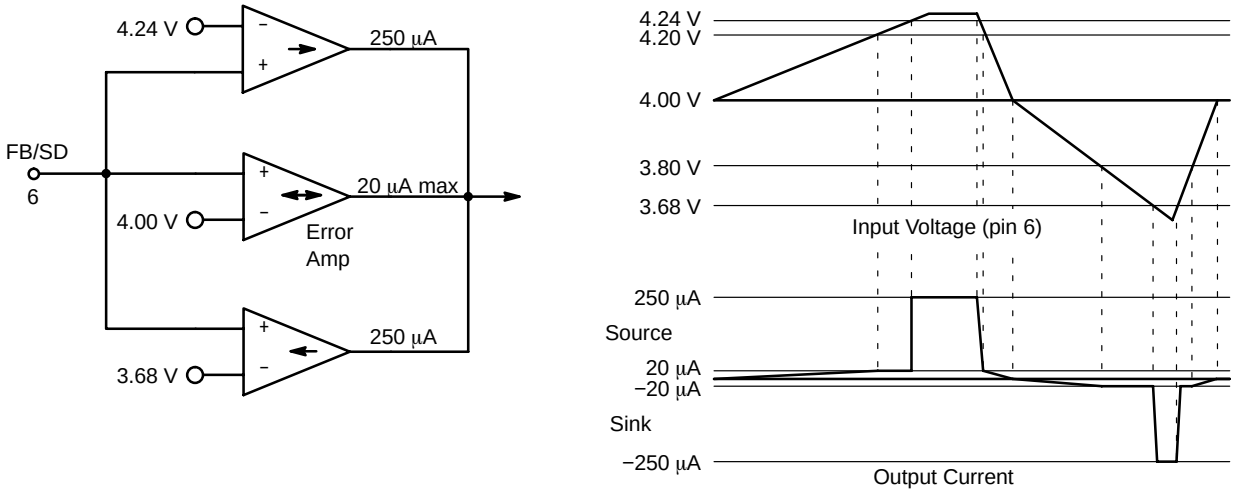


Figure 18. Representative Schematic of Voltage Loop Error Amplifier

Multipliers

This control chip incorporates two multipliers. One is used for the reference multiplier to provide the full−wave rectified sine wave signal to the ac error amplifier, and the other is used for the power limiting circuit. One of the weaknesses of analog multipliers is that it is very difficult to design them with good accuracy. Their k−factors typically have tolerances of ±10% to ±20%.

Tolerance build−up in a circuit can cause difficulties in the overall loop design. It is highly desirable to allow signals to utilize as much voltage or current variation as possible to minimize noise problems, while not driving devices into saturation. Variations in tolerances of the various blocks can make this a difficult problem.

The multipliers in the NCP1650 use a novel design that is inherently more accurate than a linear, analog multiplier. Unlike a linear analog multiplier, the inputs are not matched circuits. Input a (analog) is fed in to a voltage−to−current converter. This can be done very accurately in an integrated circuit. The other input, Input p (PWM), is compared to a ramp using a standard PWM comparator. The main error in this circuit comes from variations in the ramp peak−to−peak voltage and from its non−linearity. The ramp in this chip is trimmed to an accuracy of 1% and is fed with a high frequency, constant current source for good linearity. Testing of qualification lots indicates that maximum production variations should not exceed ±4.0%.

The voltage at input a is converted to a proportional current, which is either fed to the load filter, or shunted by the PWM comparator. Since the PWM ramp is quite linear, changes in the p input will result in a proportional change in duty cycle. (e.g. If the output of the PWM comparator is low 30% of the cycle, 70% of the input a current will be delivered to the load). The output voltage is simple the averaged current multiplied by the load resistance. The capacitor reduces the ripple of the output waveform.

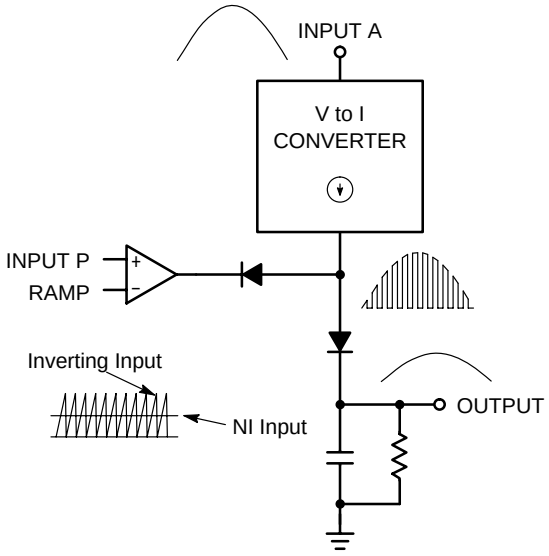


Figure 19. Switching Multiplier

Power Limit Circuit

The power limiting circuit measures the real power input to the PFC converter and regulates the output power if the limit it reached. It is OR'ed with the voltage loop in a manner similar to a constant voltage, constant current regulator. The voltage loop will dominate as long as the power demand is below the limit level. It should be understood that in the constant power mode, the output voltage is reduced in order to maintain a constant power level. Since this is a boost converter, the output voltage can only be reduced until it reaches the level of the peak of the input waveform. At that time, the power switch will shut down, but the rectifier will still allow the output filter capacitor to charge, so constant power cannot be maintained below this point.

The accuracy of this circuit is very important for a cost effective design. Since power supplies are specified for a maximum power rating, the circuit should be designed for worst−case tolerances. A tolerance of $\pm$20% for the power limiting circuit would require that the nominal output power design be 20% above the specification so that a unit which controller is 20% low will still provide the specified output power. This means that the power stage must also be designed to provide power at a level 20% greater than that its nominal level since some units may not limit until that point. The bottom line is that the power stage must be designed to deliver a maximum power of twice the tolerance of the limiting circuit. This translates into many dollars of overdesign of power components.

Other chips offer tolerance stack−ups of 25% to 50% for their power limiting circuits. This chip's tolerance stack−up is 15%. For a 1.0 kW unit this translates into a savings of 200 to 700 W for the power stage design.

Overshoot Protection

Load dumps can be very dangerous with a PFC unit. Due to the slow response time, and high output voltage, it is possible for a 400 V output to surge to 800 V when the load is suddenly removed. This type of event can cause catastrophic destruction to the PFC unit as well as to a secondary converter or other load that is connected to its output. To protect against these transients, the Feedback/ Shutdown input is monitored by a comparator that shuts down the PWM if the feedback voltage exceeds 8% of the nominal feedback level a. When the output voltage is reduced to less than this 8% window, the PWM resumes operation.

Shutdown

It is sometimes desirable to shutdown the PFC converter without removing input power. For these cases, the feedback pin is pulled to ground using an open collector device (or equivalent). When the feedback voltage is below 0.75 V, the unit is in a low power shutdown state. This feature will also hold the chip in the shutdown state when it is turned on into a line voltage of less than 53 V, as the feedback voltage at that time is the rectified, filtered input voltage.

Pros: Many "handles" available. Can use standard values from spreadsheet, or tweak for optimum performance. Variable−gain voltage loop provides quick recovery from large transients. Tightly controlled multipliers allow economical worst−case power limit designs.

Cons: Loop gain dependence on input line voltage prevents optimal loop compensation over the full line voltage range.

In addition to the NCP1650, which works in a traditional boost PFC topology, the NCP165x family also includes the NCP1651. The NCP1651 allows a single−stage, isolated step−down power conversion with PFC for many low−mid power applications where the output voltage is not very low and can handle some ripple. As shown in Figure 20, the NCP1651 based flyback converter provides a uniquely simple alternative to two−stage approaches commonly used. The NCP1651 includes all the relevant significant feature improvements of the NCP1650 and also includes a high−voltage start−up circuitry.

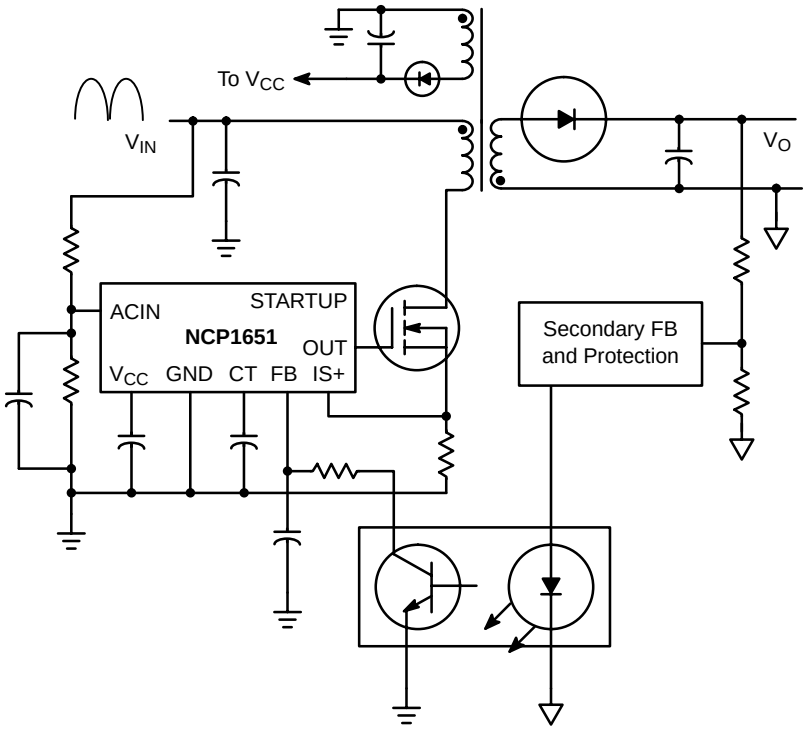


Figure 20. Single Stage PFC Using the NCP1651

CONCLUSION

The number of choices available to the PFC designer has grown significantly over the past few years, even over the past few months. This is due to the increased interest in complying with EN61000−3−2 and its derivatives, coupled with an enthusiastic spirit of competition among the semiconductor suppliers. The end users reap increasing benefits as PFC becomes better and more cost effective. Designers benefit from the increasing capability of these IC controllers, with more options available to execute the designs.

On the other hand, the designer's job has become more complicated as a result of the plethora of design approaches at his fingertips. Just surveying them is difficult enough, but understanding each of them well enough to make an informed, cost−effective choice is a big challenge. It has been an objective of this paper to increase the designers' awareness of this trend and to provide some insight into the details. The information is out there and readily available to the interested, ambitious designer.

CHAPTER 2

Methodology for Comparison of Active PFC Approaches

There are many different driving factors for designing PFC circuits as outlined in Chapter 1. Depending on end applications requirements and the prominent driving factors, the choice of a PFC circuit will vary. Until very recently, only one or two topologies have been widely utilized for PFC implementations. For higher power circuits, the traditional topology of choice is the boost converter operating in continuous conduction mode (CCM) and with average current mode control (ACMC). For lower power applications, typically the critical conduction mode (CRM) boost topology is utilized. As the range of circuits and applications incorporating PFC has expanded, the need for more diversified PFC solutions has grown. Many of the emerging solutions use variations of the established topologies, while some truly novel techniques have also emerged.

It is often difficult to provide an instantaneous answer to the question: “Which approach is the most suitable for a given application or power range?” The answer depends in part on the design priorities and various trade−offs. However, the other part of the answer lies in benchmarking of different approaches for a given application. In this handbook, results of such a benchmarking effort have been presented with detailed analysis.

The choice of a correct application is critical in carrying out such a benchmarking study. It is commonly accepted that at power levels below 100 W, the CRM approach is more appropriate, while for power levels above 200 W, the CCM approach is admittedly sensible. The power range of 100−200 W represents the gray area where either approach could be used. As a result, it is most pertinent to evaluate the performance of different approaches somewhere within this power range. A 150 W (input) power level was chosen as a target application. Also, since most applications are required to operate over universal input voltage (85−265 Vac, 50/60 Hz), that was chosen as the input voltage range. In terms of the output voltage, it was decided to evaluate a complete power system instead of PFC only circuits. As a result, a 12 V, 10 A output was chosen (assuming 80% total efficiency). Adding the second stage to the comparisons provides a more accurate picture of the capabilities and limitations of various PFC approaches. Specifically, one of the approaches chosen allows a single stage isolated PFC conversion and eliminates one full power stage. For this approach, the comparison to a PFC boost front−end would be meaningless. All the systems were designed to a hold−up time (line drop−out) specification of 20 ms (1 European line cycle).

2.1 Choice of Approaches

From the approaches described in Chapter 1 and other available approaches, the following were identified as the suitable candidates for this study. The accompanying figures for each approach depict the complete system implementation including input filtering and dc−dc conversion as needed. The dc−dc converter designs for these comparisons are based on a paper study using a commercially available design package (Power 4−5−6).

In each of the four approaches the major blocks are labeled Fn, Pn and Dn, where F, P and D indicate filter, PFC and downconverter, respectively, and n indicated the approach (n = 1 to 4).

1. Critical Conduction Mode boost converter with fixed output voltage. As shown in Figure 21, this approach creates a fixed (400 V) output voltage at the PFC output and a dc−dc converter is used to step the 400 V down to 12 V output. The controller used for the PFC front−end is the MC33260 which offers some benefits over the other multiplier based critical conduction mode controllers.

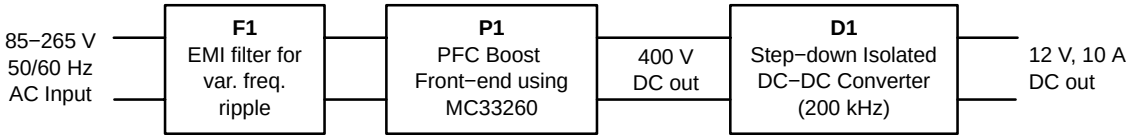


Figure 21. Critical Conduction Mode PFC with Fixed Output Voltage

2. Critical Conduction Mode boost converter with variable output voltage. As shown in Figure 22, this approach creates uses a follower boost topology for the PFC section and creates a variable output (200−400 V). A dc−dc converter steps down the voltage to the 12 V output. Compared to approach 1, this approach is expected to yield better PFC stage efficiency and cost at the expense of a more challenging second stage design. The MC33260 is used as the PFC controller for this design also since it can be configured very easily in the follower boost mode.

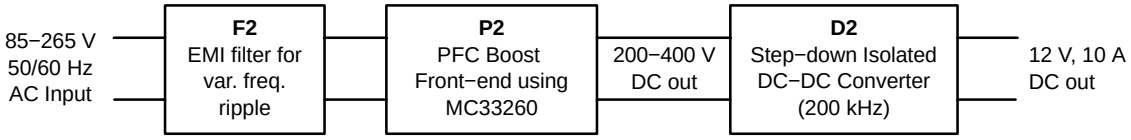


Figure 22. Critical Conduction Mode PFC with Variable Output Voltage

3. Continuous conduction mode boost converter with fixed output voltage. As shown in Figure 23, this approach creates a fixed (400 V) output voltage using a CCM boost topology. The step down conversion from 400 V to 12 V is similar to the approach 1. The NCP1650 is used as the PFC controller for this approach.

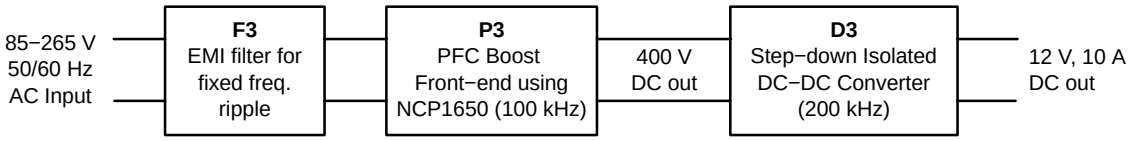


Figure 23. Continuous Conduction Mode PFC with Fixed Output Voltage

4. Continuous conduction mode flyback converter with isolation and step down. This novel approach allows the consolidation of all circuitry into one single power conversion stage as shown in Figure 24. Because this approach stores all the rectified line energy in the output capacitor, the output will have significant ripple at twice the line frequency. The controller used for this approach is NCP1651.

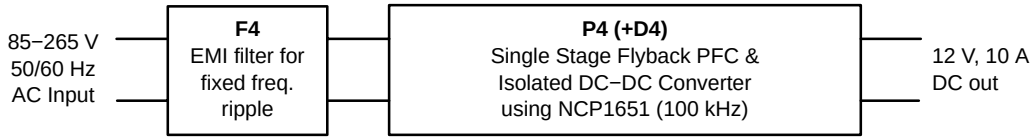


Figure 24. Continuous Conduction Mode Isolated Flyback PFC

2.2 Test Methodology

All the above PFC approaches (P1−P4) were designed, built and characterized. Each converter went through minor modifications in order to achieve local optimization without making major component changes. It is recognized that each approach can be optimized further through a more aggressive design and selection of components. However, the focus of this work was to compare the different approaches and the design approach for all the circuits was very similar. Each PFC circuit was tested for the following parameters:

1. Operation over line and load ranges (Vin = 85 to 265 Vac, Pout = 75 W to 150 W)
2. Line and load regulation
3. Input current total harmonic distortion (THD), individual harmonic contributions, and power factor
4. Power conversion efficiency

The test set−up is depicted in Figure 25 below.

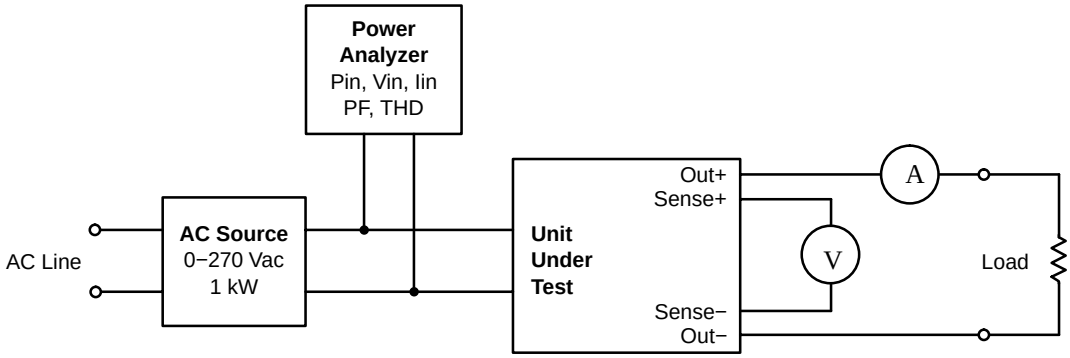


Figure 25. Test Set−Up for Performance Measurements

Equipment Used for Measurements

AC Source: Triathlon Precision AC Source

Power Analyzer: Voltech PMi Precision Power Analyzer

Load: Two types of loads were used:

- For static load measurements, a bank of high power ceramic resistors was used.
- For dynamic load measurements, a Kikusui PLZ303W Electronic Load was used.

Voltmeter: Keithley 175 Autoranging Multimeter

Current Sense: Current measurement were performed using a 5.0 mΩ shunt resistor along with a Keithley 175 A Autoranging Multimeter

Test Methodology

The circuit is tested utilizing an isolated ac source with input voltages ranging from 85 to 265 Vac. Input parameters are measured with the power analyzer. They include input power (Pin), rms input voltage (Vin), rms input current (Iin), power factor level (PF), and total harmonic distortion (THD).

For the two stage approach, the unit under test consists of the first stage PFC section while the load is a bank of high power resistors. The resistor network is used to test the PFC circuit due to its high output voltage (400 V) which is above the electronic load voltage rating. For the one stage approach, the unit under test consists of the PFC flyback circuit while the output is loaded with an electronic load as the lower 12 V output allows for its use.

The output voltage is measured directly at the output sense pins using a Kelvin sensing scheme. There is virtually no current flowing through the sense leads and therefore no voltage drop that can cause an erroneous reading. On the contrary, measuring output voltage across the resistor load can cause a wrong reading as voltage drops occur between the UUT and the load, the voltage drop varying with the amount of current flowing.

The load current is measured using a 5.0 mΩ shunt resistor. The voltage drop across the shunt resistor is measured and the load current can be calculated based on the shunt resistance value.

2.3 Criteria for Comparisons

The comparisons were carried out between the performances of PFC circuits P1−P4. These are summarized in Chapter 5. As mentioned before, paper designs were performed for downconverter approaches D1−D3. It is noted that the designs D1 and D3 are identical as they have the same input and output specifications. The comparisons of complete system approaches are also provided in Chapter 5. The key metrics for comparing power systems are cost, size and performance. It is not possible to provide an absolute cost metric for this handbook as the cost structures depend on many factors. However, the comparisons take into account relative costs of different approaches and provides details of the trade−offs involved. The size comparison is based on comparison of the sizes of major power train components for the different approaches.

2.4 Trend Charts/Effects on Variations in Conditions

While all the comparisons are made based on identical input and output conditions to provide a true comparative picture, in real life, different applications will have varying requirements. In such cases, one approach or topology may be more suitable for a given application than other may. Following variations in operating or applications conditions are explored in Chapter 5. They include expectations of components and component attributes as a function of output power.

CHAPTER 3

Critical Conduction Mode (CRM) PFC and DC-DC Stage

PFC Converter Modes

The boost converter is the most popular topology used in PFC applications. It can operate in various modes such as Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), and Critical Conduction Mode (CRM). This chapter provides the analysis of the CRM operation using the MC33260. As shown in Chapter 1, in this mode the inductor current decays to zero before the start of the next cycle and the frequency varies with line and load variations. The major benefit of CRM is that the current loop is intrinsically stable and there is no need for ramp compensation. This chapter also includes design guidelines for a traditional boost preregulator and a follower boost preregulator using the CRM technique. It also highlights some of the benefits of each topology and provides paper designs for the second stage dc−dc converter.

Traditional Boost versus Follower Boost

The traditional boost converter is designed to have a constant output voltage greater than the maximum peak rectified line voltage while the follower boost output voltage varies with respect to the peak line voltage. The main difference between the traditional boost and the follower boost topology preregulators is that the follower boost inductor size is reduced drastically and the power switch conduction losses are lower. The MC33260 allows the user to program the converter to operate in either mode. Relevant expressions for the design of a converter for given operating conditions along with a design example are provided below. Operating results for the specified converter designs are also provided.

The following inequality has to be satisfied for an MC33260 based boost converter to be configured in traditional boost mode. For lower values of C_T, the converter will operate in follower boost mode, where Vout is proportional to Vin.

$$C_T \geq C_{int} + \frac{4\, K_{osc}\, L_p\, P_{in\,max}\, I^2_{regL}}{Vin^2_{\,min}}$$

where C_T is the oscillator capacitor of the MC33260

Kosc, gain over maximum swing = 6400

C_{int}, internal capacitance of the MC33260
C_T pin = 15 pF

Vin_{min}, ac operating line voltage = 85 V

IregL, regulation Low Current Reference = 200 μA

L_P, primary inductance value

The internal circuitry of the C_T pin utilizes an on−time control method. In this circuit, C_T is charged by the square of the feedback current and compared to Vcontrol. When the feedback current is lower than IregL (please refer to the MC33260 data sheet for more details), the regulation block output (which determines the on−time) is at its maximum. The maximum on−time is inversely proportional to the square of the output voltage. This property allows for follower boost operation.

Figure 26 is provided to help in the selection of the C_T capacitor based on user defined output regulation voltage level.

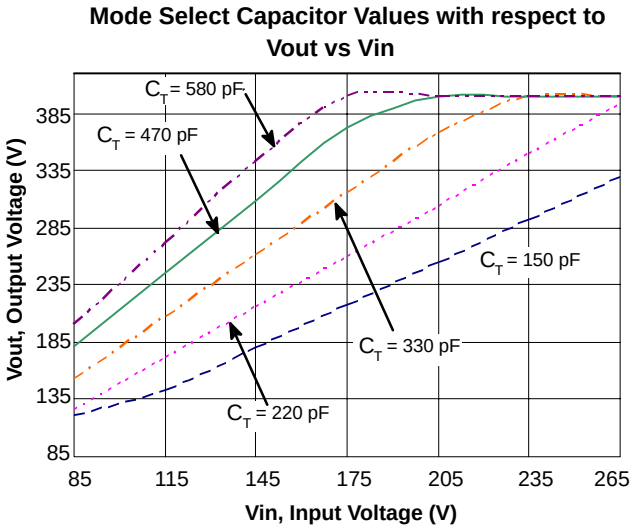


Figure 26. Mode Select Capacitor Values with Respect to V_{out} vs. V_{in} at Full Load

As shown in Figure 26, the choice of C_T capacitor allows the user to select the range of output voltage for a given application. If the C_T value is high enough, the converter will operate at a fixed output voltage, i.e., in traditional boost mode. On the other hand, a low C_T value will lead to V_{out} equal to Vin(pk). Depending on the application, the ideal solution may lie in−between.

Also worth noting while utilizing the MC33260, the V_{out} and Vin relationship depicted in Figure 1 holds for full load operation. As the output power level drops, the output voltage will actually increase for a given C_T, and at light loads, the operation will tend to approach the traditional boost operation. This behavior is depicted in Figure 27. However, the full load behavior is the most pertinent for design since it creates the maximum stress and conduction losses. Since the follower boost reduces the conduction losses significantly at this condition, the benefits are reflected in the improved efficiency. Similarly, the hold−up time specification of a system is usually at full load operation and low line, so the choice of the most appropriate

V_{out} vs. Vin relationship must be made with full load conditions in mind.

Various Load Conditions with Respect to V_{out} vs. V_{in}

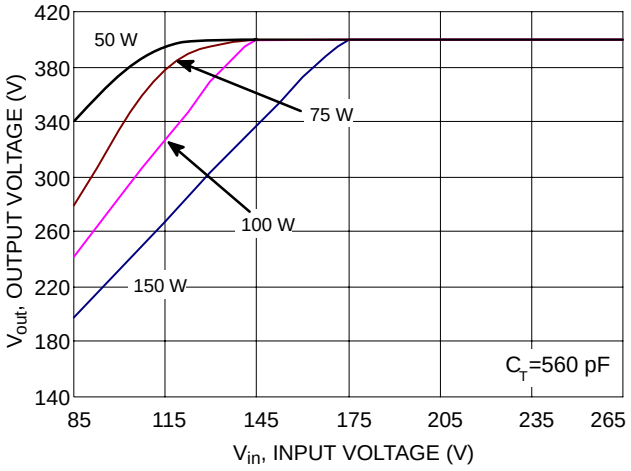


Figure 27. V_{out} vs. V_{in} with Respect to C_T = 560 pF at Various Load Conditions

MC33260: 150 W Power Factor Pre−regulator Design Example (CRM)

Following are the design basic specifications that will govern the main attributes of the circuit components, that is inductor size, MOSFET, output rectifier and output diode, to name a few.

Rated Output Power:	P_{out} = 150 W
Universal Input Voltage Range:	Vin: 85 to 265 Vac
Line Frequency:	f_{line} = 47−63 Hz
Switching Frequency:	f_{sw} = 25−476 kHz
Nominal Regulated Output Voltage:	V_{out} = 400 Vdc ± 8% (Traditional Boost) 200−400 Vdc ± 8% (Follower Boost)*
System Efficiency:	η > 90%
Hold−Up Time:	t_{holdup} = 20 ms

*Voltage range based on input voltage requirements for the dc−dc stage, see dc−dc section for more details.

Selection Process

Below are the design equations for the main components in both the traditional boost and follower boost. Each equation applies to both topologies unless otherwise noted. There are many other factors involved in the design process. However, the equations below are intended to provide a framework for the design.

Inductor (Lp)

The design of a CRM inductor presents a challenge because of the high peak currents which can lead to higher conduction losses. It is designed such that the switching cycle begins at zero current. The time it takes to reach zero is based on the input line voltage and the inductance, which also dictates the operating frequency range. The design of the inductor is based on the maximum ripple current at minimum line voltage and minimum switching frequency. The minimum switching frequency which occurs at the peak of the ac line needs to be above audible range. In this case, 25 kHz was chosen for the traditional boost and 43 kHz for the follower boost. If you chose the minimum switching frequency to be the same for both preregulators, the inductance value in the follower will be higher than 200 μH.

$$Iin_{pk} = \frac{\sqrt{2} \cdot P_{out}}{\eta \cdot Vin_{min}}$$

$$Icoil\_pk = 2 \cdot Iin_{pk}$$

$$Lp = \frac{2 \cdot T_{total} \cdot \left(\frac{Vout}{\sqrt{2}} \cdot Vin_{min}\right) \cdot Vin_{min}}{Vout \cdot Icoil\_pk} = 607\ \mu H \text{ for the traditional boost}$$

$$Lp = \frac{2 \cdot T_{total} \cdot \left(\frac{Vout}{\sqrt{2}} \cdot Vin_{min}\right) \cdot Vin_{min}}{Vout \cdot Icoil\_pk} = 200\ \mu H \text{ for the follower boost}$$

Another design criterion is the high current ripple in CRM. As a result of the high ripple, the core flux swing is bigger compared to the CCM mode. Higher flux swing results in higher core losses and rules out materials such as powdered iron. Detailed discussion on properties of the material is beyond the scope of this paper, but it is something to keep in mind in the design of the inductor. It is apparent from the above equations that the follower boost approach results in significantly smaller inductor size. The traditional boost inductor was designed by TDK (SRW42EC−U07V002) and the follower boost by Thomson Orega (10689480).

Power Switch

The power switch Q1 should be carefully selected to avoid high levels of power losses. The losses are typically dependent on switching frequency, rms current, duty cycle, and the rise and fall times. These parameters breakdown into two types of losses: conduction and switching. For the CRM operation, the MOSFET turn−on switching losses are minimized since the current is zero at the MOSFET turn−on. Hence, the focus is placed primarily on minimization of the conduction losses. Consequently, the selection process is based on three key parameters; transistor rms current, drain to source voltage and on resistance ($R_{DS(on)}$). The root mean square (rms) value of the switch current I_Q, can be derived by averaging the entire cycle of the square of the switch current presented below in the equation. Once this is determined, the power dissipation can be calculated based on the $R_{DS(on)}$ of the chosen MOSFET.

$$IQ = \sqrt{\frac{1}{6} \cdot \frac{4\sqrt{2} \cdot Vin_{min}}{9 \cdot \pi \cdot Vout}} \cdot Icoil\_pk$$

On a side note, an identical power MOSFET Q1 was used in both the traditional and follower boost circuits for practical reasons. However, the conduction losses in the follower boost circuit are actually lower than in the traditional boost. The follower boost uses a longer off−time which yields to a smaller switch duty cycle and lower conduction losses. This helps in reducing system cost by reducing the size and cost of the power switch.

Output Rectifier

The output diode selection is based on reverse voltage capability, forward current and an estimated power budget. CRM operation significantly simplifies the diode operation and selection because reverse recovery time is not of importance. In other words, the selection process is very user biased and an ON Semiconductor MUR460E Ultrafast rectifier was chosen for this design example. Choosing an ultrafast diode helps minimize thermal stress in the MOSFET.

Output Capacitor

Selection of the output capacitor C_{out} is another important design step. The capacitance value is dictated by the output voltage, output ripple voltage, and the amount of energy that needs to be stored. It is fairly costly and usually requires a voltage rating of 400 V or greater. An important factor related to the amount of energy the capacitor needs to store is the system's hold−up requirements. Generally, hold−up times range from 16 to 50 ms. A great majority of the industry requirement is 20 ms. The minimum output voltage ($Vout_{min}$) for the traditional boost is 280 V and 150 V for the follower boost. This takes into consideration the minimum voltage the PFC preregulator will allow the output voltage to drop to while sustaining the output load. In other words, how much energy needs to be stored which stems from the energy equation:

$$\text{Energy} = \text{Power x Time}$$

$$\text{where power} = 150\ \text{W (output power)}$$
$$\text{and time} = 20\ \text{ms (hold} - \text{up time)}$$

In solving the above energy equation, C_{out} needs to store 3 J. Now C_{out} can easily be solved for by rearranging the next equation. The traditional boost is designed for an output voltage of 400 V while the follower boost is designed for an output voltage in the range of 200 V to 400 V.

$$\Delta U = U_1 - U_2 = \frac{1}{2} C_{out}(Vout^2 - Vout^2{}_{min})$$

$$Cout = \frac{2 \cdot \Delta U}{Vout^2 - Vout_{min}{}^2} = \frac{2 \cdot 3}{400^2 - 280^2}$$
$$= 74\ \mu F\ \text{for the Traditional Boost}$$

$$Cout = \frac{2 \cdot \Delta U}{Vout^2 - Vout_{min}{}^2} = \frac{2 \cdot 3}{200^2 - 150^2}$$
$$= 342\ \mu F\ \text{for the Follower Boost}$$

In the follower boost in the worst−case scenario, the smaller the minimum output voltage, the higher C_{out} is. For example, choosing C_{out} such that at low line voltage V_{out} equals 200 V would allow partial benefits of the follower boost solution, while not requiring a very large capacitor for hold−up time requirements. Another distinct benefit of selecting $Vout_{min}$ at such intermediate level is that it does not constrain the performance of the second stage significantly. Usually, the efficiency of dc−dc converters suffers significantly if they have to operate over a wide input range.

The calculated capacitor values for the both converters are 74 μF and 342 μF respectively. The traditional boost had a significant amount of output ripple voltage which caused the device to go into overvoltage protection therefore, a 220 μF capacitor was used. In order to avoid over dimensioning of C_{out}, further filtering the feedback pin will help prevent OVP triggering. This validates that there are trade−offs in every aspect of the application and in this case, the primary trade−off for both the traditional and follower boost is the size and cost of C_{out}.

The aforementioned specifications with respect to hold−up times leads to the discussion of minimum input voltage for the dc−dc converter stage which is further discussed later in this chapter.

Current Sense

A current sense resistor (R_{CS}) is inserted in series with the diode bridge rectifier (Figure 28). The current sense block operates by converting the inductor current to a negative voltage. This voltage is applied to the current sense through the overcurrent protection resistor (R_{OCP}). As long as the voltage across R_{OCP} is below −60 mV, the internal current sense comparator resets the PWM latch which forces the gate drive signal low. During this condition, the MOSFET is off. This is a valuable protection scheme especially at start−up of the PFC when C_{out} attempts to charge to twice that of the input voltage. Below are some useful equations in helping to select R_{CS} and R_{OCP}.

Dissipation capability for RCS:

$$P_{CS} = \frac{1}{6} \cdot R_{CS} \cdot Icoil\_pk^2$$

Overcurrent protection resistor:

$$R_{OCP} = \frac{R_{CS} \cdot Icoil\_pk}{I_{OCP}}$$

Less power dissipation is usually desired for R_{CS}; in this case, 0.7 Ω was chosen due to availability. In this power range, it is highly recommended to use a 0.5 Ω R_{CS} in order to keep the power dissipation low.

Circuit Schematic and Bill of Materials

Below is a functional schematic of the MC33260 boost converter implementation. A schematic and bill of material can be found in the appendix at the end of this report.

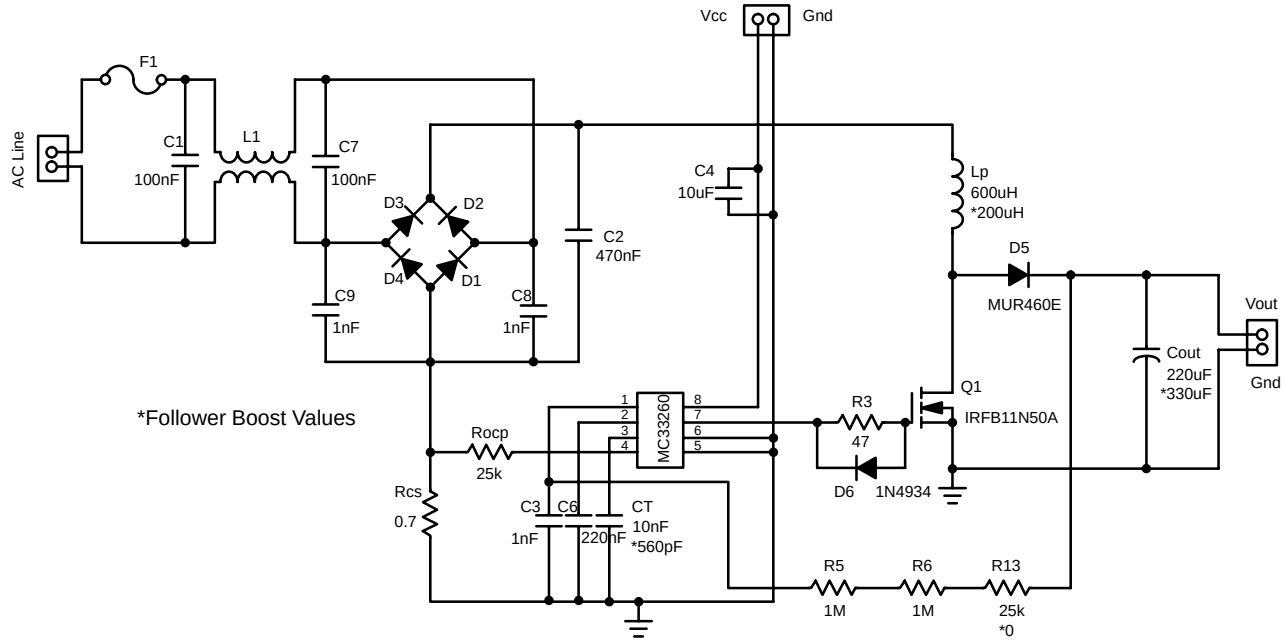


Figure 28. MC33260 Traditional and Follower Boost Schematic

EMI Considerations

EMI is present in every PFC, especially at high frequencies. The MC33260 offers a synchronization option to facilitate EMI reduction. There exists both radiated and conducted EMI. The focus in this case will be on conducted EMI which breaks down into two categories, common mode and differential mode. The data presented below was taken without an optimized EMI input filter. EMI considerations and results are addressed in Chapter 6.

Results

The following tables summarize the design example and illustrate the calculated/selected values for both the traditional and follower boost preregulators. This section also contains some plots that sum up power factor, THD, and efficiency at different power levels. A fixed resistive load was used in taking the measurements for the traditional boost whereas a variable resistive load was used for the follower boost. In addition, an EXCEL spreadsheet (www.onsemi.com / site / products / summary/ 0,4450,MC33260,00.html) helped in verifying the design parameters.

Table 1. Design Table − Traditional and Follower Boost

Mode Select	Traditional Boost	Follower Boost
P_O (W)	150	150
L_p (μH)	607	200
C_O (μF)	220	330
R_{CS} (Ω)	0.7	0.7
R_{OCP} (kΩ)	20	20
C_T (pF)	10000	560

Pros and Cons of the Traditional vs. Follower Boost

In comparing the traditional versus follower boost, there are a few key points to take away. For the same power level, the follower boost mode utilizes a smaller inductor which leads to utilization of less board space and ultimately lower cost. The downside is that it requires a higher capacitance value. There is some flexibility in choosing the output capacitor value, with the trade−off of the desired output ripple voltage and the design of the dc−dc conversion stage.

Table 2. Measurement Results for the Traditional Boost

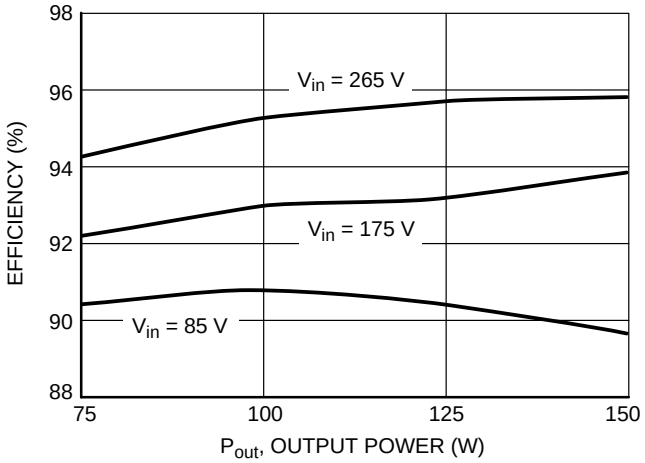
150 W PFC Front End − MC33260 Traditional Boost				
Vin (Vac)	85	115	175	265
Efficiency (%)	87.8	91.6	94.3	96.2
THD (%)	8.87	11.04	14.8	17.6
PF (%)	99.49	99.32	98.83	97.61
Vout (V)	401.5	408.3	414.6	418

Table 3. Measurement Results for the Follower Boost

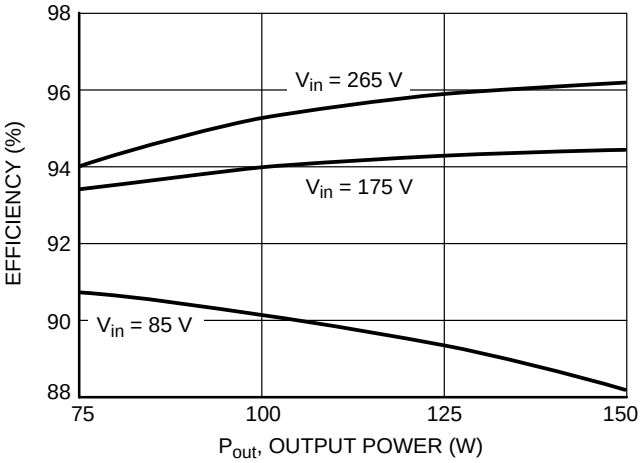
150 W PFC Front End − MC33260 Follower Boost				
Vin (Vac)	85	115	175	265
Efficiency (%)	89.5	92.5	93.7	95.9
THD (%)	5.95	6.21	10.87	21
PF (%)	99.76	99.75	99.25	97.37
Vout (V)	203	276	391	400.7

Design Performance Curves

There are many interesting observations that can be made upon closer examination of the data. The following curves are representative of the actual data and can be used as reference points. These curves give practical information that may be useful when trying to meet the required specifications in terms of power factor, total harmonic distortion and efficiency. It is likely that the performance can be optimized.



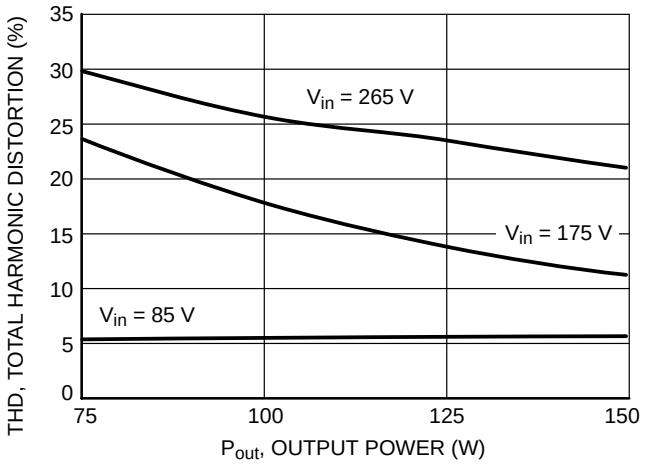
FB: Efficiency vs. Output Power



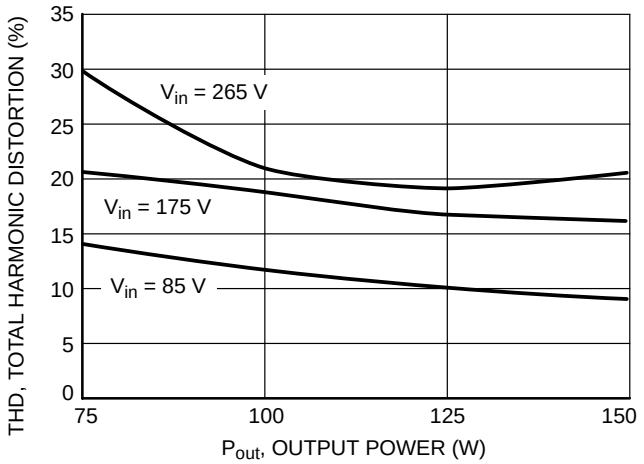
TB: Efficiency vs. Output Power

Figure 29. Efficiency vs. Output Power for Follower and Traditional Boost

In comparing the efficiency of the traditional and follower boost, it is evident that the follower boost has a slightly higher efficiency at both high line (265 Vac) and low line (85 Vac). Based on a power budget, the losses in the inductor do not vary much since the peak inductor current Icoil−pk is the same in both preregulators. Only the winding dc resistance and core losses vary. Still, the majority of the losses are due to the main power switch Q1 and the output diode D5 (Figure 28). The follower boost exhibits a longer off−time which causes a smaller duty cycle and thus lower conduction losses in Q1. The power budget calculations for Q1 and D5 in follower boost mode were 2.26 W versus 2.46 W in the traditional boost mode. On the other hand, as the input voltage increases, both preregulators improve significantly in efficiency.



FB: Total Harmonic Distortion vs. Output Power



TB: Total Harmonic Distortion vs. Output Power

Figure 30. Total Harmonic Distortion vs. Output Power for Follower and Traditional Boost

In measuring THD, it is important to pay attention to the equipment classification and the desired harmonic limit. In this case, the MC33260 exhibits higher THD. The THD content represented in Figure 30 includes the 2^{nd}, 3^{rd}, and every odd harmonic up to the 9^{th}. At high line (265 Vac), the THD level is much higher than at low line (85 Vac) in both preregulators due to the higher switching frequency.

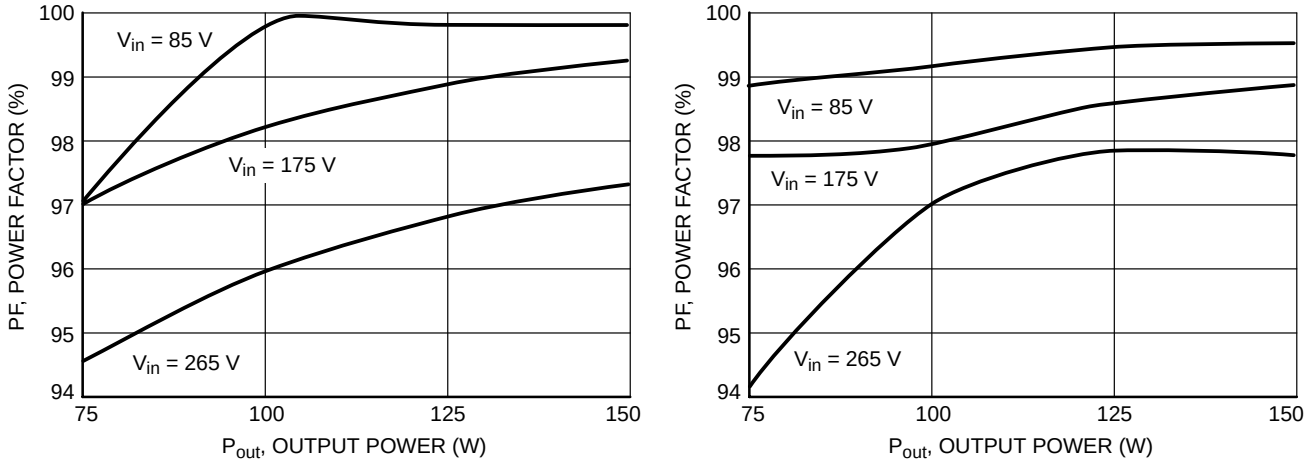


Figure 31. Power Factor vs. Output Power for Follower and Traditional Boost

Measuring power factor requires a very reliable power meter that accurately measures both apparent power (product of RMS voltage and RMS current) and real power. Power factor in the in the follower boost is slightly higher than traditional boost. This is partly due to the lower switching frequency versus traditional, since high power factor and low harmonics go hand−in−hand.

Second Stage DC−DC Converter

This section compares and summarizes the two−switch forward second stage for all three downconverter approaches, D1, D2 and D3. Some advantages of the two−switch forward converter include lower switch voltage and low output ripple. Power 4−5−6 software was used in the paper design process.

As mentioned in Chapter 2, designs D1 and D3 are identical as they have the same input and output specifications. This will help the designer understand the differences on all three approaches and help to select the optimum solution for their application. The most important attributes in Table 5 will be discussed in the following paragraphs.

120 W DC−DC Design Example

The design of the dc−dc converter stage is based on the following parameters. It is intended to operate in continuous mode.

Rated Output Power: P_{out} = 120 W

Input Voltage Range: Vin = 280−432 V
(Traditional Boost MC33260 and NCP1650)
150−425 V (Follower Boost MC33260)

Nominal Regulated Output Voltage: V_{out} = 12 V ± 10%

Switching Frequency: f_{sw} = 200 kHz

System Efficiency: η = 80%

Transformer

The input voltage for D1 and D3 is based on a range of 280 V−432 V, whereas the input voltage for D2 is based on a range of 150 V−425 V. The minimum input voltage for D1−D3 takes into consideration the hold−up time of the bulk capacitor in the PFC stage. Hold−up time is the the amount of time at a rated output power of 150 W at the PFC stage, that the capacitor voltage discharges to an operating minimum. The start point of the dropout is the minimum input voltage to the dc−dc stage. The maximum voltage of 280 V and 150 V respectively is the overvoltage protection of the PFC stage. Due to the lower input voltage of D2, the transformer requires a smaller turns−ratio. An EFD20 core was chosen for D1 and D3 and an EFD30 for D2.

Power Switch

One of the main reasons for choosing a two−switch forward topology for the converter stage is that the peak switch voltage is significantly higher in conventional single−switch forward topologies, which in turn can be very costly since it requires a MOSFET rating of 900 V or higher. As mentioned above, the selection criteria used for the switches are input peak current, drain to source voltage and power dissipation. D2 utilizes a 500 V, 0.95 Ω switch while D1 and D3 use a 600 V, 3.0 Ω switch. As mentioned above D2 transformer turns−ratio is half of D1 and D3. Consequently, the power switch drain current is twice as high. In order to minimize conduction losses, a smaller $R_{DS(on)}$ switch was chosen.

Inductor and Capacitor Filter Design

The LC filter in the two−switch forward topology serves two purposes. It stores energy for the output load during the off−time of the power switches. Secondly, it minimizes output ripple voltage on the output of the power supply. Typically the filter inductor is much larger than the filter capacitor.

Power Diode

There are two choices in choosing a diode: Schottky, and ultrafast. The output rectifier must be selected to minimize power losses and maximize efficiency. The most important parameters to consider are the diode forward current, I_F, forward voltage, V_F, and the reverse voltage, V_R. The diode must be able to sustain the high currents necessary to supply the load and withstand the high reverse voltage and not burnout. I_F should be at least equal to average output current and V_R should be greater than the sum of the output voltage plus the input voltage reflected to the secondary.

$$V_R \geq Vin_{max} \cdot \frac{Ns}{Np}$$

In this case, D1 and D3 use Schottky diodes versus an ultrafast diode for D2. Again, due to the lower turns−ratio in the transformer used in D2, the forward current and blocking voltage will be significantly higher. As a result, a schottky diode could not meet the electrical requirements and an ultrafast was used. There is little difference in price between these two diodes.

Table 4. DC−DC Two−Switch Forward Detail Comparisons (POWER 456)

Attribute	D1 MC33260 2−Switch Forward	D2 MC33260 2−Switch Forward	D3 NCP1650 2−Switch Forward
Transformer	Ratio: 10:1 0.629 in^2 0.257 in^3	Ratio: 5:1 1.44 in^2 0.68 in^3	Ratio: 10:1 0.629 in^2 0.257 in^3
Power Switch	600 V 3.0 $R_{DS(on)}$ TO220 0.077 in^2 0.067 in^3	500 V 0.95 $R_{DS(on)}$ TO220 0.077 in^2 0.067 in^3	600 V 3.0 $R_{DS(on)}$ TO220 0.077 in^2 0.067 in^3
Inductor	26 μH 10.6 Apk 1.00 in^2 0.507 in^3	26 μH 10.83 Apk 1.00 in^2 0.507 in^3	26 μH 10.6 Apk 1.00 in^2 0.507 in^3
Power Diode	Schottky 60 V, 15 A V_F = 0.62 V TO220 0.077 in^2 0.067 in^3	Ultrafast 100 V,10 A V_F = 0.80 V TO220 0.077 in^2 0.067 in^3	Schottky 60 V, 15 A V_F = 0.62 V TO220 0.077 in^2 0.067 in^3
Output Capacitor(s)	220 μF, 16 V 0.26 Apk 0.19 in^2 0.85 in^3	220 μF, 16 V 0.45 Apk 0.19 in^2 0.85 in^3	220 μF, 16 V 0.26 Apk 0.19 in^2 0.85 in^3
Frequency Range	200 kHz Fixed	200 kHz Fixed	200 kHz Fixed
Control	I−mode	I−mode	I−mode
Total Volume	1.75 in^3	2.17 in^3	1.75 in^3

Table 5. DC−DC Two−Switch Forward Stage

Attribute	D1 MC33260	D2 MC33260− Follower Boost	D3 NCP1650
***Cost ($)**	3.24	4.10	3.24
Efficiency @ Low Line (%)	90.2	89.3	90.2
Power Density (W/in^3)	68.57	55.29	68.57

*Cost is for budgetary purpose only and is based on 1,000 units. Actual production costs may vary significantly.

Once again, the table above provides a summary for the dc−dc stage. It is not simple to make a thorough comparison because the optimization design for this stage has not been created. However, some merits can clearly be seen. As with any comparison, there are many variables and trade−offs involved.

CHAPTER 4

Continuous Conduction Mode (CCM) PFC

This section walks the user through the designs of a continuous conduction mode boost PFC circuit utilizing the NCP1650 controller, and a continuous conduction mode flyback PFC circuit utilizing the NCP1651 controller. The description here is restricted to major design choices and their analyses. More in−detail designs are provided in the products' data sheets and application notes. A comprehensive excel spreadsheet is available for each product for a quick computation of the component values and an easy generation of a bill of materials. These spreadsheets can be downloaded from the NCP1650 and NCP1651 product folders at:

www.onsemi.com / site / products / summary / 0,4450, NCP1650,00.html#Design%20&%20Development% 20Tools

NCP1650: 150 W Power Factor Pre−regulator Design Example (CCM Boost)

I. Circuit Description and Calculations

The NCP1650 power factor controller is a fixed frequency, average current mode controller designed to work in continuous or discontinuous mode operation. It was specifically created to answer power supply designers' growing concerns with satisfying government issued energy regulations. The latest trend of regulations, such as IEC1000−3−2 requires the use of PFC preconverter in power supplies with power ratings of 75 W or higher. The NCP1650 power factor circuit example featured in this document is designed to work from a universal input and provide 150 W of output power. This designed can be scaled to provide higher output power of up to 5.0 kW.

In order to start the design, first the circuit basic specifications must be defined. These specifications will govern the main attributes of the circuit components, that is inductor size, selection of the MOSFET, output rectifier and output diode, to name a few. The following parameters will be used to calculate the various component values. The formulae are given for continuous conduction mode (CCM) operation, which is the preferred operating mode for the topology. It is worthwhile to note that NCP1650 controller also works in discontinuous conduction mode (DCM).

Maximum rated output power: $Pout_{max}$ = 150 W

Minimum operating line voltage: Vin_{min} = 85 Vac

Maximum operating line voltage: Vin_{max} = 265 Vac

Line frequency: f_{line} = 47−63 Hz

Nominal switching frequency: f_{sw} = 100 kHz

Nominal regulated output voltage: Vout = 400 Vdc ± 8%

System efficiency: η = 0.9 (expected)

Because this circuit uses a boost mode configuration, it is necessary that the output voltage be greater than the peak of the rectified input voltage. The design requiring a universal input, for a maximum line voltage of 265 Vac, the peak line voltage will reach 375 Vdc, hence an output voltage of 400 Vdc is chosen.

Inductor

The inductor selection is somewhat iterative and is determined based on the peak current, operating mode (CCM: constant current, DCM: discontinuous, CRM: critical conduction), ripple current, output ripple voltage, components stress and losses, as well as board space. As the design equations will show, most of these parameters move in opposite directions, working against each other, and optimizing the inductor design will require some trade−offs. It is up to the circuit designer to prioritize which parameter is more crucial to satisfy the design requirements.

A first approximation of the inductor value L can be obtained with the following equation:

$$L = \frac{Vin^2_{min} \cdot T}{2 \cdot I\% \cdot Pout_{max} \cdot \eta} \cdot \left[1 - \left(\frac{\sqrt{2} \cdot Vin_{min}}{Vout}\right)\right]$$

where L = inductance value

Vin_{min} = minimum operating line voltage

$Pout_{max}$ = maximum rated output power

T = period

Vout = nominal regulated output voltage

I% = ratio of allowable pk−pk ripple current to peak current in the inductor (20−40% typical)

η = efficiency

The following chart helps in defining a range of inductances based on the allowable ripple current. It is recommended to use a value of inductance that falls within the 20−40% range of input current ripple shaded in grey.

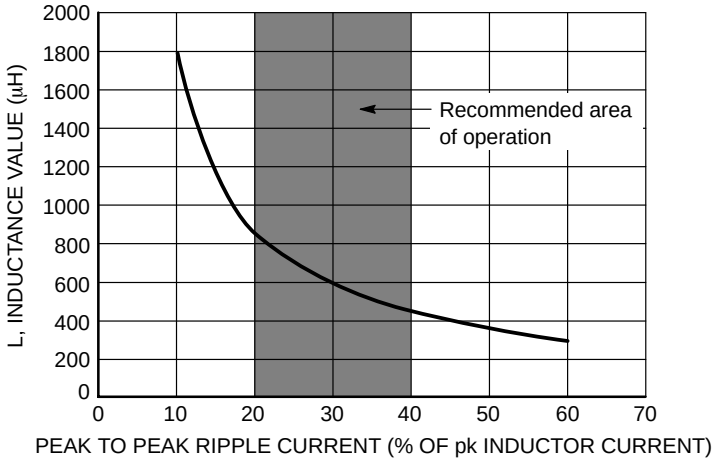


Figure 32. Recommended Inductance as a Function of Ripple Current

It is advised to adjust the value of L to minimize the ripple current while confining it to a reasonable size to minimize board space. Typically, a maximum peak to peak ripple current of 20% to 40% of the peak inductor current is acceptable.

Selecting the minimum recommended inductance will make for a smaller size inductor but also for higher switch peak current, larger ripple currents, and larger output ripple voltage. Hence a bigger MOSFET and larger output capacitors will be needed to handle the higher components stress. The smaller inductance value will also force the device to operate in discontinuous mode at high line, increasing input filtering requirements, strain on the components and total harmonic distortion (THD) levels.

Selecting the maximum recommended inductance to minimize components stress and guarantee continuous conduction mode operation can be costly in both board real estate and inductor cost. Larger inductor value also leads to higher winding losses.

Utilizing the excel spread sheet allows the user to quickly experiment with different values of L and observe its impact on the design parameters. This particular design was optimized for an 800 μH inductor. It yields the following:

Peak inductor current: Ipk = 3.3 A

Output capacitor ripple current: I_C rms = 1.30 A rms

Output voltage ripple: Vout ripple = $\pm$32 V (or $\pm$8%)

CCM is ensured from 40° to 140° at high line, full load.

Even though this range may appear insufficient to prevent the controller from going into DCM at high line and thus resulting in higher THD, the circuit actually operates in CCM for a wide range of inputs. In addition, THD levels remain more than adequate at high line as indicated in the results section, well below the 10% mark.

The actual design of the inductor can be done in a variety of ways. Core material and size, bobbin, and wire selection can be done by the user or left to experienced magnetics manufacturers such as Coilcraft (www.coilcraftcom) or TDK (www.component.tdk.com). The inductor utilized in this design was provided by TDK electronic components and can be ordered under the reference number SRW28LEC−U25V002.

Power Switch

The power MOSFET selection is based on the maximum drain to source voltage, V_{DS}, and maximum switch current. V_{DS} is determined by the output voltage of the PFC pre−converter. The maximum switch current is the same as the peak inductor current. The peak inductor current is a function of the maximum line current and the allowable ripple current. It will occur at the peak of low line input voltage, when the current demand is at its highest, as illustrated in Figure 33.

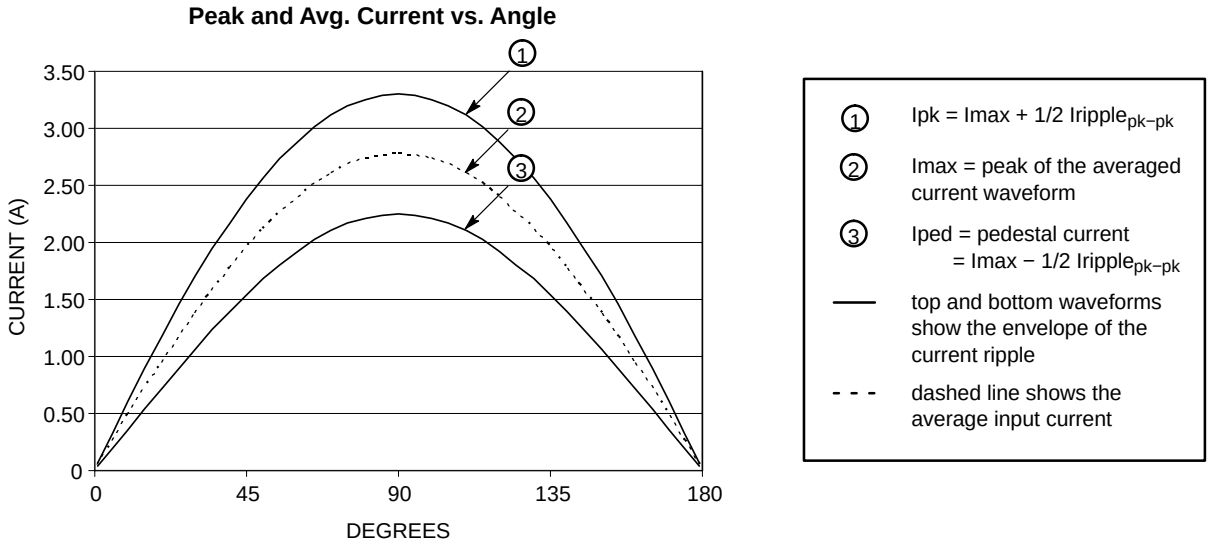


Figure 33. Peak and Average Line Current vs. Angle

The peak current can be calculated as the sum of the peak of the averaged line current waveform and half of the peak to peak current ripple.

$$Ipk = \frac{\sqrt{2} \cdot Pin}{Vin} + \frac{I\%}{2}\left(\frac{\sqrt{2} \cdot Pin}{Vin}\right)$$

The highest peak current will occur at low line and full load.

In order to minimize switching and conduction losses, keep in mind to select a MOSFET with low gate charge, low capacitance and low $R_{DS(on)}$. This design utilizes an IRFB11N50A MOSFET from International Rectifier. This particular MOSFET was chosen for its low $R_{DS(on)}$ of 0.52 Ω, 500 V drain to source voltage, and 11 A drain current rating. Its total gate charge of 52 nC and low input capacitance of 1423 pF helped in reducing switching losses.

Output Rectifier

The output rectifier must be selected with care to minimize power losses and maximize efficiency. The most important parameters to consider are the diode forward current, I_F, the reverse voltage, V_R, and the maximum reverse recovery time, trr. The diode must be able to sustain the high currents necessary to supply the load and withstand the high reverse voltage and not burnout. I_F should then be higher than the peak inductor current and V_R should be greater than Vout plus the output voltage ripple. The average diode current can be calculated using the Excel spreadsheet.

The peak diode current is equal to the peak inductor current. The non repetitive peak forward diode current rating, IFSM, should be chosen accordingly.

Power dissipation in the output rectifier can be calculated with the excel spread sheet. Given the manufacturer forward voltage and reverse recovery time of the output diode, the design aid will compute the reverse recovery losses, conduction losses and total losses in the rectifier. As the calculations will point out, at 100 kHz, the switching losses become significant. Selecting a rectifier with a low reverse recovery time, like an ON Semiconductor ultrafast MUR family diode helps in lowering the switching losses. Having a low forward voltage drop minimizes conduction losses.

This design utilizes ON Semiconductor ultrafast diode MURH860CT. This diode has a forward current capability of 8.0 A, a forward voltage of 2.5 V, a reverse voltage rating of 600 V, and a reverse recovery time of 35 ns.

Output Capacitor

The output capacitor is picked based on its capacitance value and voltage rating. The voltage rating is dictated by the output voltage of the preconverter circuit. The capacitance value depends on the level of output voltage ripple allowed and on the hold up time in brownout conditions.

The level of output ripple is typically set by the secondary stage input requirements. Vout −Vripple must be greater than the minimum required input voltage of the second stage.

For this design, an output ripple of less than 16% peak to peak is desired, that is, less than ± 32 V. The output voltage ripple can be approximated with the Excel spread sheet. A minimum capacitance of 33 μF is necessary to achieve this requirement. Using a Cout value of 100 μF at low line yields an output voltage ripple of 11.8 V peak to peak (measured on the board) which is well below the 32 Vpp of ripple that we want to achieve.

Typical power supplies require a minimum holdup time in case of loss of the power mains during which the supply must be able to sustain its load output. 20 ms of holdup time is an accepted standard in the industry. The minimum capacitance required for a 20 ms holdup time can be calculated as:

$$Cout = \frac{2 \cdot Pout \cdot t_{hold}}{Vout^2 - Vout^2_{min}}$$

where t_{hold} is the minimum hold up time and $Vout_{min}$ is the minimum output voltage that Cout is allowed to discharged down to in a period of 20 ms.

Again, the minimum output voltage is dictated by the secondary stage minimum required input voltage to sustain its load. For this design, a $Vout_{min}$ of 280 V is necessary for a second stage dc−dc forward converter with an output load of 120 W (12 V, 10 A).

The value of Cout can now be computed. The calculation yields a Cout value of 74 μF. To meet both the minimum holdup time and output voltage ripple requirements, the next higher standard capacitance value of 100 μF is chosen for this design.

Finally, in selecting the proper capacitor for the design, one must take into account the maximum rms currents flowing through the capacitor. Assuming a constant dc resistive load, the rms current can be calculated as follows:

$$I_C rms = \sqrt{\left[\frac{32 \cdot \sqrt{2} \cdot Pin^2}{9 \cdot \pi \cdot Vin \cdot Vout} - \left(\frac{Vout}{Rload}\right)^2\right]}$$

where Vout/Rload can be substituted by the rms output current in the case of a non resistive load. It is important to make sure the capacitor (current and power) ratings are not exceeded.

The last thing to keep in mind in order to reduce power dissipation is to minimize the ESR of the capacitor. It is always a good idea to parallel multiple capacitors together if the layout permits it. This also helps in spreading the rms current and power dissipation between the different capacitors, allowing the user to pick lower current rating and therefore smaller devices.

This design uses a 100 μF, 450 V Panasonic aluminum electrolytic capacitor.

EMI Considerations

EMI is present in every PFC, especially at high frequencies. There exists both radiated and conducted EMI. The focus in this case will be on conducted EMI which breaks down into two categories, common−mode and differential mode. The data presented below was taken without an optimized EMI input filter. EMI considerations and results are addressed in Chapter 6.

Control Circuit Design

The control circuit design is facilitated by the Excel design tool, that allows the user to design the values of all the components in a step−by−step function. The tool ensures that the components chosen do not cause any of the IC parameters limitations to be exceeded.

DC−DC Converter

The dc−dc second stage design for the NCP1650 traditional boost is covered in Chapter 3. Please refer to paragraph entitled “120 W DC−DC Design Example” for additional information.

II. Circuit Schematic and Bill of Materials

Following is a functional schematic of the NCP1650 boost converter implementation. A complete schematic and the bill of material can be found in the appendix at the end of this report.

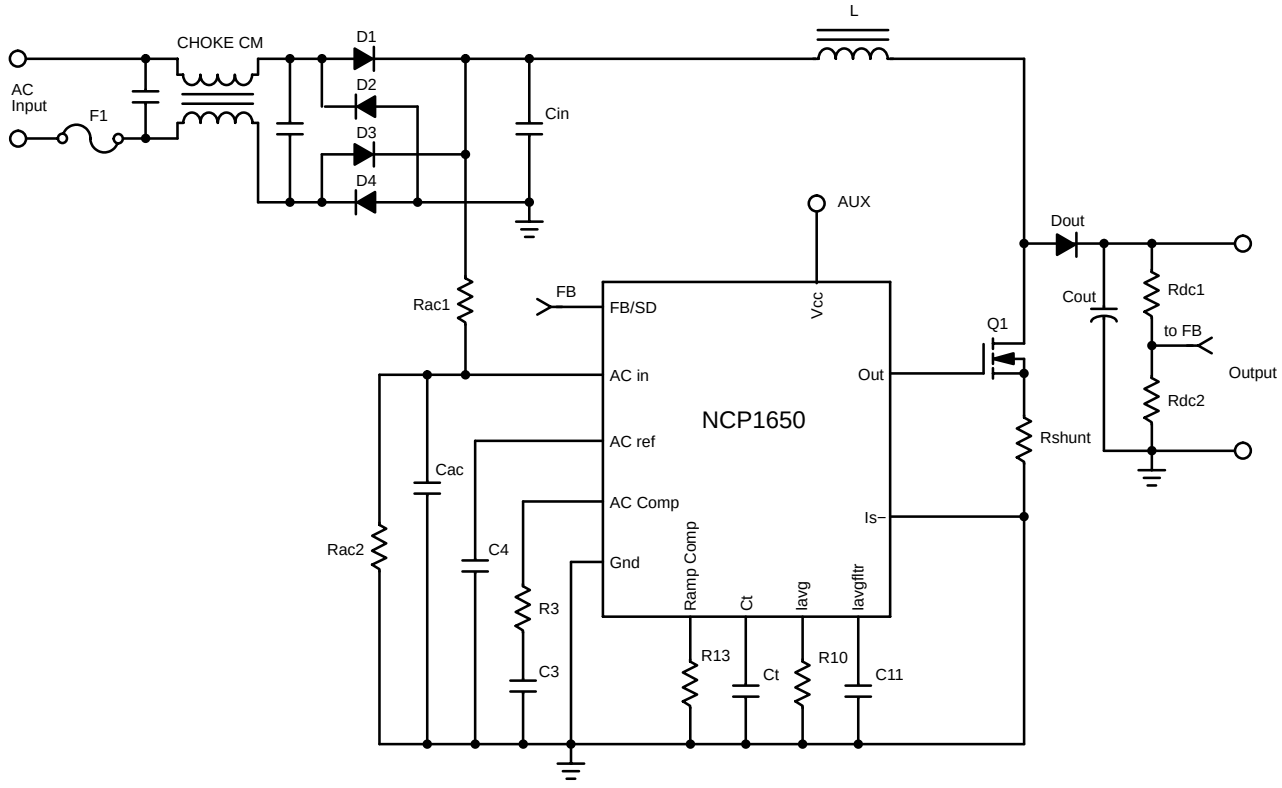


Figure 34. NCP1650 PFC Boost Converter Simplified Schematic

III. NCP1650 Board Results

The measurements on the NPC1650 board were performed and the following data was obtained.

Table 6. NCP1650 PFC Circuit Results Using the 800 μH Inductor

Vin (Vac)	85	115	230	265
Pin (W)	173	166	159.8	158.6
Iline (rms)	2.04	1.44	0.69	0.597
Vout (V)	404.2	404.6	404.7	404.8
Iout (A)	0.375	0.374	0.371	0.371
Efficiency (%)	87.6	91.2	94.0	94.7
PF (%)	99.76	99.78	99.77	99.6
THD (%)	4.67	4.19	5.51	6.32

Table 6 shows that a good efficiency can be expected from the NCP1650 throughout the input voltage range. Efficiency suffers a little at lower line voltages. This is because the line current increases at lower line voltage, which results in higher power dissipation in the MOSFET and output rectifier. On the other hand, very good power factor (PF) and THD performance are observed at all input voltages.

It is also interesting to vary the output load to change the output power of the circuit and observe its effects on efficiency, power factor, and total harmonic distortion. The following three plots illustrate the results.

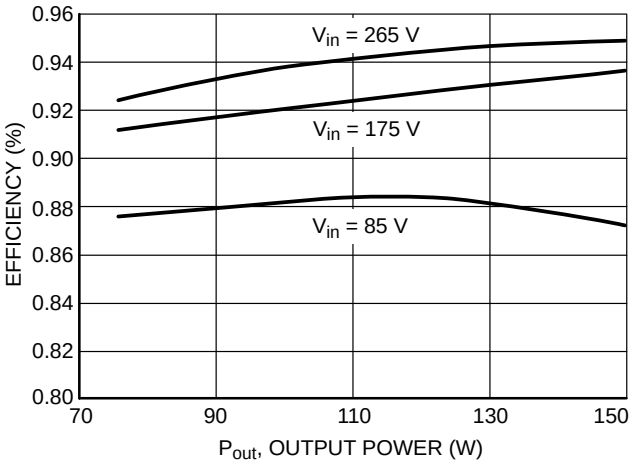


Figure 35. Efficiency vs. Output Power

As Figure 35 indicates, the higher the line input voltage, the higher the efficiency. At higher line voltage, the input current needed to sustain the load is lower and less power is dissipated in the various components, leading to a more efficient circuit. At low line, the efficiency starts dropping at higher output power because the line current is much greater and therefore the power dissipation in the power MOSFET and output rectifier is also greater.

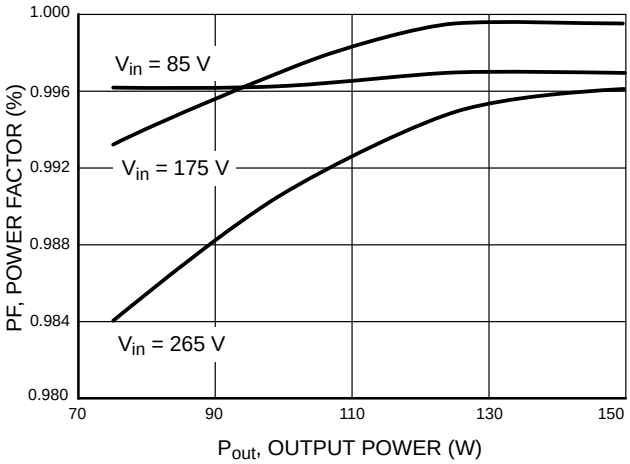


Figure 36. Power Factor vs. Output Power

As Figure 36 indicates, power factor improves as the output power increases. At lower output power levels and high line (175 Vac and 265 Vac), the circuit operates in discontinuous mode. DCM operation forces faster di/dt and higher peak currents in the power switch and output rectifier. Power factor levels suffer as a result. At low input line voltage, the device operates in CCM whatever the output power and therefore distortion does not become an issue. Adding more inductance to the inductor would help extend the range over which the circuit will run in CCM and help improve the power factor levels throughout.

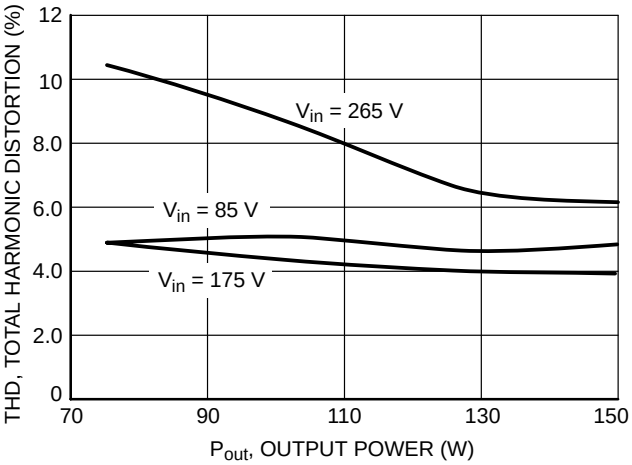


Figure 37. THD vs. Output Power

One can see on Figure 37, similarly to the power factor, THD is much higher at high line for low output powers. Again, this is because the controller operates in discontinuous mode. This results in higher di/dt and therefore in higher distortion levels. Because of the rapid transitions of the input current waveform, it is a lot harder to filter in the EMI filter. It can be observed in comparison that at high line, high output power, THD levels are much lower because the controller is then working in CCM. Adding inductance to the inductor would allow it to maintain CCM operation longer and help in reducing THD. Again, this will results in a larger inductor, which may go against satisfying the design constraints.

In many systems, the requirement from the customer is to meet the harmonic reduction requirements for the load range of 75 W to full power. In that case, it is important to keep the circuit in CCM at 230 Vac and 75 W load in order to ease the compliance with IEC 1000−3−2.

NCP1651: 120 W Single Stage Power Factor Design Example (Flyback)

I. Circuit Description and Calculations

The NCP1651 is a single stage power factor controller designed to work in a flyback configuration. This controller presents the significant advantage of combining both the first stage power factor pre−conversion along with the secondary stage dc−dc conversion into one IC. This results in multiple savings for the user as the number of surrounding components and magnetic devices is greatly reduced.

Similarly to the NCP1650 PFC project, in order to start the design, the circuit basic specifications must be defined. These specifications will govern the main attributes of the circuit components, mainly, the transformer size and the selection of the MOSFET, the output rectifier and the output diode. The following parameters will be used to calculate the various component values.

Maximum rated output power: $Pout_{max}$ = 120 W

Minimum operating line voltage: Vin_{min} = 85 Vac

Maximum operating line voltage: Vin_{max} = 265 Vac

Line frequency: f_{line} = 47−63 Hz

Nominal switching frequency: f_{sw} = 100 kHz

Nominal regulated output voltage: Vout = 12 Vdc $\pm$ 10%

System efficiency: η = 0.8 (expected)

Transformer

While in a two stage approach, the input of the dc−dc stage is regulated at 400 V, the input of the one−stage flyback is unregulated and subject to variations in the line voltage. For that reason, the flyback topology is subject to high peak currents and necessitates a rugged transformer.

The design of the transformer was done using the ON Semiconductor design aid available online for downloading. Similarly to the design of the NCP1650, the primary inductance of the transformer was chosen to minimize input ripple current. A higher inductance value will yield a lower primary peak current but will favor copper losses. An inductance value of 800 μH is therefore used.

Choosing the right turns ratio is more complicated and is somewhat of a balancing act. On the one hand, using a large turn ratio means that lower power dissipation in the MOSFET and output rectifier can be achieved. The large turns ratio allows a small primary current to sufficiently support the load. Because power dissipation in the MOSFET is proportional to Ip^2 x $R_{DS(on)}$, a small diminution in primary current can lead to a large reduction in power dissipation. In addition, having a large turns ratio yields to a low secondary voltage and decreases the voltage stress on the secondary diode during the off−state. An output rectifier with a low reverse voltage rating (V_R) can then be selected. This is important because lower V_R diodes have lower forward voltage drops (V_F). Diode losses being proportional to I_F x V_F, it helps in minimizing the diode power dissipation.

On the other hand, using a small turns ratio has numerous advantages, the obvious being size and cost. One typically tries to keep the turns ratio below 20:1 to confine the transformer to a reasonable size and cost. Second, having a small turns ratio means that only a small portion of the output voltage is being reflected back to the primary i.e., in this design 12 V/turn x 7 turns = 84 V. In addition, primary leakage inductance grows with the number of turns due to capacitance coupling of the wire and increases the magnitude of voltage ringing on the drain of the MOSFET. Because the power MOSFET is subjected to the rectified input voltage plus the reflected voltage and leakage spikes, it is recommended that the turns ratio be kept to a minimum.

A first approximation of the transformer turn ratio can be obtained from the following diagram. It expresses the maximum expected drain−to−source voltage (V_{DS}) of the MOSFET (not including leakage inductance contribution) and secondary voltage according to the transformer turns ratio. This should allow user to choose the right turns ratio to minimize the power dissipation in the MOSFET and output diode.

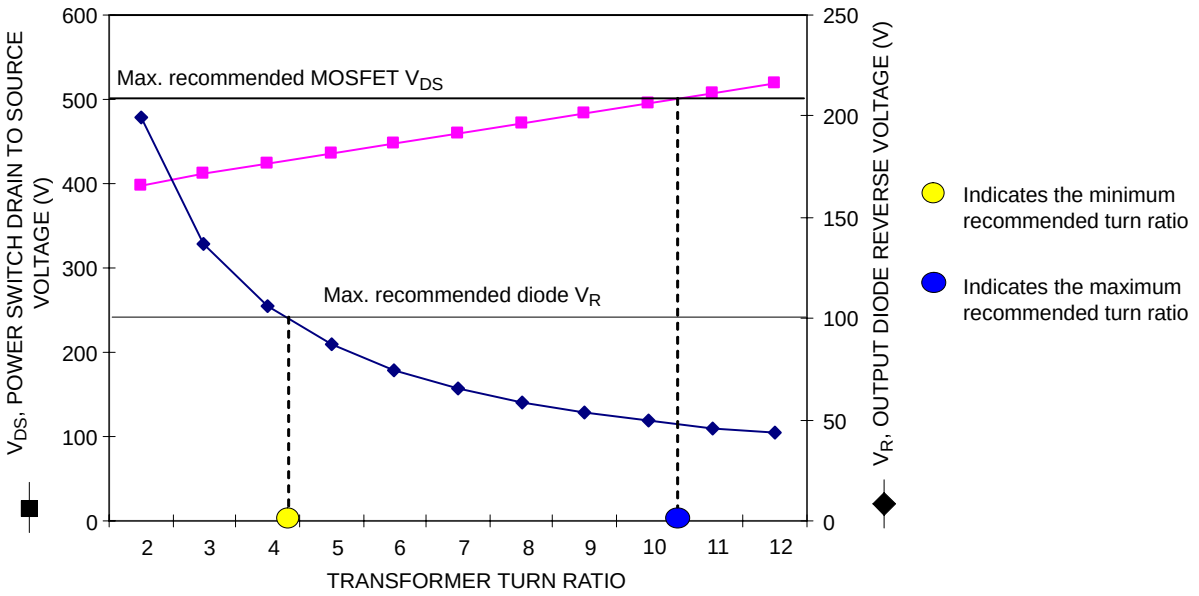


Figure 38. V_{DS} and V_R vs. Transformer Turns Ratio (12 V Output)

The turns ratio is selected to keep the drain−to−source voltage to a reasonable level. A lower V_{DS} allows to select a MOSFET with a lower $R_{DS(on)}$, and therefore lower conduction losses. The lower the drain−to−source voltage, the lower the $R_{DS(on)}$. The expected V_{DS} shown in Figure 38 does not include the voltage ringing generated by the primary leakage inductance of the transformer. The leakage inductance contribution becomes worse at higher turns ratios. Consequently, it is necessary to keep some level of safety margin in selecting the V_{DS} rating of the MOSFET. It is recommended to select a turns ratio that will yield a V_{DS} inferior to 500 V or to the left of the reference point in Figure 38. This design prefers to use a MOSFET with a V_{DS} rating of 800 V. This allows for 300 V of margin while maintaining a low $R_{DS(on)}$, see MOSFET section. If the MOSFET voltage ringing becomes more pronounced, the use of a snubber will become necessary to protect the switch at the detriment of efficiency as the snubber dissipates heat while absorbing the voltage spikes.

In selecting the output diode, the lowest forward voltage yields to the lowest power dissipation (neglecting switching losses). Because the forward voltage magnitude is directly related to the reverse voltage rating, picking a diode with a low V_R helps in minimizing losses. Lowest V_R are achieved at smaller turns ratio. It is recommended to select a turns ratio producing a V_R lower than 100 V or to the right of the reference point in Figure 38.

The auxiliary winding is there to supply the controller bias voltage when in operation. It is designed to provide a minimum of 12 V to the Vcc pin of the NCP1651 IC and therefore utilizes the same turns ratio as the secondary winding. A Zener diode clamps the voltage at 18 V to protect against ringing. The auxiliary winding should be connected to be in phase with the secondary winding.

It is important to specify to the transformer manufacturer to keep the primary leakage inductance to a minimum in order to minimize the size of the voltage ringing that appears across the MOSFET when it turns off. If the leakage inductance is very large, a transient voltage suppressor will have to be added to protect the MOSFET.

In summary, some tradeoffs have to be made in order to pick the right magnetics. Either the design is optimized to reduce power losses in the MOSFET and in the output diode or it is optimized to lower voltage stress on the MOSFET and losses in the transformer and snubber. A lower turns ratio will favor higher peak currents in the primary and higher forward voltage in the output rectifier. A higher transformer turns ratio will favor leakage inductance, core and winding losses, as well as a higher drain−to−source voltage. Choosing the right ratio has a lot to do with the available offering of MOSFETs and rectifiers and their electrical characteristics.

Power Switch

The power MOSFET selection is based on the maximum drain to source voltage and maximum peak current Ipk. V_{DS} is determined by the rectified input voltage plus the reflected output voltage and leakage inductance voltage.

$$V_{DS} = \sqrt{2} \cdot Vin_{max} + \frac{Np}{Ns} \cdot Vout + I_p \cdot \sqrt{\frac{Lp(leakage)}{Cp + Coss}}$$

where $\frac{Np}{Ns}$ is the primary to secondary turns ratio, Ip is the primary transformer current, Lp(leakage) is the primary winding leakage inductance, Cp is primary winding parasitic capacitance (1.0 nF typ.), and Coss is the MOSFET output capacitance (800 pF here).

The maximum switch current is the same as the primary winding peak current. The primary current is a function of the maximum line current and the allowable ripple current. It can be approximated with the following equation, or also using the Excel design aid.

$$Ipk = \frac{\sqrt{2} \cdot Pin \cdot T}{Vin_{min} \cdot ton} + \frac{2 \cdot \sqrt{2} \cdot Vin_{min} \cdot ton}{Lp}$$

where Lp is the primary winding inductance and ton is the power MOSFET on time. The highest peak current will occur at low line and high load. Figure 39 shows the different currents flowing through the transformer. The minimum and maximum currents of the line current waveform are represented by the pedestal current, Iped, and the peak current, Ipk respectively.

In order to minimize switching and conduction losses, keep in mind to select a MOSFET with low gate charge, low capacitance and low $R_{DS(on)}$. This design utilizes a CoolMOS SPP11N80C3 MOSFET from Infineon. This particular MOSFET was chosen for its low $R_{DS(on)}$ of 0.45 Ω, 800 V drain to source voltage, and 11 A drain current rating. Its gate charge of 60 nC and low device capacitance of 1600 pF helped in reducing switching losses.

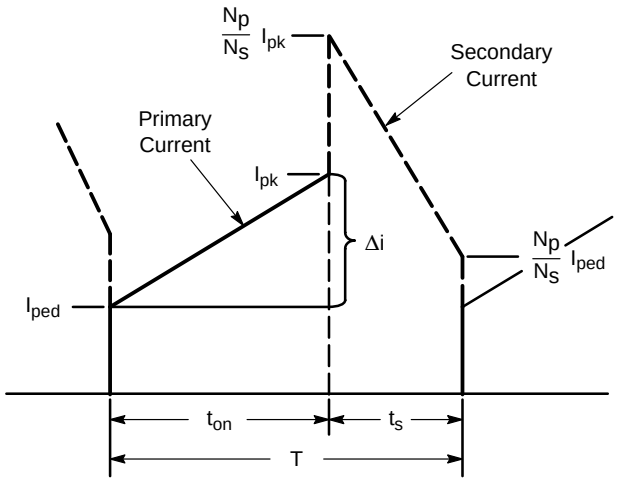


Figure 39. Primary and Secondary Currents of the Flyback Transformer

Output Rectifier

The output rectifier must be selected to minimize power losses and maximize efficiency. The most important parameters to consider are the diode forward current, I_F, forward voltage, V_F, and the reverse voltage, V_R. The diode must be able to sustain the high currents necessary to supply the load and withstand the high reverse voltage, making the device type selection (Schottky vs. ultrafast) very important. I_F should be at least equal to the average output current, and V_R should be greater than the sum of the output voltage plus the input voltage reflected to the secondary.

$$V_R \geq Vout + \sqrt{2} \cdot Vin_{max} \cdot \frac{Ns}{Np}$$

Power dissipation in the output rectifier can be calculated with the excel spread sheet. Average power losses are a combination of conduction and recovery losses. Having a low forward voltage drop will minimize conduction losses. Part of the conduction losses are also related to the transformer turns ratio. As the turns ratio increases, the stress and power dissipation will increase as the peak diode current will go up. This relationship can be seen in the formula calculating the output diode power dissipation:

$$Pd = V_F \cdot I_F \cdot (1-D) \text{ with } I_F = \frac{(Ipk + Iped)}{2} \cdot \frac{Np}{Ns}$$

It is interesting to note that the average current will remain the same as it is dependent on the load only. Also, the reverse voltage rating will move in the opposite direction of the peak current and decrease at higher turns ratios.

The average power losses are independent of the recovery losses since this design uses a Schottky diode. Conduction losses dominate the power dissipation.

This design utilizes ON Semiconductor Schottky diode MBR10100. This diode has a forward current capability of 10 A, a reverse voltage rating of 100 V, and forward voltage rating of 0.95 V.

Output Capacitor

One of the trade−offs made in achieving a high level of input performance and system cost savings is in the output voltage characteristics. The flyback converter has no intermediate energy storage, so the output capacitor serves dual functions: energy storage for line frequency and filtering capacitor for switching frequency ripple. This results in a capacitor substantially bigger than usual to insure that ripple voltage remains low and that hold−up times are met during brownout conditions.

The output capacitor is picked based on its capacitance value, voltage and rms current ratings. The capacitance value depends on the level of output voltage ripple desired. Acceptable levels of output ripple are typically around 5% or less, that is less than 600 mV for this design. The voltage ripple has two components, one due to the line frequency, the other due to the switching of the part. Both can be calculated with the Excel design aid spreadsheet. The voltage rating is dictated by the output voltage of the circuit plus the output ripple voltage.

The rms current rating of the capacitor is directly related to the level of ripple current to which it will be exposed. Because there is no series inductance between the output diode and output capacitor, the latter will be subjected to very large current transients due to the high switching currents in the circuit. Those high current transients can not only add some voltage ripple to the output due to ESR of the capacitor, but also damage the capacitor if not selected properly.

Usually, manufacturers list capacitors' rms current capabilities. A good rule of thumb is to choose a capacitor with an rms current rating equal to or greater than about 60% of the peak to peak capacitor current value. The peak to peak capacitor ripple current can be approximated with the Excel spreadsheet.

For this design, two large can 16 V, 15,000 μF aluminum electrolytic capacitors mounted in parallel with two 16 V, 680 μF surface mount electrolytic caps from United Chemicon were used. This rather odd assortment makes for a fairly compact capacitor bank. This capacitance value at first may appear excessive but it was necessary to not only meet the output ripple voltage requirements but also to handle the high ripple current (21 A peak). By paralleling and combining two different types of capacitors, not only is the ESR reduced, but the rms current is also spread out among them. The capacitor's ESR are such that the low frequency current ripple is mostly directed through the heavy duty 15,000 μF capacitors which have the lowest impedance and the highest current rating. Even though the 680 μF have a lower current rating, their maximum ripple current capability is not exceeded due to the sharing of the load. Using this combination of capacitors, we obtained a 120 Hz voltage ripple of 2.03 Vpp at high line. If achieving a lower ripple level is a major concern, additional capacitance can be added to the output. Adding two additional 15,000 μF capacitors further reduces the voltage ripple down to 1.57 Vpp. It is also good practice to add a 0.1 μF ceramic capacitor to snub out any high frequency component that can be present.

II. Circuit Schematic and Bill of Material

Following is a functional schematic of the NCP1651 PFC implementation. A complete schematic and the circuit bill of material can be found in the appendix at the end of this report.

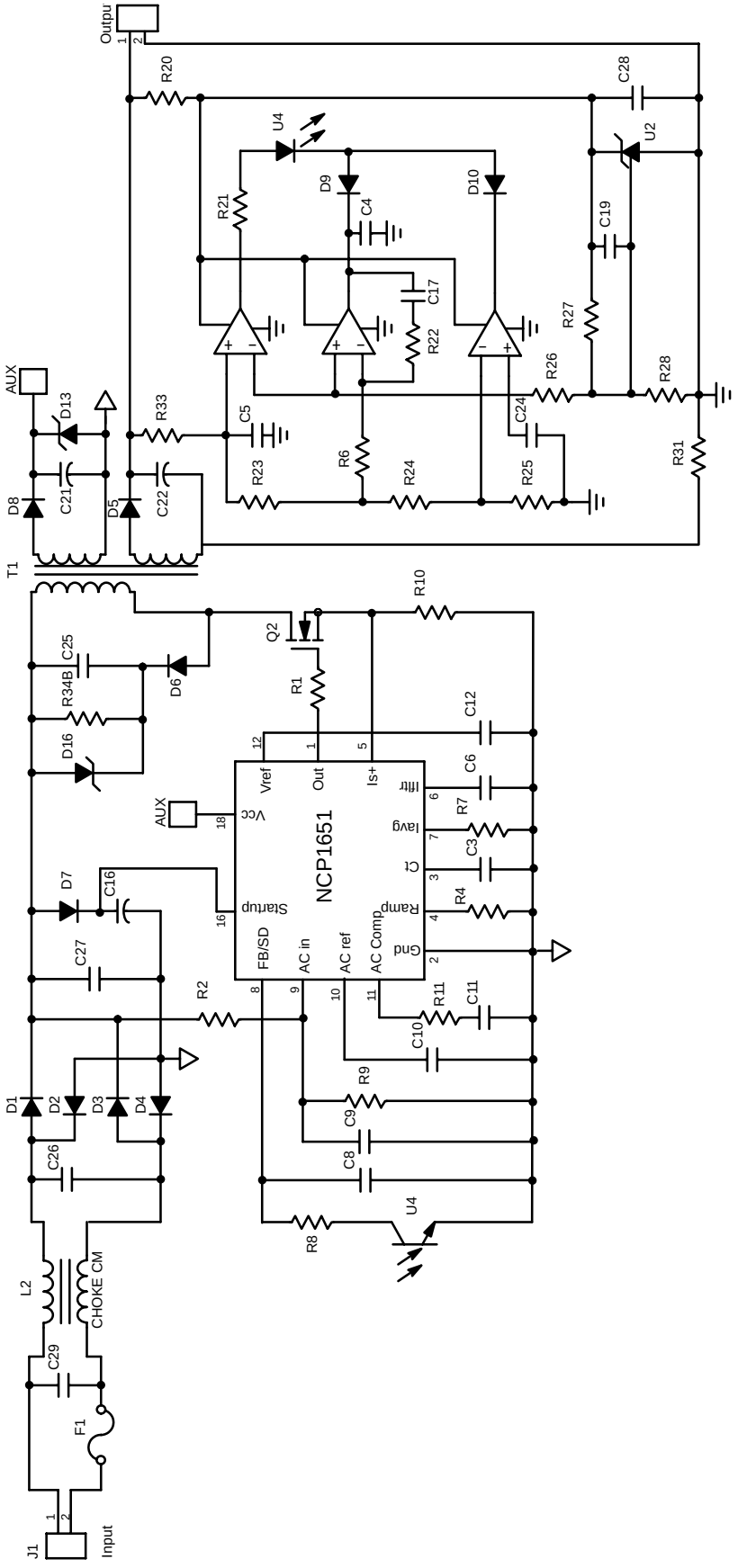


Figure 40. Simplified NCP1651 One Stage Flyback Power Factor Converter Schematic

III. NCP1651 Results

The measurements on the NCP1651 board were performed and the following results were observed.

Table 7. NCP1651 PFC Circuit Results

Vin (Vac)	85	115	230	265
Pin (W)	153.8	146	140.1	140.3
Iline(rms)	1.80	1.27	0.63	0.56
Vout (V)	11.72	11.78	11.77	11.78
Iout (A)	10	10	10	10
Efficiency (%)	76.2	80.7	84.0	84.0
PF (%)	99.79	99.86	96.70	93.87
THD (%)	4.76	4.29	6.4	7.9

Table 7 shows that a good efficiency can be expected from the NCP1651 at the input voltage range of 115 Vac and above. Efficiency suffers at low line voltage. The line current increasing at lower line voltage, higher power dissipation is observed in the MOSFET and output rectifier. On the other hand, very good power factor (PF) and THD performance are observed at all input voltages. A slight decrease in PF and THD performance is observed at 265 Vac as the device alternates between DCM and CCM depending where we are on the rectified sinewave. DCM occurs near the zero crossing while CCM is maintain throughout the rest of the cycle period.

It is also interesting to vary the output load to change the output power of the circuit and observe its effects on efficiency, power factor, and total harmonic distortion. The following three plots illustrate the results.

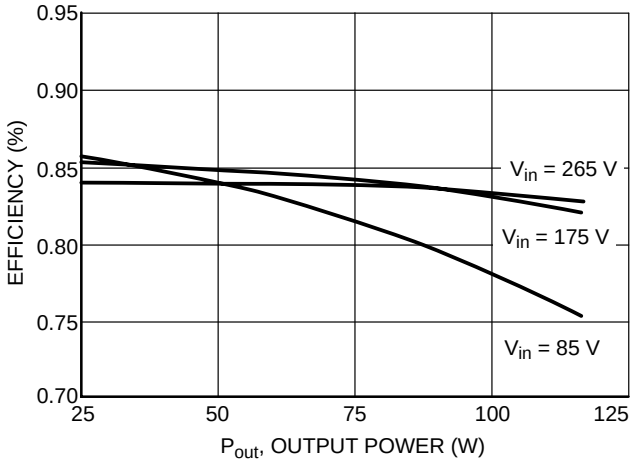


Figure 41. Efficiency vs. Output Power

As Figure 41 indicates, the higher the line input voltage, the higher the efficiency. At higher line voltage, the input current needed to sustain the load is lower and less power is dissipated in the various components, leading to a more efficient circuit. Efficiency is typically lower at higher loads when the line current is much greater and therefore the power dissipation in the power MOSFET and output rectifier are greater. This accentuates at low line, high loads, for the same reason.

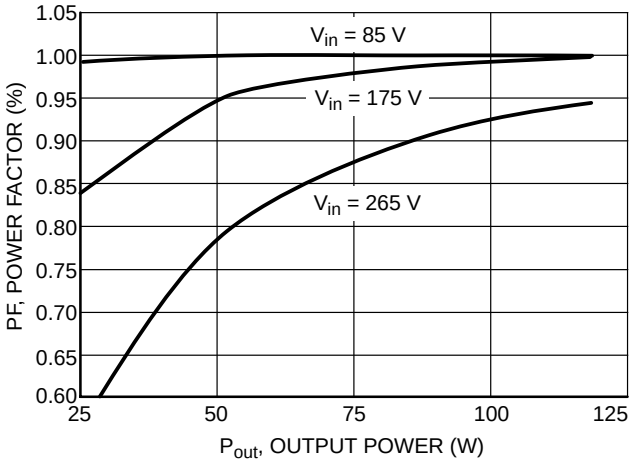


Figure 42. Power Factor vs. Output Power

As Figure 42 indicates, power factor improves as the output power increases. At lower output power levels and high line (175 Vac and 265 Vac), the circuit operates in discontinuous mode. DCM operation forces faster di/dt and higher peak currents in the power switch and output rectifier. The higher the line voltage and the lower the output power, the shorter the power switch on time becomes and the more the power factor level suffers as a result. At low input line voltage, the device operates in CCM whatever the output power and therefore distortion does not become an issue. Adding more inductance to the primary would help extend the range over which the circuit will run in CCM and help improve the power factor levels throughout.

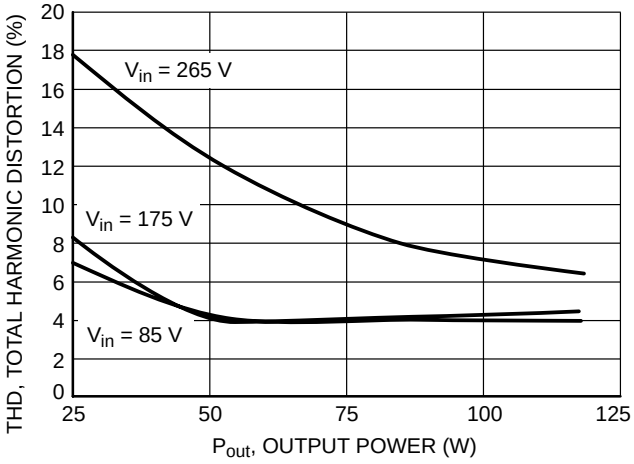


Figure 43. THD vs. Output Power

As seen on Figure 43, similarly to the power factor, THD is much higher at high line for low output powers. Again, this is because the controller operates in discontinuous mode. This results in higher di/dt and therefore in higher distortion levels. Because of the rapid transitions of the input current waveform, it is a lot harder to filter in the EMI filter. In contrast at high line, high output power, THD levels are much lower because the controller is then working in CCM. Using more primary inductance would help maintain CCM operation longer and reduce THD. However, a larger inductor may go against satisfying some of the design constraints.

CHAPTER 5

Detailed Analysis and Results of the Four Approaches

This chapter provides a detailed analysis of the results obtained with the four different approaches. Comparative analyses and rankings are provided for the topologies for given criteria. There are two sections to this chapter; the first addresses the PFC preregulator and the second addresses the overall design. In addition, some trend charts for different power levels are provided for the designer's benefit.

PFC Preregulator Stage

This section addresses the main power components of the first stage. For ease of comparing the four implementations, some assumptions were made. The details of the work are centered around 150 W. Table 8 summarizes the size and electrical characteristics for each design attribute.

Table 8. PFC Detail Comparisons

Attribute	P1− MC33260 CRM Boost	P2− MC33260 CRM Follower Boost	P3− NCP1650 CCM Boost	P4− NCP1651 CCM Flyback
Inductor	607 μH 5.54 Apk 1.76 in^2 2.97 in^3	200 μH 5.54 Apk 1.25 in^2 1.57 in^3	800 μH 3.4 Apk 1.17 in^2 1.64 in^3	800 μH pri, 6.6 Apk 10 μH sec, 7:1, 3.80 in^2 8.68 in^3
Output Capacitor(s)	220 μF, 450 V 2.17 Apk 0.759 in^2 1.34 in^3	330 μF, 450 V 2.81 Apk 1.49 in^2 2.05 in^3	100 μF, 450 V 1.30 Apk 0.59 in^2 0.812 in^3	31,360 μF, 16 V 21 Apk 1.14 in^2 1.60 in^3
Power Switch	500 V 0.52 Ω $R_{DS(on)}$ TO220 0.077 in^2 0.067 in^3	500 V 0.52 Ω $R_{DS(on)}$ TO220 0.077 in^2 0.067 in^3	500 V 0.52 Ω $R_{DS(on)}$ TO220 0.077 in^2 0.067 in^3	800 V 0.45 Ω $R_{DS(on)}$ TO220 0.077 in^2 0.067 in^3
Power Diode	Ultrafast 600 V, 4.0 A V_F = 1.28 V Axial Lead 0.034 in^2 0.017 in^3	Ultrafast 600 V, 4.0 A V_F = 1.28 V Axial Lead 0.034 in^2 0.017 in^3	Ultrafast 600 V, 8.0 A V_F = 2.5 V TO220 0.077 in^2 0.067 in^3	Schottky 80 V, 10 A V_F = 0.95 V TO220 0.077 in^2 0.067 in^3
Frequency Range	25−476 kHz	43−476 kHz	100 kHz Fixed	100 kHz Fixed
RCD Clamp	N/A	N/A	N/A	13 kΩ, 6.0 W 0.01 μF, 1.0 kV ceramic 1.5KE250+1.5KE100 0.53 in^2 0.88 in^3
TVS	N/A	N/A	N/A	MUR460 .06 in^2 .0094 in^3
Control	V−mode	V−mode	I−mode	I−mode
Total Volume	4.39 in^3	3.70 in^3	2.59 in^3	*11.30 in^3

*Includes both PFC and dc−dc stages.

EMI components were omitted from this table as the EMI filter had not been optimized at the time the readings were made. For a comprehensive description of the EMI filter elements and their effect on the circuits' performance, please refer to Chapter 6.

Inductor/Transformer

Based on the results in Table 8, it appears as if the MC33260 follower boost solution represents the cheapest and most compact board design, considering the low inductance value. As mentioned earlier however, P2's inductor is subjected to large flux swings as a result of the high current ripple, and extra care has to be given in selecting the magnetic core. Furthermore, P1 and P2 operate in CRM and are exposed to much larger inductor currents. They will typically require larger gauge wire to handle the current capacity. When designing the inductor it is also very important to minimize DCR to lessen conduction losses. Strictly comparing the two CRM PFCs, the difference in inductance value for P1 and P2 validates that the follower boost indeed allows for a smaller inductor for the same given conditions.

When it comes to achieving the most compact board design, the NCP1650 yields the best solution. Because it operates in CCM, it needs to handle the least amount of peak current. As a result, this design uses the smallest core, an EER28, and makes for a very small inductor. P4 utilizes a flyback transformer combining the boost inductor of the first stage with the two−switch forward transformer of the second stage. It is therefore the largest and most costly magnetic component of all four designs. However, using this approach saves two whole magnetic components vs. the three necessary to implement a traditional boost PFC plus dc−dc stage approach. Refer to Chapter 3 for specific size.

Power Switch

The power switch is a fixed parameter for the first three approaches. For the CRM operation, the MOSFET turn−on switching losses are minimized since the current is zero at the MOSFET turn−on. Hence, the focus is placed primarily on minimization of the conduction losses. The peak current in both P1 and P2 are much higher than in P3, hence they exhibit higher conduction losses because they operate in CRM versus CCM for P3. As a result, P1 and P3 are more prone to thermal losses and special attention needs to be given in selecting the heatsinks for the MOSFETs. Because P4 uses a flyback topology, it necessitates a higher voltage rating MOSFET as its drain−to−source voltage exceeds 500 V. The higher drain−to−source voltage is due to the reflected secondary voltage and the voltage ripple from the primary winding leakage inductance that add to the rectified line voltage. In order to dampen the effect of the leakage inductance and protect the MOSFET, it is necessary to add a snubber circuit between the rectified line and the drain of the power switch. Unfortunately, this addition lowers the efficiency of the converter, particularly at low line where the primary current is higher. On a more positive note, P4 allows the use of a single MOSFET vs. the two necessary in the two stage approaches.

Power Diode

CRM operation significantly simplifies the diode operation and selection because reverse recovery time is not of importance. The diode in P3 must be able to sustain the high currents necessary to supply the load and withstand the high reverse voltage; therefore, a TO220 package was chosen to handle the high power dissipation. An axial lead ultrafast diode was sufficient for P1 and P3 since the power dissipation was substantially lower. The lower voltage rating requirement of P4 allows the use of an 80 V, 10 A Schottky rectifier. It eliminates switching losses and reduces power dissipation. The diode is still subject to high currents and need proper heatsinking to dispense the 10 W of conduction losses. If board size is not a major concern, the TO247 package may be more suitable, as it has a higher power rating.

Output Capacitor

The largest output capacitance is used in P4. Although it appears excessive at first, the amount of capacitance is necessary in order to cope with the high current ripple. Strictly looking at the first stage, the second largest output capacitor is used in P2. This is a byproduct of the higher output voltage ripple present in the follower boost. Ideally, P1 and P3 would use the same output capacitance but as explained in Chapter 3, additional capacitance was needed for P1 to lower its output voltage ripple to an acceptable level. Once combining the two stages however, the amount of capacitance used in P4 approach does not appear as excessive in comparison.

Table 9. PFC Preregulator Stage

Attribute	F1+P1 MC33260 CRM Boost	F2+P2 MC33260 CRM Follower Boost	F3+P3 NCP1650 CCM Boost
*Cost ($)	7.20	7.75	6.44
THD @ 265 Vac (%)	17.6	21	6.26
Efficiency @ 85 Vac (%)	88	89.5	87
Power Density (W/in^3)	34.16	40.54	57.91
Hold−up Capability (ms)	20	20	20

*Cost is for budgetary purpose only and is based on 1,000 units. Actual production costs may vary significantly.

Results for the Preregulator Stage

Table 9 addresses the results for the preconverter stage only and, in the spirit of making a fair comparison, P4 cannot be included at this point. From a cost and efficiency standpoint, P1 through P3 are comparable. Typically, if savings are made on the primary side by using a cheaper inductor or MOSFET, it is usually offset on the secondary side by the need for better or larger components than what would have been required otherwise. As with P3, savings are realized on the primary side by using a cheap inductor, while

it requires a beefier rectifier on the secondary side. To the opposite, P1 and P2 require larger components on the primary side but can get away with cheaper parts on the secondary. Efficiency wise, a noticeably slightly higher efficiency can be observed in the traditional and follower boost mode partly due to low turn−on losses of the MOSFET. If the primary focus is to achieve low THD levels, P3 is by far the best solution. However, the design of P3's control loop is much more complex as current mode converters require ramp compensation when operating at duty cycles higher than 50%. P1 and P2 employing a voltage control mode of operation, ramp compensation is not necessary. Consequently, if ease of design is favored, P1 and P2 provide the simplest implementation with the lowest external component count. The best power density is still obtained with P3 due to the smaller size components it uses.

Below is a graphical representation of the efficiency observed over a 75 W−150 W range.

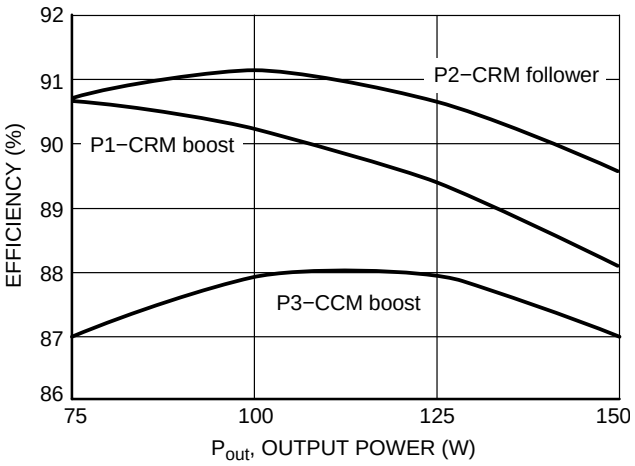


Figure 44. Efficiency vs. Output Power for the MC33260, MC33260 Follower Boost, and the NCP1650

As can be seen in Figure 44, P1 and P2 show better efficiency at low power versus P3 because they operate in CRM and are more suitable for low power applications. At higher power, the efficiency curves begin to converge demonstrating that the NCP1650 CCM Boost Converter is more suitable. As output power consumption requirement increases, peak currents increase particularly for the CRM converters and more power gets dissipated in the power switch and inductor.

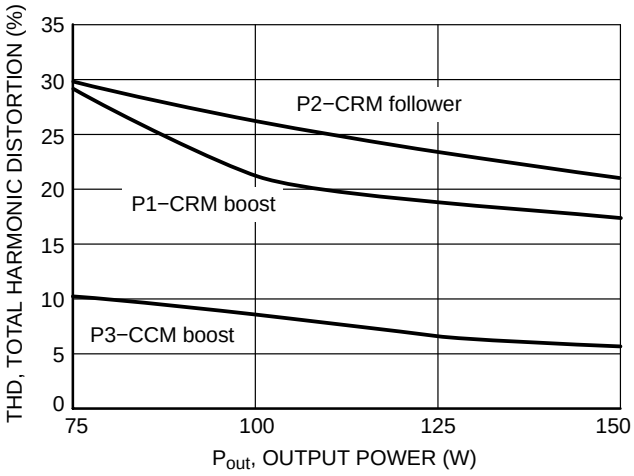


Figure 45. Total Harmonic Distortion vs. Output Power for the MC33260, MC33260 Follower Boost, and the NCP1650

As Figure 45 indicates P3 exhibits lower levels of THD across the power range because of its fixed frequency and lower di/dt characteristics which are easier to filter at the EMI stage. The MC33260 controller used in P1 and P2 has a minimum off time of 2.0 μs, which induces some dead time close to zero crossing. This phenomenon exacerbates at the lower power range, thus the higher distortion. In addition, the operating frequency varying with line and load, the implementation of the EMI filter is more difficult and THD suffers as a result. The higher peak current found in the CRM converters also contributes to the high THD.

Results for the Complete Power Stage

Table 10 summarizes the results of PFC pre−regulator stage and dc−dc stage. It is intended to guide the user in selecting the right topology based on system considerations such as cost, THD, efficiency, and power density. The details of the dc−dc stage analysis are contained in Chapter 3.

Table 10. Complete Power Stage

Attribute	F1+P1+D1 MC33260 CRM Boost	F2+P2+D2 MC33260− CRM Follower Boost	F3+P3+D3 NCP1650 CCM Boost	F4+P4 NCP1651 CCM Flyback
***Cost ($)**	10.44	11.85	9.68	10.54
THD @ 265 Vac (%)	17.6	21	6.26	4.76
Efficiency @ 85 Vac (%)	79.19	79.92	79.01	76.20
Efficiency @ 115 Vac (%)	82.62	82.60	82.26	80.7
Power Density (W/in^3)	19.54	20.44	27.64	10.61

*Cost is for budgetary purpose only and is based on 1,000 units. Actual production costs may vary significantly.

Some key points to take away: The cheapest solution is obtained with the CCM boost as Table 12 attests. However, depending on cost structure and volumes, further analysis could reveal otherwise. The CCM boost PFC circuits also yield the lowest THD levels. In comparison, the MC33260 approach will always be on the edge of passing IEC 1000−3−2 due to its CRM mode of operation. It is highly suggested to design with the NCP1650/1651 in order to guarantee IEC compliance. In terms of efficiency, the four approaches yield to similar levels although the single stage approach (NCP1651) exhibits the lowest efficiency. The NCP1651 is more suitable for higher output voltages (24 V, 48 V, and above) where higher efficiency can be expected. 12 V represents a boundary for this power level. When it comes to ease of use, the CRM boost PFC circuits make for the simplest implementation. Because CRM has an inherently stable current loop, it does not require compensation. The CCM boost PFC circuit does require more external components to stabilize the loop. However, it is still the most compact design in terms of power density. In the NCP1651, power density is dominated by the flyback transformer. A typical two stage PFC application uses 3 stages of magnetics, the boost inductor, the dc−dc transformer, and the output choke. Each component requires some real estate in its surrounding area and the volume sum of all three magnetic components is somewhat equivalent to that of the NCP1651 transformer. For that reason, the power density can be misleading and should only be used as a guideline.

Each design has tradeoffs in terms of cost, attributes, and design time. If the main goal is to obtain the lowest THD level at the lowest cost, then the CCM boost PFCs represent the best solution. Otherwise, if ease of implementation is more important the CRM boost PFC controllers are best.

Trend Charts

The details of the work presented thus far are centered around 150 W. The following tables provide some trends based on different power levels and can be viewed as sensitivity analyses to changes in different conditions. Projected values for each of the design attributes can be seen at each power level for every approach. Efficiency and cost assumptions can be derived consequently. Tables 11 and 12 cover a power range from 100 W−400 W whereas Table 13 covers a more extensive range 100 W−1000 W, and Table 14 only covers the 100 W−200 W range, in accordance with each controller specification.

The following assumptions were made in completing the tables. The value of C_{out} is based on 30% output voltage ripple and 20 ms holdup time. The primary inductance Lp is based on 20% line current ripple for CCM. The primary inductance of the MC33260 circuits was based on a switching period of 40 μs. The flyback transformer design is more iterative and was optimized for low power dissipation in the various components and to ease components selection based on the circuit electrical characteristics.

Table 11. Trend Chart for the Traditional Boost − MC33260

Traditional Boost MC33260							
			MOSFET				
P_{out} (W)	L_p (μH)	C_{out} (μF)	V_{DS}	I_{DSpk}	R_{cs} (Ω)	R_{ocp} (kΩ)	C_T (nF)
100	910	49	500	3.70	0.7	12.6	7.15
150	606	73.5	500	5.54	0.7	18.9	7.15
200	455	98	500	7.39	0.7	25.2	7.15
250	364	123	500	9.24	0.7	31.5	7.15
400	227	196	500	14.78	0.7	50.5	7.15

Table 12. Trend Chart for the Follower Boost − MC33260

Follower Boost MC33260							
			MOSFET				
P_{out} (W)	L_p (μH)	C_{out} (μF)	V_{DS} (V)	I_{DSpk} (A)	R_{cs} (Ω)	R_{ocp} (kΩ)	C_T (nF)
100	519	229	500	3.70	0.7	12.6	1.01
150	346	343	500	5.54	0.7	18.9	1.01
200	259	457	500	7.39	0.7	25.2	1.01
250	208	571	500	9.24	0.7	31.6	1.01
400	130	914	500	14.78	0.7	50.5	1.01

Table 13. Trend Chart for the Traditional Boost − NCP1650

Traditional Boost NCP1650						
			MOSFET		D_{out}	
P_{out} (W)	L_p (μH)	C_{out} (μF)	V_{DS} (V)	I_{DSpk} (A)	V_R (V)	$I_F$pk (A)
100	1260	49	500	2.18	400	1.85
150	840	74	500	3.27	400	2.77
200	630	98	500	4.36	400	3.7
250	505	123	500	5.45	400	4.62
400	320	196	500	8.71	400	7.39
600	210	294	500	13.09	400	11.09
800	160	392	500	17.41	400	14.79
1000	125	490	500	21.85	400	18.48

Table 14. Trend Chart for the Single Stage Flyback − NCP1651

One Stage Flyback NCP1651								
	T1		C_{out}		MOSFET		D_{out}	
P_{out} (W)	L_p (μH) (Note 1)	Np/Ns	I_{ripple} (A)	C_{out} (μF) (Note 2)	V_{DS} (V) (Note 3)	I_{DSpk} (A)	V_R (V) (Note 3)	$I_F$pk (A)
100	800	9.0	19.8	31,360	800	4.75	80	42.7
150	800	5.0	22.0	31,360	800	9.62	100	48.1
200	800	3.0	22.8	31,360	800	18.22	150	54.6

1. Changing the primary inductance value does not greatly affect the design parameters therefore a value of 800 μH was used throughout. A higher inductance value would help lower the MOSFET peak current however a very large amount of inductance is needed to lower the ripple current by only a few mA. Additional cost spent on the magnetics is not worth the slightly improvement in current ripple.
2. Cout value is the amount of capacitance necessary to meet the ±10% output voltage ripple requirement and the capacitor ripple current. If low capacitance value with high ripple current rating capacitor were available, smaller capacitor could have been used.
3. Values indicated are actual electrical ratings of the device recommended for the design.

As seen on Table 14, the output power range is rather narrow. Because of the low output voltage of 12 V, it is very hard to accommodate higher output power for this particular topology. Higher power level means higher peak currents in the circuit, putting extra stress on the various components and drastically increasing power losses. At 200 W, the transformer turns ratio has to be kept low in order to keep the output capacitor current ripple to a manageable level. However, this causes a higher peak current in the transformer, MOSFET, and output rectifier. It also increases the reverse voltage of the boost diode, requiring a device with a larger V_F.

It is however possible to attain higher levels of output power at higher output voltages while keeping the components to reasonable sizes. For example, a 200 W/ 24 V circuit with a 800 μH primary inductance, 5 turns ratio transformer would exhibit a V_{DS} of 495 V, a 8.70 A MOSFET peak current, a 99 V boost diode reverse voltage with a 43.5 A peak current, and a 20.82 A output capacitor ripple current. As can be seen, those numbers are a lot more manageable than the ones displayed in Table 14, and therefore good circuit performance can be expected.

CHAPTER 6

EMI Considerations

Background

EMI, or electromagnetic interference, is usually created by electronic equipment and is the result of rapid voltage or current transitions within a device. The more abrupt the transition, the worse the noise interference becomes. In a typical switching power supply such as a flyback, the incessant on and off switching of the power MOSFET generates voltage pulse trains. Each one those pulse carries harmonics above its fundamental frequency. The sum of all these harmonics creates a spectrum of noise in the high frequency range.

Most electronic devices emit some type of EMI or radio frequency signal. Although it may appear benign at first, EMI can become a real problem when it starts interfering with other apparatus in the adjoining area. The severity of these interferences can be as small of a nuisance as induced snow on a TV screen, or it can be as serious as interferences with an airplane electronic flight controls.

Because of the universal presence of electronic devices around us and of the numerous negative effects that they can have, many agencies have put regulations into place to minimize their nuisances in our daily lives. The Federal Communication Commission, or FCC, is an independent US government agency in charge of regulating radio, television, satellite, and cable communications, as well controlling radio frequency interferences. As such a body, the FCC has issued a set of recommended emission limits that devices should operate under so as not to interfere with others.

EMI requirements applying to power supplies such as listed in this application note fall under FCC's Part 15 Subpart B regulation. Part 15 Subpart B applies to unintentional radiators of RF interference from low power devices such as power line carrier systems, TV receivers and interfaces. These devices generate radio frequencies that can be transmitted back into the ac line and to other connected devices, causing interferences.

EMI interference can be classified in two main categories, radiated and conducted. Radiated emissions are transmitted trough the air and are mostly present above 30 MHz. Conducted emissions are transmitted trough the ac mains and are mostly present below 30 MHz.

The emission limits as stated in the FCC rules Part 15 (1990), apply to conducted interferences on the mains leads between 450 kHz and 30 MHz, and radiated interferences measured at 10 m or 3.0 m from 30 MHz to 960 MHz and above. The upper level of frequency measurement depends on the highest frequency used or generated by the device.

EMI Measurement Results

For the purpose of this comparison, only conducted emissions were considered, and therefore all measurements fall under the 30 MHz limit. FCC recommends that for this frequency range EMI levels should be no higher than 48 dBuV.

Figures 46, 47, 50, 51, below show the conducted emission level before implementation of the EMI filter in each of the topologies. Figures 48, 49, 52, 53, depict how emission levels have dropped below the FCC recommended levels after addition of the EMI filter.

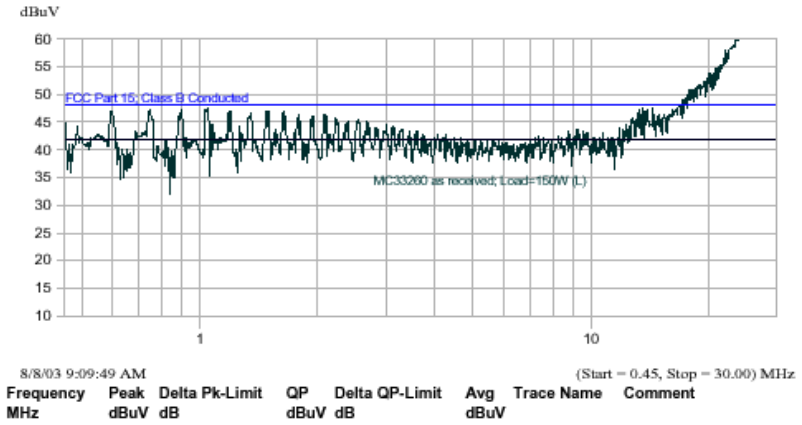


Figure 46. MC33260 Board with no EMI Filter (Line)

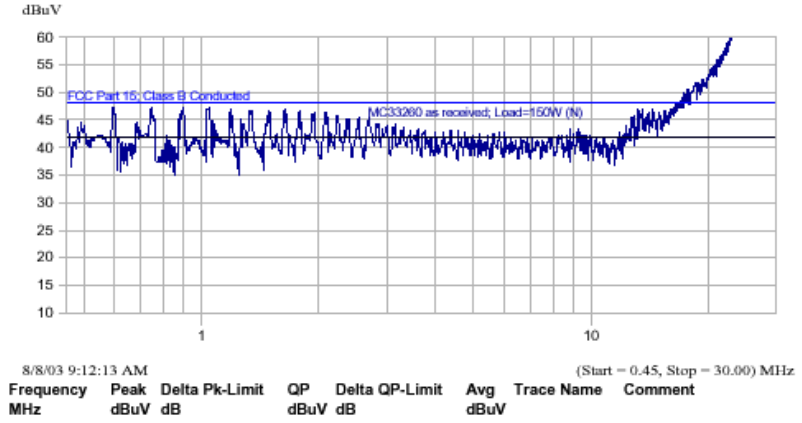


Figure 47. MC33260 Board with no EMI Filter (Neutral)

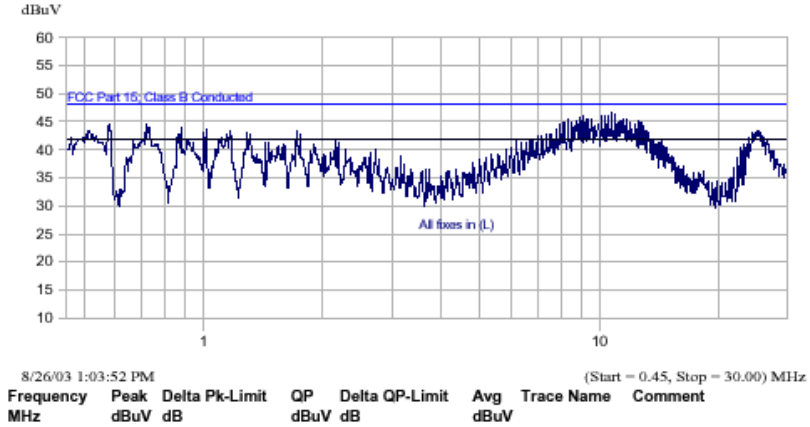


Figure 48. MC33260 Board with EMI Filter (Line)

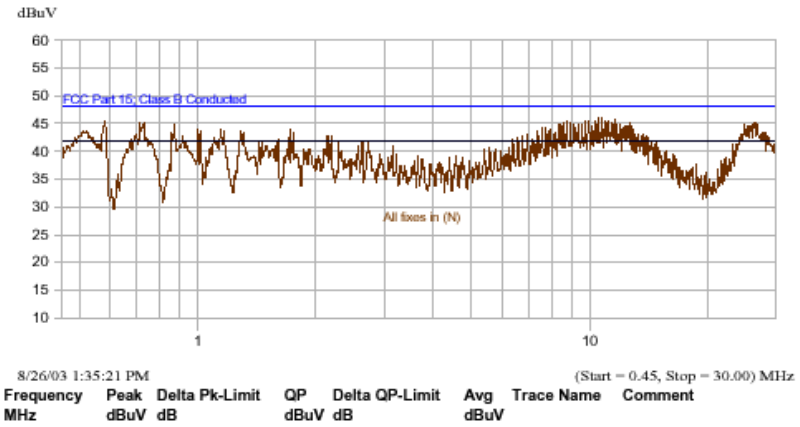


Figure 49. MC33260 Board with EMI Filter (Neutral)

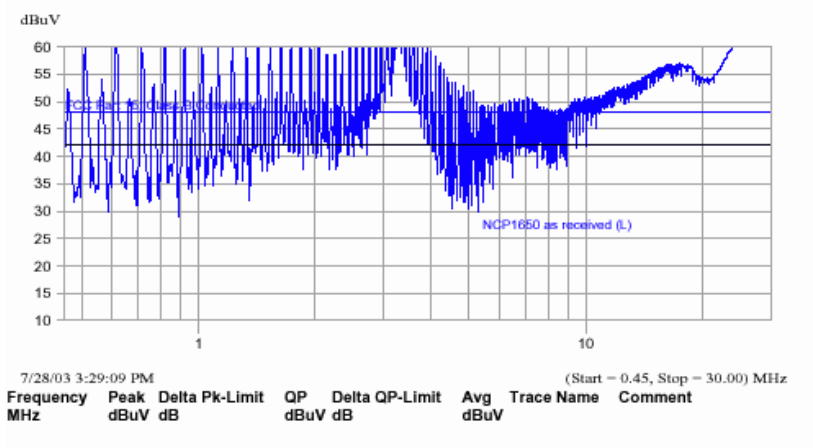


Figure 50. NCP1650 Board with no EMI Filter (Line)

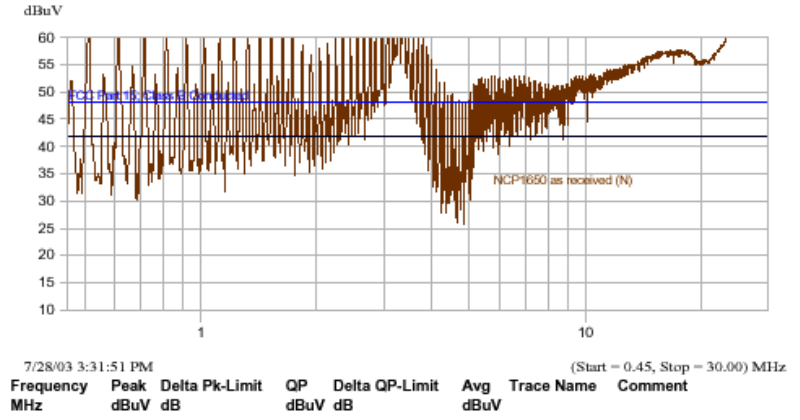


Figure 51. NCP1650 Demo Board without EMI Filter (Neutral)

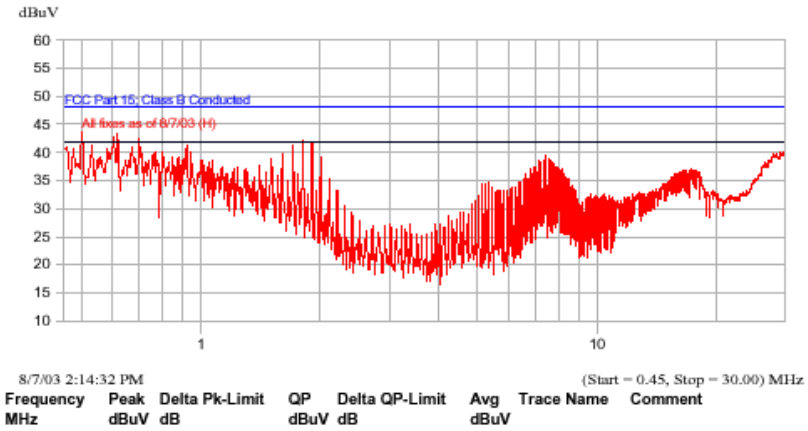


Figure 52. NCP1650 Board with EMI Filter (Line)

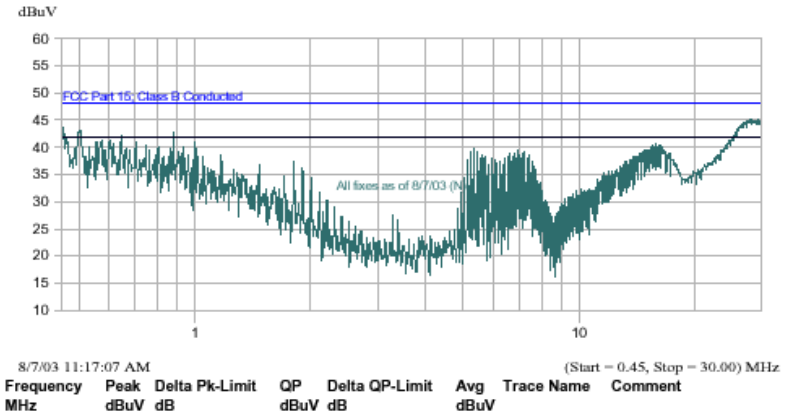


Figure 53. NCP1650 Board with EMI Filter (Neutral)

The following changes were made to the circuits in order to meet the line conducted EMI requirements when working into resistive loads.

Changes to the MC33260:

1. Addition of Coilcraft filter BU10−6003R0B as first line choke after the ac connector.
2. Changed the boost rectifier to a soft recovery MSR1560 with Ferronics 21−201−B ferrite bead in series.
3. Changed the power MOSFET to a “full−pack” type package to lower its capacitance to ground. STF9NK90Z (8.0 A, 900 V) from ST Microelectronics was used here.
4. Placed an RC snubber from drain to ground. (R = 33 Ω, C = 470 pF) with a small ferrite bead (Ferronics 21−031−B) in series. This bead absorbs some of the high frequency energy in the current spike when the snubber charges up.
5. Added an LC filter to the output after the output electrolytic capacitor (L = 47 μH, C = 0.1 μF).
6. Added a 10 Ω resistor in series with the turn off diode (D6). This value is a compromise between heat in the FET and EMI.
7. Added a ferrite bead (Fair−Rite 2773009112) between the Vcc connector and C4. This bead may not be needed when circuit is “stand−alone”.

Changes to the NCP1650:

The changes to the circuit are summarized in Figure 54 below.

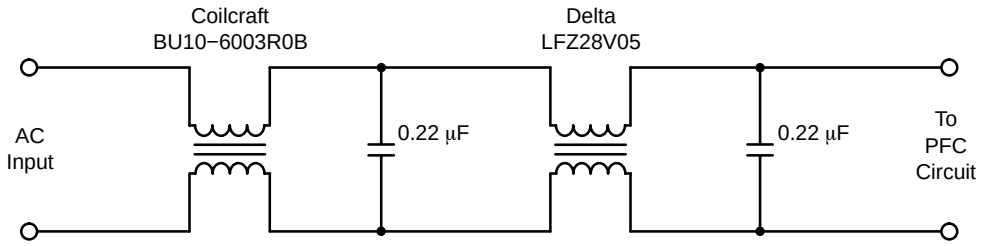


Figure 54. NCP1650 EMI Filter Schematic

Coilcraft BU10−6003R0B: inductance = 60 mH, Iac max = 3.0 A, DCR max = 40 mΩ

Delta Electronics LFZ28V05: inductance = 22 mH, Iac max = 1.3 A, DCR max = 0.36 mΩ

It is important to note that the components used in the EMI filter implementation are not optimized. Inductor selection was based on availability and not necessarily on the best choice. All three circuits use similar size filters. However, typically CRM topologies require larger inductor chokes to filter out EMI. Because CRM converters use variable frequency switching and have higher peak currents in the inductor, they do require more substantial components and a more complex design. In comparison, the CCM converter uses fixed frequency operation and is subject to smaller peak currents. As a result, the EMI filter design is more compact and cost effective and a smaller common mode inductor could have been used.

Lastly, even though those changes greatly improve the EMI signature, they are detrimental to the efficiency of the circuit. The addition of a snubber to the MC33260 circuits increases power dissipation. Additional power is also lost in the EMI filtering stage due to the DCR of the inductors and ESR of the capacitors. The use of a 900 V TO247 MOSFET as recommended to lower capacitance to ground is done at the cost of a higher $R_{DS(on)}$ (1.1−1.3 Ω now) and also negatively affects efficiency.

It is also important to note that implementing an EMI filter is a complex and iterative process. Not only does it require the use of specialized equipment, but the measurements need also to be done in very specific conditions to prevent parasitic effects from the surroundings that could falsify the readings.

For these reasons, and for the sake of keeping this report brief, only the results have been published. In addition, those results can only be viewed as recommendations and should serve by no mean as a substitute from a rigorous assessment by a competent body. In order to obtain full compliance with the EMI directives, the apparatus will have to be certified by an accredited testing facility.

If the power supply is destined to the European market, it may be necessary to seek conformity through the local agencies, as different requirements are enforced there. For more information on those standards, contact the IEC (International Electrotechnical Commission), the CENELEC (European Committee for Electrotechnical Standardization), or the CISPR (International Special Committee on Radio Interference).

REFERENCES

The following references were chosen for their relevance to the material in this paper, and are but a small sample of the vast library available to the interested reader.

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[2] Joel Turchi, *Power Factor Correction Stages Operating in Critical Conduction Mode AND8123/D Rev. 0*, ON Semiconductor, July 2003, http://www.onsemi.com/pub/Collateral/AND8123−D.PDF.

[3] Joel Turchi, *An Innovative Controller for Compact and Cost−Effective PFC Solutions*, http://www.chipcenter.com/analog/tn029.htm.

[4] Lloyd H. Dixon, Jr., *High Power Factor Preregulators for Off−Line Power Supplies*, Power Supply Design Seminar, SEM−800, Unitrode (now Texas Instrument) 1991.

[5] Lloyd H. Dixon, Jr., *Average Current Mode Control of Switching Power Supplies*, Application Note U140, Unitrode (now Texas Instrument).

[6] Alan Ball, *NCP1650/D Power Factor Controller, Rev. 1*, ON Semiconductor, March 2002.

[7] Alan Ball, *NCP1650 Benchtop Assistance, AND8084, Rev. 0*, ON Semiconductor, May 2002.

[8] Marty Brown, *Power Supply Cookbook*, Butterworth−Heinemann 1994.

[9] Tim Williams, *EMC for Product Designers: Meeting the European Directive*, third edition, Newnes 2001.

[10] Roland W. Gubisch, *Inside FCC Part 15 and Canada's Corresponding Standards*, http://www.cemag.com/99ARG/Gubish31.html 1999.

APPENDIX

Table 15. MC33260 Converter Bill of Materials

Ref Des	Description	Part Number	Manufacturer
C1,C7	Cap, 100 nF, 275 Vac X2	BC1601−ND	BC Components
C2	Cap, 470 nF, 275 Vac	BC1601−ND	BC Components
C3	Cap, 1.0 nF	−	−
C4	Cap, 10 μF, alum elec, 25 V	−	−
Cout:traditional boost	Cap, 220 μF, alum elec, 450 V	ECO−S2WP221CX	Panasonic
Cout:follower boost	Cap, 330 μF, alum elec, 450 V	ECE−S2WP331EX	Panasonic
C8,C9	1.0 nF	−	−
C_T traditional boost	10 nF	−	−
C_T follower boost	560 pF	−	−
D1−4	1.0 A, 600 V Fast Recovery Rectifier	1N4934	ON Semiconductor
D5	4.0 A, 600 V Switchmode Power Rectifier	MUR460E	ON Semiconductor
D6	1.0 A, 100 V Fast Recovery Rectifier	1N4934	ON Semiconductor
F1	2.0 A	Standard	−
Lp	Choke, Common Mode, 50 mH	47283900	Thomson Orega
L2:traditional boost	Inductor, 607 μH, axial	SRW42EC−U07V002	TDK
L2:follower boost	Inductor, 200 μH, axial	10689480	Thomson Orega
Q1	MOSFET	IRFB11N50A	IR
R3	Resistor, 47 Ω	−	−
Rcs	Resistor, 0.7 Ω, 3.0 W	−	−
R5,R6	Resistor, 1.0 M	−	−
Rocp	Resistor, 20 k	−	−
*R13	Resistor, 25 k	−	−
IC1	GreenLine Compact Power Factor Controller	MC33260	ON Semiconductor

*For traditional boost only.

1. Non−shaded values are the original non−EMI optimized filter values.
   Shaded values are the optimized EMI filter values, c.f. Chapter 6.

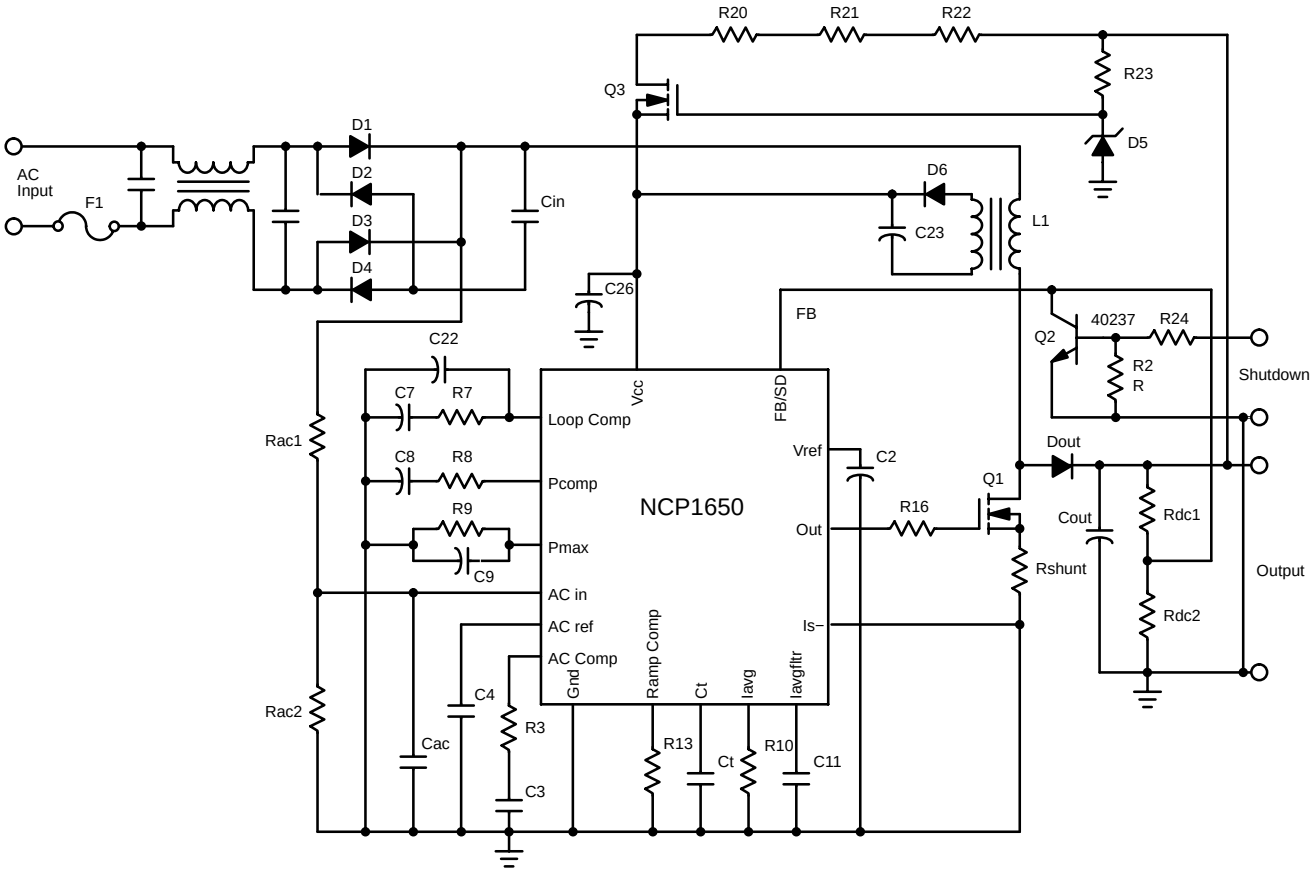

Figure 55. NCP1650 150 W PFC Boost Converter Schematic

Table 16. NCP1650 PFC Circuit Bill of Materials

Ref Des	Description	Part Number	Manufacturer
C2	Cap, ceramic, chip, 0.1 μF, 50 V	C1608X7R1H104KT	TDK
C3	Cap, ceramic, chip, 0.01 μF, 50 V	C1608X7R2A103M	TDK
C4	Cap, ceramic, chip, 1.0 nF, 50 V	C1608X7R1H102K	TDK
C5	Cap, ceramic, chip, 0.022 μF, 50 V	C1608X7R1H223K	TDK
C7	Cap, ceramic, chip, 47 μF, 6.3 V	C3225X5R0J476MT	TDK
C8	Cap, ceramic, chip, 22 μF, 16 V	C3225X5R1C226MT	TDK
C9	Cap, ceramic, chip, 4.7 μF, 10 V	C3216X5R1A475KT	TDK
C11	Cap, ceramic, chip, 470 pF, 50 V	C1608C0G1H471JT	TDK
C14	Cap, ceramic, chip, 470 pF, 50 V	C1608C0G1H471JT	TDK
C20	Cap, X type, 0.47 μF, 275 Vac	ECQ−U2A474ML	Panasonic (Digi−P10734−ND)
−	Cap, X type, 0.1 μF, 275 Vac	−	−
−	Cap, X type, 0.22 μF, 275 Vac	−	−
C21	Cap, polyprop, 0.1 μF, 400 Vdc	MKP1841−410−405	Vishay−Sprague
C22	Cap, ceramic, chip, 0.1 μF, 50 V	C1608X7R1H104KT	TDK
C23	Cap, alum elect, 100 μF, 25 V	ECA−1EM101I	Panasonic (Digi−P10413TB−ND)
C25	Cap, alum elect, 100 μF, 450 V	ECO−S2WP101BA	Panasonic (Digi−P7427−ND)
C26	Cap, ceramic, chip, 1.0 μF, 25 V	C3216X7R1E105KT	TDK
D1−D4	Diode, rectifier, 600 V, 3.0 A	1N5406	ON Semiconductor
D5	Diode, zener, 18 V, axial lead	MMSZ5248BT1	ON Semiconductor
D6	Diode, signal, 75 V, 200 mA, SOT−23	BAS19LT1	ON Semiconductor
D7	Diode, ultra−fast, 600 V, 8.0 A	MURHF860CT	ON Semiconductor
F1	Fuse, 2.0 A, 250 Vac	1025TD2A	Bussman
L1	Inductor, 800 μH, 3.4 A max	SRW28LEC−U25V002	TDK
L2[2]	Inductor, 18 mH, 1.3 A sat, com mode	LFZ28V06	Delta Electronics
L3[2]	Inductor, 10 μH, 3.0 A sat, com mode	BU10−6003R0B	Coilcraft
L2[2]	Inductor, 100 μH, 2.5 A sat, diff mode	TSL1315−101K2R5	TDK
L3[2]	Inductor, 100 μH, 2.5 A sat, diff mode	TSL1315−101K2R5	TDK
Q1	FET, 10.5 A, 0.7 Ω, 600 V, N−chl	FQP12N60	Fairchild
Q2	Bipolar transistor, 50 V	MMBT2222ALT1	ON Semiconductor
Q3	FET, 6.6 A, 0.52 Ω, 500 V	IRFiB7N50A	International Rectifier
R3	Resistor, SMT, 1.40 k, 1.0%	CRCW12061401F	Vishay
R4	Resistor, axial lead, 178 k, _ watt, 1.0%	CMF−55−178K00FKRE	Vishay
R5	Resistor, axial lead, 3.57 k, _ watt, 1.0%	CMF−55−3K5700FKBF	Vishay
R6	Resistor, axial lead, 178 k, _ watt, 1.0%	CMF−55−178K00FKRE	Vishay
R7	Resistor, SMT, 6.2 k	CRCW12066K20JNTA	Vishay
R8	Resistor, SMT, 8.9 k	CRCW12068K90JNTA	Vishay
R9	Resistor, SMT, 66.5 k, 1.0%	CRCW12066652F	Vishay
R10	Resistor, SMT, 9.53 k, 1.0%	CRCW12069531F	Vishay
R13	Resistor, SMT, 63.4 k, 1.0%	CRCW1206342F	Vishay

1. Add isolation to MOSFET and ground the heatsink.
2. Non−shaded values are the original non−EMI optimized filter values.
   Shaded values are the optimized EMI filter values, c.f. Chapter 6.

Table 16. NCP1650 PFC Circuit Bill of Materials (continued)

Ref Des	Description	Part Number	Manufacturer
R16	Resistor, SMT, 10	CRCW1206100JRE4	Vishay
R20	Resistor, axial lead, 10 k, _ watt	CCF−07−103J	Vishay
R21	Resistor, axial lead, 10 k, _ watt	CCF−07−103J	Vishay
R22	Resistor, axial lead, 10 k, _ watt	CCF−07−103J	Vishay
R23	Resistor, axial lead, 1.2 M, _ watt	CCF−07−125J	Vishay
R25	Resistor, SMT, 4.7 k	CRCW12064K70JNTA	Vishay
R26	Resistor, SMT, 12 k	CRCW120612K0JNTA	Vishay
R27	Resistor, axial lead, 453 k, _ watt, 1.0%	CMF−55−453K00FKBF	Vishay
R28	Resistor, axial lead, 453 k, _ watt, 1.0%	CMF−55−4533F	Vishay
R29	Resistor, axial lead, 9.09 k, _ watt, 1.0%	CCF−55−9K09FHR362	Vishay
R30	Resistor, SMT, 0.052 Ω, 1.0 W, 1.0%	WSL2512R0500FTB	Vishay
U1	PFC Controller	NCP1650	ON Semiconductor

3. Add isolation to MOSFET and ground the heatsink.
4. Non−shaded values are the original non−EMI optimized filter values.
   Shaded values are the optimized EMI filter values, c.f. Chapter 6.

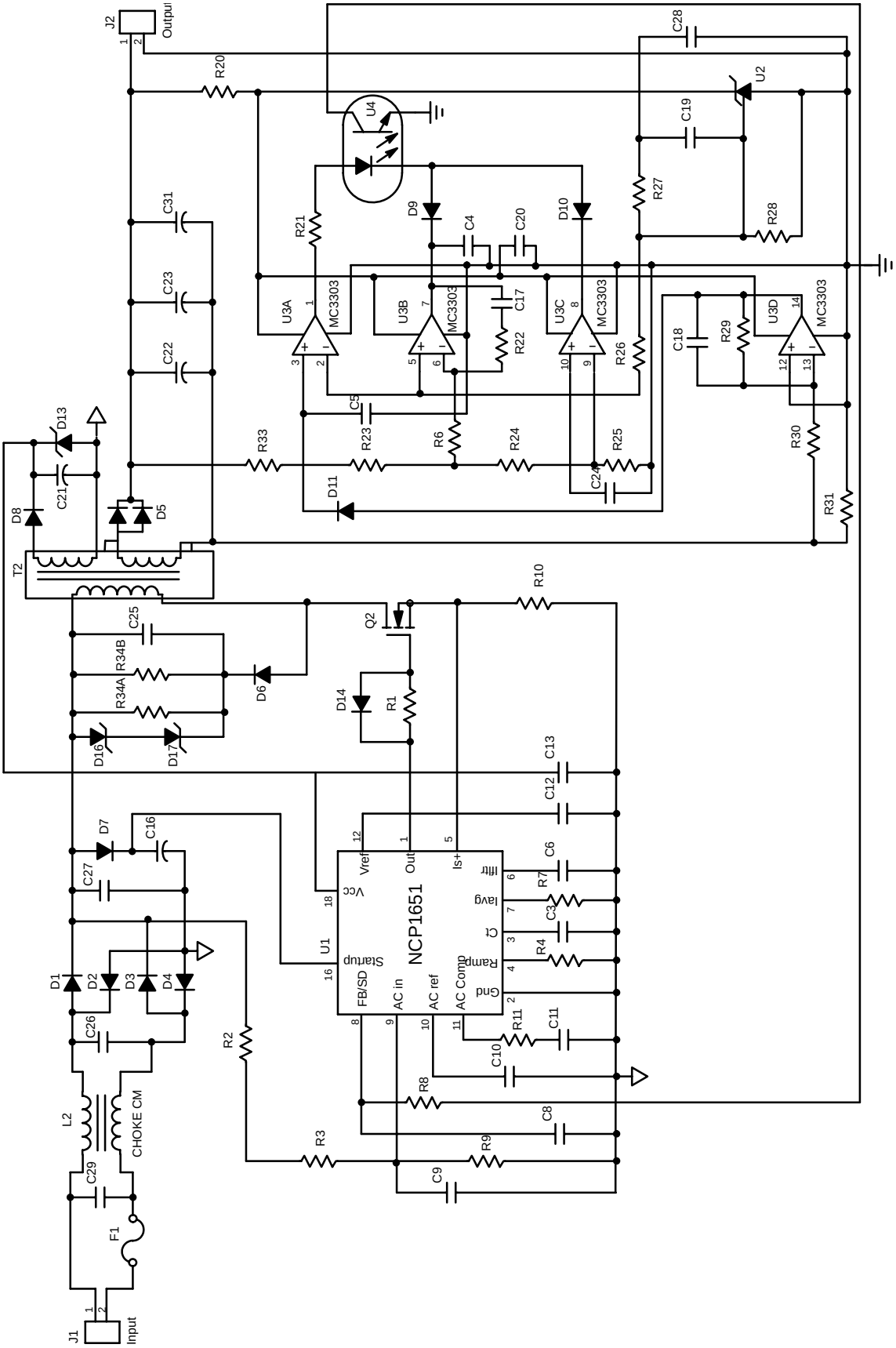

Figure 56. NCP1651 120 W One Stage PFC Flyback Converter Schematic

Table 17. NCP1651 PFC Circuit Bill of Materials

Ref Des	Description	Part Number	Manufacturer
C1	Cap, ceramic, chip, 1000 pf, 50 V	C3216X7R1H105KT	TDK
C3	Cap, ceramic, chip, 470 pF, 50 V	C1608C0G1H471JT	TDK
C5	Cap, ceramic, chip, 470 pf, 50 V	C1608C0G1H471JT	TDK
C6	Cap, ceramic, chip, 470 pF, 50 V	C1608X7R1H471KT	TDK
C8	Cap, ceramic, chip, 0.022 μF, 50 V	C1608X7R1H223KT	TDK
C9	Cap, ceramic, chip, 0.022 μF, 50 V	C1608X7R1H223KT	TDK
C10	Cap, ceramic, chip, 0.001 μF, 50 V	C1608X7R1H102KT	TDK
C11	Cap, ceramic, chip, 10 nF, 50 V	C1608X7R1H103KT	TDK
C12, C13	Cap, ceramic, chip, 0.1 μF, 50 V	C1608X7R1H104KT	TDK
C16	Cap, alum elect, 2.2 μF, 450 V (0.394 dia x 0.492 H)	ECA−2WHG2R2 EKA00DC122P00	Panasonic (Digi−P5873) Vishay Sprague (20)
C17	Cap, ceramic, chip, 22 μF, 10 V	C3225X5R0J226MT	TDK
C18	Cap, ceramic, chip, 0.047 μF, 50 V	C1608X7R1H473KT	TDK
C19	Cap, ceramic, chip, 0.01 μF, 50 V	C1608X7R1H103KT	TDK
C20	Cap, ceramic, chip, 1.0 μF, 25 V	C3216X7R1E105KT	TDK
C21	Cap, alum elect, 220 μF, 25 V	−	−
C22, 23	Cap, alum elect, 15000 μF, 16 V (5.4 A rms min) x2 Cap, alum elect, 680 μF, 16 V, x2 in parallel w/above	ECO−S1CP153AA MVZ16VC681MJ10TP	Panasonic (Digi−P6864−ND) United Chemicon
C24	Cap, ceramic, chip, 0.01 μF, 50 V	C1608X7R1H103KT	TDK
C25	Cap, ceramic, 0.001 μF, 1.0 kV	ECK−03A102KBP	Panasonic
C26	Cap, 1.2 μF, 275 Vac, X cap	ECQ−U2A125ML	Panasonic (Digi−P11012−ND)
C27	Cap, polypropylene, 0.68 μF, 400 Vdc	MKP1841−468−405	Vishay−Sprague
C28	Cap, ceramic, chip, 1.0 μF, 25 V	C3216X7R1E105KT	TDK
D1—D4	Diode, rectifier, 800 V, 3.0 A	1N5408	ON Semiconductor
D5	Diode, ultrafast, 100 V, 20 A	MBR10100CT	ON Semiconductor
D6	Diode, ultrafast, 600 V, 1.0 A	MUR460	ON Semiconductor
D7	Diode, rectifier, 800 V, 1.0 A	1N4006	ON Semiconductor
D8—D11	Diode, switching, 120 V, 200 mA, SOT−23	BAS19LT1	ON Semiconductor
D12	TVS, 200 V, 5.0 W	1.5KE250A	ON Semiconductor
D16	TVS, 100 V, 5.0 W in series w/above	1.5KE100A	ON Semiconductor
D13	Zener Diode, 18 V, 0.3 W	AZ23CK18	Vishay Dale
F1	Fuse, 2.0 A, 250 Vac	1025TD2A	Bussman
L2	Inductor, diff mode, 2.5 A sat, 100 μH	TSL1315−101K2R5	TDK
L3	Inductor, diff mode, 2.5 A sat, 100 μH	TSL1315−101K2R4	TDK
Q1	FET, 11 A, 800 V, 0.45 Ω, N−channel	SPA11N80C3	Infineon
Q2	Bipolar, npn, 30 V, SOT−23	MMBT2222ALT1	ON Semiconductor
R1	Resistor, SMT1206, 10 Ω	CRCW120610R0F	Vishay Dale
R2	Resistor, axial lead, 180 k, _ watt	−	−
R3	Resistor, axial lead, 180 k, _ watt	−	−
R4	Resistor, SMT1206, 182 k	CRCW12061823F	Vishay Dale

Table 17. NCP1651 PFC Circuit Bill of Materials (continued)

Ref Des	Description	Part Number	Manufacturer
R5	Resistor, SMT2512, 0.12 Ω, 1.0 watt	WSL2512, 0.12 Ω 1%	Vishay Dale
R7	Resistor, SMT1206, 11.56 k	CRCW12061152F	Vishay Dale
R8	Resistor, SMT1206, 680 Ω	CRCW1206	Vishay Dale
R9	Resistor, axial lead, 3.6 k, _ watt	−	−
R11	Resistor, SMT1206, 1.2 k	CRCW1206	Vishay Dale
R20	Resistor, SMT1206, 2.0 k	CRCW1206	Vishay Dale
R21	Resistor, SMT1206, 2.0 k	CRCW1206	Vishay Dale
R22	Resistor, SMT1206, 5.1 k	CRCW1206	Vishay Dale
R23	Resistor, SMT1206, 210 Ω, 1.0%	CRCW1206	Vishay Dale
R24	Resistor, SMT1206, 174 Ω, 1.0%	CRCW1206	Vishay Dale
R25	Resistor, SMT1206, 2.05 k, 1.0%	CRCW1206	Vishay Dale
R26	Resistor, SMT1206, 3.3 k	CRCW1206	Vishay Dale
R27	Resistor, SMT1206, 7.5 k	CRCW1206	Vishay Dale
R28	Resistor, SMT1206, 3.3 k	CRCW1206	Vishay Dale
R29	Resistor, SMT1206, 3.01 k, 1.0%	CRCW1206	Vishay Dale
R30	Resistor, SMT1206, 301 Ω, 1.0%	CRCW1206	Vishay Dale
R31	1.0 W, 0.07 Ω resistor	WSL2516	Vishay Dale
R32	1.0 W, 0.07 Ω resistor	WSL2517	Vishay Dale
R33	Resistor, SMT1206, 40.2 k, 1.0%	CRCW1206	Vishay Dale
R34	Resistor, axial lead, 39k, 2.0 W, x 3 in parallel	−	−
R35	Resistor, SMT1206, 4.7 k	CRCW1206	Vishay Dale
R36	Resistor, SMT1206, 12 k	CRCW1206	Vishay Dale
R37	Resistor, SMT1206, 100 k	CRCW1206	Vishay Dale
T1	Transformer, flyback	SRW54EC−U03V004	TDK
U1	PFC Controller	NCP1651	ON Semiconductor
U2	2.5 V programmable ref, SOIC	TL431ACD	ON Semiconductor
U3	Quad Op amp	MC3303D	ON Semiconductor
U4	Optocoupler, 1:1 CTR, 4 pin	SFH615AA−X007	Vishay Dale

Design of Power Factor Correction Circuit Using Greenline™ Compact Power Factor Controller MC33260

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APPLICATION NOTE

Prepared by
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Introduction

The MC33260 is an active power factor controller that functions as a boost pre−converter which, meeting international standard requirement in electronic ballast and off−line power supply application. MC33260 is designed to drive a free running frequency discontinuous mode, it can also be synchronized and in any case, it features very effective protections that ensure a safe and reliable operation.

This circuit is also optimized to offer extremely compact and cost effective PFC solutions. It does not entail the need of auxiliary winding for zero current detection hence a simple coil can be used instead of a transformer if the MC33260 Vcc is drawn from the load (please refer to page 19 of the data sheet). While it requires a minimum number of external components, the MC33260 can control the follower boost operation that is an innovative mode allowing a drastic size reduction of both the inductor and the power switch. Ultimately, the solution system cost is significantly lowered.

Also able to function in a traditional way (constant output voltage regulation level), any intermediary solutions can be easily implemented. This flexibility makes it ideal to optimally cope with a wide range of applications.

This application note will discuss on the design of power factor correction circuit with MC33260 with traditional boost constant output voltage regulation level operation and follower boost variable output voltage regulation level operation. For derivation of the design equations related to the IC please refer to MC33260 data sheet.

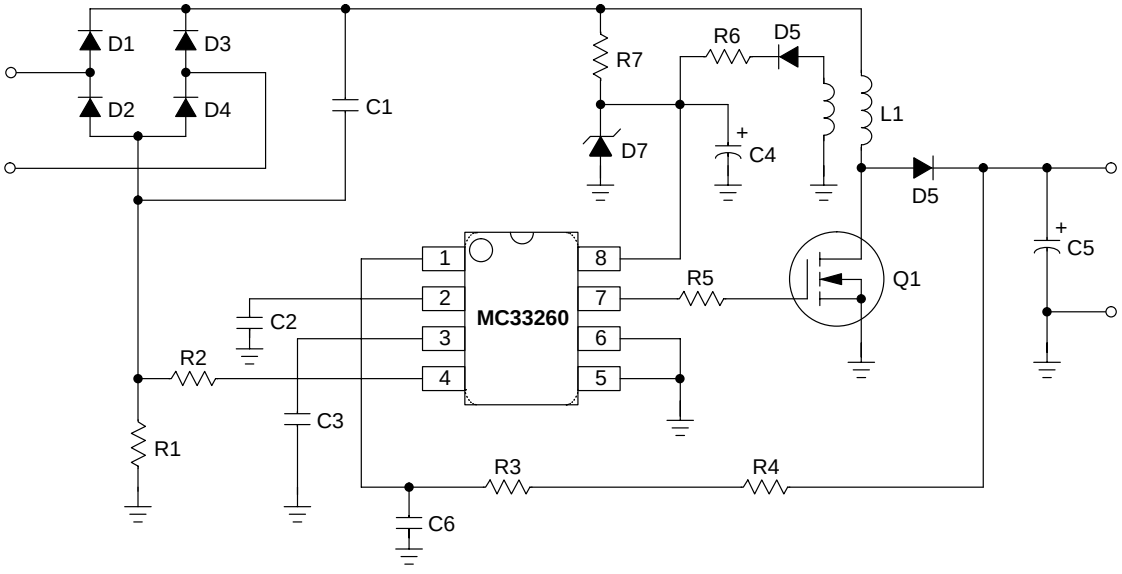

Figure 1. Application Schematic of MC33260

PFC Techniques

Many PFC techniques have been proposed, boost topology, which can operate in continuous and discontinuous mode, is the most popular. Typically, continuous mode is more favorable for high power application for having lower peak current. On the other hand, for less than 500 W application, discontinuous mode offers smaller inductor size, minimal parts count and lowest cost. This paper will discuss design of PFC with MC33260, which operates in critical conduction mode.

Discontinuous Conduction Mode Operation

Critical conduction mode operation presents two major advantages in PFC application. For critical conduction mode, the inductor current must fall to zero before start the next cycle. This operation results in higher efficiency and

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eliminates boost rectifier reverse recovery loss as MOSFET cannot turn−on until the inductor current reaches zero.

Secondly, since there are no dead−time gaps between cycles, the ac line current is continuous thus limiting the peak switch to twice the average input current. The converter works right on critical conduction mode, which results in variable frequency operation.

Inductor Waveform

$$\frac{V}{L} = \frac{di}{dt} \quad (1)$$

Equation (1) is the center of the operation of PFC boost converter where $V=V_{in}(t)$, the instantaneous voltage across the inductor. Assuming the inductance and the on−time over each line half−cycle are constant, di is actually the peak current, I_{Lpk}, this is because the inductor always begins charging at zero current.

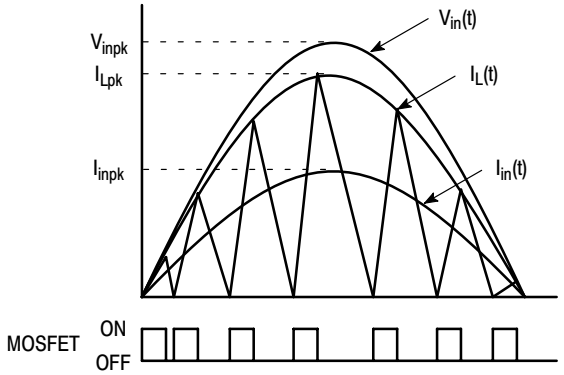

Figure 2. Inductor Waveform

Design Criteria

The basic design specification concerns the following:

- Mains Voltage Range: $V_{ac(LL)} - V_{ac(HL)}$
- Regulated DC Output Voltage: V_o
- Rated Output Power: P_o
- Expected Efficiency, η

PFC Power Section Design

Instantaneous Input Voltage, $V_{in}(t)$

Peak Input Voltage, V_{inpk}

Both $V_{in}(t)$ and V_{inpk} are related by below equation

$$V_{in}(t) = V_{inpk}\sin(\omega t) \quad (2)$$

$$\text{where} \quad V_{inpk} = \sqrt{2}\,V_{inrms} \quad (3)$$

Instantaneous Input Current, $I_{in}(t)$

Peak Input Current, I_{inpk},

Both $I_{in}(t)$ and I_{inpk} are related by below equation

$$I_{in}(t) = I_{inpk}\sin(\omega t), \quad (4)$$

$$\text{where} \quad I_{inpk} = \sqrt{2}\,I_{inrms} \quad (5)$$

Input power of the PFC circuit, P_{in} can be expressed in following equation, by substituting equation (3) and (5).

$$P_{in} = V_{inrms}I_{inrms} = \frac{V_{inpk}}{\sqrt{2}} \cdot \frac{I_{inpk}}{\sqrt{2}} = \frac{V_{inpk}I_{inpk}}{2} \quad (6)$$

The output power, P_o is given by:

$$P_o = V_oI_o = \eta P_{in} \quad (7)$$

PFC circuit efficiency is needed in the design equation, for low line operation, it is typically set at 92% while 95% for high line operation. Substituting equation (6) into equation (7),

$$P_o = \eta P_{in} = \eta\,\frac{V_{inpk}I_{inpk}}{2} \quad (8)$$

Express the above equation in term of I_{inpk},

$$I_{inpk} = \frac{2P_o}{\eta V_{inpk}} = \frac{\sqrt{2}\,P_o}{\eta V_{inrms}} \quad (9)$$

The average input current is equal to average inductor current, $I_{L(avg)}$,

$$I_{L(avg)} = I_{in} \quad (10)$$

It has been understood that peak inductor current, I_{Lpk} is exactly twice the average inductor current, $I_{L(avg)}$ for critical conduction operation.

$$I_{Lpk} = 2I_{L(avg)} = \frac{2\sqrt{2}\,P_o}{\eta V_{inrms}} \quad (11)$$

Since I_{Lpk} is maximum at minimum required ac line voltage, $V_{ac(LL)}$,

$$I_{Lpk} = \frac{2\sqrt{2}\,P_o}{\eta V_{ac(LL)}} \quad (12)$$

Switching Time

In theory, the on−time, $t_{(on)}$ is constant. In practice, $t_{(on)}$ tends to increase at the ac line zero crossings due to the charge on output capacitor C_{out}. Let $V_{ac} = V_{ac(LL)}$ for initial $t_{(on)}$ and $t_{(off)}$ calculations.

On−time

By solving inductor equation (1), on−time required to charge the inductor to the correct peak current is:

$$t_{(on)} = I_{Lpk}\frac{L_P}{Vinpk} \quad (13)$$

Substituting equation (3) and (12) into equation (13), results in:

$$t_{(on)} = \frac{2\sqrt{2}\,P_o}{\eta V_{ac(LL)}} \cdot \frac{L_P}{\sqrt{2}\,V_{ac(LL)}} = \frac{2P_oL_P}{\eta V^2_{ac(LL)}} \quad (14)$$

Off−time

The instantaneous switch off−time varies with the line and load conditions, as well as with the instantaneous line voltage. Off−time is analyzed by solving equation (1) for the inductor discharging where the voltage across the inductor is V_o minus V_{in}.

$$t_{(off)} = \frac{I_{Lpk} L_P}{V_o - V_{inpk}\sin(\omega t)} \quad (15)$$

Multiplying nominator and denominator with $V_{inpk}\sin\omega(t)$ results in:

$$t_{(off)} = \frac{\frac{I_{Lpk} L_P}{V_{inpk}\sin(\omega t)}}{\frac{V_o - V_{inpk}\sin(\omega t)}{V_{inpk}\sin(\omega t)}} = \frac{t_{(on)}}{\frac{V_o}{\sqrt{2}\,Vinpk|\sin(\theta)|} - 1} \quad (16)$$

where $\omega t = \theta$

The off−time, $t_{(off)}$ is greatest at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.

The off−time is at a minimum at ac line crossings. This equation is used to calculate $t_{(off)}$ as Theta approaches zero.

$$t_{(off)min} = \frac{I_{Lpk} L_P}{V_o}, \theta = 0^\circ \quad (17)$$

Switching Frequency

$$f = \frac{1}{t_{(on)} + t_{(off)}} \quad (18)$$

Switching frequency changes with the steady state line and load operating conditions along with the instantaneous input line voltage. Typically, the PFC converter is designed to operate above the audible range after accommodating all circuit and component tolerances. 25 kHz is a good first approximation. Higher frequency operation that can significantly reduce the inductor size without negatively impacting efficiency or cost should also be evaluated.

The minimum switching frequency occurs at the peak of the ac line voltage. As the ac line voltage traverses from peak to zero, $t_{(off)}$ approaches zero producing an increase in switching frequency.

Inductor Value

Maximum on−time needs to be programmed into the PFC controller timing circuit. Both $t_{(on)max}$ and $t_{(off)max}$ will be individually calculated and added together to obtain the maximum conversion period, t_{total}. This is required to obtain the inductor value.

$$t_{(on)max} = \frac{2P_o L_P}{\eta V^2_{ac(LL)}} \quad (19)$$

$$t_{(off)max} = \frac{I_{Lpk} L_P}{V_o - V_{inpk}}, (\theta) \approx 90^\circ \quad (20)$$

The exact inductor value can be determined by solving equation (21) by substituting equation (19) and (20) at the selected minimum operating frequency.

$$t_{total} = t_{(on)max} + t_{(off)max} \quad (21)$$

Equation (21) becomes

$$t_{total} = \frac{\sqrt{2} P_o L_P V_o}{V^2_{ac(LL)} \eta \left(\frac{V_o}{\sqrt{2}} - V_{ac(LL)}\right)} \quad (22)$$

By rearranging in term of L_p,

$$L_p = \frac{t_{total}\left(\frac{V_o}{\sqrt{2}} - V_{ac(LL)}\right)\eta V^2_{ac(LL)}}{\sqrt{2} V_o P_o} \quad (23)$$

Equation (23) can be rewritten by substituting rearranged equation (12) in term of $\sqrt{2}P_o$.

$$L_p = \frac{2 \times t_{total}\left(\frac{V_o}{\sqrt{2}} - V_{ac(LL)}\right)V_{ac(LL)}}{V_o I_{Lpk}} \quad (24)$$

Let the switching cycle t = 40μs for universal input (85 to 265 V_{ac}) operation and 20 μs for fixed input (92 to 138 V_{ac}, or 184 to 276 V_{ac}) operation.

Inductor Design Summary

The required energy storage of the boost inductor is:

$$W_L = \frac{1}{2} L_P I^2_{Lpk} \quad (25)$$

The number of turns required for a selected core size and material is:

$$N_P = \frac{L_P I_{Lpk} 10^6}{B_{max} A_e} \quad (26)$$

where B_{max} is in Teslas and A_e is in square millimeters (mm^2)

The required air gap to achieve the correct inductance and storage is expressed by:

$$l_{gap} = \frac{4\pi 10^{-7} N^2_p A_e}{L_P} \text{ mm} \quad (27)$$

Design of Auxiliary Winding

MC33260 does not entail an auxiliary winding for zero current detection. Hence if DC voltage can be tapped from the SMPS or electronic ballast connected to the output of PFC, this step can be skipped. Then an inductor is what it needs.

The auxiliary winding exhibits a low frequency ripple (100−120 Hz). The Vcc capacitor must be large enough (about 47 μF) to minimize voltage variations. As a rule of thumb, you can use the below equation to estimate the auxiliary turn number:

$$N_{aux} = \frac{N_p \cdot V_{aux}}{V_L} = \frac{N_p \cdot V_{aux}}{V_o - V_{ac(HL)}} \quad (28)$$

The MC33260 V_{CC} maximum voltage being 16 V, one must add a resistor (in the range of 22 Ω) and a 15 V zener to protect the circuit against excessive voltages. Vaux should be chosen above the Under−Voltage Lockout threshold (10 V) and below the zener voltage.

Selection of Output Capacitor

The choice of output capacitance value is dictated by the required hold−up time, t_{hold} or the acceptable output ripple voltage, V_{orip} for a given application. As a rule of thumb, can start with 1 μF/watt.

Selection of Semiconductors

Maximum currents and voltages must first be determined for over all operating conditions to select the MOSFET and boost rectifier. As a rule of thumb, derate all semiconductors to about 75−80% of their maximum ratings. This implying the need of devices with at least 500 V breakdown voltage. Bipolar transistors are an acceptable alternative to MOSFET if the switching frequency is maintained fairly low. High voltage diodes with recovery times of 200 ns, or less should be used for the boost rectifier. One series of the popular devices is the MURXXX Ultrafast Rectifier Series from ON Semiconductor.

Maximum power MOSFET conduction losses.

$$P_{(on)max} \approx \frac{1}{6} \times R_{ds(on)} \times I^2_{Lpk} 1 - \frac{1.2 \times V_{ac(LL)}}{V_o} \quad (29)$$

Designing the Oscillator Circuit

For traditional boost operation, C_T is chosen with below equation:

$$C_T \geq \frac{2 \times K_{osc} \times L_P \times P_{in} \times V^2_o}{V^2_{ac(LL)} \times R^2_o} - C_{int} \quad (30)$$

Design of Regulation and Overvoltage Protection Circuit

The output voltage regulation level can be adjusted by R_o,

$$R_o \approx \frac{V_o}{200\ \mu A} \quad (31)$$

Designing the Current Sense Circuit

The inductor current is converted into a voltage by inserting a ground referenced resistor, R_{CS} in series with the input diode bridge. Therefore a negative voltage proportional to the inductor current is built.

The current sense resistor losses, P_{Rcs}:

$$P_{Rcs} = \frac{1}{6} \times R_{CS} \times I^2_{Lpk} \quad (32)$$

Overcurrent protection resistor, R_{OCP} can be determined with below equation:

$$R_{OCP} = \frac{R_{CS} \times I_{Lpk}}{I_{OCP}} \quad (33)$$

Current Limiting With Boost Topology Power Factor Correction Circuit

Unlike buck and flyback circuits, because there is no series switch between input and output in the boost topology, high current occurring with the start−up inrush current surge charging the bulk capacitor and fault load conditions cannot be limited or controlled without additional circuitry.

The MC33260 Zero Current Detection uses the current sensing information to prevent any power switch turn on as long as some current flows through the inductor. Then, during start−up, the power MOSFET is not allowed to turn on while in−rush current flows. Then there is no risk to have the power switch destroyed at start−up because of the in−rush current.

In the same way, in an overload case, the power MOSFET is kept off as long as there is a direct output capacitor charge current, i.e., when the input voltage is higher than the output voltage. Consequently, overload working is fully safe for the power MOSFET. This is one of the major advantages compared to MC33262 and competition.

Current Limiting for Start−up Inrush

Initially V_o is zero, when the converter is turned on, the bulk capacitor will charge resonantly to twice Vin. The voltage can be as high as 750 V if V_{in} happens to be at the peak high−line 265 V condition (375 V). The peak resonant charging current through the inductor will be many times greater than normal full load current. the inductor must be designed to be much larger and more expensive to avoid saturation. The boost shunt switch cannot do anything to prevent this and could be worse if turned on during start−up.

The inrush current and voltage overshoot during the start−up phase is intolerable. A fuse is not suitable, as it will blow each time the supply is turned on.

There are several methods that may be used to solve the start−up problem:

1. Start−up Bypass Rectifier

This is implemented by adding an additional rectifier bypassing the boost inductor. The bypass rectifier will divert the start−up inrush current away from the boost inductor as shown in Figure 3. The bulk capacitor charges through D_{bypass} to the peak AC line voltage without resonant overshoot and without excessive inductor current. D_{bypass} is

reverse−biased under normal operating conditions. If load overcurrent pulls down V_o, D_{bypass} conducts, but this is probably preferable to having the high current flowing through boost inductor.

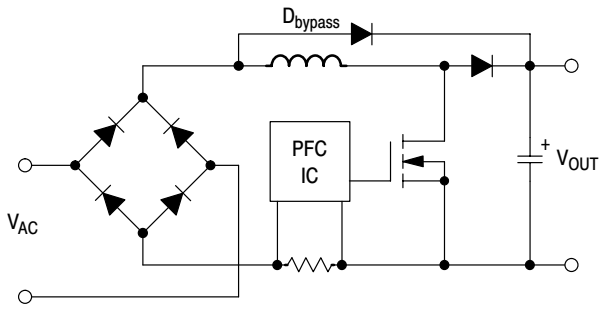

Figure 3. Rectifier bypass of start−up inrush current

2. External Inrush Current Limiting Circuit

For low power system, a thermistor in series with the pre−converter input will limit the inrush current. Concern is the thermistor may not respond fast enough to provide protection after a line dropout of a few cycles.

A series input resistor shunted by a Triac or SCR is a more efficient approach. A control circuit is necessary. This method can function on a cycle−by−cycle basis for protection after a dropout.

Load Overcurrent Limiting

If an overcurrent condition occurs and exceeds the boost converter power limit established by the control circuit, V_o will eventually be dragged down below the peak value of the AC line voltage. If this happens, current will rise rapidly and without limit through the series inductor and rectifier. This may result in saturation of the inductor and components will fail. The control circuit holds off the shunt switch, since the current limit function is activated. It cannot help to turn the switch ON − the inductor current will rise even more rapidly and switch failure will occur.

Typically, a power factor correction circuit is connected to another systems like switched mode power supply or electronic ballast. These downstream converters typically will have current limiting capability, eliminating concern about load faults. However, a downstream converter or the bulk capacitor might fail. Hence there is a possibility of a short circuit at the load.

If it is considered necessary to limit the current to a safe value in the event of a downstream fault, some means external to the boost converter must be provided.

Design Example I − Traditional Boost Constant Output Voltage Regulation Level Operation Power Factor Correction

The basic design specification concerns the following:

- Mains Voltage Range: $V_{ac(LL)} - V_{ac(HL)} = 85 - 265\ V_{ac}$
- Regulated DC Output Voltage: $V_o = 400\ V_{dc}$
- Rated Output Power: $P_o = 80$ W
- Expected Efficiency, $\eta > 90\%$

A. The input power, Pin is given by

$$P_{in} = \frac{P_o}{\eta} = \frac{80}{0.92} = 86.96\ W$$

B. Input diode current is maximum at $V_{inrms} = V_{ac(LL)}$

$$I_{inpk} = \frac{\sqrt{2}P_o}{\eta V_{ac(LL)}} = \frac{\sqrt{2} \times 80}{0.92 \times 85} = 1.447\ A$$

C. Inductor design

1. Inductor peak current:

$$I_{Lpk} = 2I_{inpk} = 2 \times 1.447 = 2.894\ A$$

2. Inductor value:

$$L_p = \frac{2 \times t_{total}\left(\frac{V_o}{\sqrt{2}} - V_{ac(LL)}\right)V_{ac(LL)}}{V_o I_{Lpk}}$$

$$= \frac{2 \times 40 \times 10^{-6}\left(\frac{400}{\sqrt{2}} - 85\right)85}{400 \times 2.894} = 1.162\ mH$$

Let the switching cycle t = 40 μs for universal input (85 to 265 V_{ac}) operation.

3. The number of turns required for a selected core size and material is:

$$N_P = \frac{L_P I_{Lpk} 10^6}{B_{max} A_e} = \frac{1.162 \times 10^{-3} \times 2.894 \times 10^{-6}}{0.3 \times 60}$$

$$= 186.8\ turns \approx 187\ turns$$

Using EPCOS E 30/15/7, B_{max} =0.3 T and $A_e = 60\ mm^2$.

4. The required air gap to achieve the correct inductance and storage is:

$$l_{gap} = \frac{4\pi 10^{-7} N_p^2 A_e}{L_P}$$

$$= \frac{4\pi \times 10^{-7} \times 187^2 \times 60 \times 10^{-6}}{1.162 \times 10^{-3}}$$

$$= 2.269\ mm$$

5. Design of Auxiliary Winding

$$N_{aux} = \frac{V_{aux} N_P}{\left(V_o - V_{ac(HL)}\right)} = \frac{14 \times 187}{(400 - 265)}$$

$$= 19.4\ turns \approx 20\ turns$$

Round up to 20 turns to make sure enough voltage at the auxiliary winding.

D. To determine the output capacitor

As rule of thumb, for 80 W output, start with 100 μF, 450 V capacitor.

E. Calculation of MOSFET conduction losses

A 8A, 500V MOSFET, MTP8N50E is chosen. The on resistance, $R_{ds(on)} \approx 1.75\,\Omega$@100°C. Therefore, maximum power MOSFET conduction losses is:

$$P_{(on)max} \approx \frac{1}{6} \times R_{ds(on)} \times I^2_{Lpk}\left(1 - \frac{1.2 \times V_{ac(LL)}}{V_o}\right)$$

$$= \frac{1}{6} \times 1.75 \times 2.894^2\left(1 - \frac{1.2 \times 85}{400}\right) = 1.82\ W$$

F. Design of regulation and overvoltage protection circuit

The output voltage regulation level can be adjusted by R_o,

$$R_o \approx \frac{V_o}{200\,\mu A} = \frac{400}{200\,\mu A} = 2\ M\Omega$$

Use two 1 MΩ resistors in series.

G. Designing the oscillator circuit

For traditional boost operation, C_T is chosen with below equation:

$$C_T \geq \frac{2 \times K_{osc} \times L_P \times P_{in} \times V^2_o}{V^2_{ac(LL)} \times R^2_o} - C_{int} =$$

$$\frac{2 \times 6400 \times 1.162mH \times 86.96 \times 400^2}{85^2 \times 2M\Omega^2} - 15pF = 7.16nF$$

Use 10 nF capacitor.

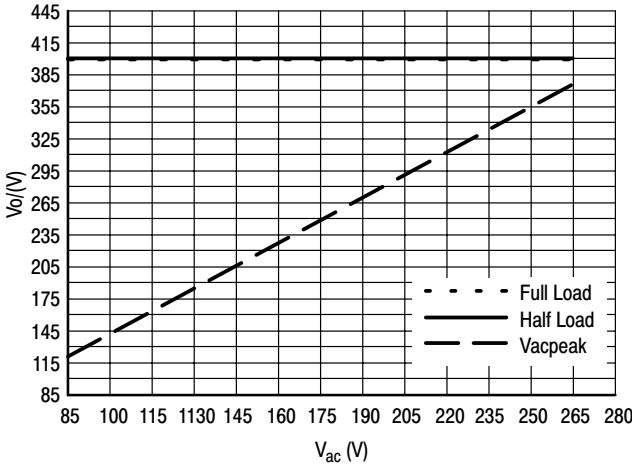

Figure 4. Theoretical V_o versus V_{ac} with C_T = 10nF

H. Design of the current sense circuit

Choose $R_{cs} = 0.68\ \Omega$

1. So the current sense resistor losses, P_{Rcs}:

$$P_{Rcs} = \frac{1}{6} \times R_{CS} \times I^2_{Lpk} = \frac{1}{6} \times 1 \times 2.894^2 = 0.949\ W$$

Therefore the power rating of R_{CS} is chosen to be 2 W.

2. Overcurrent protection resistor, R_{OCP} can be determined with below equation:

$$R_{OCP} = \frac{R_{CS} \times I_{Lpk}}{I_{OCP}} = \frac{0.68 \times 2.894}{205\,\mu A} = 9600\ \Omega$$

Use 10000 Ω resistor. This provide current limit at 3.01 A versus calculated value of I_{Lpk} = 2.894 A.

80 W, Universal Input, Traditional Boost Constant Output Voltage Level Regulation Operation Power Factor Correction Circuit Part List

Index	Value	Comment	Index	Value	Comment
C1	0.63 μF@600 V	Filtering Capacitor	R6	22 Ω@0.25 W	Aux Winding Resistor
C2	680 nF	Pin 2 $V_{control}$ Capacitor	R7	100 KΩ@2 W	Start−up Resistor
C3	10 nF	Pin 3 Oscillator Capacitor	R8	1N5406	Input Diode
C4	100 μF@50 V	Aux Capacitor, E−Cap	D1	1N5406	Input Diode
C5	100μF@450V	Output Capacitor, E−Cap	D2	1N5406	Input Diode
C6	1 nF@50 V	Feedback Filtering Capacitor	D3	1N5406	Input Diode
R1	0.68 Ω@2 W	Current Sense Resistor	D4	1N4937	Aux Winding Diode
R2	10 KΩ@0.25 W	OCP Sensing Resistor	D5	MUR460	Boost Diode
R3	1 MΩ@0.25 W	Feedback Resistor	D6	1N5245	Aux 15 V Zener Diode
R4	1 MΩ@0.25 W	Feedback Resistor	D7	MTP8N50E	Power MOSFET
R5	10 Ω@0.25 W	Gate Resistor	Q1	1.162 mH	Inductor

* E 30/15/7, N67 Material from EPCOS
Primary − 187 turns of # 23 AWG, Secondary − 19 turns of # 23 AWG.
Gap length 2.269mm total for a primary inductance L_P of 1.162mH.

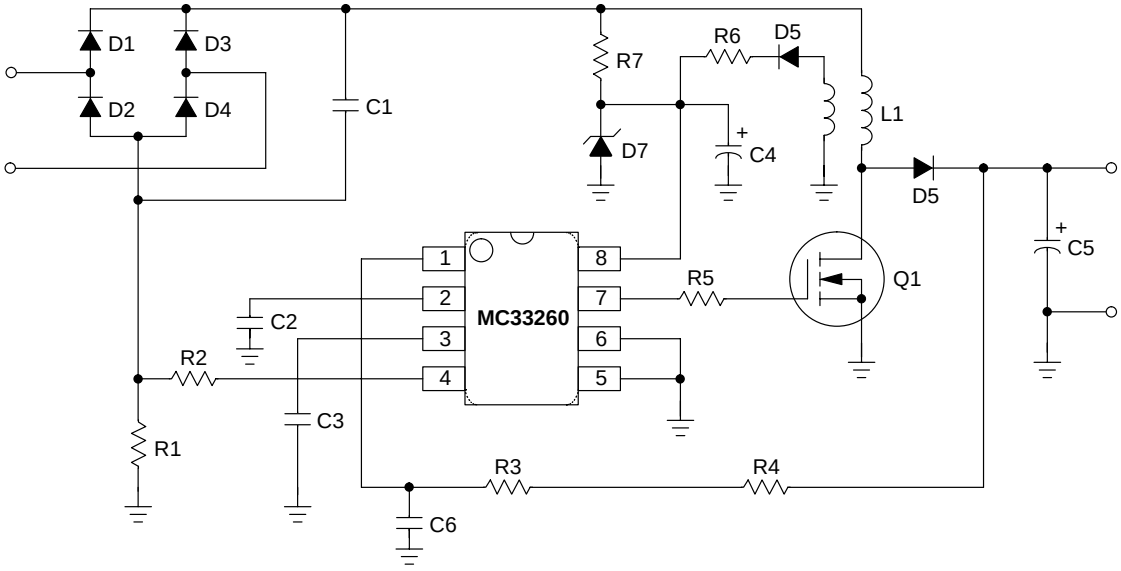

Figure 5. 80 W Universal Input, Traditional Boost Constant Output Voltage Regulation Level Operation Power Factor Correction Circuit

Design Table for Universal Input, Traditional Boost Constant Output Voltage Regulation Level Operation Power Factor Correction

P_o	25	50	75	100	125	150	200	(Watts)
L_P	3.720	1.860	1.240	0.930	0.744	0.620	0.465	(mH)
C_o	33	68	100	100	150	150	220	(μF)
R_{CS}	2	1	0.68	0.5	0.39	0.33	0.25	Ω
R_{OCP}	10000	10000	10000	9100	9100	9100	9100	Ω
C_{in}	0.22	0.63	0.63	1.0	1.0	1.0	1.0	(μF)
C_T	10	10	10	10	10	10	10	(nF)
Q	MTP4N50E		MTP8N50E			MTW14N50E		
D^{out}	MUR160		MUR460					
D_{in}	1N4007		1N5406					

Design Example II − Follower Boost Variable Output Voltage Regulation Level Operation Power Factor Correction

The basic design specification concerns the following:

- Mains Voltage Range: $V_{ac(LL)} - V_{ac(HL)} = 85 - 265\ V_{ac}$
- Maximum Regulated DC Output Voltage: $V_o = 400\ V_{dc}$
- Minimum Regulated DC Output Voltage: $V_{omin} = 140\ V_{dc}$
- Rated Output Power: $P_o = 80$ W
- Expected Efficiency, $\eta > 90\%$

A. The input power, P_{in} is given by

$$P_{in} = \frac{P_o}{\eta} = \frac{80}{0.92} = 86.96\ W$$

B. Input diode current is maximum at $V_{inrms} = V_{ac(LL)}$

$$I_{inpk} = \frac{\sqrt{2}P_o}{\eta V_{ac(LL)}} = \frac{\sqrt{2} \times 80}{0.92 \times 85} = 1.447\ A$$

C. Inductor design

1. Inductor peak current:

$$I_{Lpk} = 2I_{inpk} = 2 \times 1.447 = 2.894\ A$$

2. Inductor value, for follower boost operation, $V_o = V_{omin}$:

$$L_p = \frac{2 \times t_{total}\left(\frac{V_{omin}}{\sqrt{2}} - V_{ac(LL)}\right)}{V_{omin} I_{Lpk}}$$

$$= \frac{2 \times 40 \times 10^{-6}\left(\frac{140}{\sqrt{2}} - 85\right)85}{140 \times 2.894} = 0.235\ \mu H$$

Let the switching cycle t = 40 μs for universal input (85 to 265 V_{ac}) operation.

3. The number of turns required for a selected core size and material is:

$$N_P = \frac{L_P I_{Lpk} 10^6}{B_{max} A_e} =$$

$$\frac{0.235 \times 10^{-3} \times 2.894 \times 10^6}{0.3 \times 32.1} = 70.6\ \text{turns} \approx 71\ \text{turns}$$

Using EPCOS E 20/10/6, N67 material, B_{max} =0.3 T and A_e = 32.1 mm^2.

4. The required air gap to achieve the correct inductance and storage is:

$$l_{gap} = \frac{4\pi 10^{-7} N_p^2 A_e}{L_P}$$

$$= \frac{4\pi \times 10^{-7} \times 71^2 \times 32.1 \times 10^{-6}}{0.235 \times 10^{-3}}$$

$$= 0.856\ \text{mm}$$

5. Design of Auxiliary Winding

$$N_{aux} = \frac{V_{aux} N_P}{\left(V_o - V_{ac(HL)}\right)} = \frac{14 \times 71}{(400 - 265)}$$

$$= 7.4\ \text{turns} \approx 8\ \text{turns}$$

Round up to 8 turns to make sure enough voltage at the auxiliary winding.

D. To determine the output capacitor

As rule of thumb, for 80 W output, start with 100 μF, 450 V capacitor.

E. Calculation of MOSFET conduction losses

A 4A, 500 V MOSFET, MTP4N50E is chosen. The on resistance, $R_{ds(on)} \approx 1.75\ \Omega$@100°C. Therefore, maximum power MOSFET conduction losses is:

$$P_{(on)max} \approx \frac{1}{6} \times R_{ds(on)} \times I_{Lpk}^2 \left(1 - \frac{1.2 \times V_{ac(LL)}}{V_{omin}}\right)$$

$$= \frac{1}{6} \times 1.75 \times 2.894^2 \left(1 - \frac{1.2 \times 85}{140}\right) = 0.66\ \text{W}$$

F. Design of regulation and overvoltage protection circuit

The output voltage regulation level can be adjusted by R_o,

$$R_o \approx \frac{V_o}{200\ \mu A} = \frac{400}{200\ \mu A} = 2\ M\Omega$$

Use two 1MΩ resistors in series.

G. Designing the Oscillator Circuit

For follower boost operation, C_T is chosen with below equation:

$$C_T \geq \frac{2 \times K_{osc} \times L_P \times P_{in} \times V_o^2}{V_{ac(LL)}^2 \times R_o^2} - C_{int} =$$

$$\frac{2 \times 6400 \times 0.234mH \times 86.96 \times 140^2}{85^2 \times 2\ M\Omega^2} - 15pF = 162\ pF$$

Use 150 pF capacitor.

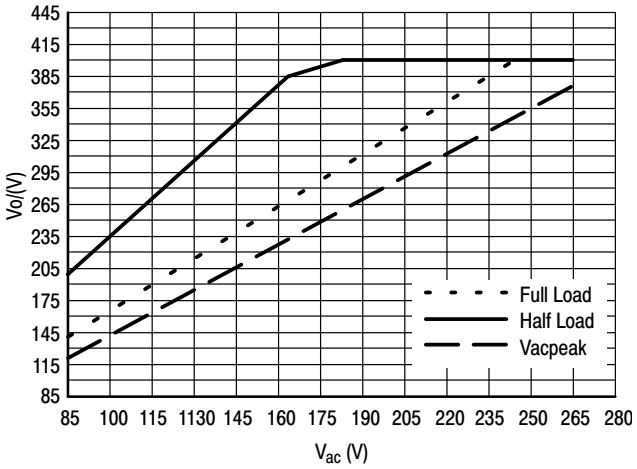

Figure 6. Theoretical V_o versus V_{ac} with C_T = 150pF

H. Design of the Current Sense Circuit

Choose R_{cs} = 0.68 Ω

1. So the current sense resistor losses, P_{Rcs}:

$$P_{Rcs} = \frac{1}{6} \times R_{CS} \times I_{Lpk}^2$$

$$= \frac{1}{6} \times 0.68 \times 2.894^2 = 0.949\ \text{W}$$

2. Overcurrent protection resistor, R_{OCP} can be determined with below equation:

$$R_{OCP} = \frac{R_{CS} \times I_{Lpk}}{I_{OCP}} = \frac{0.68 \times 2.894}{205\ \mu A} = 9600\ \Omega$$

Use 10000 Ω resistor. This provide current limit at 3.01 A versus calculated value of I_{Lpk} = 2.894 A.

80 W, Universal Input, Follower Boost Variable Output Voltage Regulation Level Operation Power Factor Correction Circuit Part List

Index	Value	Comment	Index	Value	Comment
C1	0.63 μF@600 V	Filtering Capacitor	R6	22 Ω@0.25 W	Aux Winding Resistor
C2	680 nF	Pin 2 $V_{control}$ Capacitor	R7	100 KΩ@2 W	Start−up Resistor
C3	150 pF	Pin 3 Oscillator Capacitor	D1	1N5406	Input Diode
C4	100 μF@50 V	Aux Capacitor, E−Cap	D2	1N5406	Input Diode
C5	100 μF@450 V	Output Capacitor, E−Cap	D3	1N5406	Input Diode
C6	1 nF@50 V	Feedback Filtering Capacitor	D4	1N5406	Input Diode
R1	0.68 Ω@2 W	Current Sense Resistor	D5	1N4937	Aux Winding Diode
R2	10 KΩ@0.25 W	OCP Sensing Resistor	D6	MUR460	Boost Diode
R3	1 MΩ@0.25 W	Feedback Resistor	D7	1N5245	Aux 15 V Zener Diode
R4	1 MΩ@0.25 W	Feedback Resistor	Q1	MTP4N50E	Power MOSFET
R5	10 Ω@0.25 W	Gate Resistor	L1*	0.235 mH	Inductor

* E 20/10/6, N67 Material from EPCOS
Primary − 71 turns of # 23 AWG, Secondary − 8 turns of # 23 AWG.
Gap length 0.865 mm total for a primary inductance L_P of 0.235 mH.

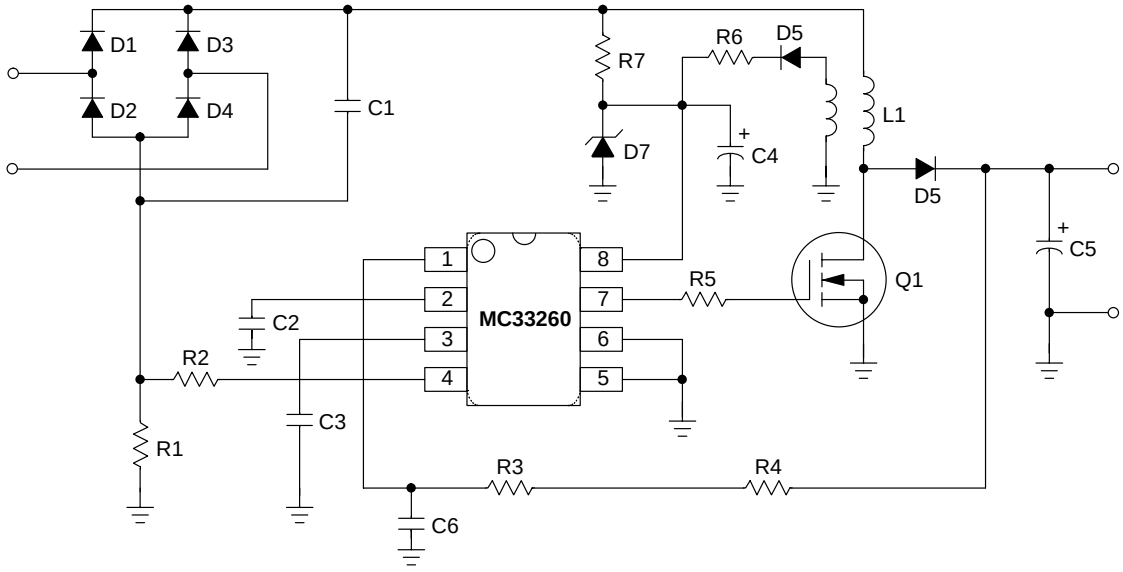

Figure 7. 80 W Universal Input, Follower Boost Variable Output Voltage Regulation Level Operation Power Factor Correction Circuit

Design Table for Universal Input, Follower Boost Variable Output Voltage Regulation Level Operation Power Factor Correction

P_o	25	50	75	100	125	150	200	(Watts)
L_P	0.752	376	0.251	0.188	0.150	0.102	0.094	(mH)
C_o	33	68	100	100	150	150	220	(μF)
R_{CS}	2	1	0.68	0.5	0.39	0.33	0.25	Ω
R_{OCP}	10000	10000	10000	9100	9100	9100	9100	Ω
C_{in}	0.22	0.63	0.63	1.0	1.0	1.0	1.0	(μF)
C_T	0.162	0.162	0.162	0.162	0.162	0.162	0.162	(nF)
Q	MTD2N50E		MTP4N50E		MTP8N50E			
D_{out}	MUR160		MUR460					
D_{in}	1N4007		1N5406		1N5406			

AND8106/D

100 Watt, Universal Input, PFC Converter

ON Semiconductor

ON Semiconductor®

http://onsemi.com

APPLICATION NOTE

General Description

This 100 watt converter demonstrates the wide range of features found on the NCP1650. This chip is capable of controlling PFC converters well into the kilowatt range.

In addition to excellent power factor, this chip offers fixed frequency operation in continuous and discontinuous modes of operation. It has a wide variety of protection features, including instantaneous current limiting, average current limiting, and true power limiting.

This unit will provide 400 V of well regulated power from an input source with a frequency range from 50 Hz to 60 Hz, and a voltage range of 85 V_{rms} to 265 V_{rms}. It is fully self contained and includes a high voltage start−up circuit, and bias supply that operates off of the boost inductor.

Features

- Fixed Frequency Operation
- Shutdown Circuit
- Operation Over the Universal Input Range
- Multiple Protection Schemes
- True Power Limiting
- Start−Up and Bias Circuits Included

Circuit Description

Start−Up Circuit

The start−up circuit allows the unit to use power from the input line to begin operation, and then shuts down to allow operation off of the bias winding, which reduces losses in the circuit.

The start−up circuit has three modes of operation. One is used for starting the NCP1650 when the chip is functional, one is for bias power during shutdown operation, and the third is the off state.

When power is initially applied to the unit, the gate of the pass transistor will be high, and the FET will be fully enhanced. The current into the V_{CC} capacitance at pin 1 will be limited by the three 10 kΩ resistors in series with the FET.

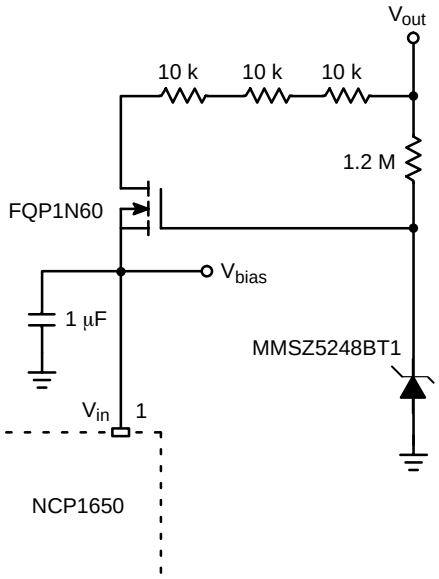

Figure 1. Start−Up Circuit Schematic

This circuit will provide current as long as the FET is enhanced. For this to occur, the gate to source voltage must be greater than the gate threshold voltage. For this device that value is nominally, 4.0 V. The zener breakdown voltage is 18 V, so the FET will turn off at:

$$Vchg_{max} = 18\ V - 4.0\ V = 14\ Volts$$

As the output capacitor is charged up during the turn−on sequence, the bias supply voltage will also increase until the source of the FET exceeds 14 V. At this point, the FET will cease conduction, and all of the V_{CC} power will be supplied via the bias circuit from the power inductor.

If the unit is commanded into the shutdown mode, the chip will reduce its bias current to 0.5 mA and the start−up circuit will then maintain a regulated voltage of approximately 14 V on the V_{CC} pin until the device becomes operational.

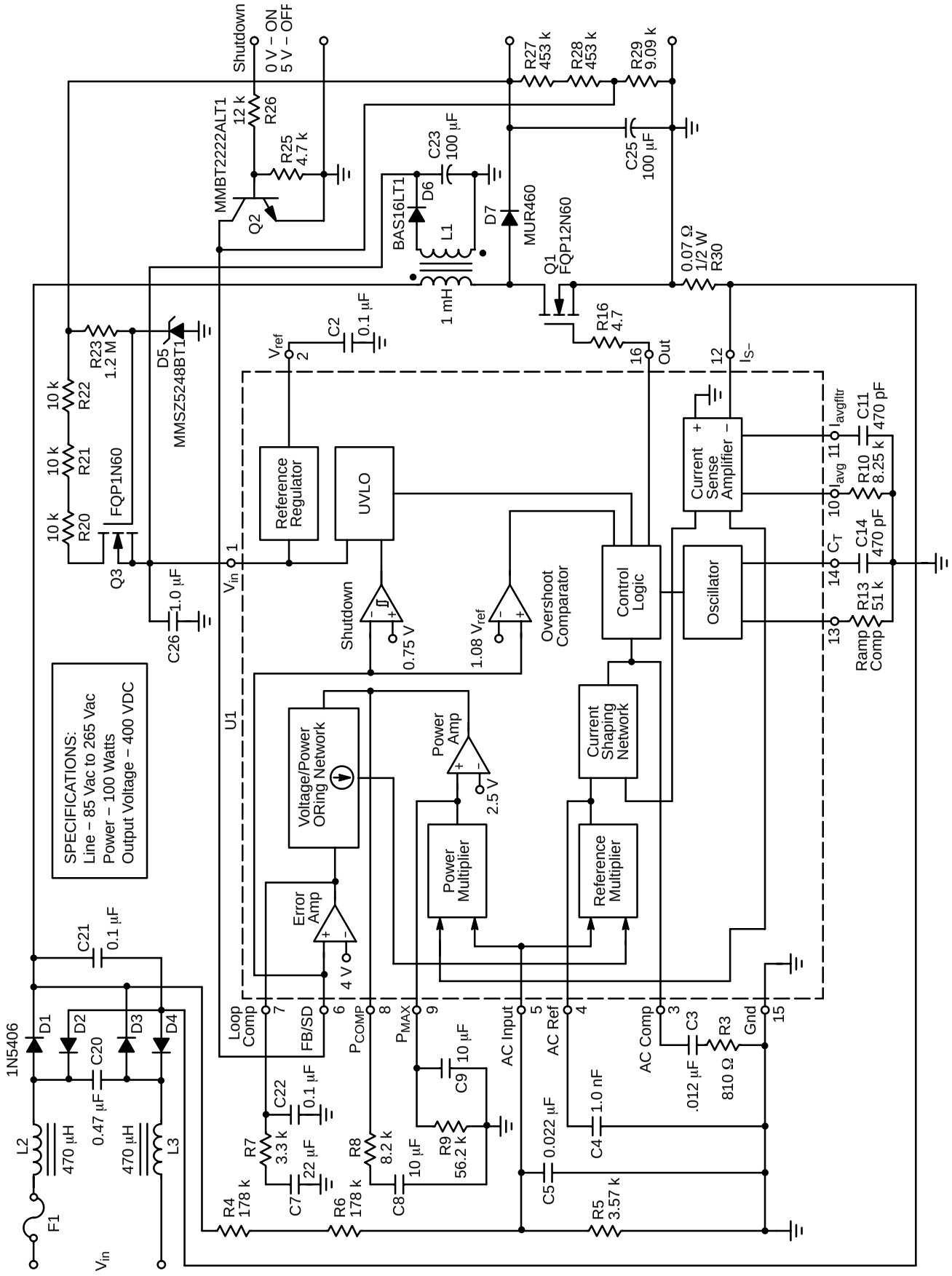

Figure 2. Applications Circuit Schematic

Voltage Regulation Loop

The output voltage is sensed and reduced to the reference level by the resistive divider consisting of R27, R28 and R29. The output voltage of this divider is sensed by the non−inverting input of the error amplifier and compared to the internal 4.0 V reference.

Assuming that the unit in not in a power limit condition, the voltage error signal will dominate the loop and be fed through the OR'ing network to provide one of the inputs to the reference multiplier. The other reference multiplier input is the divided down rectified AC input signal.

The output of this multiplier is a haversine signal that is an accurate replica of the input AC signal. The current shaping network compares the average current from the current sense amplifier to the reference voltage and forces this current to follow the AC reference voltage. The current out of the current sense amplifier is filtered at a frequency that is less than the switching frequency, but greater than the rectified line frequency.

This current is fed into the output filter capacitor(s) that filter it to a DC level.

Power Regulation Loop

The power multiplier generates the product of the input current (from the current sense amplifier) and the AC rectified input voltage, to generate a signal that represents the input power of the unit. This signal is filtered to a frequency of less than the line frequency, so that it's output is a DC level.

If the load is increased to a level that exceeds the maximum power limit of the circuit, the output of the power multiplier will reach 2.5 V and the output of the power error amplifier will go to some level above ground. This signal will then override the signal from the voltage error amplifier (labeled "error amp" on the schematic), and will dominate the OR'ing network.

This signal then determines the level of the reference signal out of the reference multiplier, and determines the input current to the power converter. It should be noted that as this is a boost converter, the power limit circuit will only fold back the output voltage until it reaches the level of the peak line voltage. At this point the converter will shut down, but the input voltage will continue to charge the output capacitors through the rectifier.

Shutdown Circuit

The shutdown circuit will inhibit the operation of the power converter and put the NCP1650 into a low power shutdown mode. To activate this circuit, apply 5.0 V to the red test point, with the black jack being "ground". Be aware that the black jack is actually hot as it is connected to the output of the input bridge rectifiers. An isolated 5.0 V supply should be used.

If this circuit is not being used, the terminals can be left open, as there is enough resistance built in to the circuit to keep the transistor (Q2) in it's off state.

PCB

The printed circuit board Gerber files are located on the ON Semiconductor website under the name NCP650−PCB1.

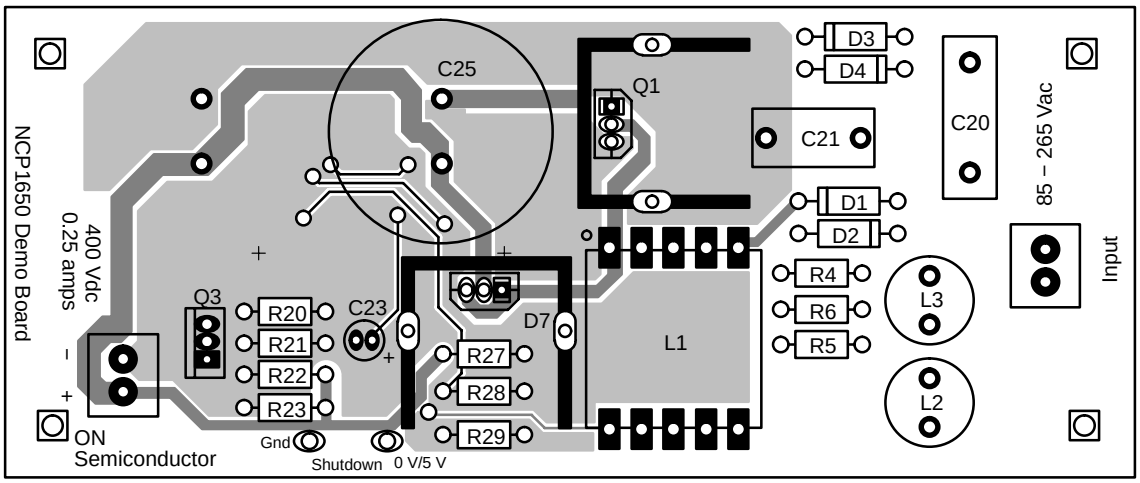

Table 1.

Ref Des	Description	Part Number	Manufacturer
C2	Cap, Ceramic, Chip, 0.1 μF, 50 V	C1608X7R1H104KT	TDK
C3	Cap, Ceramic, Chip, .012 μF, 50 V	C1608X7R1H123KT	TDK
C4	Cap, Ceramic, Chip, 1.0 nF, 50 V	C1608X7R1H102K	TDK
C5	Cap, Ceramic, Chip, 0.022 μF, 50 V	C1608X7R1H223K	TDK
C7	Cap, Ceramic, Chip, 22 μF, 6.3 V	C3225X5R0J226MT	TDK
C8	Cap, Ceramic, Chip, 10 μF, 10 V	C3225X5R1A106MT	TDK
C9	Cap, Ceramic, Chip, 4.7 μF, 10 V	C3216X5R1A475KT	TDK
C11	Cap, Ceramic, Chip, 470 pF, 50 V	C1608C0G1H471JT	TDK
C14	Cap, Ceramic, Chip, 470 pF, 50 V	C1608C0G1H471JT	TDK
C20	0.47 μF, 275 Vac, X Cap	ECQ−U2A474ML	Panasonic
C21	Cap, Polyprop, 0.1 μF, 400 Vdc	MKP1841−410−405	Vishay−Sprague
C22	Cap, Ceramic, Chip, 0.1 μF, 50 V	C1608X7R1H104KT	TDK
C23	100 μF, Alum Elect, 25 V	ECA−1EM101I	Panasonic
C25	100 μF, Alum Elect, 450 V	ECO−S2WP100EX	Panasonic
C26	Cap, Ceramic, Chip, 1.0 μF, 25 V	C3216X7R1E105KT	TDK
D1−D4	Diode, Rectifier, 600 V, 3.0 A	1N5406	ON Semiconductor
D5	Diode, Zener, 18 V, Axial Lead	MMSZ5248BT1	ON Semiconductor
D6	Diode, Signal, 75 V, 200 mA, SOT−23	BAS19LT1	ON Semiconductor
D7	Diode, Ultra−Fast, 600 V, 8.0 A	MURHF860CT	ON Semiconductor
F1	Fuse, 2.0 A, 250 Vac	1025TD2A	Bussman
L1	Inductor, 1000 μH, 2.4 A Max	CTX22−15557	Coiltronics
L2	2.5 A Sat, 100 μH Inductor, Diff Mode	TSL1315S−101K2R5	TDK
L3	2.5 A Sat, 100 μH Inductor, Diff Mode	TSL1315S−101K2R5	TDK
Q1	FET, 10.5 A, 0.7 Ω, 600 V, N−chl	FQP12N60	Fairchild
Q2	Bipolar Transistor, 50 V	MMBT2222ALT1	ON Semiconductor
Q3	FET, 1.0 A, 600 V, N−chl	FQP1N60	Fairchild
R3	Resistor, SMT, 810 Ω	CRCW1206810JNTA	Vishay
R4	Resistor, Axial Lead, 178 k, _ Watt, 1%	CMF−55−178K00FKRE	Vishay
R5	Resistor, Axial Lead, 3.57 k, _ Watt, 1%	CMF−55−3K5700FKBF	Vishay
R6	Resistor, Axial Lead, 178 k, _ Watt, 1%	CMF−55−178K00FKRE	Vishay
R7	Resistor, SMT, 8.6 k	CRCW12068K60JNTA	Vishay
R8	Resistor, SMT, 9.1 k	CRCW12069K10JNTA	Vishay
R9	Resistor, SMT, 56.2 k, 1%	CRCW120656K2FKTA	Vishay
R10	Resistor, SMT, 8.25 k, 1%	CRCW12068K2FKTA	Vishay
R13	Resistor, SMT, 51 k	CRCW120651K0JNTA	Vishay
R16	Resistor, SMT, 10	CRCW1206100JRE4	Vishay
R20	Resistor, Axial Lead, 10 k, _ Watt	CCF−07−103J	Vishay
R21	Resistor, Axial Lead, 10 k, _ Watt	CCF−07−103J	Vishay
R22	Resistor, Axial Lead, 10 k, _ Watt	CCF−07−103J	Vishay
R23	Resistor, Axial Lead, 1.2 M, _ Watt	CCF−07−125J	Vishay
R25	Resistor, SMT, 4.7 k	CRCW12064K70JNTA	Vishay

Table 1. (continued)

Ref Des	Description	Part Number	Manufacturer
R26	Resistor, SMT, 12 k	CRCW120612K0JNTA	Vishay
R27	Resistor, Axial Lead, 453 k, _ Watt, 1%	CMF−55−453K00FKBF	Vishay
R28	Resistor, Axial Lead, 453 k, _ Watt, 1%	CMF−55−4533F	Vishay
R29	Resistor, Axial Lead, 9.09 k, _ Watt, 1%	CCF−55−9K09FHR362	Vishay
R30	1.0 W, 0.07 Ω, 1% Resistor	WSL2512R0700FTB	Vishay
U1	PFC Controller	NCP1650	ON Semiconductor
	Hardware		
H1	Printed Circuit Board	NCP1650−PWB1	www.onsemi.com
H2	Connector	171602	Weidmuller
H3	Connector	171602	Weidmuller
H4	Test Point, Red	5005	Keystone
H5	Test Point, Black	5006	Keystone
H6	Standoff, 4−40, Alum, Hex, .500 Inches	8403	HH Smith
H7	Standoff, 4−40, Alum, Hex, .500 Inches	8403	HH Smith
H8	Standoff, 4−40, Alum, Hex, .500 Inches	8403	HH Smith
H9	Standoff, 4−40, Alum, Hex, .500 Inches	8403	HH Smith
H10	Heatsink, TO−220	590302B03600	Aavid Thermalloy
H11	Heatsink, TO−220	590302B03600	Aavid Thermalloy

Table 2. Vendor Contacts

Vendor	U.S. Phone/Internet
ON Semiconductor	1−800−282−9855 www.onsemi.com/
TDK	1−847−803−6100 www.component.tdk.com/
Vishay	www.vishay.com/
Bussman (Cooper Ind.)	1−888−414−2645 www.cooperet.com/
Coiltronics (Cooper Ind.)	1−888−414−2645 www.cooperet.com/
Fairchild	www.fairchildsemi.com/
Panasonic	www.eddieray.com/panasonic/
Weidmuller	www.weidmuller.com/
Keystone	1−800−221−5510 www.keyelco.com/
HH Smith	1−888−847−6484 www.hhsmith.com/
Aavid Thermalloy	www.aavid.com/

Performance Data

Table 3. Regulation

Line/Load	No Load	50 Watts	100 Watts
85 V_{rms}	405.5	405.1	403.9
115 V_{rms}	405.6	405.2	404.3
220 V_{rms}	405.4	405.5	404.9
265 V_{rms}	438.4	405.5	405

Table 4. Harmonics and Distortion

	115 Vac, 100 Watts		230 Vac, 100 Watts	
	V harmon	**A harm. %**	**V harmon**	**A harm. %**
2^{nd}	0.084	0.03	0.169	0.12
3^{rd}	0.505	2.8	0.722	2.6
5^{th}	0.482	1.3	0.132	4.4
7^{th}	0.168	0.5	0.075	0.17
9^{th}	0.074	0.17	0.133	0.23
11^{th}	0.088	0.13	0.134	0.17
13^{th}	0.212	0.27	0.073	0.15
15^{th}	0.324	0.37	0.265	0.28
17^{th}	0.413	0.35	0.488	0.32
19^{th}	0.632	0.31	1.12	0.44
PF	–	0.998	–	0.9928
THD (A)	–	3.68	–	6.2
I_{fund}	–	0.919	–	0.451

Table 5. Efficiency

	85 V_{rms}	**115 V_{rms}**	**230 V_{rms}**	**265 V_{rms}**
P_{in} @ No Load	2.87	4.06	5.07	5.11
Pin	108.8	106.9	103.2	103.7
Vo	403.2	404.3	404.9	405
Io	0.246	0.246	0.243	0.244
Efficiency	0.912	0.930	0.953	0.953

Power Factor Correction Stages Operating in Critical Conduction Mode

Prepared by: Joel Turchi
ON Semiconductor

ON Semiconductor®
http://onsemi.com

APPLICATION NOTE

This paper proposes a detailed and mathematical analysis of the operation of a critical conduction mode Power factor Corrector (PFC), with the goal of easing the PFC stage dimensioning. After some words on the PFC specification and a brief presentation of the main critical conduction schemes, this application note gives the equations necessary for computing the magnitude of the currents and voltages that are critical in the choice of the power components.

INTRODUCTION

The IEC1000−3−2 specification, usually named Power Factor Correction (PFC) standard, has been issued with the goal of minimizing the Total Harmonic Distortion (THD) of the current that is drawn from the mains. In practice, the legislation requests the current to be nearly sinusoidal and in phase with the AC line voltage.

Active solutions are the most effective means to meet the legislation. A PFC pre−regulator is inserted between the input bridge and the bulk capacitor. This intermediate stage is designed to output a constant voltage while drawing a sinusoidal current from the line. In practice, the step−up (or boost) configuration is adopted, as this type of converter is easy to implement. One can just notice that this topology requires the output to be higher than the input voltage. That is why the output regulation level is generally set to around 400 V in universal mains conditions.

Basics of the Critical Conduction Mode

Critical conduction mode (or border line conduction mode) operation is the most popular solution for low power applications. Characterized by a variable frequency control scheme in which the inductor current ramps to twice the desired average value, ramps down to zero, then immediately ramps positive again (refer to Figures 2 and 4), this control method has the following advantages:

- *Simple Control Scheme:* The application requires few external components.
- *Ease of Stabilization:* The boost keeps a first order converter and there is no need for ramp compensation.
- *Zero Current Turn On:* One major benefit of critical conduction mode is the MOSFET turn on when the diode current reaches zero. Therefore the MOSFET switch on is lossless and soft and there is no need for a low trr diode.

On the other hand, the critical conduction mode has some disadvantages:

- Large peak currents that result in high dl/dt and rms currents conducted throughout the PFC stage.
- Large switching frequency variations as detailed in the paper.

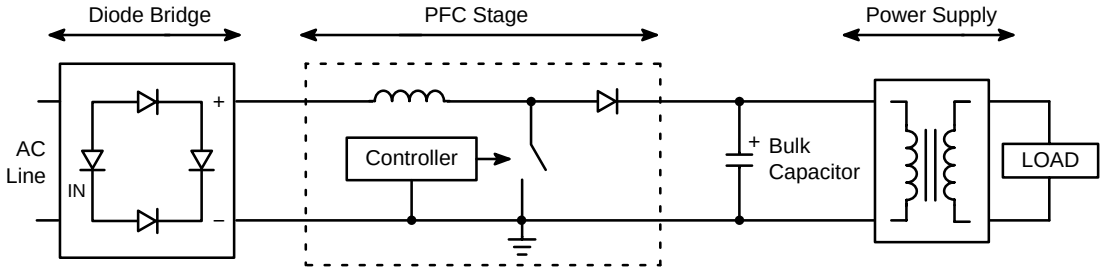

Figure 1. Power Factor Corrected Power Converter

PFC boost pre−converters typically require a coil, a diode and a Power Switch. This stage also needs a Power Factor Correction controller that is a circuit specially designed to drive PFC pre−regulators. ON Semiconductor has developed three controllers (MC33262, MC33368 and MC33260) that operate in critical mode and the NCP1650 for continuous mode applications.

One generally devotes critical conduction mode to power factor control circuits below 300 W.

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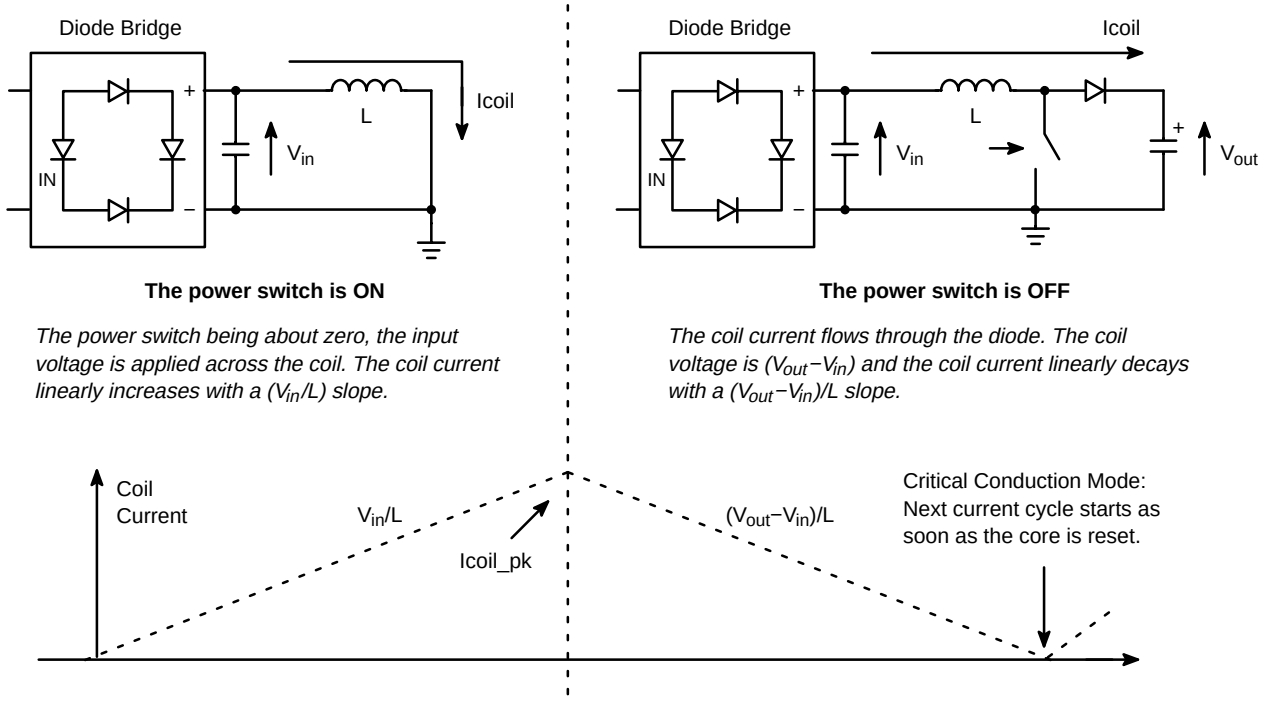

Figure 2. Switching Sequences of the PFC Stage

In critical discontinuous mode, a boost converter presents two phases (refer to Figure 2):

- The on−time during which the power switch is on. The inductor current grows up linearly according to a slope (V_{in}/L) where V_{in} is the instantaneous input voltage and L the inductor value.
- The off time during which the power switch is off. The inductor current decreases linearly according to the slope (V_{out}−V_{in})/L where V_{out} is the output voltage. This sequence terminates when the current equals zero.

Consequently, a triangular current flows through the coil. The PFC stage adjusts the amplitude of these triangles so that in average, the coil current is a (rectified) sinusoid (refer to Figure 4). The EMI filter (helped by the 100 nF to 1.0 μF input capacitor generally placed across the diodes bridge output), performs the filtering function.

The more popular scheme to control the triangles magnitude and shape the current, forces the inductor peak current to follow a sinusoidal envelope. Figure 3 diagrammatically portrays its operation mode that could be summarized as follows:

- The diode bridge output being slightly filtered, the input voltage (V_{in}) is a rectified sinusoid. One pin of the PFC controller receives a portion of V_{in}. The voltage of this terminal is the shaping information necessary to build the current envelope.
- An error amplifier evaluates the power need in response to the error it senses between the actual and wished levels of the output voltage. The error amplifier bandwidth is set low so that the error amplifier output reacts very slowly and can be considered as a constant within an AC line period.
- The controller multiplies the shaping information by the error amplifier output voltage. The resulting product is the desired envelope that as wished, is sinusoidal, in phase with the AC line and whose amplitude depends on the amount of power to be delivered.
- The controller monitors the power switch current. When this current exceeds the envelope level, the PWM latch is reset to turn off the power switch.
- Some circuitry detects the core reset to set the PWM latch and initialize a new MOSFET conduction phase as soon as the coil current has reached zero.

Consequently, when the power switch is ON, the current ramps up from zero up to the envelope level. At that moment, the power switch turns off and the current ramps down to zero (refer to Figures 2 and 4). For simplicity of the drawing, Figure 4 only shows 8 “current triangles”. Actually, their frequency is very high compared to the AC line one. The input filtering capacitor and the EMI filter averages the “triangles” of the coil current, to give:

$$< Icoil >_T = \frac{Icoil\_pk}{2} \qquad \text{(eq. 1)}$$

where $<Icoil>_T$ is the average of one current triangle (period T) and Icoil_pk is the peak current of this triangle.

As Icoil_pk is forced to follow a sinusoidal envelop ($k*V_{in}$), where k is a constant modulated by the error amplifier, $<Icoil>_T$ is also sinusoidal $\left(< Icoil > T = \frac{k * Vin}{2} = \frac{k * \sqrt{2} * Vac * \sin(\omega t)}{2} \right)$. As a result, this scheme makes the AC line current sinusoidal.

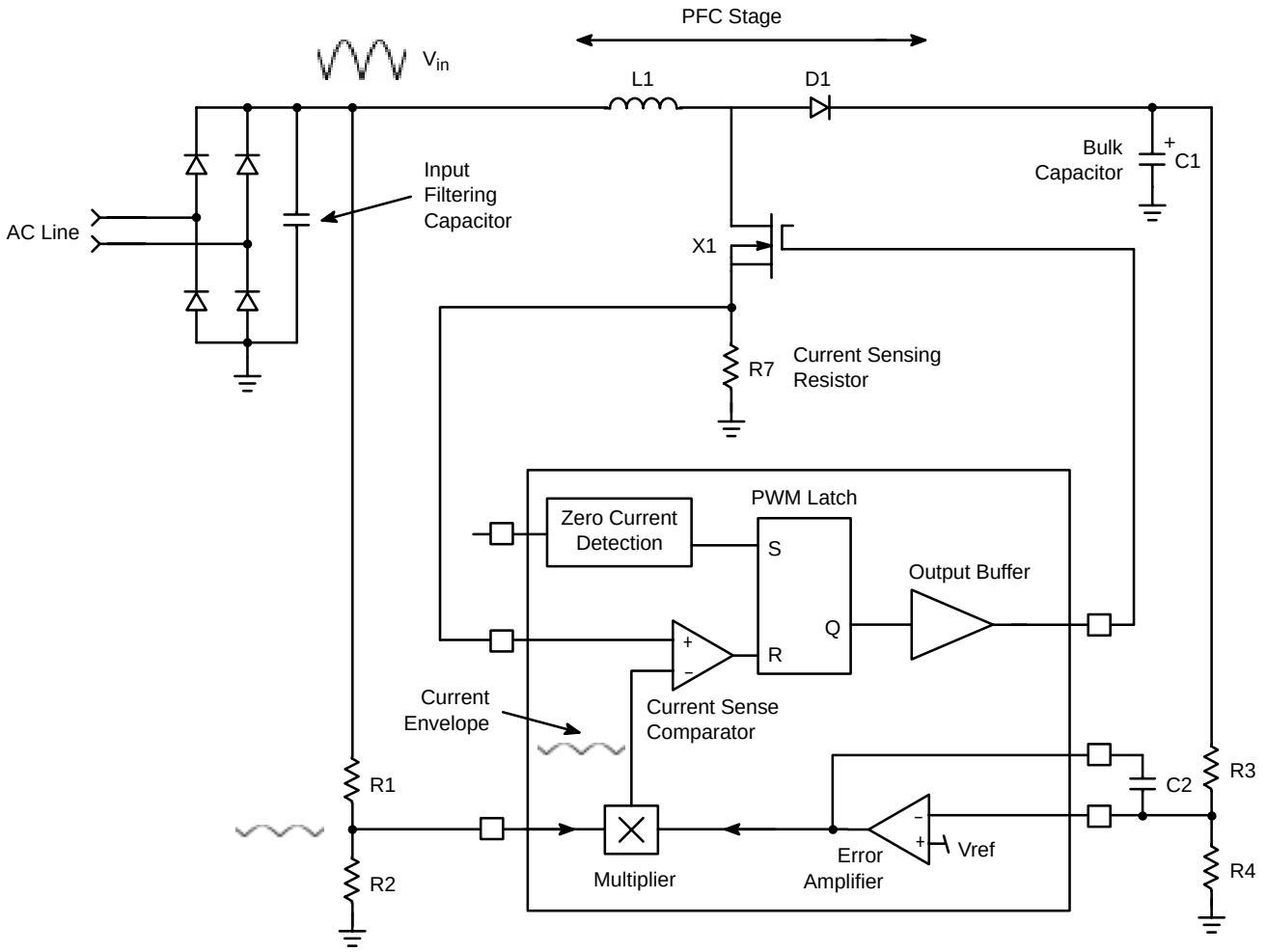

Figure 3. Switching Sequences of the PFC Stage

The controller monitors the input and output voltages and using this information and a multiplier, builds a sinusoidal envelope. When the sensed current exceeds the envelope level, the Current Sense Comparator resets the PWM latch and the power switch turns off. Once the core has reset, a dedicated block sets the PWM latch and a new MOSFET conduction time starts.

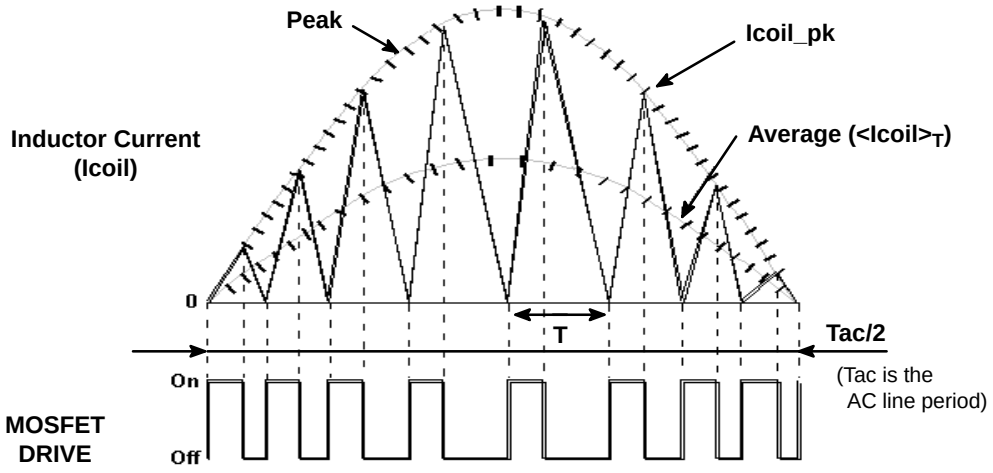

Figure 4. Coil Current

During the power switch conduction time, the current ramps up from zero up to the envelope level. At that moment, the power switch turns off and the current ramps down to zero. For simplicity of the drawing, only 8 "current triangles" are shown. Actually, their frequency is very high compared to the AC line one.

One can note that a simple calculation would show that the on−time is constant over the sinusoid: $ton = 2 * L * \frac{< Pin >}{Vac^2}$ and that the switching frequency modulation is brought by the off−time that equals:

$$toff = 2 * \sqrt{2} * L * \frac{< Pin >}{Vac * (Vout - \sqrt{2} * Vac * \sin(\omega t))} * \sin(\omega t) = ton * \frac{\sqrt{2} * Vac * \sin(\omega t)}{Vout - \sqrt{2} * Vac * \sin(\omega t)} \quad \text{(eq. 2)}$$

That is why the MC33260 developed by ON Semiconductor does not incorporate a multiplier inputting a portion of the rectified AC line to shape the coil current. Instead, this part forces a constant on−time to achieve in a simplest manner, the power factor correction.

Main Equations

Switching Frequency

As already stated, the coil current consists of two phases:

- The power switch conduction time (ton). During this time, the input voltage applies across the coil and the current increases linearly through the coil with a (V_{in}/L) slope:

$$Icoil(t) = \frac{Vin}{L} * t \quad \text{(eq. 3)}$$

This phase ends when the conduction time (ton) is complete that is when the coil current has reached its peak value (Icoil_pk). Thus:

$$Icoil\_pk = \frac{Vin}{L} * ton \quad \text{(eq. 4)}$$

The conduction time is then given by:

$$ton = \frac{L * Icoil\_pk}{Vin} \quad \text{(eq. 5)}$$

- The power switch off time (toff). During this second phase, the coil current flows through the output diode and feeds the output capacitor and the load. The diode voltage being considered as null when on, the voltage across the coil becomes negative and equal to (V_{in}−V_{out}). The coil current decreases then linearly with the slope ((V_{out}−V_{in})/L) from (Icoil_pk) to zero, as follows:

$$Icoil(t) = Icoil\_pk - \left(\frac{Vout - Vin}{L} * t\right) \quad \text{(eq. 6)}$$

This phase ends when Icoil reaches zero, then the off−time is given by the following equation:

$$toff = \frac{L * Icoil\_pk}{Vout - Vin} \quad \text{(eq. 7)}$$

The total current cycle (and then the switching period, T) is the sum of ton and toff. Thus:

$$T = ton + toff = L * Icoil\_pk * \frac{Vout}{Vin * (Vout - Vin)} \quad \text{(eq. 8)}$$

As shown in the next paragraph (equation 15), the coil peak current can be expressed as a function of the input power and the AC line rms voltage as follows: $Icoil\_pk = 2 * \sqrt{2} * \frac{< Pin >}{Vac} * \sin(\omega t)$, where ω is the AC line angular frequency. Replacing Icoil_pk by this expression in equation (8) leads to:

$$T = 2 * \sqrt{2} * \frac{L * < Pin >}{Vac} * \sin(\omega t) * \frac{Vout}{\sqrt{2} * Vac * \sin(\omega t) * (Vout - Vin)} \quad \text{(eq. 9)}$$

This equation simplifies:

$$T = \frac{2 * L * < Pin > * Vout}{Vac^2 * (Vout - Vin)} \quad \text{(eq. 10)}$$

The switching frequency is the inverse of the switching period. Consequently:

$$\mathbf{f = \frac{Vac^2}{2 * L * < Pin >} \left(1 - \frac{\sqrt{2} * Vac * \sin(\omega t)}{Vout} \right)} \quad \text{(eq. 11)}$$

This equation shows that the switching frequency consists of:

- One term $\left(\frac{Vac^2}{2 * L * < Pin >} \right)$ that only varies versus the working point (load and AC line rms voltage).
- A modulation factor $\left(1 - \frac{\sqrt{2} * Vac * \sin(\omega t)}{Vout} \right)$ that makes the switching frequency vary within the AC line sinusoid.

The following figure illustrates the switching frequency variations versus the AC line amplitude, the power and within the sinusoid.

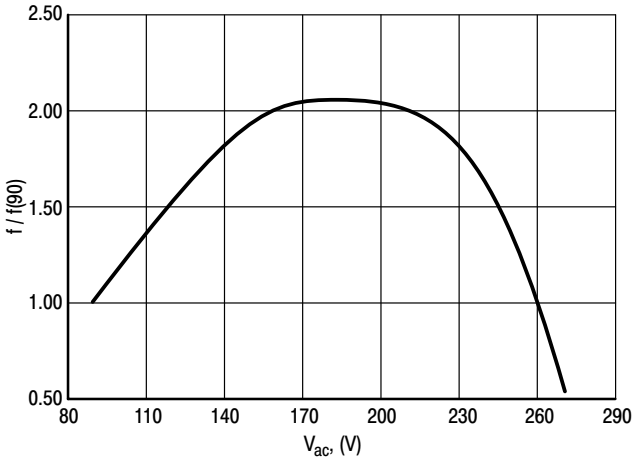

Figure 5. Switching Frequency Over the AC Line RMS Voltage (at the Sinusoid top)

The figure represents the switching frequency variations versus the line rms voltage, in a normalized form where f(90) = 1. The plot drawn for V_{out} = 400 V, shows large variations (200% at Vac = 180 V, 60% at Vac = 270 V). The shape of the curve tends to flatten if V_{out} is higher. However, the minimum of the switching frequency is always obtained at one of the AC line extremes (VacLL or VacHL where VacLL and VacHL are respectively, the lowest and highest Vac levels).

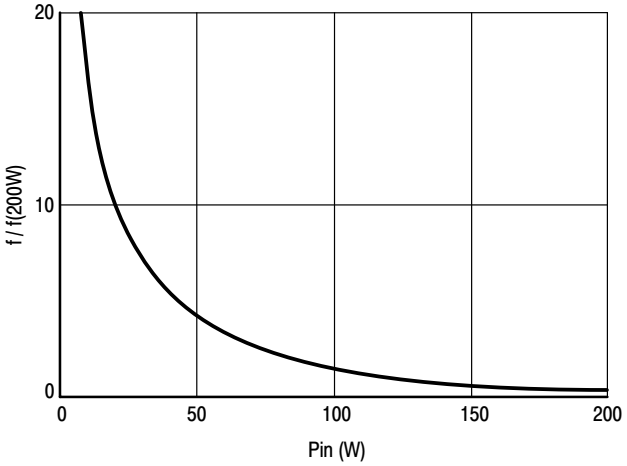

Figure 6. Switching Frequency vs. the Input Power (at the Sinusoid top)

This plot sketches the switching frequency variations versus the input power in a normalized form where f(200 W) = 1. The switching frequency is multiplied by 20 when the power is 10 W. In practice, the PFC stage propagation delays clamp the switching frequency that could theoretically exceed several megaHertz in very light load conditions. The MC33260 minimum off−time limits the no load frequency to around 400 kHz.

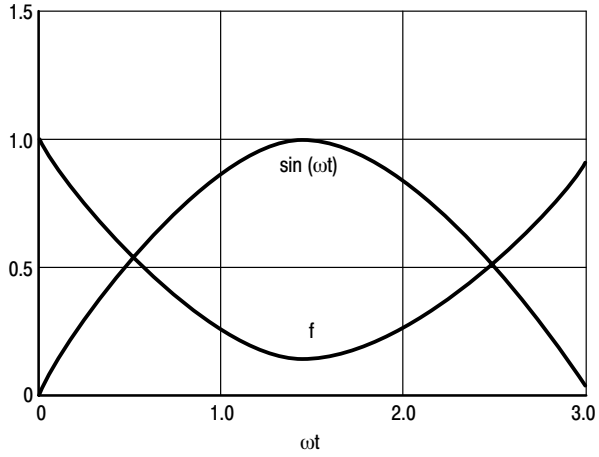

Figure 7. Switching Frequency Over the AC Line Sinusoid @ 230 Vac

This plot gives the switching variations over the AC line sinusoid at Vac = 230 V and V_{out} = 400 V, in a normalized form where f is taken equal to 1 at the AC line zero crossing. The switching frequency is approximately divided by 5 at the top of the sinusoid.

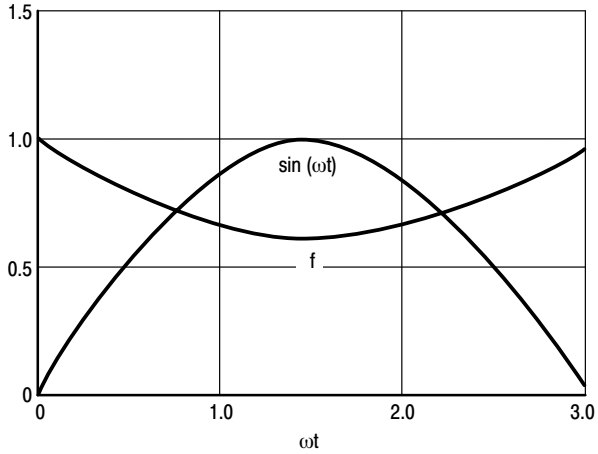

Figure 8. Switching Frequency Over the AC Line Sinusoid @ 90 Vac

This plot shows the same characteristic but for Vac = 90 V. Similarly to what was observed in Figure 5 (f versus Vac), the higher the difference between the output and input voltages, the flatter the switching frequency shape.

Finally, the switching frequency dramatically varies within the AC line and versus the power. This is probably the major inconvenience of the critical conduction mode operation. This behavior often makes tougher the EMI filtering. It also can increase the risk of generating interference that disturb the systems powered by the PFC stage (for instance, it may produce some visible noise on the screen of a monitor).

In addition, the variations of the frequency and the high values it can reach (up to 500 kHz) practically prevent the use of effective tools to damp EMI and reduce noise like snubbing networks that would generate too high losses.

One can also note that the frequency increases when the power diminishes and when the input voltage increases. In light load conditions, the switching period can become as low as 2.0 μs (500 kHz). All the propagation delays within the control circuitry or the power switch reaction times are no more negligible, what generally distorts the current shape. The power factor is then degraded.

The switching frequency variation is a major limitation of the system that should be reserved to application where the load does not vary drastically.

Coil Peak and RMS Currents

Coil Peak Current

As the PFC stage makes the AC line current sinusoidal and in phase with the AC line voltage, one can write:

$$Iin(t) = \sqrt{2} * Iac * \sin(\omega t) \qquad \text{(eq. 12)}$$

where Iin(t) is the instantaneous AC line current and Iac its rms value.

Provided that the AC line current results from the averaging of the coil current, one can deduct the following equation:

$$Iin(t) = < Icoil >_T = \frac{Icoil\_pk}{2} \qquad \text{(eq. 13)}$$

where $<Icoil>_T$ is the average of the considered coil current triangle over the switching period T and Icoil_pk is the corresponding peak.

Thus, the peak value of the coil current triangles follows a sinusoidal envelope and equals:

$$Icoil\_pk = 2 * \sqrt{2} * Iac * \sin(\omega t) \qquad \text{(eq. 14)}$$

Since the PFC stage forces the power factor close to 1, one can use the well known relationship linking the average input power to the AC line rms current and rms voltage ($< Pin > = Vac * Iac$) and the precedent equation leads to:

$$Icoil\_pk = 2 * \sqrt{2} * \frac{< Pin >}{Vac} * \sin(\omega t) \qquad \text{(eq. 15)}$$

The coil current peak is maximum at the top of the sinusoid where $\sin(\varpi t) = 1$. This maximum value, (Icoil_pk)H, is then:

$$(Icoil\_pk)H = 2 * \sqrt{2} * \frac{< Pin >}{Vac} \qquad \text{(eq. 16)}$$

From this equation, one can easily deduct that the peak coil current is maximum when the required power is maximum and the AC line at its minimum voltage:

$$\mathbf{Icoil\_max = 2 * \sqrt{2} * \frac{< Pin > max}{VacLL}} \qquad \text{(eq. 17)}$$

where <Pin>max is the maximum input power of the application and VacLL the lowest level of the AC line voltage.

Coil RMS Current

The rms value of a current is the magnitude that squared, gives the dissipation produced by this current within a 1.0 Ω resistor. One must then compute the rms coil current by:

- First calculating the “rms current” within a switching period in such a way that once squared, it would give the power dissipated in a 1.0 Ω resistor during the considered switching period.
- Then the switching period being small compared to the input voltage cycle, regarding the obtained expression as the instantaneous square of the coil current and averaging it over the rectified sinusoid cycle, to have the squared coil rms current.

This method will be used in this section.

As above explained, the current flowing through the coil is:

- ($I_M(t) = Vin * t/L = Icoil\_pk * t/ton$) during the MOSFET on−time, when 0<t<ton.
- ($I_D(t) = Icoil\_pk - \{(Vout - Vin) * t/L\} = Icoil\_pk * (T - t)/(T - ton)$) during the diode conduction time, that is, when ton<t<T.

Therefore, the rms value of any coil current triangle over the corresponding switching period T, is given by the following equation:

$$< (Icoil)rms >_T = \sqrt{\frac{1}{T} * \left(\int_0^{ton} \left[\frac{Icoil\_pk * t}{ton} \right]^2 * dt + \int_{ton}^{T} \left[Icoil\_pk * \frac{T - t}{T - ton} \right]^2 * dt \right)} \quad \text{(eq. 18)}$$

Solving the integrals, it becomes:

$$< (Icoil)rms >_T = \sqrt{\frac{1}{T} * \left(\left[\frac{Icoil\_pk^2}{ton^2} * \frac{ton^3}{3} \right] + \left[\frac{-(T - ton)}{3 * Icoil\_pk} * \left(\left[Icoil\_pk * \frac{T - T}{T - ton} \right]^3 - \left[Icoil\_pk * \frac{T - ton}{T - ton} \right]^3 \right) \right] \right)} \quad \text{(eq. 19)}$$

The precedent simplifies as follows:

$$< (Icoil)rms >_T = \sqrt{\frac{1}{T} * \left(\frac{Icoil\_pk^2 * ton}{3} + \left[\frac{-(T - ton)}{3 * Icoil\_pk} * (-Icoil\_pk^3) \right] \right)} \quad \text{(eq. 20)}$$

Rearrangement of the terms leads to:

$$< (Icoil)rms >_T = I_{coil\_pk} * \sqrt{\frac{1}{T} * \left(\frac{ton}{3} + \frac{T - ton}{3} \right)} \quad \text{(eq. 21)}$$

Calculating the term under the root square sign, the following expression is obtained:

$$< (Icoil)rms >_T = \frac{Icoil\_pk}{\sqrt{3}} \quad \text{(eq. 22)}$$

Replacing the coil peak current by its expression as a function of the average input power and the AC line rms voltage (equation 15), one can write the following equation:

$$< (Icoil)rms >_T = 2 * \sqrt{\frac{2}{3}} * \frac{< Pin >}{Vac} * \sin(\omega t) \quad \text{(eq. 23)}$$

This equation gives the equivalent rms current of the coil over one switching period, that is, at a given V_{in}. As already stated, multiplying the square of it by the coil resistance, gives the resistive losses at this given V_{in}. Now to have the rms current over the rectified AC line period, one must not integrate $<(Icoil)rms>_T$ but the square of it, as we would have proceeded to deduct the average resistive losses from the dissipation over one switching period. However, one must not forget to extract the root square of the result to obtain the rms value.

As the consequence, the coil rms current is:

$$(Icoil)rms = \sqrt{\frac{2}{Tac} * \int_0^{Tac/2} < (I_{coil})rms >_T^2 * dt} \quad \text{(eq. 24)}$$

where Tac = 2*π/ω is the AC line period (20 ms in Europe, 16.66 ms in USA). The PFC stage being fed by the rectified AC line voltage, it operates at twice the AC line frequency. That is why, one integrates over half the AC line period (Tac/2).

Substitution of equation (23) into the precedent equation leads to:

$$(Icoil)rms = \sqrt{\frac{2}{Tac} * \int_0^{Tac/2} \left[2 * \sqrt{\frac{2}{3}} * \frac{< Pin >}{Vac} * \sin(\omega t) \right]^2 * dt} \quad \text{(eq. 25)}$$

This equation shows that the coil rms current is the rms value of: $2 * \sqrt{\frac{2}{3}} * \frac{< Pin >}{Vac} * \sin(\omega t)$, that is, the rms value of a sinusoidal current whose magnitude is $(2 * \sqrt{\frac{2}{3}} * \frac{< Pin >}{Vac})$. The rms value of such a sinusoidal current is well known (the amplitude divided by $\sqrt{2}$).

Therefore:

$$\mathbf{Icoil(rms)} = \frac{\mathbf{2}}{\sqrt{\mathbf{3}}} * \frac{< \mathbf{Pin} >}{\mathbf{Vac}} \quad \text{(eq. 26)}$$

Switching Losses

The switching losses are difficult to determine with accuracy. They depend of the MOSFET type and in particular of the gate charge, of the controller driver capability and obviously of the switching frequency that varies dramatically in a critical conduction mode operation. However, one can make a rough estimation if one assumes the following:

- The output voltage is considered as a constant. The output voltage ripple being generally less than 5% the nominal voltage, this assumption seems reasonable.
- The switching times (δt and t_{FR}, as defined in Figure 9), are considered as constant over the sinusoid.

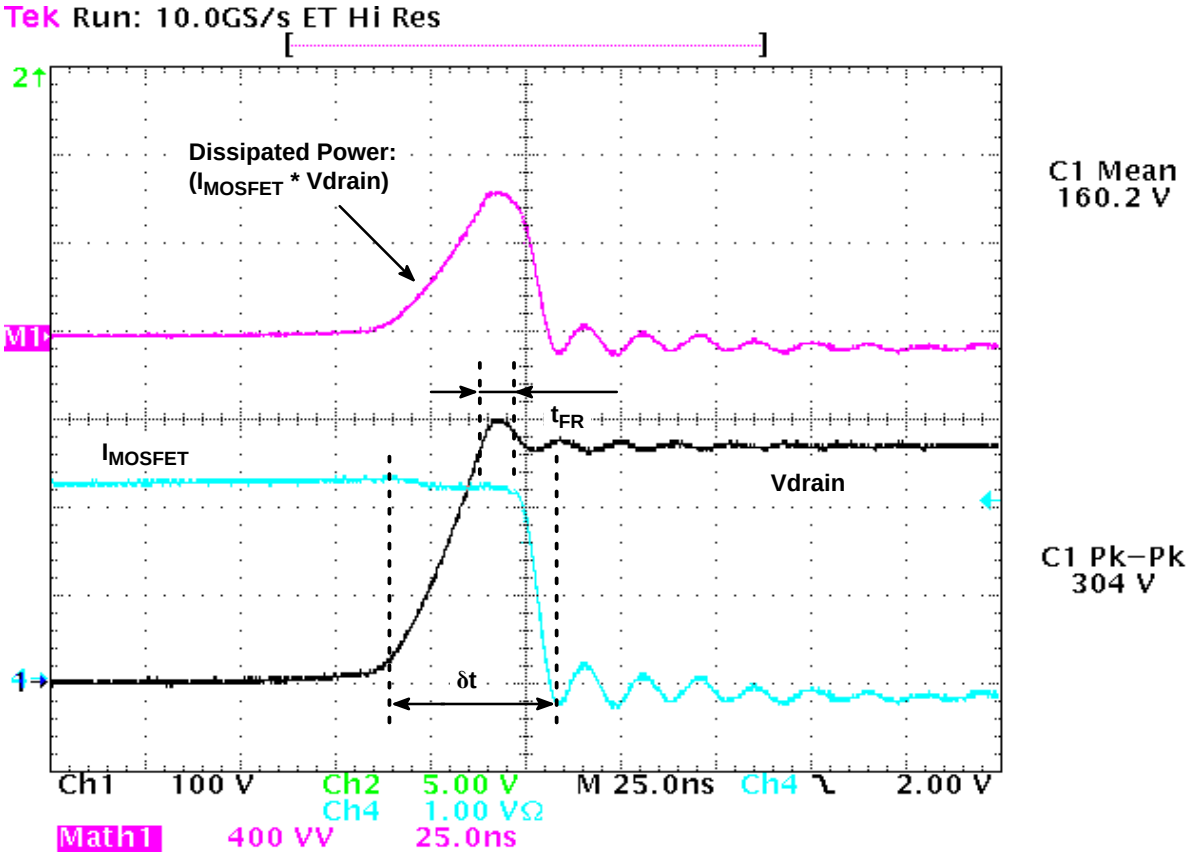

Figure 9. Turn Off Waveforms

Figure 9 represents a turn off sequence. One can observe three phases:

- During approximately the second half of the gate voltage Miller plateau, the drain−source voltage increases linearly till it reaches the output voltage.
- During a short time that is part of the diode forward recovery time, the MOSFET faces both maximum voltage and current.
- The gate voltage drops (from the Miller plateau) below the gate threshold and the drain current ramps down to zero.

"δt" of Figure 9 represents the total time of the three phases, "t_{FR}" the second phase duration.

Therefore, one can write:

$$psw = \left(\frac{Vout * Icoil\_pk}{2} * \frac{\delta t - t_{FR}}{T}\right) + \left(Vout * Icoil\_pk * \frac{t_{FR}}{T}\right) \quad \text{(eq. 27)}$$

where: δt and t_{FR} are the switching times portrayed by Figure 9 and T is the switching period.

Equation (8) gives an expression linking the coil peak current and the switching period of the considered current cycle (triangle): $T = \frac{L * Icoil\_pk}{Vin} * \frac{Vout}{Vout - Vin}$.

Substitution of equation (8) into the equation (27) leads to:

$$psw = \frac{Vin * (Vout - Vin) * (\delta t + t_{FR})}{2 * L} \quad \text{(eq. 28)}$$

This equation shows that the switching losses over a switching period depend of the instantaneous input voltage, the difference between the instantaneous output and input voltages, the switching time and the coil value. Let's calculate the average losses (<psw>) by integrating psw over half the AC line period:

$$< psw > = \frac{2}{Tac} * \int_{0}^{Tac/2} \frac{Vin * (Vout - Vin) * (\delta t + t_{FR})}{2 * L} * dt \quad \text{(eq. 29)}$$

Rearranging the terms, one obtains:

$$< psw > = \frac{\delta t + t_{FR}}{2 * L} * \left\{ \left(\frac{2}{Tac} * \int_{0}^{Tac/2} Vin * Vout * dt \right) - \left(\frac{2}{Tac} * \int_{0}^{Tac/2} Vin^2 * dt \right) \right\} \quad \text{(eq. 30)}$$

V_{out} being considered as a constant, one can easily solve this equation if one remembers that the input voltage average value is $(2 * \sqrt{2} * Vac/\pi)$ and that $(Vac^2 = \frac{2}{Tac} * \int_{0}^{Tac/2} Vin^2 * dt)$. Applying this, it becomes:

$$< psw > = \frac{\delta t + t_{FR}}{2 * L} * \left(\frac{2 * \sqrt{2} * Vac * Vout}{\pi} - Vac^2 \right) \quad \text{(eq. 31)}$$

Or in a simpler manner:

$$< psw > = \frac{2 * (\delta t + t_{FR}) * Vac^2}{\pi * L} * \left(\frac{Vout}{\sqrt{2} * Vac} - \frac{\pi}{4} \right) \quad \text{(eq. 32)}$$

The coil inductance (L) plays an important role: the losses are inversely proportional to this value. It is simply because the switching frequency is also inversely proportional to L.

This equation also shows that the switching losses are independent of the power level. One could have easily predict this result by simply noting that the switching frequency increased when power diminished.

Equation (32) also shows that the lower the ratio (V_{out}/Vac), the smaller the MOSFET switching losses. That is because the "Follower Boost" mode that reduces the difference between the output and input voltages, lowers the switching frequency. In other words, this technique enables the use of a smaller coil for the same switching frequency range and the same switching losses.

For instance, the MC33260 features the "Follower Boost" operation where the pre−converter output voltage stabilizes at a level that varies linearly versus the AC line amplitude. This technique aims at reducing the gap between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage[1].

How to extract δt and t_{FR}?

- The best is to measure them.
- One can approximate δt as the time necessary to extract the gate charge Q3 of the MOSFET (refer to Figure 10). Q3 being not always specified, instead, one can take the sum of Q1 with half the Miller plateau gate charge (Q2/2). Knowing the drive capability of the circuit, one can deduct the turn off time ($\delta t = Q3/I_{drive}$ or $\delta t = [Q1 + (Q2/2)]/I_{drive}$).
- In a first approach, t_{FR} can be taken equal to the diode forward recovery time.

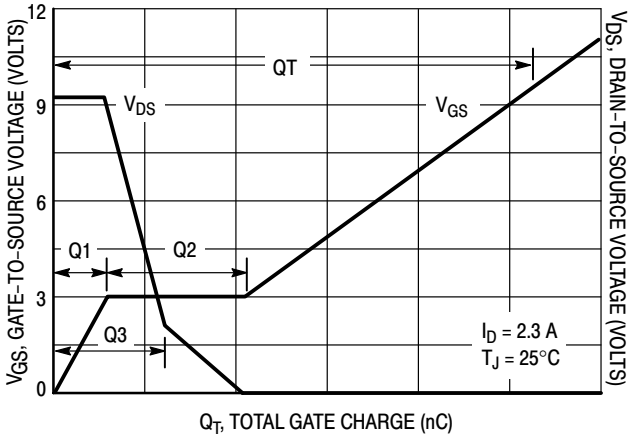

Figure 10. Typical Total Gate Charge Specification of a MOSFET

One must note that the calculation does not take into account:

- The energy consumed by the controller to drive the MOSFET (Qcc*Vcc*f), where Qcc is the MOSFET gate charge necessary to charge the gate voltage to Vcc, Vcc the driver supply voltage and f the switching frequency.
- The energy dissipated because of the parasitic capacitors of the PFC stage. Each turn on produces an abrupt voltage change across the parasitic capacitors of the MOSFET drain−source, the diode and the coil. This results in some extra dissipation across the MOSFET ($1/2*C_{parasitic}*\Delta V^2*f$), where $C_{parasitic}$ is the

considered parasitic capacitor and ΔV the voltage change across it.

[1] Refer to MC33260 data sheet for more details at http://www.onsemi.com/.

However, equation (32) should give a sufficient first approach approximation in most applications where the two listed sources of losses play a minor role. Nevertheless, the losses produced by the parasitic capacitors may become significant in light load conditions where the switching frequency gets high. As always, bench validation is key.

Power MOSFET Conduction Losses

As portrayed by Figure 4, the coil current is formed by high frequency triangles. The input capacitor together with the input RFI filter integrates the coil current ripple so that the resulting AC line current is sinusoidal.

During the on−time, the current rises linearly through the power switch as follows:

$$Icoil(t) = \frac{Vin}{L} * t \qquad \text{(eq. 33)}$$

where V_{in} is the input voltage ($Vin = \sqrt{2} * Vac * \sin(\omega t)$), L is the coil inductance and t is the time.

During the rest of the switching period, the power switch is off. The conduction losses resulting from the power dissipated by Icoil during the on−time, one can calculate the power during the switching period T as follows:

$$p_T = \frac{1}{T} * \int_0^{ton} Ron * Icoil(t)^2 * dt = \frac{1}{T} * \int_0^{ton} Ron * \left(\frac{Vin}{L} * t\right)^2 * dt \qquad \text{(eq. 34)}$$

where Ron is the MOSFET on−time drain source resistor, ton is the on−time.

Solving the integral, equation (34) simplifies as follows:

$$p_T = \frac{Ron}{T} * \left(\frac{Vin}{L}\right)^2 * \int_0^{ton} t^2 * dt = \frac{1}{3} * Ron * \left(\frac{Vin}{L}\right)^2 * \frac{ton^3}{T} \qquad \text{(eq. 35)}$$

As the coil current reaches its peak value at the end of the on−time, $Icoil\_pk = Vin * ton/L$ and the precedent equation can be rewritten as follows:

$$p_T = \frac{1}{3} * Ron * Icoil\_pk^2 * \frac{ton}{T} \qquad \text{(eq. 36)}$$

One can recognize the traditional equation permitting to calculate the MOSFET conduction losses in a boost or a flyback ($\frac{1}{3} * Ron * Ipk^2 * d$, where Ipk is the peak current and d, the MOSFET duty cycle).

One can calculate the duty cycle (d = ton/T) by:

- Either noting that the off−time (toff) can be expressed as a function of ton (refer to equation 2) and substituting this equation into (T = ton + Toff),
- Or considering that the critical conduction mode being at the border of the continuous conduction mode (CCM), the expression giving the duty−cycle in a CCM boost converter applies.

Both methods lead to the same following result:

$$d = \frac{ton}{T} = 1 - \frac{Vin}{Vout} \qquad \text{(eq. 37)}$$

Substitution of equation (37) into equation (36) leads to:

$$p_T = \frac{1}{3} * Ron * Icoil\_pk^2 * \left(1 - \frac{Vin}{Vout}\right) \qquad \text{(eq. 38)}$$

One can note that the coil peak current (Icoil_pk) that follows a sinusoidal envelop, can be written as follows: $Icoil\_pk = 2 * \sqrt{2} * \frac{< Pin >}{Vac} * \sin(\omega t)$ (refer to equation 15).

Replacing V_{in} and Icoil_pk by their sinusoidal expression, respectively ($\sqrt{2} * Vac * \sin(\omega t)$) and ($2 * \sqrt{2} * \frac{< Pin >}{Vac} * \sin(\omega t)$), equation (38) becomes:

$$p_T = \frac{1}{3} * Ron * \left(2 * \sqrt{2} * \frac{< Pin >}{Vac} * \sin(\omega t)\right)^2 * \left(1 - \frac{\sqrt{2} * Vac * \sin(\omega t)}{Vout}\right) \qquad \text{(eq. 39)}$$

That is in a more compact form:

$$p_T = \frac{8}{3} * Ron * \left(\frac{< Pin >}{Vac}\right)^2 * \left[\sin^2(\omega t) - \left(\frac{\sqrt{2} * Vac}{Vout} * \sin^3(\omega t)\right)\right] \qquad \text{(eq. 40)}$$

Equation (40) gives the conduction losses at a given V_{in} voltage. This equation must be integrated over the rectified AC line sinusoid to obtain the average losses:

$$< p > Tac = \frac{8}{3} * Ron * \left(\frac{< Pin >}{Vac}\right)^2 * \frac{2}{Tac} * \int_0^{Tac/2} \left[\sin^2(\omega t) - \left(\frac{\sqrt{2} * Vac}{Vout} * \sin^3(\omega t)\right)\right] * dt \qquad \text{(eq. 41)}$$

If the average value of $\sin^2(\omega t)$ is well known (0.5), the calculation of $<\sin^3(\omega t)>$ requires few trigonometry remembers:

- $\sin^2(\alpha) = \frac{1 - \cos(2\alpha)}{2}$
- $\sin(\alpha) * \cos(\beta) = \frac{\sin(\alpha + \beta) + \sin(\alpha - \beta)}{2}$

Combining the two precedent formulas, one can obtain:

$$\sin^3(\omega t) = \frac{3 * \sin(\omega t)}{4} - \frac{\sin(3\omega t)}{4} \quad \text{(eq. 42)}$$

Substitution of equation 42) into equation (41) leads:

$$< p >_{Tac} = \frac{8}{3} * Ron * \left(\frac{< Pin >}{Vac}\right)^2 * \frac{2}{Tac} * \int_0^{Tac/2} \left[\sin(\omega t)^2 - \left(\frac{3 * \sqrt{2} * Vac}{4 * Vout} * \sin(\omega t)\right) + \left(\frac{\sqrt{2} * Vac}{4 * Vout} * \sin(3\omega t)\right)\right] * dt \quad \text{(eq. 43)}$$

Solving the integral, it becomes:

$$< p >_{Tac} = \frac{8}{3} * Ron * \left(\frac{< Pin >}{Vac}\right)^2 * \left[\frac{1}{2} - \left(\frac{3 * \sqrt{2} * Vac}{4 * Vout} * \frac{2}{\pi}\right) + \left(\frac{\sqrt{2} * Vac}{4 * Vout} * \frac{2}{3\pi}\right)\right] \quad \text{(eq. 44)}$$

Equation (44) simplifies as follows:

$$< p >_{Tac} = \frac{4}{3} * Ron * \left(\frac{< Pin >}{Vac}\right)^2 * \left[1 - \left(\frac{8 * \sqrt{2} * Vac}{3\pi * Vout}\right)\right] \quad \text{(eq. 45)}$$

This formula shows that the higher the ratio (Vac/V_{out}), the smaller the MOSFET conduction losses. That is why the "Follower Boost" mode that reduces the difference between the output and input voltages, enables to reduce the MOSFET size.

For instance, the MC33260 features the "Follower Boost" operation where the pre−converter output voltage stabilizes at a level that varies linearly versus the AC line amplitude. This technique aims at reducing the gap between the output and input voltages to optimize the boost efficiency and minimize the cost of the PFC stage[2].

By the way, one can deduct from this equation the rms current ((I_M)rms) flowing through the power switch knowing that $< p >_{Tac} = Ron * (I_M)^2$rms :

$$(I_M)rms = \frac{2}{\sqrt{3}} * \frac{< Pin >}{Vac} * \sqrt{1 - \left(\frac{8 * \sqrt{2} * Vac}{3\pi * Vout}\right)} \quad \text{(eq. 46)}$$

Dissipation within the Current Sense Resistor

PFC controllers monitor the power switch current either to perform the shaping function or simply to prevent it from being excessive. That is why a resistor is traditionally placed between the MOSFET source and ground to sense the power switch current.

The MC33260 monitors the whole coil current by monitoring the voltage across a resistor inserted between ground and the diodes bridge (negative sensing – refer to Figure 15). The circuit utilizes the current information for both the overcurrent protection and the core reset detection (also named zero current detection). This technique brings two major benefits:

- No need for an auxiliary winding to detect the core reset. A simple coil is sufficient in the PFC stage.
- The MC33260 detects the in−rush currents that may flow at start−up or during some overload conditions and prevents the power switch from turning on in that stressful condition. The PFC stage is significantly safer.

Some increase of the power dissipated by the current sense resistor is the counter part since the whole current is sensed while circuits like the MC33262 only monitor the power switch current.

Dissipation of the Current Sense Resistor in MC33262 Like Circuits

Since the same current flows through the current sense resistor and the power switch, the calculation is rather easy. One must just square the rms value of the power switch current (I_M)rms calculated in the previous section and multiply the result by the current sense resistance.

[2] Refer to MC33260 data sheet for more details at http://www.onsemi.com/.

Doing this, one obtains:

$$< \mathbf{pRs} > \mathbf{262} = \frac{\mathbf{4}}{\mathbf{3}} * \mathbf{Rs} * \left(\frac{< \mathbf{Pin} >}{\mathbf{Vac}}\right)^{\mathbf{2}} * \left[\mathbf{1} - \left(\frac{\mathbf{8} * \sqrt{\mathbf{2}} * \mathbf{Vac}}{\mathbf{3\pi} * \mathbf{Vout}}\right)\right] \quad \text{(eq. 47)}$$

where $<pRs>_{262}$ is the power dissipated by the current sense resistor Rs.

Dissipation of the Current Sense Resistor in MC33260 Like Circuits

In this case, the current sense resistor Rs derives the whole coil current. Consequently, the product of Rs by the square of the rms coil current gives the dissipation of the current sense resistor:

$$< pRs > 260 = Rs * (Icoil(rms))^2 \quad \text{(eq. 48)}$$

where Icoil(rms) is the coil rms current that as expressed by equation (26), equals: $Icoil(rms) = \frac{2}{\sqrt{3}} * \frac{< Pin >}{Vac}$.

Consequently:

$$< \mathbf{pRs} > \mathbf{260} = \frac{\mathbf{4} * \mathbf{Rs}}{\mathbf{3}} * \left(\frac{< \mathbf{Pin} >}{\mathbf{Vac}}\right)^{\mathbf{2}} \quad \text{(eq. 49)}$$

Comparison of the Losses Amount in the Two Cases

Let's calculate the ratios: $< pRs > 262 / < pRs > 260$. One obtains:

$$< pRs > 262 / < pRs > 260 = 1 - \left(\frac{8 * \sqrt{2} * Vac}{3\pi * Vout}\right) \quad \text{(eq. 50)}$$

If one considers that (8/3 π) approximately equals 0.85, the precedent equation simplifies:

$$< \mathbf{pRs} > \mathbf{262} / < \mathbf{pRs} > \mathbf{260} \approx \mathbf{1} - \frac{\mathbf{0.85} * \mathbf{Vm}}{\mathbf{Vout}} \quad \text{(eq. 51)}$$

where Vm is the AC line amplitude.

Average and RMS Current through the Diode

The diode average current can be easily computed if one notes that it is the sum of the load and output capacitor currents:

$$Id = I_{load} + I_{Cout} \quad \text{(eq. 52)}$$

Then, in average:

$$< Id > = < I_{load} + I_{Cout} > = < I_{load} > + < I_{Cout} > \quad \text{(eq. 53)}$$

At the equilibrium, the average current of the output capacitor must be 0 (otherwise the capacitor voltage will be infinite). Thus:

$$< \mathbf{Id} > = < \mathbf{I_{load}} > = \frac{\mathbf{Pout}}{\mathbf{Vout}} \quad \text{(eq. 54)}$$

The rms diode current is more difficult to calculate. Similarly to the computation of the rms coil current for instance, it is necessary to first compute the squared rms current at the switching period level and then to integrate the obtained result over the AC line sinusoid.

As portrayed by Figure 4, the coil discharges during the off time. More specifically, the current decays linearly through the diode from its peak value (Icoil_pk) down to zero that is reached at the end of the off−time. Taking the beginning of the off−time as the time origin, one can then write:

$$Icoil(t) = Icoil\_pk * \frac{toff - t}{toff} \quad \text{(eq. 55)}$$

Similarly to the calculation done to compute the coil rms current, one can calculate the "diode rms current over one switching period":

$$Id(rms)^2_T = \frac{1}{T} * \int_0^{toff} \left[Icoil\_pk * \frac{toff - t}{toff}\right]^2 * dt \quad \text{(eq. 56)}$$

Solving the integral, one obtains the expression of the "rms diode current over one switching period":

$$Id(rms)_T = \sqrt{\frac{toff}{3 * T}} * Icoil\_pk \quad \text{(eq. 57)}$$

Substitution of equation (15) that expresses Icoil_pk, into the precedent equation leads to:

$$Id(rms)_T = 2 * \sqrt{\frac{2}{3}} * \frac{< Pin >}{Vac} * \sqrt{\frac{toff}{T}} * \sin(\omega t) \quad \text{(eq. 58)}$$

In addition, one can easily show that toff and T are linked by the following equation:

$$toff = T * \frac{Vin}{Vout} = T * \frac{\sqrt{2} * Vac * \sin(\omega t)}{Vout} \quad \text{(eq. 59)}$$

Consequently, equation (58) can be changed into:

$$Id(rms)_T = \frac{2 * \sqrt{2 * \sqrt{2}}}{\sqrt{3}} * \frac{< Pin >}{\sqrt{Vac * Vout}} * \left(\sqrt{\sin(\omega t)}\right)^3 \quad \text{(eq. 60)}$$

This equation gives the equivalent rms current of the diode over one switching period, that is, at a given V_{in}. As already stated in the Coil Peak and RMS Currents section, the square of this expression must be integrated over a rectified sinusoid period to obtain the square of the diode rms current.

Therefore:

$$Id(rms)^2 = \frac{2}{Tac} * \int_0^{Tac/2} \frac{8 * \sqrt{2}}{3} * \frac{< Pin >^2}{Vac * Vout} * \sin^3(\omega t) * dt \quad \text{(eq. 61)}$$

Similarly to the Power MOSFET Conduction Losses section, the integration of ($\sin^3(\omega t)$) requires some preliminary trigonometric manipulations:

$$\begin{cases} \sin^3(\omega t) = \sin(\omega t) * \sin^2(\omega t) = \sin(\omega t) * \left(\frac{1 - \cos(2\omega t)}{2}\right) = \frac{1}{2} * \sin(\omega t) - \frac{1}{2} * \sin(\omega t) * \cos(2\omega t) \\ \text{And :} \\ \sin(\omega t) * \cos(2\omega t) = \frac{1}{2} * (\sin(-\omega t) + \sin(4\omega t)) \\ \text{Then :} \\ \sin^3(\omega t) = \frac{3}{4} * \sin(\omega t) - \frac{1}{4} * \sin(3\omega t) \end{cases}$$

Consequently, equation (61) can change into:

$$Id(rms)^2 = \frac{2}{Tac} * \int_0^{Tac/2} \frac{8 * \sqrt{2}}{3} * \frac{Pin^2}{Vac * Vout} * \left[\frac{3 * \sin(\omega t)}{4} - \frac{\sin(3\omega t)}{4}\right] * dt \quad \text{(eq. 62)}$$

One can now solve the integral and write:

$$Id(rms)^2 = \frac{16 * \sqrt{2}}{3 * Tac} * \frac{< Pin >^2}{Vac * Vout} * \left(\frac{3 * (\cos(\omega 0) - \cos(\omega Tac/2))}{4\omega} + \frac{\cos(3\omega Tac/2) - \cos(3\omega 0)}{12\omega}\right) \quad \text{(eq. 63)}$$

As ($\varpi * Tac = 2\pi$), we have:

$$Id(rms)^2 = \frac{16 * \sqrt{2}}{3} * \frac{Pin^2}{Vac * Vout} * \left(\frac{3 * (1 - \cos(\pi))}{4\omega * Tac} + \frac{\cos(\pi) - 1}{12\omega * Tac}\right) \quad \text{(eq. 64)}$$

One can simplify the equation replacing the cosine elements by their value:

$$Id(rms)^2 = \frac{16 * \sqrt{2}}{3} * \frac{< Pin >^2}{Vac * Vout} * \left(\frac{6}{8 * \pi} - \frac{1}{12 * \pi}\right) \quad \text{(eq. 65)}$$

The square of the diode rms current simplifies as follows:

$$Id(rms)^2 = \frac{32 * \sqrt{2}}{9 * \pi} * \frac{< Pin >^2}{Vac * Vout} \quad \text{(eq. 66)}$$

Finally, the diode rms current is given by:

$$\mathbf{Id(rms) = \frac{4}{3} * \frac{\sqrt{2 * \sqrt{2}}}{\pi} * \frac{< Pin >}{\sqrt{Vac * Vout}}} \quad \text{(eq. 67)}$$

Output Capacitor RMS Current

As shown by Figure 11, the capacitor current results from the difference between the diode current (I1) and the current absorbed by the load (I2):

$$Ic(t) = I1(t) - I2(t) \quad \text{(eq. 68)}$$

Thus, the capacitor rms current over the rectified AC line period, is the rms value of the difference between I1 and I2 during this period. As a consequence:

$$Ic(rms)^2 = \frac{2}{Tac} * \int_0^{Tac/2} (I1 - I2)^2 * dt \quad \text{(eq. 69)}$$

Rearranging $(I1-I2)^2$ leads to:

$$Ic(rms)^2 = \frac{2}{Tac} * \int_0^{Tac/2} [I1^2 + I2^2 - (2 * I1 * I2)] * dt \quad \text{(eq. 70)}$$

Thus:

$$Ic(rms)^2 = I1(rms)^2 + I2(rms)^2 - \frac{4}{Tac} * \int_0^{Tac/2} I1 * I2 * dt \quad \text{(eq. 71)}$$

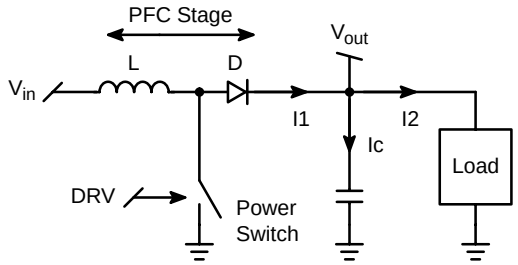

Figure 11. Output Capacitor Current

One knows the first term ($I1(rms)^2$). This is the diode rms current calculated in the previous section. The second and third terms are dependent of the load. One cannot compute them without knowing the characteristic of this load.

Anyway, the second term ($I2(rms)^2$) is generally easy to calculate once the load is known. Typically, this is the rms current absorbed by a downstream converter. On the other hand, the third term is more difficult to determine as it depends on the relative occurrence of the I1 and I2 currents. As the PFC stage and the load (generally a switching mode power supply) are not synchronized, this term even seems impossible to predict. One can simply note that this term tends to decrease the capacitor rms current and consequently, one can deduct that:

$$Ic(rms) \leq \sqrt{I1(rms)^2 + I2(rms)^2} \quad \text{(eq. 72)}$$

Substitution of equation (67) that gives the diode rms current into the precedent equation leads to:

$$\mathbf{Ic(rms)} \leq \sqrt{\frac{\mathbf{32 * \sqrt{2} * < Pin >^2}}{\mathbf{9 * \pi * Vac * Vout}} + \mathbf{I2(rms)^2}} \quad \text{(eq. 73)}$$

where I2(rms) is the load rms current.

If the load is resistive, $I2 = V_{out}/R$ where R is the load resistance and equation (71) changes into:

$$Ic(rms)^2 = /1(rms)^2 + \left(\frac{Vout}{R}\right)^2 - \frac{4}{Tac} * \int_0^{Tac/2} /1 * \frac{Vout}{R} * dt \quad \text{(eq. 74)}$$

Thus, the capacitor squared rms current is:

$$Ic(rms)^2 = Id(rms)^2 + \left(\frac{Vout}{R}\right)^2 \frac{2 * Vout}{R} * < Id > \quad \text{(eq. 75)}$$

$$Ic(rms)^2 = \frac{32 * \sqrt{2}}{9 * \pi} * \frac{< Pin >^2}{Vac * Vout} + \left(\frac{Vout}{R}\right)^2 - \left(\frac{2 * Vout}{R} * \frac{Pout}{Vout}\right) \quad \text{(eq. 76)}$$

As $Pout = V_{out}^2/R$, the precedent equation simplifies as follows:

$$\mathbf{Ic(rms)} = \sqrt{\left[\frac{\mathbf{32 * \sqrt{2}}}{\mathbf{9 * \pi}} * \frac{\mathbf{< Pin >^2}}{\mathbf{Vac * Vout}}\right] - \left(\frac{\mathbf{Vout}}{\mathbf{R}}\right)^2} \quad \text{(eq. 77)}$$

You may find a more friendly expression in the literature: $Ic(rms) = \frac{I2}{\sqrt{2}}$, where I2 is the load current. This equation is an approximate formula that does not take into account the switching frequency ripple of the diode current. Only the low frequency current that generates the low frequency ripple of the bulk capacitor (refer to the next section) is considered (this expression can easily be found by using equation (88) and computing $Ibulk = Cbulk * dVout/dt$).

Equation (77) takes into account both high and low frequency ripples.

Output Voltage Ripple

The output voltage (or bulk capacitor voltage) exhibits two ripples.

The first one is traditional to Switch Mode Power Supplies. This ripple results from the way the output is fed by current pulses at the switching frequency pace. As bulk capacitors exhibit a parasitic series resistor (ESR – refer to Figure 12), they cannot fully filter this pulsed energy source.

More specifically:

- During the on−time, the PFC MOSFET conducts and no energy is provided to the output. The bulk capacitor feeds the load with the current it needs. The current together with the ESR resistor of the bulk capacitor form a negative voltage –(ESR*I2), where I2 is the instantaneous load current,
- During the off−time, the diode derives the coil current towards the output and the current across the ESR becomes ESR*(Id−I2), where Id is the instantaneous diode current.

This explanation assumes that the energy that is fed by the PFC stage perfectly matches the energy drawn by the load over each switching period so that one can consider that the capacitive part of the bulk has a constant voltage and that only the ESR creates some ripple.

In fact, there is an additional low frequency ripple which is inherent to the Power Factor Correction. The input current and voltage being sinusoidal, the power fed by the PFC stage has a squared sinusoid shape. On the other hand, the load generally draws a constant power. As a consequence, the PFC pre−converter delivers an amount of power that matches the load demand in average only. The output capacitor compensates the lack (excess) of input power by supplying (storing) the part of energy necessary for the instantaneous matching. Figures 13 and 14 sketch this behavior.

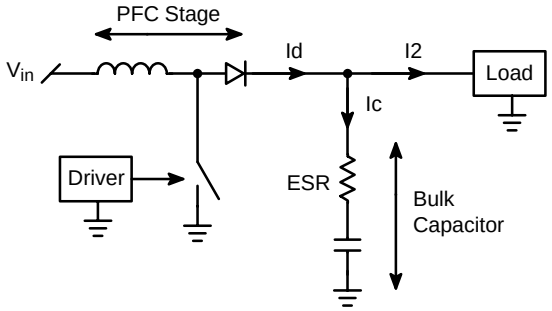

Figure 12. ESR of the Output Capacitor

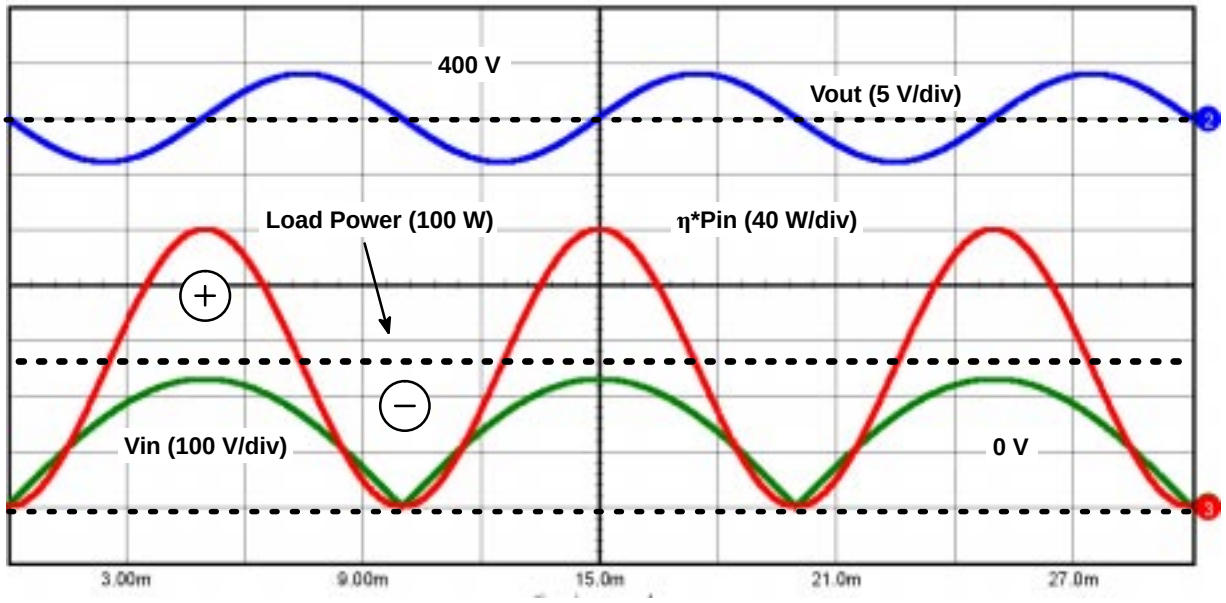

Figure 13. Output Voltage Ripple

The dashed black line represents the power that is absorbed by the load. The PFC stage delivers a power that has a squared sinusoid shape. As long as this power is lower than the load demand, the bulk capacitor compensates by supplying part of the energy it stores. Consequently the output voltage decreases. When the power fed by the PFC pre−converter exceeds the load consumption, the bulk capacitor recharges. The peak of the PFC power is twice the load demand.

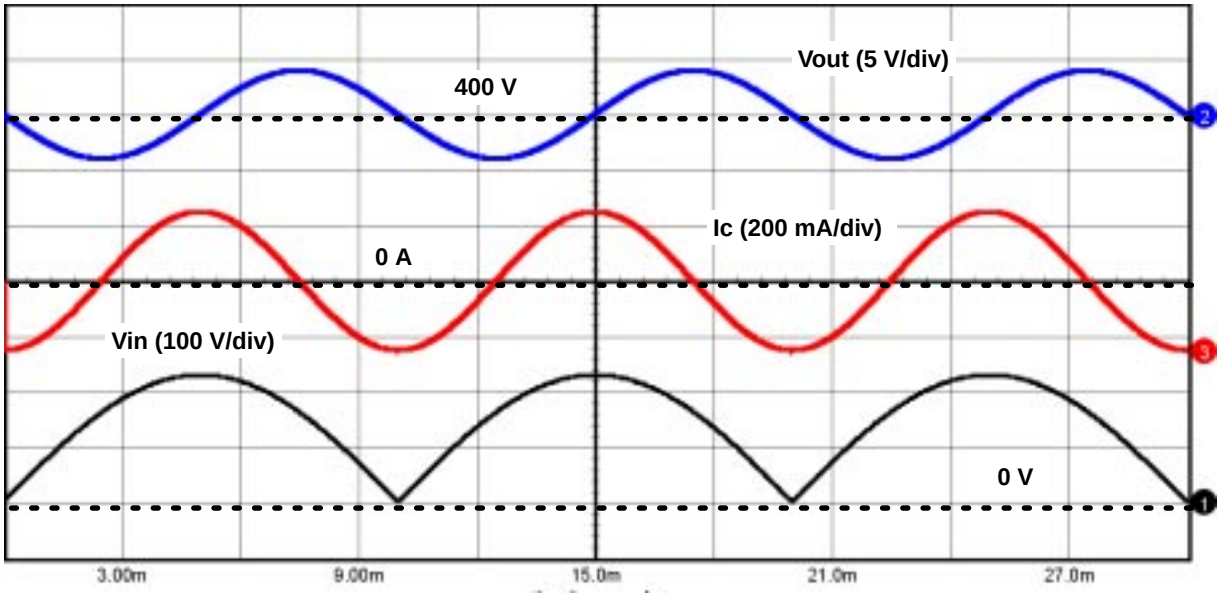

Figure 14. Output Voltage Ripple

The output voltage equals its average value when the input voltage is minimum and maximum. The output voltage is lower than its average value during the rising phase of the input voltage and higher during the input voltage decay. Similarly to the input power and voltage, the frequency of the capacitor current (represented in the case of a resistive load) is twice the AC line one.

In this calculation, one does not consider the switching ripple that is generally small compared to the low frequency ripple. In addition, the switching ripple depends on the load current shape that cannot be predicted in a general manner.

As already discussed, the average coil current over a switching period is:

$$Iin = \frac{\sqrt{2} * < Pin >}{Vac} * \sin(\omega t) \quad \text{(eq. 78)}$$

The instantaneous input power (averaged over the switching period) is the product of the input voltage ($\sqrt{2} * Vac * \sin(\varpi t)$) by Iin. Consequently:

$$Pin = 2 * < Pin > * \sin^2(\omega t) \quad \text{(eq. 79)}$$

In average over the switching period, the bulk capacitor receives a charge current ($\eta * Pin/Vout$), where η is the PFC stage efficiency, and supplies the averaged load current $< I2 > = \eta * < Pin > / Vout$. Applying the famous "capacitor formula" $I = C * dV/dt$, it becomes:

$$\eta * \frac{Pin}{Vout} - < I2 > = Cbulk * \frac{dVout}{dt} \quad \text{(eq. 80)}$$

Substitution of equation (79) into equation (80) leads to:

$$\frac{dVout}{dt} = \frac{1}{Cbulk} * \left(\frac{2 * \eta * < Pin > * \sin^2(\omega t)}{Vout} - \frac{\eta * < Pin >}{Vout} \right) \quad \text{(eq. 81)}$$

Rearranging the terms of this equation, one can obtain:

$$Vout * \frac{dVout}{dt} = \frac{\eta * < Pin >}{Cbulk} * \left[2 * \sin^2(\omega t) - 1 \right] \quad \text{(eq. 82)}$$

Noting that $\frac{d(Vout^2)}{dt} = 2 * Vout * \frac{dVout}{dt}$ and that $\cos(2\omega t) = 1 - 2 * \sin^2(\omega t)$, one can deduct the square of the output voltage from the precedent equation:

$$Vout^2 - < Vout >^2 = \frac{-\eta * < Pin >}{Cbulk * \omega} * \sin(2\omega t) \quad \text{(eq. 83)}$$

where $<V_{out}>$ is the average output voltage.

Dividing the terms of the precedent equations by the square of the average output voltage, it becomes:

$$\left(\frac{Vout}{< Vout >} \right)^2 = 1 - \frac{\eta * < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2} \quad \text{(eq. 84)}$$

Thus:

$$\frac{< Vout > + \delta Vout}{< Vout >} = \sqrt{1 - \frac{\eta * < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2}} \quad \text{(eq. 85)}$$

Where δV_{out} is the instantaneous output voltage ripple. Equation (85) can be rearranged as follows:

$$\delta Vout = < Vout > * \left(\sqrt{1 - \frac{\eta * < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2}} - 1 \right) \quad \text{(eq. 86)}$$

One can simplify this equation considering that the output voltage ripple is small compared to the average output voltage (fortunately, it is generally true). This leads to say that the term $\left(\sqrt{1 - \frac{\eta * < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2}} - 1 \right)$ is nearly zero or in other words, that $\left(\frac{\eta * < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2} \right)$ is small compared to 1. Thus, one can write that:

$$\sqrt{1 - \frac{\eta * < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2}} \approx 1 - \frac{1}{2} * \frac{\eta * < Pin > * \sin(2\omega t)}{Cbulk * \omega * < Vout >^2} \quad \text{(eq. 87)}$$

Substitution of equation (86) into equation (87), leads to the simplified ripple expression that one can generally find in the literature:

$$\delta Vout = \frac{-\eta * < Pin > * \sin(2\omega t)}{2 * Cbulk * \omega * < Vout >} \quad \text{(eq. 88)}$$

The maximum ripple is obtained when ($\sin(2\varpi t) = -1$) and minimum when ($\sin(2\omega t) = 1$). Thus, the peak−to−peak ripple that is the difference of these two values is:

$$(\delta Vout)pk-pk = \frac{\eta * < Pin >}{Cbulk * \omega * < Vout >} \quad \text{(eq. 89)}$$

And:

$$Vout = < Vout > - \frac{(\delta Vout)pk-pk}{2} * \sin(2\omega t) \quad \text{(eq. 90)}$$

Conclusion

Compared to traditional switch mode power supplies, one faces an additional difficulty when trying to predict the currents and voltages within a PFC stage: the sinusoid modulation. This is particularly true in critical conduction mode where the switching ripple cannot be neglected. As proposed in this paper, one can overcome this difficulty by:

- First calculating their value within a switching period,
- Then the switching period being considered as very small compared to the AC line cycle, integrating the result over the sinusoid period.

The proposed theoretical analysis helps predict the stress faced by the main elements of the PFC stages: coil, MOSFET, diode and bulk capacitor, with the goal of easing the selection of the power components and therefore, the PFC implementation. Nevertheless, as always, it cannot replace the bench work and the reliability tests necessary to ensure the application proper operation.

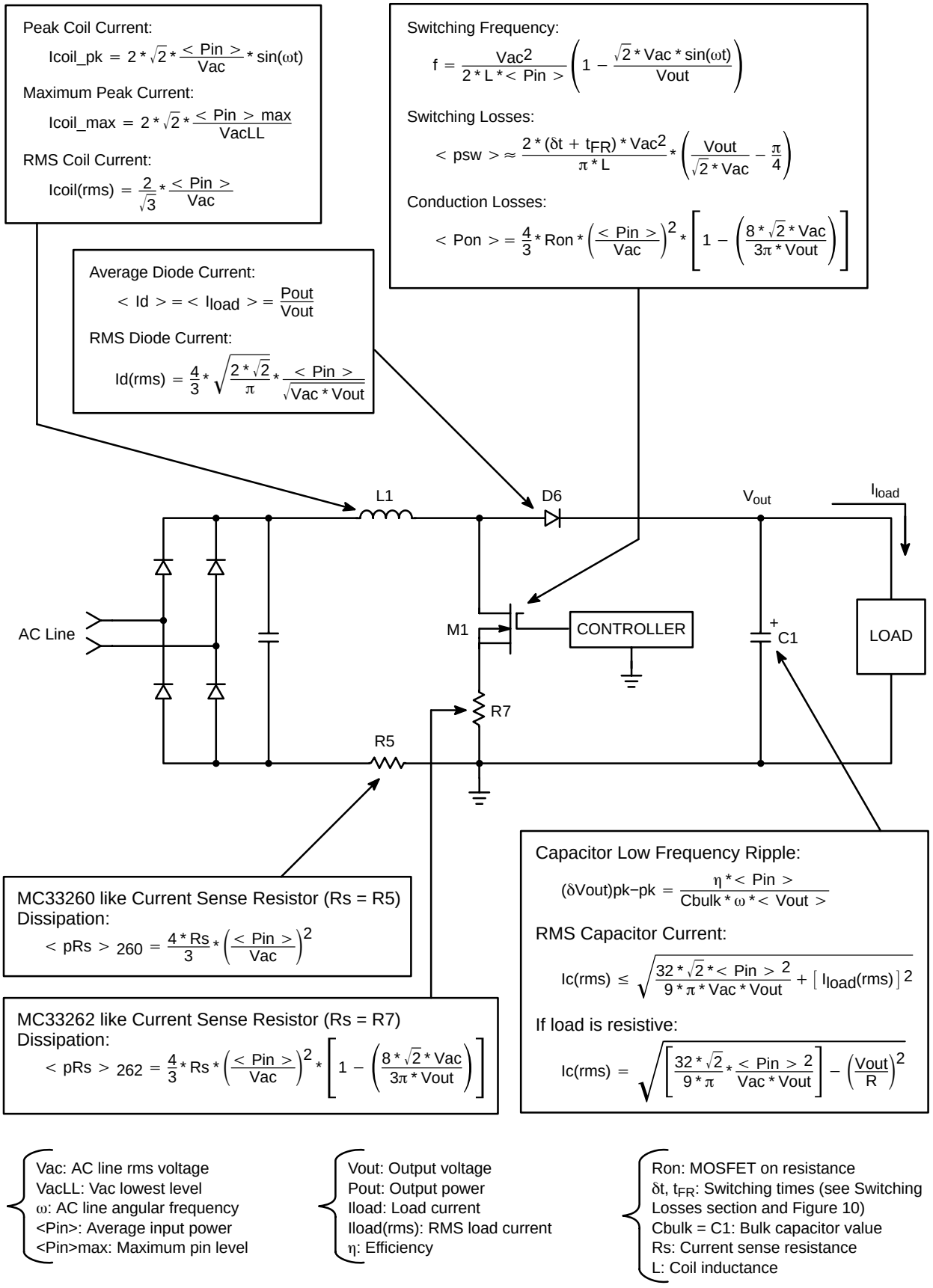

Figure 15. Summary

AND8124/D

90 W, Universal Input, Single Stage, PFC Converter

ON Semiconductor®

http://onsemi.com

General Description

This application note describes the implementation of a 90 W, universal input Flyback Power−Factor−Correction (PFC) converter using On Semiconductor's NCP1651 controller.

The NCP1651 enables a low cost single−stage (with a low voltage isolated output) PFC converter as demonstrated in this application circuit, which is designed for 48 Vdc, at 1.9 A of output current. The NCP1651 is designed to operate in the fixed frequency, continuous mode (CCM), or discontinuous (DCM) mode of operation, in a Flyback converter topology. The converter described in this application note has the following valuable features:

Features

- Wide Input Voltage Range (85 − 265 Vac)
- Galvanic Isolation
- Primary Side Cycle−by−Cycle and Average Current Limit
- Secondary Side Power Limiting
- High Voltage Start−up Circuit

Detailed Circuit Description

Operational description and design equations are contained in the NCP1651 Data Sheet. This application note addresses specific design issues related to this converter design. Please refer to Figure 2 for component reference designators.

Voltage Regulation Loop

With a Flyback topology, the output is isolated from the input by the power transformer. Output voltage regulation can be accomplished in two ways. The first, and the simplest method is by sensing the primary side voltage of the auxiliary winding. This eliminates the feedback isolation circuitry, at the expense of accuracy of voltage regulation and current sensing. The second method is to sense the secondary side voltage which is more complex, but provides better voltage regulation and transient response.

The NCP1651 demo board uses a quad operational amplifier on the secondary to perform multiple functions. One section of the amplifier is used as the error amplifier. A voltage divider comprised of R23, R24, R25 and R33 senses the output voltage and divides it down to 2.5 V. This signal is applied to the negative input of the error amplifier; the 2.5 V reference is applied to the non−inverting input of the error amplifier.

The output of the error amplifier provides a current sink that drives the LED of the optocoupler. The primary side optocoupler circuit sinks current from pin 8. This varies the voltage into the Voltage−to−Current converter that feeds the reference multiplier.

The loop operation is as follows: If the output voltage is less than its nominal value, the voltage at the output of the voltage divider (inverting input to the error amplifier) will be less than the reference signal at the non−inverting error amplifier input. This will cause the output of the error amplifier to increase. The increase in the output of the error amplifier will cause the optocoupler LED to conduct less current, which in turn will reduce the current in the optocoupler photo−transistor. This will increase the voltage at pin 8 of the chip, and in turn increase the output of the reference multiplier, causing an increase in the NCP1651 duty cycle.

The current shaping network is comprised of the ac error amplifier, buffer and current sense amplifier. This network will force the average input current to maintain a scaled replica of the current reference on pin 10. The increase of the reference voltage will cause the current shaping network to draw more input current, which translates into an increase in output current as it passes through the transformer. The increase in current will increase the output power and therefore, the output voltage. To calculate the loop stability, it is recommended that the On Semiconductor spread sheet be used. This is an easy and convenient way to check the gain and phase of the control loop.

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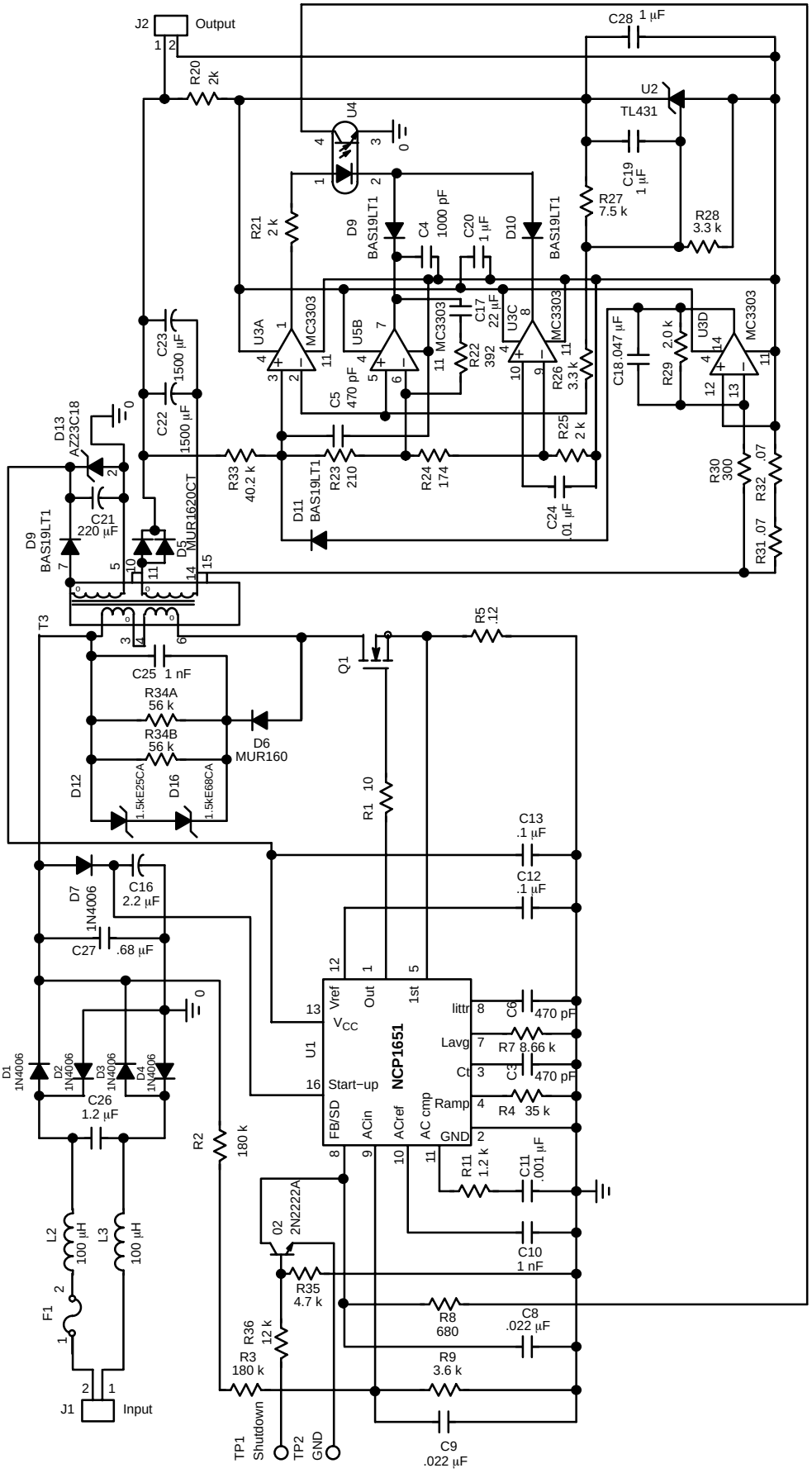

Figure 1. Applications Circuit Schematic

Overshoot/Undershoot Circuit

Two sections of the quad amplifier are used as comparators. One of these monitors the output for overvoltage condition and the other for undervoltage condition. The voltage divider requires four resistors (R33, R23, R24, and R25) in order to make the various ratios available for the two comparators as well as the error amplifier.

The undervoltage comparator provides the drive for the opto−coupler. Its output is normally in the saturated high state, which allows the flow of current into the opto−coupler to be determined by the error amplifier or overvoltage comparator. If an undervoltage condition occurs, the output of the UV comparator goes low, which reduces the drive current to the opto−coupler LED. This causes the NCP1651 to go into a high duty cycle state, and will increase the flow of current into the output until the output voltage is above the UV limit.

The over−voltage comparator's output is OR'ed with the output of the error amplifier. During an overvoltage event (e.g. a transient load dump), the output of this comparator will go to ground, and cause the maximum current to flow in the opto−coupler LED. This will pull pin 8 low and reduce the duty cycle to zero until the output voltage is below the OV limit. It should be noted that the purpose of the 680 Ω resistor (R8) in series with the opto−coupler photo transistor, is there to keep the voltage at pin 8 above the 0.5 V threshold during such events. This keeps the control chip operational and will allow immediate operation when the output voltage is again in its normal operating range. Without this resistor, the voltage on pin 8 would drop below 0.5 V, causing the NCP1651 to enter a low power shutdown mode of operation.

Current/Power Limit Circuit

The fourth section of the amplifier is biased as a differential amplifier. This section senses the DC output current, and provides a signal that is diode OR'ed into the feedback divider.

In the demo board the overload current limit was set to 125% of full load, or 2.375 A. Two resistors are used in series (to limit their maximum power dissipation) to sense the output current (R31 and R32). R29 and R30 set−the current sense amplifier gain.

Where the gain of the amplifier is:

$$G = (R29/R30) + 1 = 3000/300 + 1 = 11 \quad \text{(eq. 1)}$$

The voltage to the input of the differential amplifier is:

$$2.375\ A \cdot 0.14\ \Omega = 0.33\ V \quad \text{(eq. 2)}$$

The output voltage from the differential amplifier is:

$$V_O = 0.33 \cdot 11 = 3.63\ V \quad \text{(eq. 3)}$$

When the output load current increases, the output of the current sense amplifier will also increase. When the amplifiers output voltage, minus a diode drop (D11), increases above the 2.5 V, it pulls up the feedback signal at the inverting input of the error amplifier (when the loop is in regulation the inverting input voltage is typically 2.5 V). This causes the error amplifier signal to go low, sinking more current through the LED in the opto−coupler. This in turn drives more current in opto−coupler transistor collector, pulling it low reducing the duty cycle, folding back the output voltage.

Output Voltage Ripple

The output voltage ripple on the secondary of the transformer has two components, the traditional high frequency ripple associated with a flyback converter, and the low frequency ripple associated with the line frequency (50 Hz or 60 Hz). In this application our goal was to have the output ripple 5% of the nominal output voltage, or 2.4 V pk−pk.

The High Frequency Ripple can be Calculated by:

$$\Delta V = \sqrt{\Delta V_{cap}^2 + \Delta V_{esr}^2} \quad \text{(eq. 4)}$$

$$\Delta V_{cap} = i_{rms}\, dt / C_O \quad \text{(eq. 5)}$$

The RMS current at the peak of the sinewave (phase angle 90°).

$$i_{rms} = \sqrt{(t_{off} / T) \cdot (((I_{pk}^2 + (I_{pk}\, I_{ped}) + I_{ped}^2) / 3)) - (t_{off} / 4T) \cdot (I_{pk} + I_{ped})^2))} \quad \text{(eq. 6)}$$

$$i_{rms} = \sqrt{((3.85\ \mu / 10\ \mu)) \cdot (((13.38^2 + 13.38 \cdot 10.27 + 10.27^2) / 3) - 3.85\ \mu / 10\ \mu \cdot 4) \cdot (13.38 + 10.27)^2) = 5.78} \quad \text{(eq. 7)}$$

To meet the capacitors ripple current requirements and lower the equivalent esr, two 1500 μF capacitors were used in parallel.

$$\Delta V_{cap} = (5.78 \cdot 3.85\ \mu / 3000\ \mu) = 0.00742 \quad \text{(eq. 8)}$$

Where:

- n = Transformer Turns Ratio (3.89)
- Ipk = Peak Current Secondary (13.38)
- Iped = Pedestal Current Secondary (10.27)
- C_O = Output Capacitance (1500 μ each)
- esr = Output Capacitor Equivalent Series Resistance (0.03 Ω Each)
- T = Switching Interval

$$\Delta V_{esr} = I_{pksec} \cdot esr \quad \text{(eq. 9)}$$

$$\Delta V_{esr} = 13.38\ Apk \cdot 0.015 = 0.20\ V \quad \text{(eq. 10)}$$

$$\Delta V = \sqrt{0.00742^2 + 0.2^2 = 0.200} \quad \text{(eq. 11)}$$

The Low Frequency Portion of the Ripple:

$$\Delta V = I_{pk}\, \Delta t / C_O \quad \text{(eq. 12)}$$

$$I_{AVG} = P_O / V_O \quad \text{(eq. 13)}$$

$$I_{pk} = I_{AVG} / 0.637 \quad \text{(eq. 14)}$$

$$I_{pk} = P_O / V_O\ 0.637 = 90 / (48)(0.637) = 2.95 \quad \text{(eq. 15)}$$

If we divided the output ripple into 10° increments over one cycle (180°) the sinusoidal ripple voltage with respect to phase angle is:

$$\Delta V = \frac{(P_O / 0.637\ V_O) \cdot s_{in}(\theta)}{C_O \cdot 18 \cdot f_{line}} \quad \text{(eq. 16)}$$

In Figure 2, the low frequency output voltage ripple are plotted with respect to phase angle.

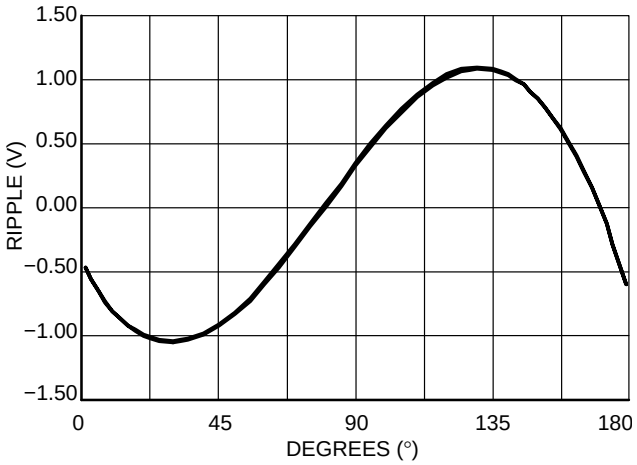

Figure 2. Calculated Output Ripple

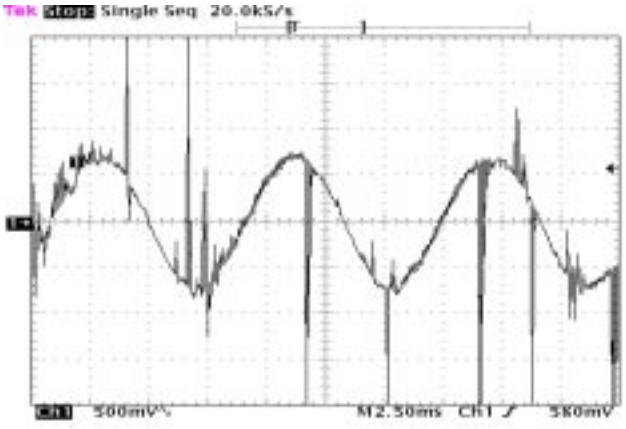

Figure 3. Measured Output Voltage Ripple

It can be seen from the calculations, and the scope waveform that as long as a capacitor with a low esr is used, that the output voltage ripple is dominated by the low frequency (120 Hz) ripple.

Hold−Up time

If the user would like to select C_O for Hold−Up time versus, voltage ripple:

$$P_{out} = \frac{1}{2}\ C_O\ V^2\ f \quad \text{(eq. 17)}$$

Rearranging the equation:

$$C_O = 2\ P_{out}\ th / V_{max}^2 - V_{min}^2 \quad \text{(eq. 18)}$$

th = One Cycle of the Line 16.67ms (60Hz)
V_{max} = 48 V
V_{min} = 36 V
P_{out} = 90 W

$$C_O = (2 \cdot 90 \cdot 16.67\ ms) / (48^2 - 36^2) = 3000\ \mu F \quad \text{(eq. 19)}$$

It is a coincidence that the output capacitor calculated for voltage ripple and hold−up time are the same value.

MOSFET Turn−off Snubber

The MOSFET in our design has a VDS rating of 800 V, the peak voltage across the device at turn−off (including the leakage inductance spike) is:

$$V_{pk}Total = V_{inmax}\ 1.414 + ((V_O + V_f)n) + V_{spike} \quad \text{(eq. 20)}$$

Where:
V_{inmax} =265 Vrms
V_O =the Output Voltage (48 V)
n =the Transformer Turns Ratio (4)
V_{spike} =Voltage Spike Due to Transformer Leakage Inductance

To provide a safe operating voltage for the MOSFET we have selected V_{spike} to be 130 V_{peak}, so when the MOSFET turns off, the maximum Drain to Source voltage is:

$$265 \cdot 1.414 + 48(4) + 130 = 697\ V \quad \text{(eq. 21)}$$

To minimize the effect of the leakage inductance spike, the coupling between the primary and secondary of the transformer needs to be as tight as possible. This can be accomplished, if your transformer requires a primary with multiple layers, by interleaving the primary and secondary windings. In our 48 Vdc application the transformer primary has 74 turns, and the secondary has 19 turns. The manufacture of the transformer, TDK, wound one layer of the primary with 45 turns, then the 19 turn secondary, and the remaining 29 turns of the primary. The results were a leakage inductance of approximately 9 μH. If we compare this to a transformer where the entire 74 turns were wound, in two layers, then the 19 turn secondary, the leakage inductance increased to 37 μH.

The energy stored in the transformer leakage:

$$E = \frac{1}{2} \cdot l_e \cdot I_{pk}^2 \quad \text{(eq. 22)}$$

Where:
l_e = Leakage Inductance (9 μH Measured)
I_{pk}= Peak Primary Current

A Second Relationship is:

$$E = \frac{1}{2} \cdot C \cdot V^2 \quad \text{(eq. 23)}$$

Where:
C= Snubber Capacitor
V= the Voltage Across the MOSFET

Combining Equations:

$$C = I_{pk}^2 \cdot I_e / ((V_O + V_f)n + V_{pk} + V_{spike})^2 - ((V_O + V_f)n + V_{pk})^2 \quad \text{(eq. 24)}$$

$$C_{snubber} = 3.8^2 \cdot 9\ \mu H / ((192 + 375 + 130)^2 - (192 + 375)^2 = 790\ pF \quad \text{(eq. 25)}$$

During the MOSFET turn−off, the capacitor C25 is charge through the Diode D6. Prior to the next ton switching cycle the capacitor C25 must be fully discharged, so $R_{snubber}$ is selected to be:

$$R_{snubber} = ((V_O + V_f)n + V_{inmax} \cdot 1.414 + V_{spike}) \quad 0.63\ \tau / (V_{spike} * C_{snubber}) \quad \text{(eq. 26)}$$

$$((192 + 375 + 130)0.63(6.5\ \mu) / (130 * 790\ pF) = 28\ k \quad \text{(eq. 27)}$$

The power in the snubber is:

$$P = \frac{1}{2} C V^2 \quad \text{(eq. 28)}$$

$$= (0.5)790\ pF(130^2)\ 100\ kHz = 0.68\ W$$

After installing the snubber in the NCP1651 Demo Board, and measuring the voltage spike, the snubber components where adjusted for maximum performance, C25 was increased to 1000 pF, and R34 was changed to 30 kΩ. The difference between the measured and calculated value can be attributed to the PWB board layout, and other parasitic components.

Evaluation Board Test Results

The results from the NCP1651 Demo Board show that using a flyback topology for a PFC converter can provide a low input Total Harmonic Distortion (THD), a high input power factor, and excellent steady state output voltage regulation.

The NCP1651 achieved a THD at 115 Vac input at full load of 3.12% with a PF of 0.998. The input THD to 6.8% THD at 230 Vac in, with a PF of 0.971.

The steady state output voltage regulation from 85 Vac to 230 Vac, and no load to full load is less than 0.02%, with an output voltage ripple meeting our design goal of 2.4 Vpk−pk, measured 2.0 V pk−pk.

Transient Response

Figures 4 through 7 show the output transient response for the 90 W converter. The test conditions for each Figure are listed below:

Table 1. Test Conditions

	V_{in}	ΔI_O
Figure 4	115 Vac	0.19 – 1.92 A
Figure 5	115 Vac	1.92 – 0.19 A
Figure 6	230 Vac	0.19 – 1.92 A
Figure 7	230 Vac	1.92 – 0.19 A

In Figure 4, the output voltage drops to 40 Vdc, and recovers in less than 160 ms. In Figure 6 the input voltage was increased to 230 Vac, and the load was switched from 10% to 100% load. The output voltage now drops only to 44 Vdc, and recovers in approximately 50 ms. The significant improvement in transient response performance is attributed to an increase in the DC gain and loop bandwidth at high line. As the input ac line voltage increases the control loop DC gain (Refer to www.onsemi.com for a copy of the excel design spreadsheet for details) increases from 42 dB at 115 Vac to 62 dB at 230 Vac and the control loop bandwidth increases from 2 Hz to 8 Hz. The result is that at high line, there is an improvement in transient response, but because there is less attenuation of the output 120 Hz ripple, it results in an increase in the input Total Harmonic Distortion (THD). The system designers will need to trade off their overall system performance THD, Power Factor, and transient response to optimize the control loop to meet their requirements.

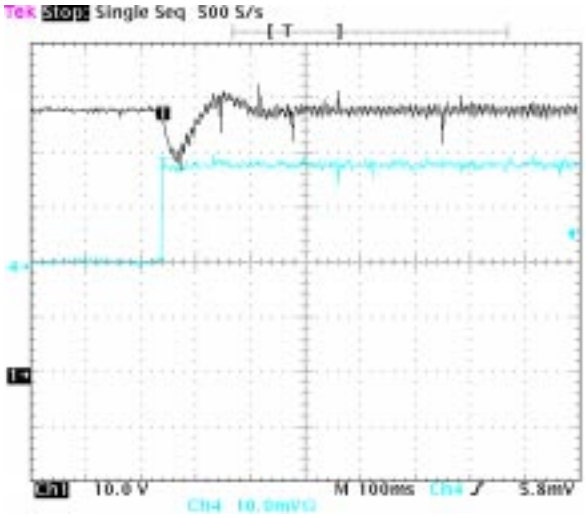

Figure 4.

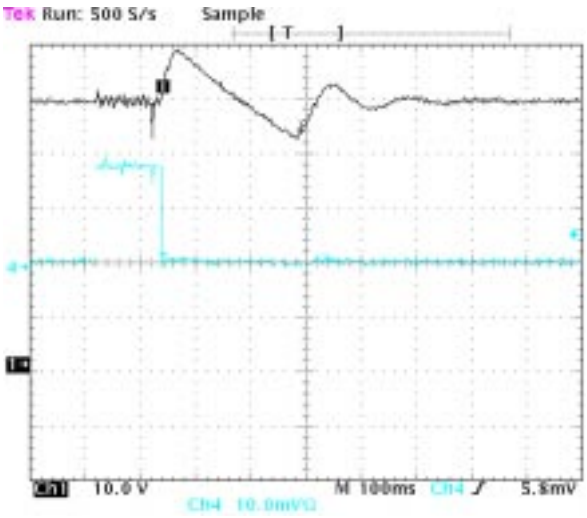

Figure 5.

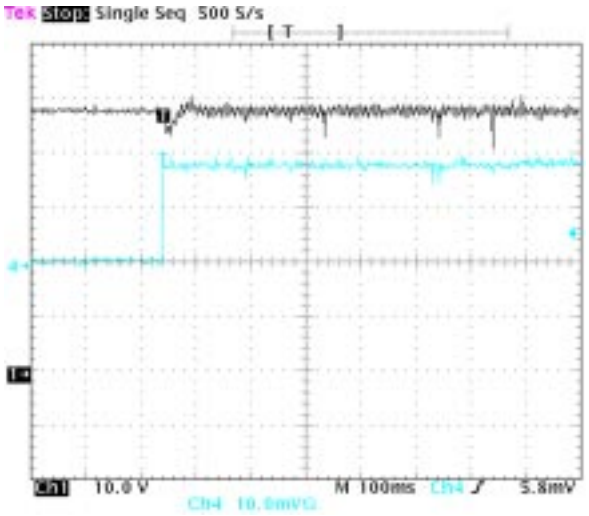

Figure 6.

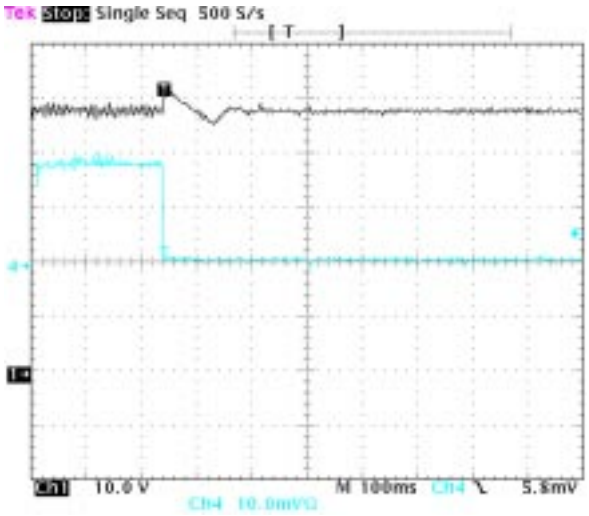

Figure 7.

Power Dissipation Estimates

The NCP1651 Demo Board power dissipation (measured) at 115 Vrms, full load, is (106.27 – 47.95 •1.92) = 14.21 W. Following table provides the calculated and estimated power loss spread among different power train components.

Components		Pd average
D1−D4	Input Rectifier	1.65 W
Q1	MOSFET	4.1 W
D5	Output rectifier	1.7 W
T3	Flyback transformer	3.5 W (estimate)
R34	Snubber resistor	0.84 W
D12	Transient suppressor	2.0 W
	miscellaneous	0.41 W
Total		14.20 W

Demo Board Operating Instructions

Connect an Ac source, 85 − 265 Vac, 47 − 64 Hz to the input terminals J1. Connect a load to the output terminals J2, the PWB is market +, for the positive output, − for the return. Turn on the ac source, and the NCP1651 will automatically start, providing 48 Vdc to the load.

Shutdown Circuit

The shutdown circuit will inhibit the operation of the power converter and put the NCP1651 into a low power shutdown mode. To activate this circuit, apply 5 V to the red test point, with the black jack being “ground”. Be aware that the black jack is actually hot as it is connected to the output of the input bridge rectifiers. An isolated 5 V supply should be used.

If this circuit is not being used, it can be left open as there is enough resistance built in to the circuit to keep the transistor (Q2) in it’s off state.

Table 2. Performance Data Regulation

Line/Load	No Load	45 W	90 W
85 Vrms	47.94	47.95	47.95
115 Vrm	47.94	47.95	47.95
230 Vrms	47.94	47.95	47.95
265 Vrms	47.94	47.94	47.95

Table 3. Harmonics & Distortion

	115 Vac 90 W		230 Vac 90 W	
	V harmon	**A harm. %**	**V harm**	**A harm%**
2nd	0.143	0.156	0.08	0.2
3rd	0.203	1.94	0.25	4.74
5th	0.13	0.6	0.12	2.88
7th	0.08	0.28	0.07	0.22
9th	0.04	0.19	0.09	0.76
11th	0.08	0.29	0.08	0.27
13th	0.16	0.32	0.06	0.33
15th	0.28	0.41	0.14	0.68
17th	0.4	0.41	0.28	0.95
19th	0.05	0.29	0.12	0.3
PF		0.998		0.971
THD(A)		3.12		6.8
Ifund		0.918		0.468

Table 4. Efficiency

	85 Vrms	**115 Vrms**	**230 Vrms**	**265 Vrms**
Pin @ No Load	1.5	1.52	1.51	1.59
Pin	109.42	106.27	105.35	105.25
Vo	47.95	47.95	47.95	47.95
Io	1.92	1.92	1.92	1.92
Efficiency	0.841	0.866	0.874	0.875

Table 5. Vendor Contact List

Vendor	**U. S. Phone / Internet**
ON Semiconductor	1−800−282−9855 www.onsemi.com/
TDK	1−847−803−6100 www.component.tdk.com/
Vishay	www.vishay.com/
Bussman (Cooper Ind.)	1−888−414−2645 www.cooperet.com/
Coiltronics (Cooper Ind.)	1−888−414−2645 www.cooperet.com/
Fairchild	www.fairchildsemi.com/
Panasonic	www.eddieray.com/panasonic/
Weidmuller	www.weidmuller.com/
Keystone	1−800−221−5510 www.keyelco.com/
HH Smith	1−888−847−6484 www.hhsmith.com/
Aavid Thermalloy	www.aavid.com/

Table 6. NCP1651 Application Circuit Parts List (Specifications:, 90 W, 85 vac to 265 vac Input Range, 48 V Output)

Ref Des	Description	Part Number	Manufacturer
C1	Cap, Ceramic, Chip, 1000 pF, 50 V	VJ0603Y102KXAAT	VISHAY
C3	Cap, Ceramic, Chip, 470 pF, 50 V	VJ0603Y471JXAAT	VISHAY
C5	Cap, Ceramic, Chip, 470 pF, 50 V	VJ0603Y471JXAAT	VISHAY
C6	Cap, Ceramic, Chip, 470 pF, 50 V	VJ0603Y471JXAAT	VISHAY
C8	Cap, Ceramic, Chip, .022 μF, 50 V	VJ0603Y223KXXAT	VISHAY
C9	Cap, Ceramic, Chip, 0.022 μF, 50 V	VJ0603Y223KXXAT	VISHAY
C10, C11	Cap, Ceramic, chip, 0.001 μF, 50 V	VJ0603Y102KXAAT	VISHAY
C12, C13	Cap, Ceramic, Chip, 0.1 μF, 50 V	VJ0606Y104KXXAT	VISHAY
C16	2.2 μF, alum elect, 450 V (0.394dia x 0.492H) (.394dia x .492H)	ECA−2WHG2R2 EKA00DC122P00	Panasonic (Digi – P5873) Vishay Sprague (20)
C17	Cap, Ceramic, Chip, 22 μF, 10 V	C3225X5R0J226MT	TDK
C18	Cap, Ceramic, Chip, .047 μF, 50 V	VJ0603Y473KXXAT	VISHAY
C19	Cap, Ceramic, Chip, .01 μF, 50 V	VJ0603Y103KXAAT	VJ0603Y103KXAAT
C20	Cap, Ceramic, Chip, 1 μF, 25 V	C3216X7R1E105KT	TDK
C21	220 μF, alum elect, 25 V	ECA1EM331	Panasonic
C22, 23	1800 μF, alum elect, 63 V (2.2A rms min) 1500 μF, alum elect, 63 V	EEU−FC1J182 EKB00JL415J00	Panasonic (Digi – P11283) Vishay Sprague (20)
C24	Cap, Ceramic, Chip, .01 μF, 50 V	VJ0603Y103KXAAT	VISHAY
C25	Cap,Ceramic, .001 μF, 1 KV	ECK−03A102KBP	Panasonic
C26	1.2 μF, 275 vac, X cap	F1778−512K2KCT0	VISHAY
C27	Cap, polypropylene, .68 uF, 400 VDC	MKP1841−468−405	Vishey − Sprague
C28	Cap, Ceramic, Chip, 1 μF, 25 V	VJ1206V105ZXXAT	VISHAY
D1 – D4	Diode, Rectifier, 800 V, 1 A	1N4006	ON Semiconductor
D5	Diode, Ultrafast, 200 V, 16 A	MUR1620CT	ON Semiconductor
D6	Diode, Ultrafast, 600 V, 1 A	MUR160	ON Semiconductor
D7	Diode, Rectifier, 800 V, 1 A	1N4006	ON Semiconductor
D8 – D11	Diode, Switching, 120 V, 200 mA, SOT−23	BAS19LT1	ON Semiconductor
D12	TVS, 214 V, 5 W	1.5KE250A	ON Semiconductor
D13	Zener Diode, 18 V	AZ23C18	VISHAY
D16	Zener Diode, 68 V	1.5kE68CA	ON Semiconductor
F1	Fuse, 2 A, 250 Vac	1025TD2A	Bussman
L2	2.5 A sat, 100 μH inductor, diff mode	TSL1315−101K2R5	TDK
L3	2.5 A sat, 100 μH inductor, diff mode	TSL1315−101K2R5	TDK
Q1	FET, 11 a, 800 V, .45 Ω, N−channel	SPA11N80C3	Infineon
Q2	Bipolar, npn, 30 V, SOT−23	MMBT2222ALT1	ON Semiconductor
R1	Resistor, SMT1206, 10	CRCW1206100JRE4	Vishey
R2	Resistor, Axial Lead, 180k, ¼ W	CMF−55−180K00FKRE	Vishey
R3	Resistor, Axial Lead, 180k, ¼ W	CMF−55−180K00FKRE	Vishey
R4	Resistor, SMT1206, 35k	CRCW120635KOJNTA	Vishey
R5	Resistor, SMT, 0.12 Ω, 1 W	WSL2512 .12Ω 1%	Vishey Dale
R7	Resistor, SMT1206, 8.66 k	CRCW12068661F	Vishey
R8	Resistor, SMT1206, 680	CRCW12066800F	Vishey

Table 6. NCP1651 Application Circuit Parts List (Specifications:, 90 W, 85 vac to 265 vac Input Range, 48 V Output)

Ref Des	Description	Part Number	Manufacturer
R9	Resistor, axial lead, 3.6k, ¼ W	CMF−55−3K600FKBF	Vishey
R11	Resistor, SMT1206, 1.2k	CRC12061K20JNTA	Vishey
R20	Resistor, SMT1206, 2.0k	CRC12062K00JNTA	Vishey
R21	Resistor, SMT1206, 2.0k	CRC12062K00JNTA	Vishey
R22	Resistor, SMT1206, 392	CRC12052K10JNTA	Vishey
R23	Resistor, SMT1206, 210, 1%	CRCW12062100F	Vishey
R24	Resistor, SMT1206, 174, 1%	CRCW12061740F	Vishey
R25	Resistor, SMT1206, 2.05k, 1%	CRCW12062051F	Vishey
R26	Resistor, SMT1206, 3.3k	CRC12063K30JNTA	Vishey
R27	Resistor, SMT1206, 7.5k	CRC12067K50JNTA	Vishey
R28	Resistor, SMT1206, 3.3k	CRC12063K30JNTA	Vishey
R29	Resistor, SMT1206, 3.01k, 1%	CRCW12063011F	Vishey
R30	Resistor, SMT1206, 301, 1%	CRCW12063010F	Vishey
R31	1w, .07 Ω resistor	WSL251R0700FTB	Vishey
R32	1w, .07 Ω resistor	WSL251R0700FTB	Vishey
R33	Resistor, SMT1206, 40.2k, 1%	CRCW120640022F	Vishey
R34	Resistor, axial lead, 20k, 2W		
R35	Resistor, SMT1206, 4.7k	CRCW12064K70NTA	Vishey
R36	Resistor, SMT1206, 12k	CRCW120612K0JNTA	Vishey
R37	Resistor, SMT1206, 100k	CRCR1206100K0JNTA	Vishey
T1	Transformer, Flyback (Lp 1 mH)	SRW42EC−U04H14	TDK
U1	PFC Controller	NCP1651	ON Semiconductor
U2	2.5 V programmable ref, SOIC	TL431ACD	ON Semiconductor
U3	Quad Op A	MC3303D	ON Semiconductor
U4	Optocoupler, 1:1 CTR, 4 pin	SFH615AA−X007	Vishay
Hardware			
H1	Printed Circuit Board		
H2	Connector	171602	Weidmuller (Digi 281−1435−ND)
H3	Connector	171602	Weidmuller (Digi 281−1435−ND)
H4	Standoff, 4−40, alum, hex, .500 inches	8403	HH Smith (Newark 67F4111)
H5	Standoff, 4−40, alum, hex, .500 inches	8403	HH Smith (Newark 67F4111)
H6	Standoff, 4−40, alum, hex, .500 inches	8403	HH Smith (Newark 67F4111)
H7	Standoff, 4−40, alum, hex, .500 inches	8403	HH Smith (Newark 67F4111)
H8	Heatsink, TO−220	590302B03600	Aavid Thermalloy
H9	Heatsink, TO−220	590302B03600	Aavid Thermalloy
H10	Test point, red	5005	Keystone (Digi 5005K−ND)
H11	Test point, black	5006	Keystone (Digi 5006K−ND)
H12	Shoulder Washer	3049K−ND	Digi−Key
H13	Insulator	4672	Keystone

An Innovative Approach to Achieving Single Stage PFC and Step-Down Conversion for Distributive Systems

Prepared by: Terry Allinder
ON Semiconductor
Sr. Application Engineer

ON Semiconductor®
http://onsemi.com

APPLICATION NOTE

INTRODUCTION

In most modern PFC circuits, to lower the input current harmonics and improve the input power factor, designers have historically used a boost topology. The boost topology can operate in the Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), or Critical Conduction Mode.

Most PFC applications using the boost topology are designed to operate over the universal input AC voltage range (85−265 Vac), at 50 or 60 Hz, and provide a regulated DC bus (typically 400 Vdc). In most applications, the load can not operate from the high voltage DC bus, so a DC−DC converter is used to provide isolation between the AC source and load, and provide a low voltage output. The advantages to this system configuration are low Total Harmonic Distortion (THD), a power factor close to unity, excellent voltage regulation, and fast transient response on the isolated DC output. The major disadvantage of the boost topology is that two power stages are required which lowers the systems efficiency, increases component count, cost, and increases the size of the power supply.

ON Semiconductor's NCP1651 (www.onsemi.com) offers a unique alternative for Power Factor Correction designs, where the NCP1651 has been designed to control a PFC circuit operating in a flyback topology. There are several major advantages to using the flyback topology. First, the user can create a low voltage isolated secondary output, with a single power stage, and still achieve a low input current distortion, and a power factor close to unity. A second advantage, compared to the boost topology with a DC−DC converter, is a lower component count which reduces the size and the cost of the power supply.

Traditionally, the flyback approach has been ignored for PFC applications because of the perceived limitations such as high peak currents and high switch voltage ratings. This paper will demonstrate the novel control approach incorporated in the NCP1651 design, coupled with advances in discrete semiconductor technology that have made the flyback approach very feasible for a range of applications.

Controller Analysis

The NCP1651 can operate in either the Continuous or Discontinuous mode of operation. The following analysis will help to highlight the advantages of Continuous versus Discontinuous mode of operation.

The table below defines a set of conditions from which the comparison will be made between the two modes of operation.

Table 1.

Po = 90 W
Vin = 85−265 Vrms (analyzed at 85 Vrms input)
Efficiency = 80%
Pin = 108 W
Vo = 48 Vdc
Freq = 100 kHz
Transformer turns ratio n = 4

Continuous Mode (CCM)

To force the inductor current to be continuous over the majority of the input voltage range (85−265 Vac) the primary inductance, Lp needs to be at least 1.0 mH. Figure 1 shows the typical current through the primary winding of the flyback transformer. During the switch on period, this current flows in the primary and during the switch off−time, it flows in the secondary.

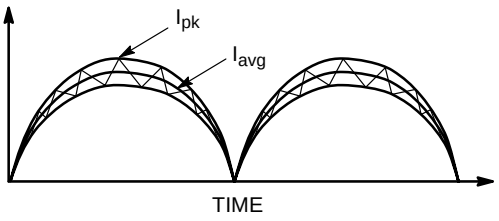

Figure 1.

Therefore, the peak current can be calculated as follows:

$$I_{pk} = I_{avg} + \frac{(1.414 \cdot V_{in} \sin \theta \cdot t_{on} \cdot 2)}{L_p} \quad \text{(eq. 1)}$$

where:

$$I_{avg} = \frac{1.414 \cdot P_{in}}{V_{in} \sin \theta} \quad \text{(eq. 2)}$$

$$T_{on} = T/(((\frac{N_S}{N_P}) \cdot (\frac{1.414 \cdot V_{in} \sin \theta}{V_O})) + 1) \quad \text{(eq. 3)}$$

For the selected operating condition:

$$T_{on} = 6.15\ \mu s \quad \text{(eq. 4)}$$

$$I_{pk} = \frac{1.414 \cdot 113}{85 \sin \theta} + \frac{1.414 \cdot 85 \cdot 6.15 \cdot 2}{1} = 3.35\ A \quad \text{(eq. 5)}$$

The analysis of the converter shows that the peak current operating in the CCM is 3.35 A.

Discontinuous Mode (DCM)

In the discontinuous mode of operation, the inductor current falls to zero prior to the end of the switching period as shown in Figure 2.

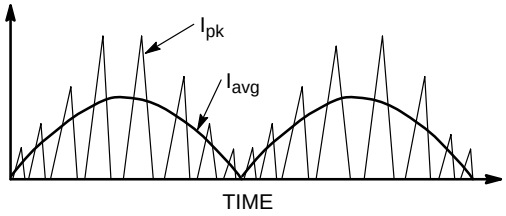

Figure 2.

To ensure DCM, Lp needs to be reduced to approximately 100 μH.

$$I_{pk} = \frac{V_{in} \sin \theta \cdot 1.414 \cdot t_{on}}{L_p} \quad \text{(eq. 6)}$$

$$I_{pk} = \frac{1.414 \cdot 85 \sin 90 \cdot 5.18}{100} = 6.23\ A$$

The results show that the peak current for a flyback converter operating in the Continuous Conduction Mode is about one half the peak current of a flyback converter operating in the Discontinuous Conduction Mode.

The lower peak current as a result of operating in the CCM lowers the conduction losses in the flyback MOSFET.

Current Harmonics Analysis

A second result of running in DCM can be higher input current distortion, Electromagnetic Interference (EMI), and a lower Power Factor, in comparison to CCM. While the higher peak current can be filtered to produce the same performance result, it will require a larger input filter.

A simple Fast Fourier Transform (FFT) was run in (ORCAD) Spice to provide a comparison between the harmonic current levels for CCM and DCM. The harmonic current levels will affect the size of the input EMI filter which in some applications are required to meet the levels of IEC1000−3−2. In the SPICE FFT model, no front end filtering was added so the result of the analysis could be compared directly.

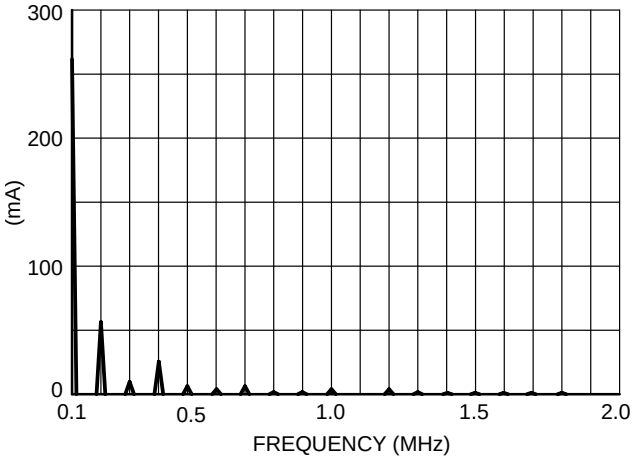

Figure 3. Continuous Conduction Mode FFT

Referring to Figure 3**,** at the 100 kHz switching frequency, the FFT is 260 mA, and the 2nd harmonic (200 kHz) is 55 mA.

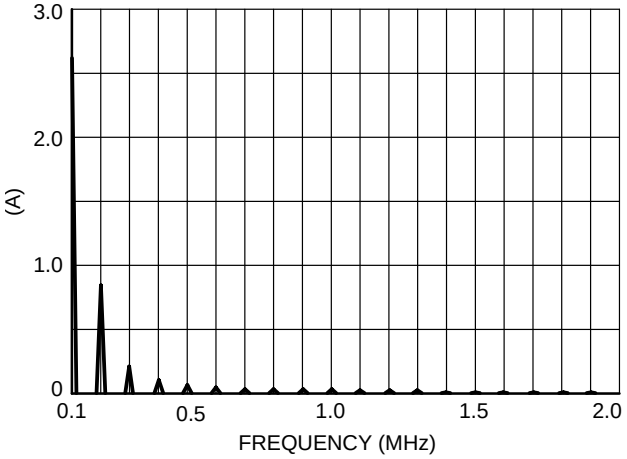

Figure 4. Discontinuous Conduction Mode FFT

Refer to Figure 4, at 100 kHz the FFT is 2.8 A, and the second harmonic (200 kHz) is 700 mA.

Results

From the result of our analysis it is apparent that a flyback PFC converter operating in CCM has half the peak current, and one tenth the fundamental (100 kHz) harmonic current compared to a flyback PFC converter operating in DCM. The results are lower conduction losses in the MOSFET and secondary rectifying diode, and a smaller input EMI filter. On the negative side to CCM operation, the flyback transformer will be larger because of the required higher primary inductance, and the leakage inductance will be higher affecting efficiency because of the leakage inductance energy that must be absorbed during the controller off time.

Some of the advantages to operating in DCM include lower switching losses because the current falls to zero prior to the next switching cycle, a smaller transformer, and in general the smaller transformer should result in a lower leakage inductance and less energy to be absorbed in the snubber.

Transformer Turn Ratio

The flyback transformer turns ratio affects several operating parameters, the secondary side peak current and the MOSFET drain to source voltage (VDS) during the controller off time, refer to Figure 8 for the application schematic.

The peak secondary current is:

Ipk prim • n

Where n is the transformer turns ratio, in our application n = 4.

Using the analysis for CCM versus DCM, the peak secondary current is:

CCM = 3.34 • 4 = 13.4 Apk

DCM = 6.23 • 4 = 24.9 Apk

It's clear from the analysis that the higher the turns ratio, there is a higher corresponding secondary side peak current resulting in higher conduction losses in the output rectifier.

A second effect of the turns ratio is the MOSFET VDS. The MOSFET VDS during the off time is:

$V_{pk} = V_{in}$ max • 1.414 + $(V_o + V_f)$ n + V_{spike}

where:

V_{in} max = 265 Vrms

V_o = the output voltage

V_f = the forward voltage drop across the output diode

V_{spike} = The voltage spike due to the transformer leakage inductance

The turns ratio in this equation determines the output voltage reflected back to the primary, $(V_o + V_f)n$.

A second effect of the turns ratio is the transformer leakage inductance, which effects Vspike. The leakage inductance is related to the coupling between the primary and the secondary of the transformer. As the turns ratio increase, there are more turns on the transformer, and unless the designer is careful in their core geometry selection and winding technique, the result will be a higher leakage inductance.

To minimize leakage inductance, a core with a wide winding window should be used; this will reduce the number of primary and secondary layers. In addition, interleaving the primary and secondary winding will increase the coupling. An example will help to illustrate the point. In our application the transformer required 74 primary turns (two layers) and 19 secondary turns (a single layer). The manufacturer of the transformer wound 45 primary turns, then the 19 turn secondary, and then the remaining 29 primary turns. The result was a measured leakage inductance of 9.0 μH.

A second transformer was wound with the entire 74 primary turns (two layers), then the 19 turn secondary, the measured leakage inductance increased to 37 μH. The reason for the increased leakage inductance was poor coupling between the primary and secondary.

Once the leakage inductance is reduced, verify that the voltage spike at turn off (Vspike) will not exceed your MOSFET VDS.

The MOSFET in our application has a VDS rating of 800 V, to provide a safety margin of at least 100 V VDS under worst case conditions:

Vspike:

$V_{spike} = VDS - V_{margin} - V_{in}$ max • 1.414 − $(V_o + V_f)$

800 − 100 − 265 • 1.414 − (48 + 0.7) 4 = 130 V

In our application the snubber circuit was designed to limit the VDS of the MOSFET to 130 Vpk. Refer to Figure 5 for the VDS waveform. The energy stored in the transformer leakage inductance is:

E = _ le I_{pk}_

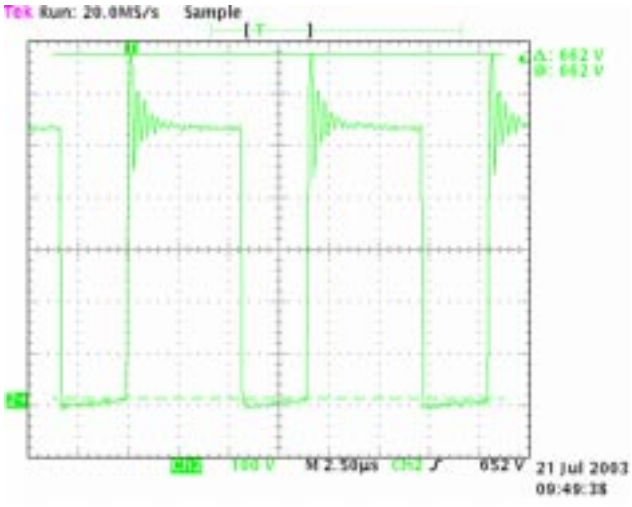

Figure 5.

The above analysis and examples illustrate the effects of the transformer turns ratio on the secondary side peak currents in the PFC and the MOSFET VDS at turn off. Careful attention should be taken when trading off turns ratio, primary inductance and duty cycle.

Output Voltage Ripple

A second consideration when using a flyback topology for PFC is that the output voltage ripple contains (on the secondary of the transformer) two components, the traditional high frequency ripple associated with a flyback converter, and the rectified line frequency ripple (100 or 120 Hz).

The high frequency ripple can be calculated by:

$$\Delta V = \sqrt{\Delta V_{cap}^2 + V_{esr}^2} \quad \text{(eq. 7)}$$

$$\Delta V_{cap} = \frac{Io_{avg} \cdot d_t}{C_o} \qquad Io_{avg} = \frac{I_p + I_{ped}}{2} \quad \text{(eq. 8)}$$

$$\Delta V_{esr} = I_{pk} \cdot esr \qquad \Delta V_{esr} = 13.38 \cdot 0.015 = 0.20\ V \quad \text{(eq. 9)}$$

where:

n = transformer turns ratio

I_{pk} = peak current (secondary) (13.38 Apk)

I_{ped} = pedestal of the secondary current (10.5 Apk)

C_o = output capacitance (3000 μ total)

esr = output capacitor equivalent series resistance (0.015_)

$d_t = T_{off}$ (3.92 μ)

$$\Delta V = \frac{\frac{13.38 + 10.5}{2}}{3000} \cdot 3.92 \qquad \text{(eq. 10)}$$

$$\_V = 0.0156\ V$$

Solving eq. 7 the high frequency ripple component on the output is:

$$\Delta V = \sqrt{0.0156^2 + 0.20^2} = 0.20\ V \quad \text{(eq. 11)}$$

The low frequency portion of the ripple:

$$\Delta V = \frac{I_{pk} \cdot d_t}{C_o} \qquad I_{avg} = \frac{P_o}{V_o} \qquad I_{pk} = \frac{I_{avg}}{0.637} \quad \text{(eq. 12)}$$

$$I_{pk} = \frac{90}{48 \cdot 0.637} = 2.95\ A$$

If the output voltage ripple is divided into 10° increments over one cycle (180°) the sinusoidal ripple voltage with respect to phase angle is:

$$\Delta V = \frac{P_o}{\frac{0.637 \cdot V_o \sin\ \theta}{C_o \cdot 18 \cdot fline}} \quad \text{(eq. 13)}$$

To calculate the total output voltage ripple:

Vripple total = eq. 7 + eq. 13.

$$\Delta V_{ripple\ total} = \sqrt{\Delta V_{cap}^2 + \Delta V_{esr}^2} + \frac{P_o}{\frac{0.637 \cdot V_o \sin\ \theta}{C_o \cdot 18 \cdot fline}} \quad \text{(eq. 14)}$$

In Figure 6, the output voltage ripple as a function of phase angle is plotted. The results show that as long as a capacitor(s) with low esr are used, that the output voltage ripple will be dominated by the low frequency ripple (100 Hz or 120 Hz).

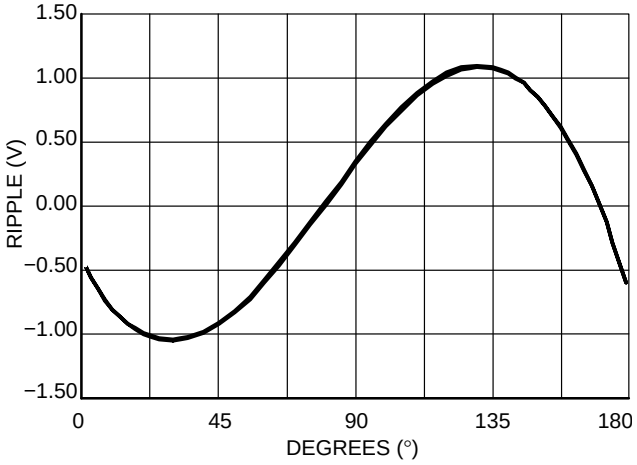

Figure 6. Output Ripple Envelope

Hold−Up Time

If the secondary output voltage is used for a distributed bus, the designer may elect to size the output capacitor for hold−up times, versus ripple. If so the output capacitors can be calculated by:

$$C_o = \frac{2 \cdot P_o \cdot th}{V_{nom}^2 + V_{min}^2} \quad \text{(eq. 15)}$$

where:

P_{out} = the maximum output power

th = the required hold−up time (we selected one cycle of the line 60 Hz, 16.67 ms)

V_{nom} = the nominal 48 Vdc output

V_{min} = 36 Vdc

$$C_o = \frac{2 \cdot 90 \cdot 16.67}{48^2 - 36^2} = 3000\ \mu F \quad \text{(eq. 16)}$$

In the above calculations for output voltage ripple and hold−up time, it is a coincidence that the same value of output capacitance was selected in both cases.

NCP1651 Features

The NCP1651 internally provides all of the necessary features that are typically seen in a PFC controller, plus some features not normally found. For example the NCP1651 has a high voltage start−up circuit, which allows the designer to connect pin 16 of the NCP1651 directly to the high voltage DC bus, eliminating bulky and expensive start−up circuitry.

After power is applied to the circuit, a high voltage FET is biased as a current source to provide current for start−up power. The high voltage start−up circuit is enabled and current is drawn from the rectified AC line to charge the V_{CC} cap. When the voltage on the V_{CC} cap reaches the turn on point for the UVLO circuit (10.8 V nominally), the start−up circuit is disabled, and the PWM circuit is enabled. With the NCP1651 enabled the bias current increases from its

standby level to the operational level. A divide−by−eight counter is preset to the count of 7, so that on start−up the chip will not be operational on the first cycle. The second V_{CC} cycle the counter is advanced to 8, and the chip will be allowed to start at this time. Refer to Figure 7.

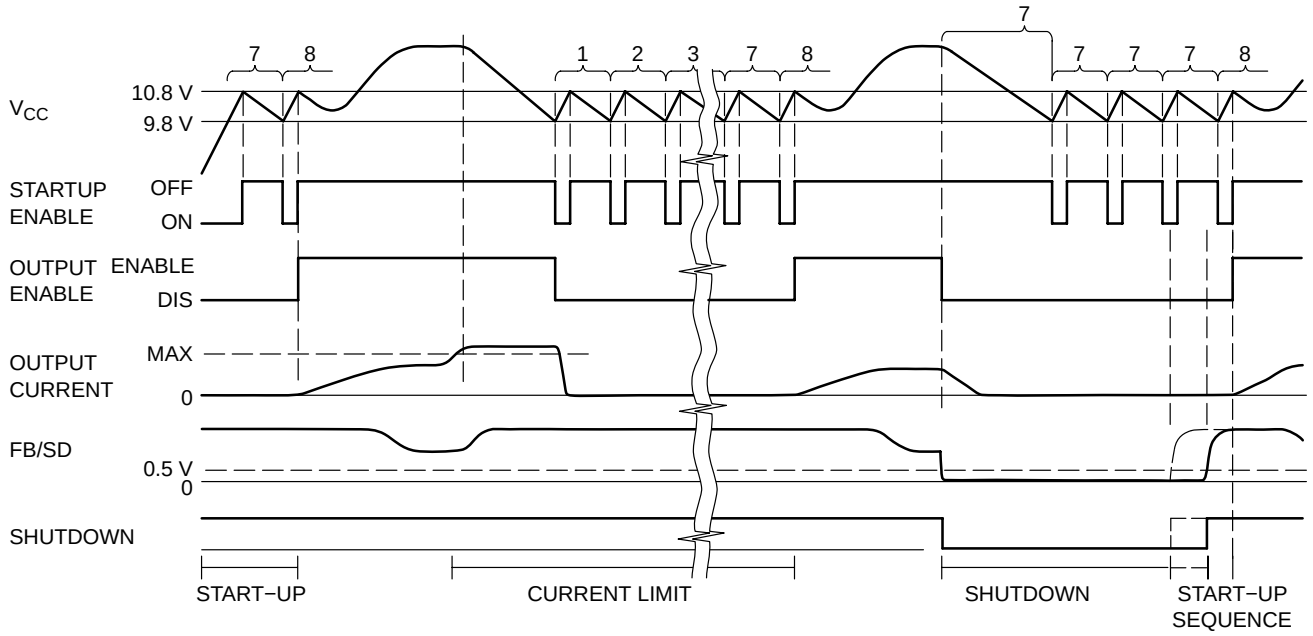

Figure 7.

In addition to providing the initial charge on the V_{CC} capacitor, the start circuit also serves as a timer for the start−up, overcurrent, and shutdown modes of operation. Due to the nature of this circuit, this chip must be biased using the start−up circuit and an auxiliary winding on the power transformer. Attempting to operate this chip off of a fixed voltage supply will not allow the chip to start.

In the shutdown mode, the V_{CC} cycle is held in the 7 count state until the shutdown signal is removed. This allows for a repeatable, fast restart. See Figure 6 for the timing diagram**.**

The unit will remain operational as long as the V_{CC} voltage remains above the UVLO under voltage trip point. If the V_{CC} voltage is reduced to the under voltage trip point, operation of the unit will be disabled, the start−up circuit will again be enabled, and will charge the V_{CC} capacitor up to the turn on voltage level. At this point the start−up circuit will turn off and the unit will remain in the shutdown mode. This will continue for the next seven cycles. On the eighth cycle, the NPC1651 will again become operational. If the V_{CC} voltage remains above the undervoltage trip point the unit will continue to operate, if not the unit will begin another divide−by−eight cycle.

The purpose of the divide−by−eight counter is to reduce the power dissipation of the chip under overload conditions and allow it to recycle indefinitely without overheating the chip.

It is critical that the output voltage reaches a level that allows the auxiliary voltage to remain above the UVLO turn−off level before the V_{CC} cap has discharged to 9.8 V level. If the bias voltage generated by the inductor winding fails to exceed the shutdown voltage before the capacitor reduces to the UVLO under voltage turn−off level, the unit will shut down and go into a divide−by−eight cycle, and will never start. If this occurs, the V_{CC} capacitor value should be increased.

CONCLUSION

It will ultimately be up to the designer to perform a trade−off study to determine which topology, Boost versus flyback, Continuous versus Discontinuous Mode of operation will meet all the system performance requirements. But the recent introduction of the NCP1651 allows the system designer an additional option yielding a less expensive, smaller solution.

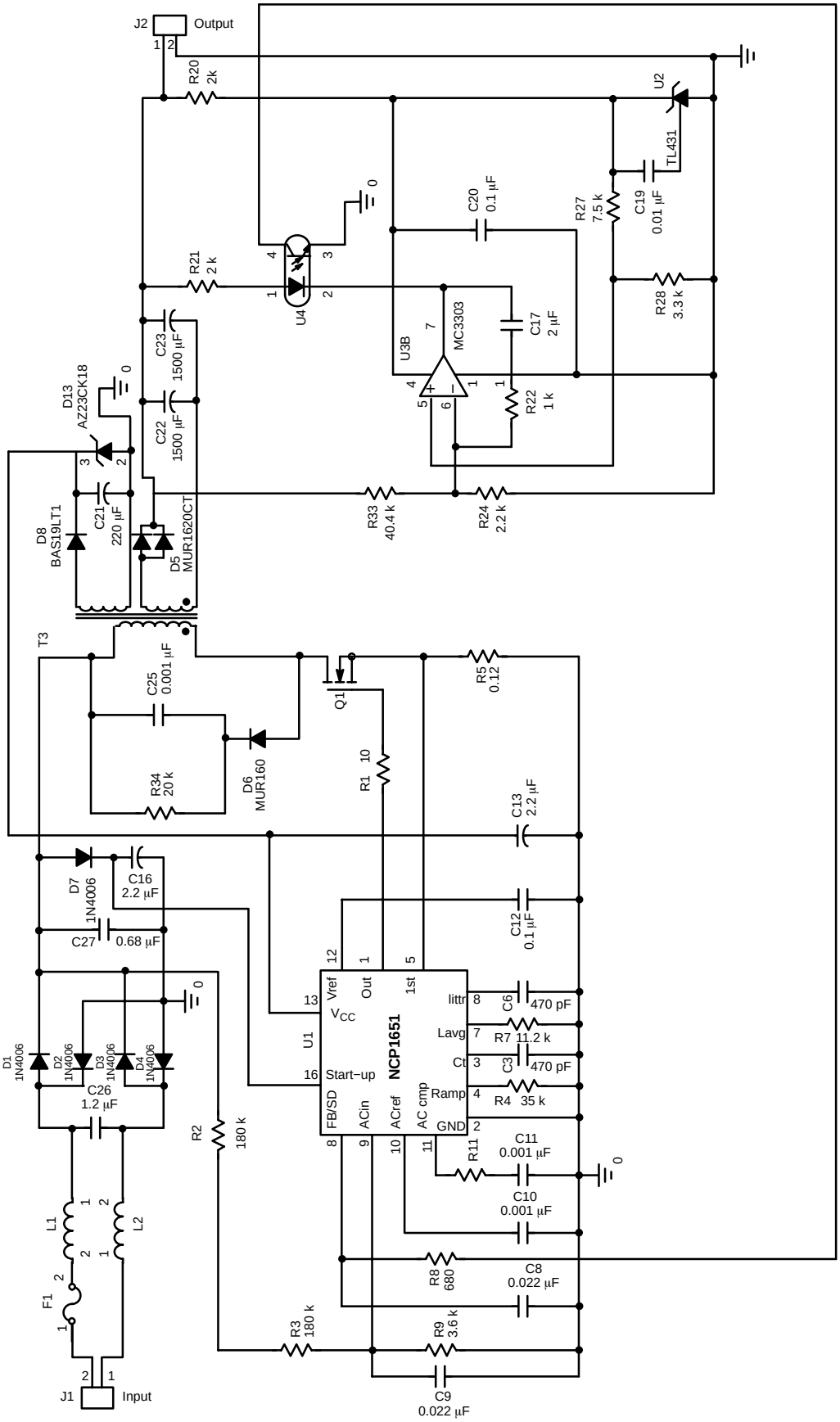

Figure 8. CCM Application Schematic

Notes

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