Primitive version

1. Feature

- ROM: 1k (1K x 14 bits)
- RAM: 41 (41 x 8 bits)
- Internal multi-band RC oscillator with programmable calibration, the band ranges include 6M, 4M, 1M and 32K.
- STACK: 4 Levels
- Support On-chip programming circuit
- I/O ports: 9 I/O Pads and 1 input Pad
- Timer/counter: 8bitsx1 (TMR_0) with pre-load function, selective signal and edges, overflow interrupt.
- Prescaler: 8 Bits
- Watchdog Timer: 20mS ~~ 2.56S
- Power-On Reset
- On chip R/C Oscillator for Watchdog Timer
- Oscillation Select:
  - -Internal RC: 6Mhz, 4Mhz, 1Mhz, 32Khz
  - -External RC
  - -Low power & Low speed crystal
  - -Standard crystal
- Operation Voltage: 2.5V ~~ 5.5V
- Instruction set: 79
- Support Timer interrupt
- Pull-up on MCLRb (PA_3)
- Weak Pull-up on I/O PAD (PA_1~PA_0).
- Wake-up from sleep on pin change.

Wake-up: 1. Watchdog timer overflow
2. Power_ON reset
3. Mclrb reset
4. Port A (PA_0, PA_1, PA_3) pin changed.

2. Pin Assignment

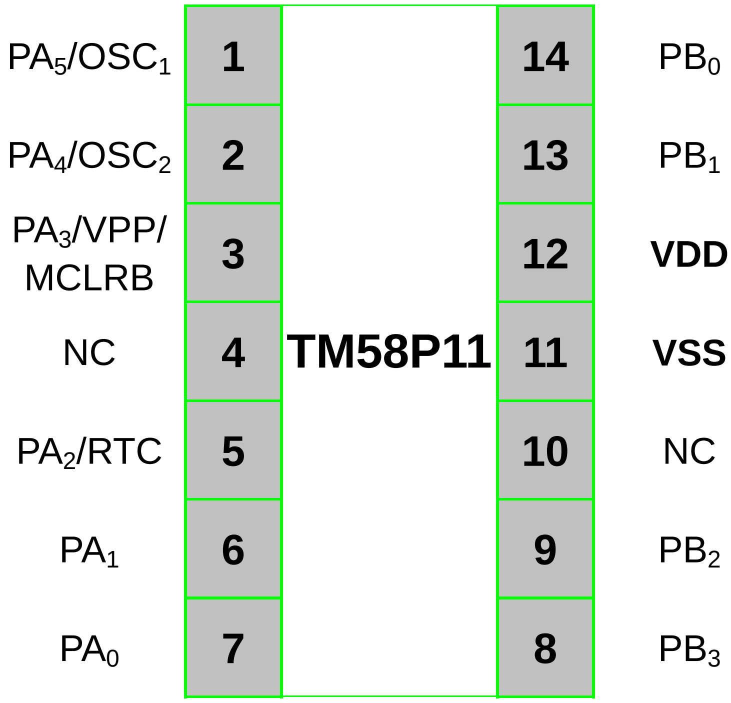

Figure1-1 Pin Assignment for DIP and SOP package types

Name	No.	Type	Description
PA_0	7	I/O	1. General purpose I/O pin 2. Internal pull-up by software programmed. 3. Wake-up from sleep mode by changing pin state.
PA_1	6	I/O	1. General purpose I/O pin. 2. Internal pull-up by software programmed. 3. Wake-up from sleep mode by changing pin state.
PA_2/ RTC	5	I/O	1. General purpose I/O pin 2. Can be configured as Timer_Clk input.
PA_3/ MCLRB/ VPP	3	I	1. Input pin only 2. If MCLRE is set and kept at logic low, the chip will be reset. 3. High voltage input when programming and verifying mode. 4. Internal pull-up by software programmed 5. Wake-up from sleep mode by changing pin state.

PA_4/ OSC_2	2	I/O	1. General purpose I/O pin 2. Crystal oscillator output.
$PA5_5$/ OSC_1	1	I/O	1. General purpose I/O pin 2. Crystal oscillator and RC oscillator input. 3. External clock input
VDD	12	P	Power input
VSS	11	P	Ground input
PB_0	14	I/O	General purpose I/O pin
PB_1	13	I/O	General purpose I/O pin
PB_2	9	I/O	General purpose I/O pin
PB_3	8	I/O	General purpose I/O pin

- Pin description

I: Input; O: Output; I/O: Bi-direction; P: Power

3. Functional Overview

- The TM58P11 is an 8-bit RISC One Time Programmable (OTP) micro controller with Haravrd architecture. It has 1Kwords of EPROM and 41 bytes RAM for memory space. The instruction set employs 79 single-word (14-bit wide) instructions. All instructions are 1 cycle (4 system clocks) except for branch instructions that take 2 cycles.
- The Core of the microcontroller:
  1. Long word instruction: each instruction has 14-bit wide and is not restricted by data bus. Since program memory (OTP) has independent bus, the memory utility is improved.
  2. Instruction pipeline: TM58P11 employs 2 stages pipeline to shrink instruction cycle. The CPU fetches instruction at phase 1 and executes at phase 2 respectively. This CPU has not data hazard problem because its execution cycle at one phase.
  3. Memory mapped register: most physical registers have unique memory address.
- The TM5811 provides 9 general purpose I/O (GPIO) pins to use for a variety of applications. The I/O pins are grouped into 2 ports (Port A and B) where most of pins can be individually configured as input mode or output mode. Additionally, PA_0, PA_1 and PA_3 can be used to generate external wake-up reset to the microcontroller. Note the GPIO resets all share the same reset vector that depends on device types.
- The TM58P11 features an internal RC oscillator that has 4 adjustable bands. Please refer to "Electrical Specification Section" for the detail on variation over operating-voltage and temperature.
- The microcontroller includes a watchdog timer (WDT) and an 8-bit prescaler. The WDT can be used to ensure the program never gets stalled or halted for more than 20 ms (WDT overflow is occurred). If a longer overflow period is desired, prescaler can extend a division ratio to 1:128 by program.
- TM58P11 supports 4 types of resets:
  1. Power_on reset
  2. Pin-changed wake-up reset
  3. WDT time-out reset
  4. MCLR reset

  These foregoing resets are recorded in the Status register. Bit 3,4 and 7 are used to record the different events. Program can interrogate these bits to determine the cause of a reset. More details on the various resets are given in the following sections.
- The 8-bit timer/counter can occupy an interrupt source. It is easy to measure the exact time scale in program.

4. Block diagram

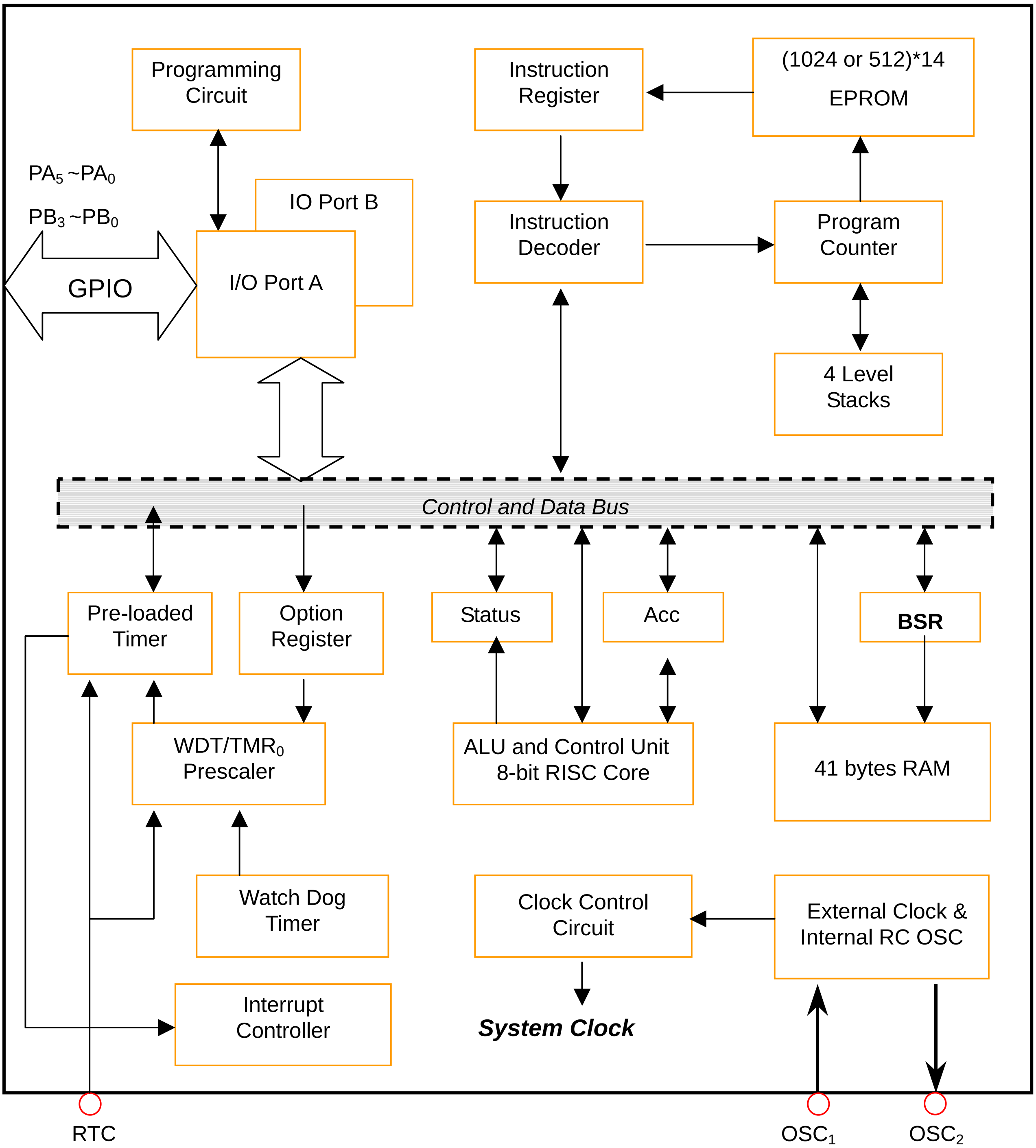

Figure 4-1 Logic Block Diagram

5. Memory Organization

TM58P11 memory is organized into program memory and data memory and called "Harvard Architecture". In general, "Harvard architecture" differs mostly from "Von Neumann architecture" in bus scheme. Harvard can access separate buses simultaneously. Considering the simplicity, we separate an instruction cycle into "fetch" and "execute" stages. TM58P11 can "fetch *ith* instruction" and "execute *(i-1)th* instruction" at the same time. The scheme overlaps instruction cycles and improves efficiency.

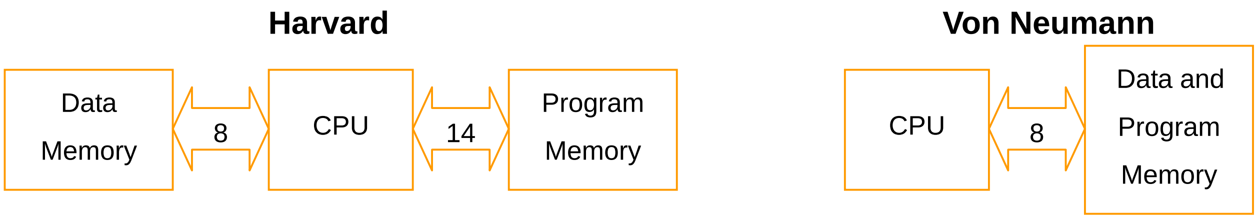

Figure 5-1 the sketches of Harvard and Von Neumann

5.1 Program memory

The internal RC oscillator provides an adjustable frequency. A calibration value is programmed to the bottom of memory that contains band and fine value. We use a MOVLA XX instruction where XX is the calibration value and its placed at the reset vector. The location is always reserved for system that locates at 3FFh. Once the reset occurs, TM58P11 will load calibration value to accumulator and change PC into 00h. User can write the value to the OSC_ADJ register or ignore it. The reset and IRQ vectors are shown in Figure 5-2.

000	MOVAM OSC_ADJ ;;**set** internal frequency
001 | 3FD	User program
3FE	LGOTO INT_Lable ;;IRQ vector
3FF	MOVLA xxH ;;**select** internal frequency

Fig 5-2 Program memory space for TM5811

TM58P11 allows directly goto any address in 1K memories without limited by page size. In addition, "lcall" and "lgoto" instructions are employed to provide flexible addressing mode.

TM58P11 provides IRQ function and IRQ vector that is located at 3FEh.

The TM58P11 can be operated in four external oscillator modes, such as low speed crystal, normal speed crystal, high-speed crystal and external RC mode. User can select one of them by programming FOSC1~0 in the configuration. It is located at 800H that contains OSC selection, WDT enable, code protection; MCLR reset enable, internal OSC and operate type selection. The detail is shown is Figure 5-3.

Note: the internal OSC enabling bit is more prior than OSC selection bits. If internal OSC is selected, then all external oscillatory methods are invalid.

Bit	Symbol	Description			
		Bit1	Bit0	OSC Type	Resonance Frequency
1~0	FOSC1~FOSC0	0	0	LS (low speed)	32~200K Hz
		0	1	NS(Normal speed)	1~10M Hz
		1	0	HS (high speed)	10~24M Hz
		1	1	External RC	20K~5.5M Hz
2	WDTE	WDTE: Watchdog enable/disable control 1: WDT enable 0: WDT disable			
3	CPT	CPT: Code Protection bit 1: OFF 0: ON			
4	MCLRE	MCLRE: WCLR reset enable 1: MCLR enable (low active) 0: MCLR disable			
5	IN_RC	IN_RC: internal RC oscillator 1: internal enable 0: internal disable			

Figure 5-3 the Definition of Configure Word

5.2 Data memory

Data memory is composed of special function registers and general-purpose registers. Furthermore, TM58P11 has 3 auxiliary registers that include the select register (Select) and the I/O direction register (IODIR_A, IODIR_B). The data memory map is shown in figure 5-4.

	00~1F	20~3F
00h	IAR	Pre_TMR0
01h	TMR0	IRQ_Mask
02h	PC	IRQ_Flag
03h	STATUS	PORT B
04h	BSR	Unimplemented
05h	OSC_ADJ	
06h	PORTA	
07h	General Purpose Register 07-0F	
8*4+16*4=96	General Purpose Register 10-1F	General Purpose Register 30-3F

Figure 5-4 The Data Memory Map of Advance Mode

5.2.1 Auxiliary registers

A. IODIR_A and IODIR_B are write-only registers. If control bit is set as “1”, the corresponding I/O pin is defined to input mode. Similarly, the zero represents output. Any direction control bit can be programmed individually as input or output by using IODIR instruction. If the chip has reset, then all I/O ports will be set as input mode.

Example 1 How to set I/O Port by using IODIR instruction

```
PORT A    Equ   06H
PORT B    Equ   23H
IODIR_A   Equ   06H
IODIR_B   Equ   07H
CLRA
IODIR     IODIR_A    ;; set Port A5~0 are output pin except for Port A3
MOVLA     03H
IODIR     IODIR_B    ;; set Port B3~2 are output and Port B1~0 are input
```

B. Select register is used to control WDT and TMR_0. It has not assigned a specific address in data memory and can only set control bits by select instruction, i.e. it is write-only register. The context of accumulator will be sent to the select register by executing the select instruction. If select register has never set by program, its default value is FFH. We drew Figure 5-5 to explain how to set select register.

Bit	Symbol	Description				
		PS2	PS1	PS0	TMR_0 rate	WDT rate
2~0	PS2~PS0	0	0	0	1:2	1:1
		0	0	1	1:4	1:2
		0	1	0	1:8	1:4
		0	1	1	1:16	1:8
		1	0	0	1:32	1:16
		1	0	1	1:64	1:32
		1	1	0	1:128	1:64
		1	1	1	1:256	1:128
3	PSA	PSA: Prescaler assignment bit 1: Prescaler assigned to WDT 0: Prescaler assigned to TMR_0				
4	EDGE0	EDGE0: TMR_0 source signal edge control bit 1:increment when H→L transition on external clock 0:increment when L→H transition on external clock				
5	SUR0	SUR0: TMR_0 clock source bit 1: External clock input 0: (Internal clock)/4 or internal instruction cycle				
6	IOPUB	IOPUB: pull up input pin (PA_3, PA_1 and PA_0) 1: disable 0: enable				
7	IOWUB	IOWUB: enable wakeup reset from pin changed 1: disable 0: enable				

Figure 5-5 Select register

5.2.2 Special function registers

- The IAR (indirect addressing register) is not a physical register and is used to assist BSR with indirect addressing. Any instruction attempts to access IAR, actually mapping to another address that is pointed by BSR. Since IAR is not a material circuit, user reads IAR itself (BSR=00H) will always return 00h. Writing to IAR itself will like NOP.

- TMR0 (Timer0) is 8-bit wide binary counter/timer. The register increases by an external signal edge applied to RTC pin, or by an instruction cycle (4 internal clocks). It has the following features.

A. Readable and writeable

B. The prescaler is assigned to TMR0 if the PSA bit (Select [3]) is clear.

C. TMR0 can set as timer mode by clearing SUR0 bit (Select [5]). In this mode, user changes the context of TMR0 by writing an adjusted value or using pre-load function.

D. If interrupt mask has enabled, then TM5811 will be interrupted when TMR0 is overflow

The other details will be described in later chapter.

- TM58P11 has 10-bit wide binary counter and 8-bit wide register are called as PC_real and PC, respectively. (program counter) is 10-bit wide binary counter and increases itself for every instruction cycle, except the following condition shown in Figure 5-6. For “call” or any instruction where the PC is the destination, that only lower 8 bit of PC are programmed by the instruction. Incrementing PC when it changes to the next higher page. It should be noted that the PL bit (Status [5]) would not be changed synchronously. The following Goto, Call, or MOVAM PC will return to the selective page, unless the PL bit has been updated in program. In order to reduce the complexity of programming, advance mode provides 2 instructions to facilitate subroutine call and branch handling which are LCALL and LGOTO. LCALL and LGOTO can address to anywhere in program memory, but does not need the page select bits. The attached operands of CALL and GOTO are 8-bit and 9-bit respectively, and so need extra bits (page select bits) to address whole memory. However, LCALL and LGOTO have 11-bit wide operands that are easy to address the total ROM space (able to address 2K).

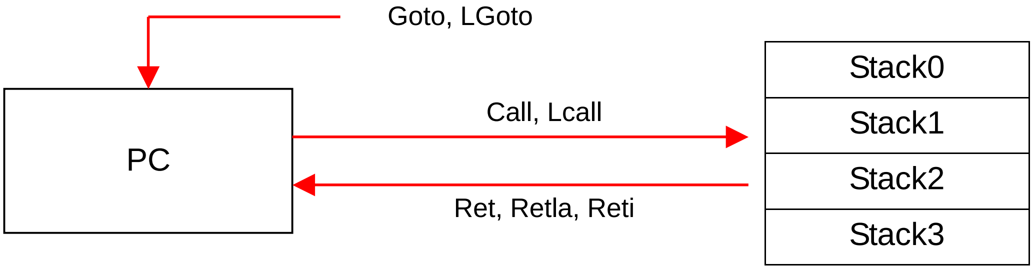

Figure 5-6 Program Counter and Branch instruction

- Status register contains page select bits, time out bit, power down bit and the status of ALU. $\overline{TO}$ and $\overline{PD}$ are controlled by hardware and unchangeable by program.

Bit	Symbol	Description	
0	C	Carry and $\overline{Borrow}$ bit:	
		ADD instruction	SUB instruction
		1: a carry occurred from the MSB 0: no carry	1: no borrow (Note1) 0: a borrow occurred from the MSB
1	DC	Nibble Carry and Nibble $\overline{Borrow}$ bit	
		ADD instruction	SUB instruction
		1: a carry from the low nibble bits of the result occurred 0: no carry	1: no borrow 0: a borrow from the low nibble bits of the result occurred
2	Z	Zero bit: 1: the result of a logic operation is zero 0: the result of a logic operation is not zero	
3	$\overline{PD}$	Power down flag bit: (Note2) 1: after power-on or by the CLRWDT instruction 0: execute SLEEP instruction	
4	$\overline{TO}$	Time out flag bit: 1: after power-on or by the CLRWDT or SLEEP instruction 0: Occur WDT time-overflow	
5	PL	Page location bit: 1: Page 1 (200H~3FFH) 0: Page 0 (000H~1FFH)	
6	--	Reserved, read as “0”	
7	IOR	IO reset bit: 1: Reset due to wake-up from SLEEP on pin change 0: Power-on reset and other reset types	

Figure 5-7 Status Register

Note1: A SUB instruction is executed by adding the 2’s complement of the subtrahend, so C = 1 represents positive result. The Figure 5-7-1 show the relation between C-bit and borrow.

B0H－50H										50H－B0H									
	C	B7	B6	B5	B4	B3	B2	B1	B0		C	B7	B6	B5	B4	B3	B2	B1	B0
		1	0	1	1	0	0	0	0			0	1	0	1	0	0	0	0
+		1	0	1	1	0	0	0	0	+		0	1	0	1	0	0	0	0
=	1	0	1	1	0	0	0	0	0	=	0	1	0	1	0	0	0	0	0

Figure 5-7-1

Note2: The $\overline{TO}$ and $\overline{PD}$ bits are active low that can be used to determine different causes of reset. The Figure 5-7-2 illustrates the value of $\overline{TO}$ and $\overline{PD}$ after the relative reset events.

$\overline{TO}$	$\overline{PD}$	Reset Event
0	0	Wake time out from sleep mode
0	1	WDT time out from normal mode
1	0	MCLR reset from sleep
1	1	Power on reset
Unchanged	Unchanged	Others

Figure 5-7-2

- TM58P11 allow 6-bit wide operand to directly access the data memory, operand<5:0> can address 00~3F directly. It doesn’t need bank select bits, and reduces the complexity of programming. BSR (bank select register) is associated with IAR to indirectly access the data memory. The addressing map is shown in Figure 5-8.

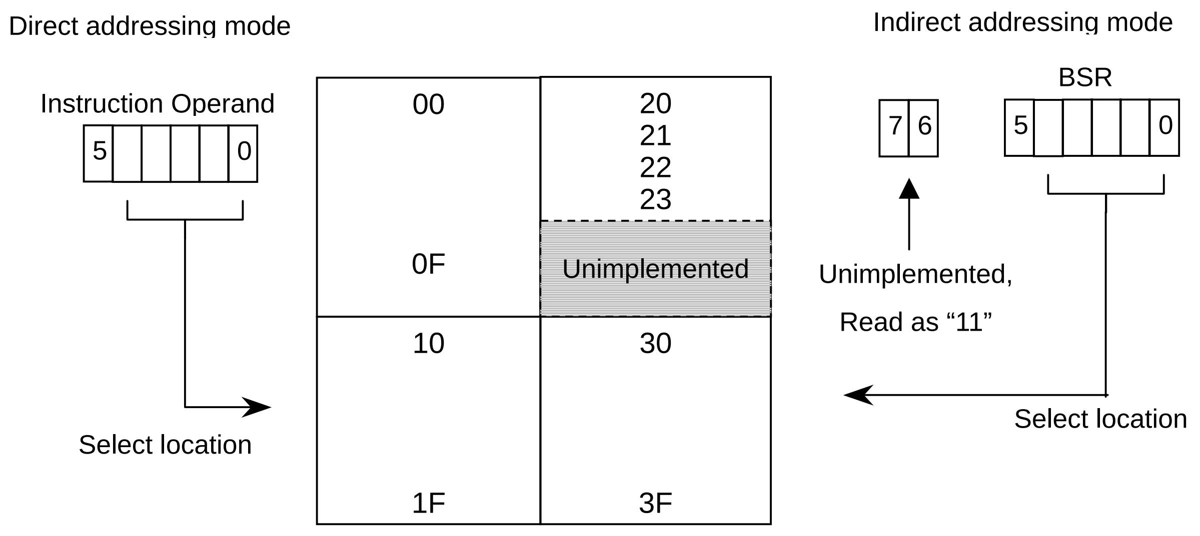

Figure 5-8 The Direct and Indirect Addressing Map

- The oscillator adjustment (OSC_ADJ) register is used to select and fine the internal RC oscillator. It contains 2 bits to select main band and other bits to modulate frequency. Figure 5-9 describes the definition of OSC_ADJ.

Bit	Symbol	Description
4-0	Fine	Fine tuner bit: *Depend on electrical character.*
6-5	Bank	Bank selection: 00: 6M 01: 4M 10: 1M 11: 32K
7	--	Unimplemented, read as “0”

Figure 5-9 oscillator adjustment register

- Port A is a programmable I/O port. Only the lower 6 bits are used. The bits 7~6 are unimplemented and read as “0”. The other bits are described at pervious section (see pin definition). Note: the PA_3 is an input pin only.

- The Interrupt Mask register and Interrupt Flag register are used to control IRQ handling. TM58P11 supports TMR_0_overflow interrupt. The schemes of the interrupt mask register and the interrupt flag register are shown in Fig 5-10 and 5-11, respectively.

Bit	Symbol	Description
7	INTM	Global enable bit: The bit has higher priority than TMR0M. 1: enable 0: disable By the way, the RETI instruction will set INTM to ‘1’.
6~1	----	Unimplemented, read as “0”
0	TMR0M	TMR0 Interrupt enable: 1:Enable Interrupt 0: Disable Interrupt

Figure 5-10 Interrupt Mask register

Bit	Symbol	Description
7~1	----	Unimplemented, read as “0”
0	TMR0F	TMR0 interrupt flag: 1: The timer0 counter overflow generates an interrupt request. TMR0F can set only by hardware. (Note) 0: TMR0F can clear only by software.

Figure 5-11 Interrupt Flag register

Note: the interrupt flags is set by hardware and cleared by software. It is useless that attempt writing ‘1’ to flag.

- The Pre_TMR0 register is used to write TMR0 automatically with the following cases.
  1. Any instruction writes to TMR0, e.g. (clrm TMR0, movam TMR0)
  2. TMR0 is overflowed

  The default value of Pre_TMR0 is 00H. If it keep default value, then TMR0 will be cleared that any instruction write to TMR0.

Example 2 Generate a counting event by using Pre_load function

```
TMR0        Equ   01H
Pre_TMR0    Equ   20H
            MOVLA     10h      ;; set prescalar rate 1:2 for TMR0
            SELECT
            MOVLA     F0h
            MOVAM     Pre_TMR0
            CLRM      TMR0     ;; the context of TMR0 is F0h
            ……                 ;; F0h will be reload to TMR0 after 32 instruction cycles
            …….
```

Functional Description

6.1 TMR0 and Watchdog timer

The Fig. 6-1 shows the block diagram of the timer0/WDT prescaler. As shown in the figure, the prescaler register can be a pre-scaler for timer0 or be a post-scaler for WDT.

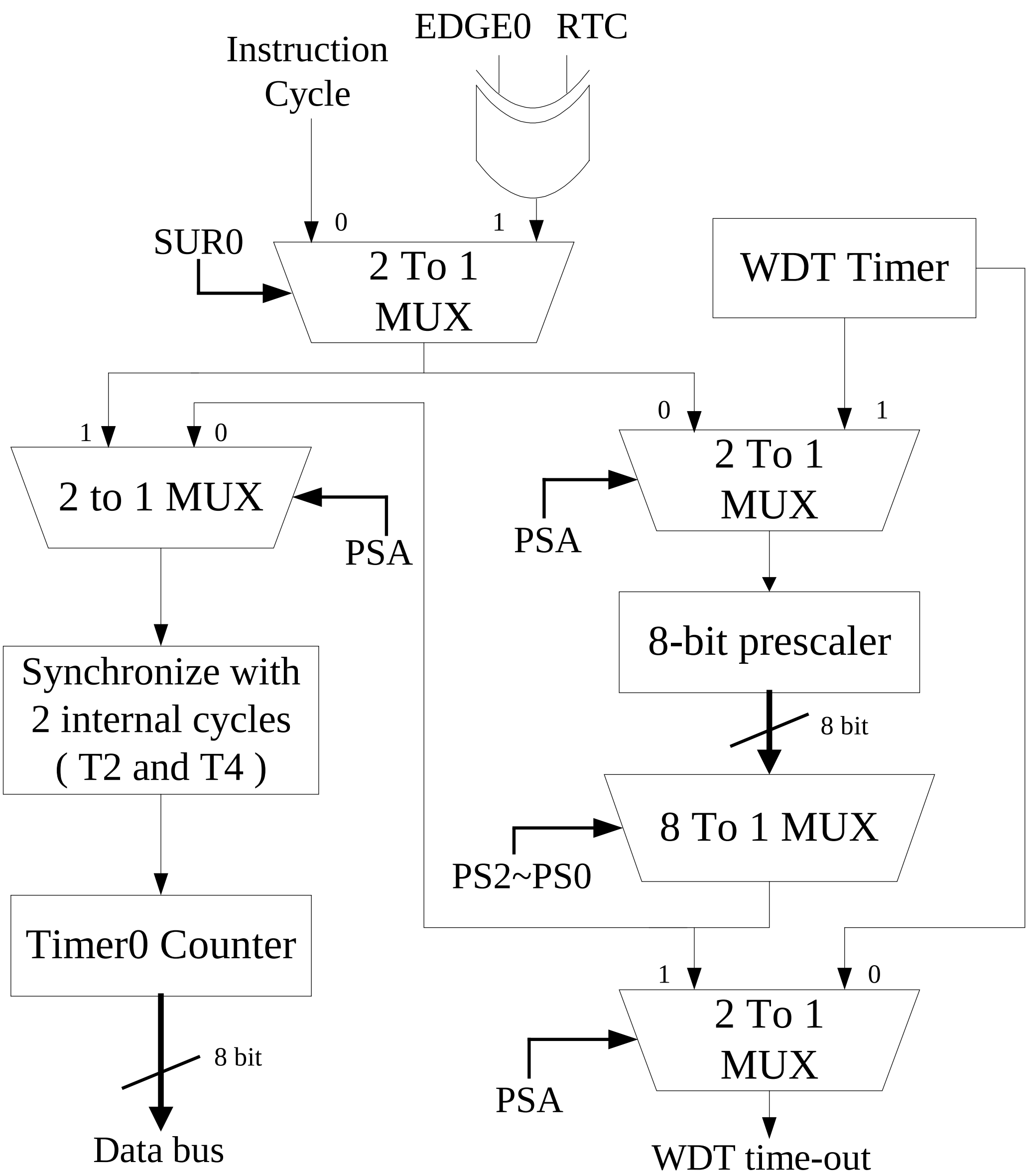

Figure 6-1 Block Diagram of the Timer0/WDT Prescaler

A. The TMR0 is an 8-bit timer/counter. The clock source of timer0 can come from the instruction cycle or the external clock.

To select the instruction clock, the SUR0 bit of the select register should be clear. When no prescaler is used, TMR0 will increase by 1 at every instruction cycle.

B. To select the external clock, the SUR0 bit of the select register should be set. In this mode, TMR0 relies on the EDGE0 bit to determine that TMR0 is increased by 1 at every falling or rising edge. When an external clock is used for TMR0, a problem must be noted that the external clock synchronizes with internal clock. TM58P11 synchronizes external clock by sampling internal clock at T2 and T4. If external pulse is smaller than 2 internal cycles, the pulse maybe ignored. Therefore, the external clock must keep stable state (high or low) for at least 2 internal cycles.

The WDT counter is a 10-bit binary counter. The clock source of WDT is provided by an independent on-chip RC oscillator that does not need any external clock. Therefore, the WDT will keep counting even if the chip has slept already. A WDT time-out will restart system and set the time-out flag bit (bit4 of status register) as "0". The WDT time-out period vary with temperature, power voltage and process. This period can be improved via the prescaler. The maximum division ratio can up to 1:128 by setting PS2~PS0 as "111".

The prescaler can be assigned to either the timer0 or the WDT via the PSA bit. Note that either WDT or timer0 can employ the prescaler simultaneously. When the prescaler is assigned to WDT, "CLRWDT" and "SLEEP" instruction will clear the prescaler and the WDT. When the prescaler is assigned to timer0, the prescaler will be cleared by any instruction that writes to timer0.

6.2 Reset

TM58P11 may be reset by one of the following conditions:

A. Power-on
B. Pin changed at sleep mode (if enabled)
C. RESETB/VPP pin input a negative pulse
D. WDT timer out reset (if enabled).

As shown in the figure 6-2, four reset conditions are listed. The voltage range of power-on is influenced by process and temperature variations. In general, we call the case as cold reset. The cold reset time may be too short for slow crystals and RC oscillators that require much longer than **setup time** (note) to oscillate. In order to insure the system is correct, the event should be synchronized with system clock.

Note: the setup time is approximately 20ms that will affect due to power voltage, process and temperature variations.

The other cases are called warm reset. The different reset events will affect registers and ram. $\overline{TO}$, $\overline{PD}$ and IOR are set and cleared differently by varied reset conditions. These bits are used to determine the type of reset. $\overline{TO}$ and $\overline{PD}$ bits maintain their status until another reset occurs. A low-pulse on the MCLR input does not change $\overline{TO}$ and $\overline{PD}$. These corresponding relations are listed in figure 6-3.

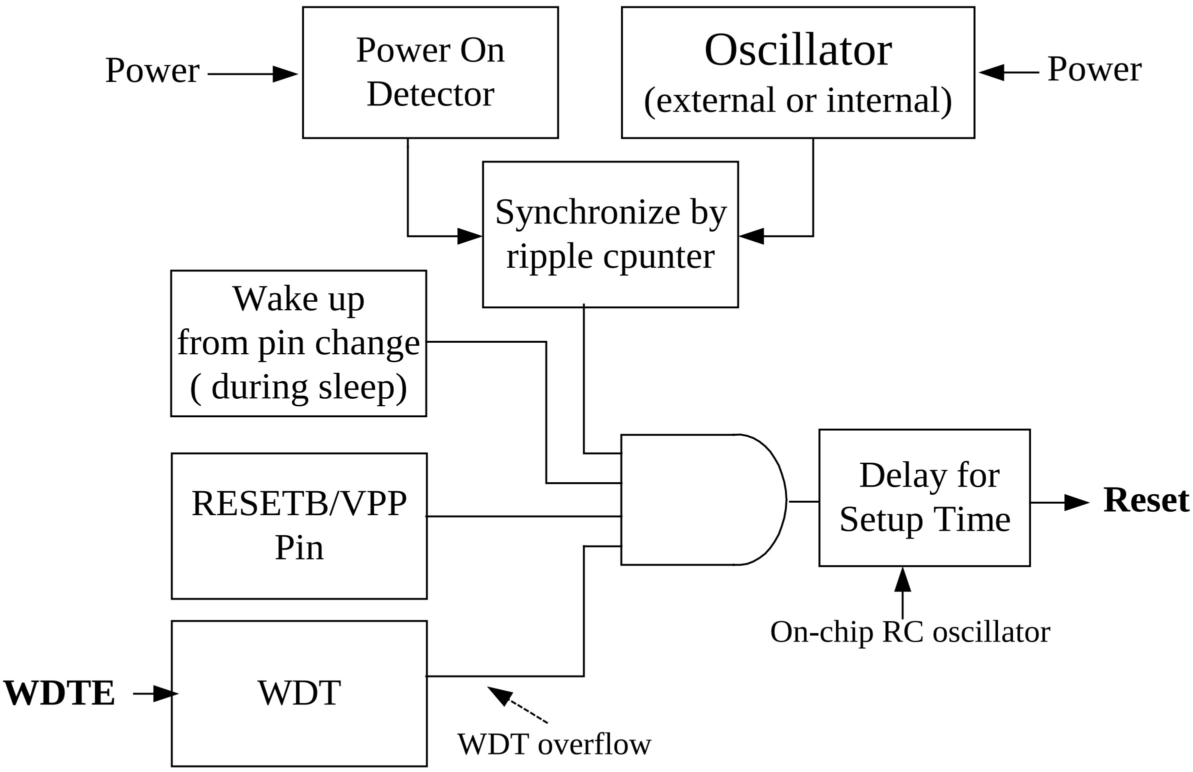

Figure 6-2 Scheme of the Reset Controller

Condition	Status Register		
	IOR	$\overline{TO}$	$\overline{PD}$
Power-on reset	0	1	1
MCLR reset during normal operation	0	1	1
MCLR reset during sleep	0	1	0
WDT reset during sleep	0	0	0
WDT reset during normal operation	0	0	1
Wake up by pin changed	1	1	0

Figure 6-3 Status register with corresponding resets

In general, cold reset resulted in ambiguities of data memory. Figure 6-4 shows a description of reset types of data memory.

Address	Name		Cold Reset	Warm Reset
N/A	Accumulator		xxxx xxxx	pppp pppp
N/A	IODIR	06	11 1111	11 1111 note1
		07	1111	1111
N/A	Select		1111 1111	1111 1111 note1
00h	IAR		---- ----	---- ----
01h	TMR0		xxxx xxxx	pppp pppp
02h	PC		11 1111 1111	11 1111 1111
03h	STATUS		0001 1xxx	?00? ?ppp note 2
04h	BSR		-xxx xxxx	-ppp pppp
05h	OSC_ADJ		0000 0000	0ppp pppp
20h	Pre_TMR0		0000 0000	0000 0000 note1
21h	IRQ_Mask		0000 0000	0000 0000
22h	IRQ_Flag		0000 0000	0000 0000
	General Purpose RAM		Xxxx xxxx	Pppp pppp

6-4 Reset for data memory

Note 1: write only

Note 2: refer to Fig. 6-3

7. Instruction Set

Mnemonic Operands	Instruction Code (Advance)	Cycles	Status Affected	OP-code
BCM M, b0	Clear bit0 of (M)	1	None	00 1100 0MMM MMMM
BCM M, b1	Similar the above description	1	None	00 1100 1MMM MMMM
BCM M, b2	Idem	1	None	00 1101 0MMM MMMM
BCM M, b3	Idem	1	None	00 1101 1MMM MMMM
BCM M, b4	Idem	1	None	00 1110 0MMM MMMM
BCM M, b5	Idem	1	None	00 1110 1MMM MMMM
BCM M, b6	Idem	1	None	00 1111 0MMM MMMM
BCM M, b7	Idem	1	None	00 1111 1MMM MMMM
BSM M, b0	Set bit0 of (M)	1	None	00 1000 0MMM MMMM
BSM M, b1	Similar the above description	1	None	00 1000 1MMM MMMM
BSM M, b2	Idem	1	None	00 1001 0MMM MMMM
BSM M, b3	Idem	1	None	00 1001 1MMM MMMM
BSM M, b4	Idem	1	None	00 1010 0MMM MMMM
BSM M, b5	Idem	1	None	00 1010 1MMM MMMM
BSM M, b6	Idem	1	None	00 1011 0MMM MMMM
BSM M, b7	Idem	1	None	00 1011 1MMM MMMM
BTMSC M, b0	If bit0 of (M) = 1, skip next instruction	1 + (skip)	None	00 0100 0MMM MMMM
BTMSC M, b1	Similar the above description	1 + (skip)	None	00 0100 1MMM MMMM
BTMSC M, b2	Idem	1 + (skip)	None	00 0101 0MMM MMMM
BTMSC M, b3	Idem	1 + (skip)	None	00 0101 1MMM MMMM
BTMSC M, b4	Idem	1 + (skip)	None	00 0110 0MMM MMMM
BTMSC M, b5	Idem	1 + (skip)	None	00 0110 1MMM MMMM
BTMSC M, b6	Idem	1 + (skip)	None	00 0111 0MMM MMMM
BTMSC M, b7	Idem	1 + (skip)	None	00 0111 1MMM MMMM
BTMSS M, b0	If bit0 of (M) = 1, skip next instruction	1 + (skip)	None	00 0000 0MMM MMMM
BTMSS M, b1	Similar the above description	1 + (skip)	None	00 0000 1MMM MMMM
BTMSS M, b2	Idem	1 + (skip)	None	00 0001 0MMM MMMM

BTMSS M, b3	Idem	1 + (skip)	None	00 0001 1MMM MMMM
BTMSS M, b4	Idem	1 + (skip)	None	00 0010 0MMM MMMM
BTMSS M, b5	Idem	1 + (skip)	None	00 0010 1MMM MMMM
BTMSS M, b6	Idem	1 + (skip)	None	00 0011 0MMM MMMM
BTMSS M, b7	Idem	1 + (skip)	None	00 0011 1MMM MMMM
CLRWDT	Clear watch-dog register	1	TO, PO	10 0000 0000 0001
SELECT	Set select register	1	None	10 0000 0000 0010
SLEEP	Enter sleep (saving) mode	1	TO, PO	10 0000 0000 0011
IODIR M	Set i/o direction	1	None	10 0000 0000 0MMM
ANDLA I	Literal . (acc) → (acc)	1	Z	11 1001 iiii iiii
XORLA I	Literal xor (acc) → (acc)	1	Z	11 1000 iiii iiii
MOVLA I	Move literal to accumulator	1	None	11 0001 iiii iiii
IORLA I	Literal ior (acc) → (acc)	1	Z	11 0011 iiii iiii
RETLA I	Return and move literal to accumulator	2	None	11 1100 iiii iiii
LCALL I	Call subroutine. However, LCALL can addressing 2K address	2	None	01 0iii iiii iiii
LGOTO I	Go branch to any address	2	None	01 1iii iiii iiii
NOP	No operation	1	None	10 0000 0000 0000
MOVAM m	Move data form acc to memory	1	None	10 0000 1MMM MMMM
COMM M, m	~(M) → (M)	1	Z	10 0010 1MMM MMMM
COMM M, a	~(M) → (acc)	1	Z	10 0010 0MMM MMMM
MOVM M, m	(M) → (M)	1	Z	10 0011 1MMM MMMM
MOVM M, a	(M) → (acc)	1	Z	10 0011 0MMM MMMM
RRM M, m	Rotate right from m to itself	1	C	10 1110 1MMM MMMM
RRM M, a	Rotate right from m to acc	1	C	10 1110 0MMM MMMM
RLM M, m	Rotate left from m to itself	1	C	10 1100 1MMM MMMM
RLM M, a	Rotate left from m to acc	1	C	10 1100 0MMM MMMM

SWAPM M, m	Swap data from m to itself	1	None	10 1101 1MMM MMMM
SWAPM M, a	Swap data from m to acc	1	None	10 1101 0MMM MMMM
CLRA	Clear accumulator	1	Z	10 0001 0000 0000
CLRM M	Clear memory M	1	Z	10 0001 1MMM MMMM
INCM M, m	(M) + 1 → (M)	1	Z	10 1000 1MMM MMMM
INCM M, a	(M) + 1 → (acc)	1	Z	10 1000 0MMM MMMM
INCMSZ M, m	(M) + 1 → (M), skip if (M) = 0	1 + (skip)	None	10 1001 1MMM MMMM
INCMSZ M, a	(M) + 1 → (acc), skip if (M) = 0	1 + (skip)	None	10 1001 0MMM MMMM
DECM M, m	Decrement M to M	1	Z	10 0110 1MMM MMMM
DECM M, a	(M) - 1 → (acc)	1	Z	10 0110 0MMM MMMM
DECMSZ M, m	(M) - 1 → (M), skip if (M) = 0	1 + (skip)	None	10 0111 1MMM MMMM
DECMSZ M, a	(M) - 1 → (acc), skip if (M) = 0	1 + (skip)	None	10 0111 0MMM MMMM
SUBAM M, m	(M)–(acc) → (M)	1	C, DC, Z	10 1010 1MMM MMMM
SUBAM M, a	(M) –(acc) → (acc)	1	C, DC, Z	10 1010 0MMM MMMM
XORAM M, m	(M) xor (acc) → (M)	1	Z	10 1011 1MMM MMMM
XORAM M, a	(M) xor (acc) → (acc)	1	Z	10 1011 0MMM MMMM
ANDAM M, m	(M). (acc) → (M)	1	Z	10 0100 1MMM MMMM
ANDAM M, a	(M). (acc) → (acc)	1	Z	10 0100 0MMM MMMM
ADDAM M, m	(M)+(acc) → (M)	1	C, DC, Z	10 0101 1MMM MMMM
ADDAM M, a	(M)+(acc) → (acc)	1	C, DC, Z	10 0101 0MMM MMMM
IORAM M, m	(M) ior (acc) → (M)	1	Z	10 1111 1MMM MMMM
IORAM M, a	(M) ior (acc) → (acc)	1	Z	10 1111 0MMM MMMM
RET	Return	2	None	11 1111 0111 1111
RETI	Return and move literal to accumulator	2	None	11 1111 1111 1111
CALL I	Call subroutine	2	None	11 0110 iiii iiii
GOTO I	Goto branch	2	None	11 101i iiii iiii

Electrical Characteristics: (Primitive)

1. Sink & Driving Current:

Vdd = 2.5V

Voh	0.5	1	1.5	2	V
	8.45	8	6.88	4.25	mA

Vol	0.25	0.5	1	V
	6.8	12.2	17.9	mA

Vdd = 5.5V

Voh	3.5	4	4.5	5	V
	30.25	24.8	17.65	9.9	mA

Vol	0.5	0.75	1	V
	24.5	35.3	43.8	mA

2. 外部 RC 震盪頻率變動範圍

Vdd = 5V,

	3.3KΩ	**4.7KΩ**	**5.6KΩ**	**10KΩ**	**47KΩ**	**100KΩ**	**330KΩ**	**470KΩ**
20pf	3.32M	2.58M	2.23M	1.37M	332K	161K	47.9K	35K
50pf	2.3M	1.74M	1.49M	890K	205K	99K	29K	21.3K
100pf	1.77M	1.32M	1.12M	660K	149K	71.7K	21K	15.4K
300pf	1.024M	747.5K	631K	363K	80K	38.2K	11.2K	8.2K

Vdd = 3V

	3.3KΩ	**4.7KΩ**	**5.6KΩ**	**10KΩ**	**47KΩ**	**100KΩ**	**330KΩ**	**470KΩ**
20pf	3M	2.6M	2.4M	1.736M	517.8K	264.6K	121.6K	60.8K
50pf	2.2M	1.8M	1.6M	1.05M	273.8K	135.8K	40.7K	30K
100pf	1.69M	1.337M	1.16M	734.6K	179.4K	88.2K	26.1K	19.2K
300pf	887.2K	667K	568.3K	334.7K	76.5K	36.9K	10.85K	7.93K

3. 工作電流與頻率

3.1 Standby Current with disable WDT: less than 0.1 μA (Vdd = 3~5V)

Standby Current with enable WDT: less than 6 μA and 2 μA for 5V and 3V respectively.

3.2 Operating current V.S Frequency

Config	Vdd	Current	Unit	Conditions
LP	5V 3V	400 40	μA	Operating for 32K & WDT on
LP	5V 3V	270 40	μA	Operating for 32K & WDT off
LP	5V 3.3V	300 50	μA	Operating for 455K
XT	3V 2.4V	0.28 0.07	mA	Operating for 455K
XT	5V 3V	1.3 0.24	mA	Operating for 1M
XT	5V 3V	1.15 0.4	mA	Operating for 4M
HS	5V 3V	1.2 0.45	mA	Operating for 4M
XT	5V 3V	1.66 0.62	mA	Operating for 8M
HS	5V 3V	1.8 0.75	mA	Operating for 8M
HS	5V 3V	2.1 0.9	mA	Operating for 10M
HS	5V 3V	2.3 1	mA	Operating for 12M
HS	5V 3V	2.5 1.09	mA	Operating for 14.4M
HS	5V 3V	2.64 1.18	mA	Operating for 16M
HS	5V 3V	3.5 1.62	mA	Operating for 24M

4. 外部 Crystal 頻率與操作電壓

Configuration	頻率範圍	適用電壓
LP (low speed)	32k	2V~6V
NS (normal speed)	1M~14.4M (註 1)	2.4V~6V
HS (high speed)	10M~24M	3V~6V

(註 1) : 455K 的情形很特殊,請參閱 3-2.