Capacitors in Broadband Applications

Proper selection of capacitors for RF broadband applications requires careful evaluation of frequency dependent parameters and circuit design requirements

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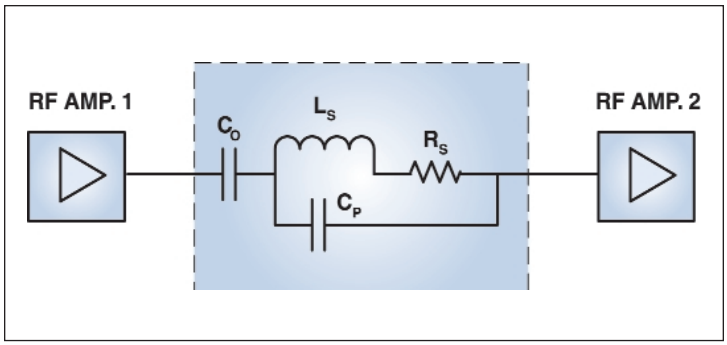
In today's rapidly expanding RF and microwave markets, numerous designs must operate over multiple octaves of frequency spectrum. Some of the more common of these include broadband bias networks such as transistor emitter and FET source bypassing, transistor collector and FET drain feed structures, as well as interstage RF coupling, DC blocking and wideband impedance matching.

This article will explore various ways to accommodate broadband application designs with the proper selection of capacitive elements. The first part of this discussion will address the implementation of a single capacitor solution followed by a multiple capacitor approach. Pertinent electrical design parameters, such as the magnitude of the impedance, insertion loss and the capacitor's parasitic elements, will be examined in detail for each method.



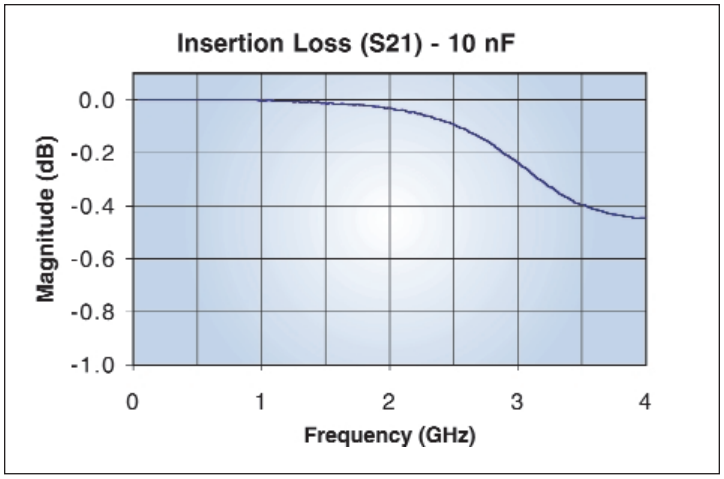
▲ **Figure 1. Interstage coupling, 50 MHz to 3.6 GHz.**

Note: The coupling capacitor C_0 is represented with its equivalent series resistance (ESR), denoted as R_S, equivalent series inductance (ESL), denoted as L_S, and parasitic parallel capacitance C_P, associated with the parallel resonant frequency (F_{PR}).

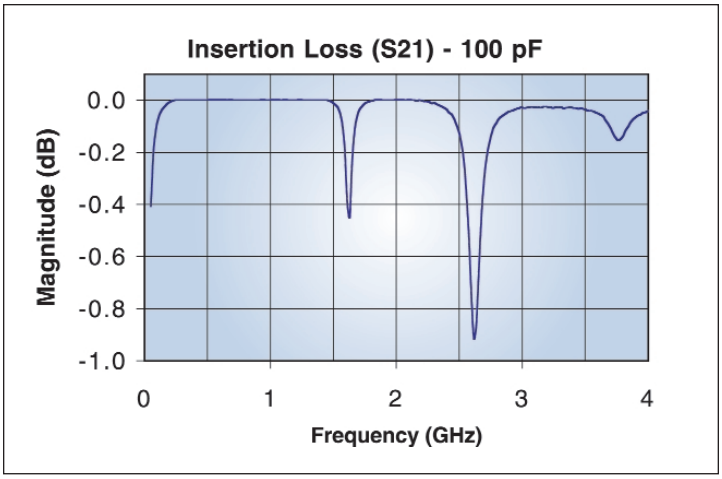
Single capacitor approach

There are many broadband applications with specific design requirements in which a single capacitor will provide an excellent functional solution. Given that the impedance of a capacitor, its equivalent series resistance (ESR), net reactance and quality factor (Q) are all frequency dependent, the designer must carefully consider these parameters before designing capacitive elements into a broadband application. Another critical parameter to take into account is the capacitor's insertion loss characteristic, i.e. the magnitude of S_{21}. By evaluating the insertion loss over the frequency band of interest, the designer can readily determine whether or not the subject capacitor is suitable for broadband DC blocking and coupling applications. This will also serve as a good starting point for selecting a broadband bypass capacitor. In contrast to DC blocking and coupling, a bypass capacitor also requires careful evaluation of its complex impedance over the entire frequency range of interest with emphasis on the inductive reactance resulting from the capacitor's parasitic inductance. The magnitude of both the real and reactive parts of the capacitor's impedance over frequency can easily be seen on a Smith chart presentation. Assessment of the net parasitic inductance will be discussed in greater detail later in this article.

In the following example, two RF amplifier stages operating in a 50-ohm network require broadband interstage coupling, as illustrated in Figure 1. Assume that the application requires DC blocking and coupling over the frequency range of 50 MHz to 3.6 GHz. In order to achieve a solution using a "one capacitor" approach, several design considerations must be judiciously evaluated beforehand. An ATC200A103 (10 nF) capacitor has



▲ **Figure 2. Insertion loss versus frequency for the 10 nF ceramic chip capacitor.**



▲ **Figure 3. Insertion loss versus frequency for the 100 pF ceramic chip capacitor.**

been selected as a starting point for this application since its large capacitance value will provide a low impedance, i.e. 0.22 ohms at 50 MHz, the lowest operating frequency in this example. Another fundamental consideration for all capacitor applications is the insertion loss over the desired frequency band. It is especially important to carefully examine the magnitude of S_{21} of a given capacitor for the presence of one or more parallel resonances falling within the desired passband. These resonances will generally show up as distinct attenuation notches at their frequencies of occurrence. Examination of a capacitor's S_{21} data will define these losses over the frequency range of interest. An insertion loss of several tenths of a dB is generally an acceptable criterion for virtually all applications.

The 10 nF capacitor used in the above example is an X7R type, which provides an excellent solution for this requirement. This is based on its large capacitance value and low insertion loss characteristic across the entire passband. Accordingly, an X7R capacitor may provide a better solution than an NPO for many multi-octave applications due to its inherently higher volumetric efficiency, i.e. the availability of more capacitance per unit volume. The higher capacitance values provided by X7R capacitors are frequently needed in order to satisfy the lower frequency requirement imposed by most broadband applications, such as the one illustrated in Figure 1.

A capacitor's series resonant frequency (F_{SR}), also referred to as self-resonance, occurs at the frequency where the capacitor's net reactance is zero and is readily seen on an S_{11} Smith chart. At this frequency, the impedance of the device will be equal to a small ESR value, generally in the order of 100 milliohms at 1 GHz for high Q ceramic chip capacitors. Therefore, a capacitor will provide its lowest impedance path required for optimal coupling and bypass functionality at its series resonant frequency. In contrast, the impedance of a capacitor at its parallel resonant frequency (F_{PR}) can be precipitously high, especially for high Q devices.

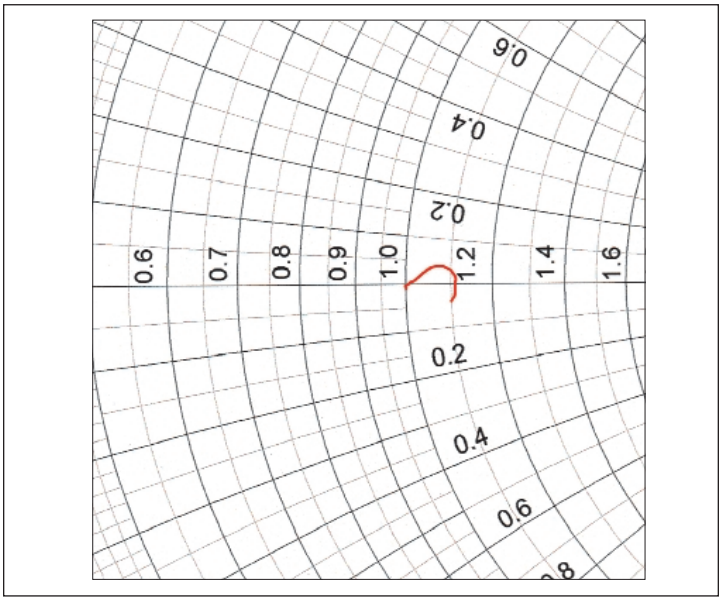
By examining the magnitude of S_{21} versus frequency of a given capacitor, excessive losses associated with F_{PR} within the frequency band of interest can be readily observed. In many broadband designs, the capacitor's series resonant frequency may be exceeded without negative consequence, with the exception of matching and bypassing applications. Exceeding F_{SR} will result in a net impedance that is inductive. This will usually not pose a problem in DC blocking and coupling applications, however, bypass and matching applications require careful scrutiny of the net impedance and the level of parasitic inductance.

In bypass applications, it is desirable to operate at the capacitor's F_{SR} where the impedance is essentially equal to the ESR and zero net reactance. For the best practical solution, the author suggests selecting the lowest standard EIA capacitor value that exhibits an F_{SR} that is slightly higher than the application bypass frequency. This will ensure that the impedance will be low with a net reactance that is capacitive. These performance characteristics are defined by S-parameter data files supplied by the manufacturer. The S-parameter files are typically derived from measurements of standard EIA capacitor values within a given product series.

For non-standard values, the magnitude and phase attributes can be estimated by interpolating the S-parameter data associated with the adjacent standard EIA capacitor values. These approximations are valid when the S-parameter data used in the interpolation has been derived from capacitors having the same basic internal design and dielectric type. Exceptions to this rule occur when there are significant deviations in the capacitor's internal design structure, such as electrode pattern geometry, electrode count and spacing, electrode end and side margins, as well as variations in the dielectric constant and loss tangent characteristics over frequency.

Insertion loss

As previously stated, a large value capacitor is generally selected in order to satisfy the low frequency region of a broadband design requirement. These applications can expose a capacitor to operating frequencies that far exceed its self-resonant frequency where the occurrence of parallel



▲ **Figure 4. Smith chart plot for the 10 nF capacitor in series through configuration.**

resonances within the desired passband are imminent. Therefore, the designer must balance between the capacitance value needed to satisfy the low frequency requirement and the inevitability of in-band parallel resonances brought about by large value capacitors. If a parallel resonance does fall within the operating passband, it will be necessary to evaluate the depth of the associated attenuation notch in order to determine whether or not this loss is acceptable for a particular design requirement. In many instances, the magnitude of S_{21} for a given capacitor may be excessive, thereby making the device unusable for a given application.

Frequently, however, the capacitor's series resistive losses at F_{PR} are great enough to damp the resulting attenuation notch. In these instances, the notches are present yet very shallow in magnitude and are frequently obscured. This operating condition is valid for many broadband designs using one capacitor. The S_{21} plots in Figures 2 and 3 show a comparison in the relationship between frequency and the magnitude of S_{21} over more than six frequency octaves (50 MHz to 4 GHz). Figure 2 illustrates the S_{21} insertion loss characteristic for an ATC200A103 (10 nF) capacitor, while Figure 3 illustrates the same parameter for an ATC100A101 (100 pF) capacitor. Both devices were measured in a series through configuration with the capacitor's electrodes parallel to the substrate, i.e. flat mount orientation.

Frequency (MHz)	Real (Ω)	Reactive (Ω)	Impedance Magnitude (Ω)
50	50	–*j* 2.5	50.06
150	50	–*j* 0.15	50
450	50.2	–*j* 0.15	50.2
900	50.8	+*j* 0.25	50.8
1800	51.5	+*j* 0.5	51.5
2400	52.2	+*j* 2	52.3
3600	52	*j* 0	52
4000	55	–*j* 2	55.04

▲ **Table 1. Complex impedance summary for the 10 nF capacitor in series through configuration.**

From Figure 2, it can be seen that the insertion loss of the selected 10 nF capacitor is less than 0.5 dB throughout the plotted frequency range, making it suitable for virtually all wireless frequency broadband applications, such as the coupling application referenced in Figure 1. In contrast, the 100 pF capacitor illustrated in Figure 3 exhibits notable in-band insertion losses, which makes it a less likely candidate for the above mentioned application. Losses that exceed several tenths of a dB within the passband could easily compromise the end performance of a circuit design. Therefore, the decision is ultimately left up to the discretion of the designer to determine whether or not these losses are acceptable for a particular design requirement.

Figure 4 is an S_{11} Smith chart representing the 10 nF capacitor sample used to generate the S_{21} data in Figure 2. Since this measurement was performed in a series through configuration, the resulting Smith chart illustration is especially useful for evaluating a capacitor's complex impedance in coupling and DC blocking applications. The Smith chart clearly shows that both the real and reactive parts of the impedance of this device are very close to the center of the chart, i.e. normalized impedance throughout the entire frequency range.

Table 1 was constructed from the Smith chart data in Figure 4 and summarizes the real and reactive parts of the impedance referenced to a 50-ohm system at eight different frequencies. The table also shows the magnitude of the impedance as calculated from the vector sum of the real and reactive parts. It becomes clear from this data that the subject 10 nF capacitor will serve as an excellent coupling and DC blocking capacitor throughout the entire frequency range.

Effects of ESR and *Q*

A capacitor's quality factor (Q) is numerically equal to the ratio of its net reactance $|X_C - X_L|$ to its equivalent series resistance (ESR), or

$$Q = \frac{|X_C - X_L|}{ESR}$$

From this expression, it can be seen that the capacitor's Q varies inversely proportional to its ESR and proportionally to the net reactance at a given frequency. The capacitor's ESR should always be taken into account over the entire frequency band of interest, as it becomes a major consideration when designing a single capacitor into a multi-octave application. This parameter is especially useful in the region where parallel resonances are present. As previously mentioned, an attenuation notch will occur at the capacitor's parallel resonant frequency (F_{PR}), the depth

of which is inversely proportional to the ESR. Therefore, the capacitor's ESR will largely determine the depth of the attenuation notch at the parallel resonant frequency.

A practical design approach is to select a capacitor large enough in value to cover the lowest operating frequency requirement, while making sure that additional losses brought about by the occurrence of in-band parallel resonances are within acceptable limits. The effects of ESR at the parallel resonant frequency are best evaluated by examining the real part of the capacitor's impedance at F_{PR}. Evaluating this impedance will give the designer a clear indication of the capacitor's usability at this frequency. If the ESR is high at the parallel resonant frequency, the resultant insertion loss will be correspondingly low. Accordingly, the associated notch depth will be shallow and generally not be discernible in the magnitude of S_{21}. This will provide for a low loss "one capacitor" broadband DC blocking and coupling solution over the frequency band of interest. The same considerations hold true for broadband bypassing applications; however, in addition to the magnitude of the impedance, an evaluation of the S_{11} Smith chart must also be taken into account.

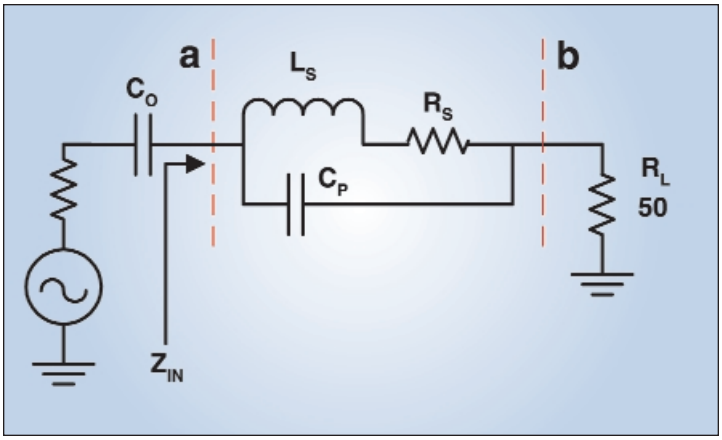
As seen in Figure 5, the parasitic elements associated with capacitor C_0 consist of L_S, R_S and C_P. The real part of the impedance looking into the parasitic branch at parallel resonance is:

$$Z_{IN\,(\mathrm{REAL})} = \frac{L_S}{R_S C_P} \quad (\text{at } F_{PR})$$

where C_P is a small parasitic capacitance associated with C_0's parallel resonant frequency and R_S and L_S are the capacitor's ESR and ESL, respectively.

From the relationship between $Z_{IN\,(\mathrm{REAL})}$, L_S, R_S and C_P, it can be seen that at F_{PR}, a low R_S will yield a high impedance, thereby giving rise to a deep attenuation notch. The converse is also true, in that a high R_S will yield a low impedance, thereby resulting in a more shallow-attenuation notch. The impedance of this network increases with decreasing values of R_S. Since this impedance is in series with the nominal capacitor C_0, the net impedance from terminal (a) to terminal (b) will increase for decreasing values of R_S and vice versa.

It is generally desirable to have very low impedance looking into the parasitic branch of the network shown in Figure 5; however, in many broadband applications, a capacitor may be required to operate substantially above its series resonant frequency and at or near its parallel resonant frequency. In these applications, it may be more advantageous to select a capacitor that exhibits high loss at its F_{PR}, since the resultant notch depth at the parallel resonant frequency will be very shallow. Under these conditions, it likely that the attenuation notch will be low enough, i.e., less than 0.1 dB, making it non-discernible in the magnitude of S_{21}. This concept can be used to provide the basis for an excellent low loss broadband "one capacitor" DC block and coupling solution over a wide range of frequencies. The same considerations hold true for broadband bypassing and matching; however, the sign ($+j$ or $-j$) and magnitude of the impedance of the subject capacitor must also be considered, as inductive properties may adversely affect these applications.



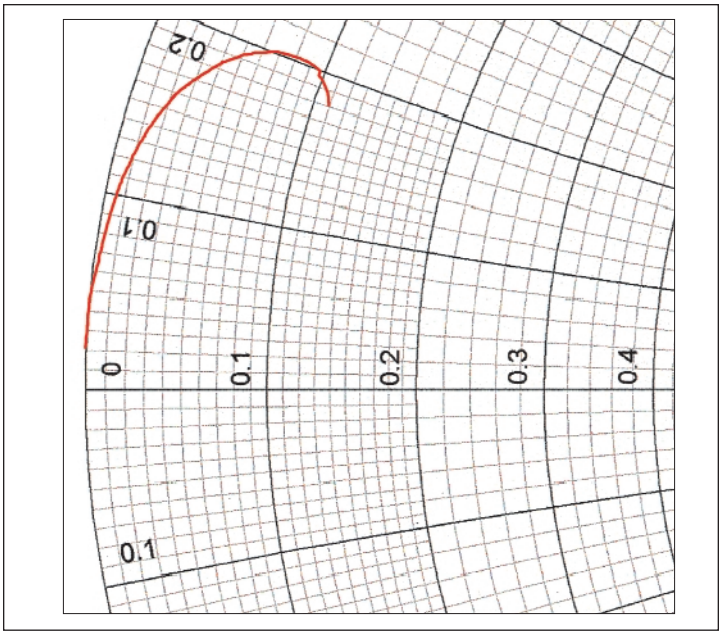
▲ **Figure 5. Nominal capacitor C_0 with parasitic elements.**

Another consideration worthy of mentioning applies to phase sensitive applications. There are rapid insertion phase transitions around zero degrees at and in proximity to the capacitor's parallel resonant frequency. This condition may cause excessive group delay, which is generally not well tolerated in phase sensitive applications. Group delay can be calculated by taking the first derivative of S_{21} insertion phase. It is especially important in these applications to know whether this resonance is present within the design passband and is generally best to avoid them if possible.

Effects of net inductance

When designing capacitors into a broadband bypassing circuit application, one of the first parameters to consider is the capacitor's parasitic inductance and its associated inductive reactance. The effects of the parasitic series inductance (ESL) and inductive reactance become more prominent at high frequencies, particularly in the region above the capacitor's series resonant frequency (F_{SR}). The net impedance decreases with increasing frequencies up to the series resonant frequency, however, as the frequency is increased above F_{SR}, the net impedance becomes inductive and gradually increases. It is acceptable to use a capacitor above its F_{SR}, as long as the inductive reactance does not become too large. A Smith chart analysis is essential for assessing the complex impedance of a device intended for these applications. Figure 6 shows a Smith chart presentation derived from a shunt to ground configuration measurement of an ATC 200A series 10 nF capacitor in the flat mount orientation, i.e. electrodes parallel to the substrate. A shunt to ground configuration was intentionally chosen, as it is best suited for evaluating the complex impedance of a capacitor intended to be used in a bypass application.

The results of a shunt measurement for the 10 nF capacitor are illustrated in the Smith chart plot in Figure 6. Table 2 summarizes the impedance data from the Smith chart illustrated in Figure 6 and tabulates the real and



▲ **Figure 6. Smith chart for the 10 nF capacitor in shunt configuration.**

reactive parts of the impedance referenced to a 50-ohm system at eight different frequencies. The table also shows the magnitude of the impedance as calculated from the vector sum of the real and reactive parts.

In order to achieve good bypass performance, the designer will opt for a low impedance and low inductive reactance. The ideal placement on the Smith chart for this configuration is at the outer rim along the real axis, i.e., zero resistance and zero reactance. This is achieved by selecting a capacitor that exhibits both low impedance and a low inductive reactance at the frequencies of interest. The 10 nF capacitor referenced above will serve as an excellent choice for bypass applications up to about 900 MHz.

As seen in Table 2, the impedance and inductive reactance look reasonably low for bypassing applications up to about 1800 MHz. However, at frequencies above 2600 MHz, the impedance and the level of inductive reactance are significant. The requirements of the design will determine whether this impedance is too high for use in bypass applications at these frequencies. An impedance magnitude of 10.82 ohms at 3.6 GHz for the subject device represents more than 20 percent of the network impedance and would not be a good candidate for bypassing or any other application at this frequency.

Frequency (MHz)	Real (Ω)	Reactive (Ω)	Impedance Magnitude (Ω)
50	0	+0	0
150	0	+*j* 0.4	0.4
450	0	+*j* 1.2	1.2
900	0	+*j* 2.4	2.4
1800	0.2	+*j* 5.2	5.20
2400	0.9	+*j* 7.6	7.65
3600	5	+*j* 9.6	10.82
4000	5.6	+*j* 8.8	10.43

▲ **Table 2. Complex impedance summary for the 10 nF shunt to ground configuration.**

The elements that make up a capacitor's parasitic inductance depend greatly on its physical design. A capacitor's form factor, i.e. ratio of length to width, plays a major role in the magnitudes of both ESR and ESL. Low parasitic resistance and inductance are achieved with form factors in which the width of the device approaches or exceeds its length dimension. For example, an ATC 180R series capacitor has a nominal length of 70 mils and a width of 105 mils, resulting in very low ESR and ESL. Other factors that influence a capacitor's parasitic elements include electrode composition, electrode pattern geometry, electrode count and spacing, case thickness and the dielectric's relative permittivity and loss tangent characteristics over frequency. Each one of these properties plays a part in the capacitors overall performance.

Likewise, the network environment that surrounds the device will prominently influence the net parasitic inductance. Details such as the mechanical and electrical properties of the substrate on which the capacitor is mounted, as well as the placement and dimensional matching between the width of the capacitor's terminations and the board traces, are factors that will all influence the net inductance. Other factors left up to the discretion of the circuit designer involve the placement and orientation of the capacitor relative to the ground plane. There are additional contributions of inductance from the interaction between the capacitor's closest electrode and its proximity to the ground plane. It is desirable to mount the device as close as possible to the ground plane by using thin boards wherever possible. The use of boards having a thickness in the order of 25 mils or less is preferable for minimizing the net inductance. Also, mounting orientation is yet another factor to be taken into account regarding its effect on the net parasitic inductance. Edge mounting a capacitor, i.e., electrodes normal to the ground plane, is typically taken as the optimal orientation, as it yields the benefit of greatly suppressing odd order parallel resonances.

In bypass applications the flat mount scenario with electrodes parallel to the ground plane may prove to be more advantageous because the net inductance resulting from this mounting orientation is lower. This also equates to a somewhat higher series resonant frequency. The designer must judiciously balance between the magnitude of net inductance and the depth of the in-band attenuation notches brought about by the presence of parallel resonances in order to determine the best mounting orientation for a given application. Evaluating the scattering parameters for the subject capacitor will always be helpful in determining this trade-off.

It is also advantageous to keep board traces as short as practical, especially between vias and neighboring devices. Inductance per unit length L_L is based on the relationship between the characteristic impedance of the substrate and the phase velocity and is stated as:

$$L_L = \frac{Z_0}{V_P} = \frac{Z_0\sqrt{\varepsilon_{EFF}}}{c} = \text{H per meter}$$

where

- L_L = inductance per unit length
- Z_0 = characteristic impedance in ohms
- V_P = phase velocity on microstrip = $c / \sqrt{\varepsilon_{EFF}}$
- c = speed of light in a vacuum (inches per second)
- ε_{EFF} = effective permittivity
- H = inductance in Henrys (H)

Examples

The following examples show calculations for determining the inductance per unit length for both Rogers RO4350 soft board and alumina. Both examples refer to a 50-ohm microstrip with typical trace width dimensions.

For convenience, c is converted from miles per seconds to inches per second by multiplying by 1.1785×10^{10}. Therefore, inductance per unit length is expressed in H per inch:

$$L_L = \frac{(1.1785\times10^{10})Z_0}{V_P} = \frac{(1.1785\times10^{10})Z_0\sqrt{\varepsilon_{EFF}}}{c}$$

Example 1:
Substrate = RO4350
ε = 3.48
ε_{EFF} = 2.83

For Z_0 = 50 ohms on microstrip
Substrate thickness = 20 mils
Trace width = 45 mils
Calculate inductance L_L in nH per inch for RO4350

Solution:

$$L_L = \frac{Z_0}{V_P} = \frac{Z_0\sqrt{\varepsilon_{EFF}}}{c}$$

$$= \frac{50\times\sqrt{2.83}}{1.1785\times10^{10}} \quad \text{(multiply by } 10^9 \text{ for nH)}$$

$$= 7.14 \text{ nH per inch}$$

L_L = 0.714 nH per 100 mils of trace.

Example 2:
Substrate = Alumina
ε = 9.9
ε_{EFF} = 6.47

For Z_0 = 50 ohms on microstrip
Substrate thickness = 25 mils
Trace width = 24.5 mils
Calculate inductance L_L in nH per inch for Alumina

Solution:

$$L_L = \frac{Z_0}{V_P} = \frac{Z_0\sqrt{\varepsilon_{EFF}}}{c}$$

$$= \frac{50\times\sqrt{6.47}}{1.1785\times10^{10}} \quad \text{(multiply by } 10^9 \text{ for nH)}$$

$$= 10.8 \text{ nH per inch}$$

L_L = 1.08 nH per 100 mils of trace.

As seen in these examples, the board traces will contribute significant amounts of additional inductance. In the example using Rogers soft-board, an increase of more than 0.7 nH per 100 mils of trace is contributed. Therefore, a capacitor exhibiting 0.6 nH of inductance mounted on this board with 100 mils of trace on either side will result in a net inductance of approximately 2 nH referenced at the far end of the traces. This represents an increase of more than twice that of the capacitor by itself. Likewise, the same capacitor mounted on an alumina substrate with 100 mils of trace on either side will result in a net inductance of 2.76 nH, an increase of more than three times that of the capacitor. Smaller trace widths should be avoided where possible, as they will contribute even higher levels of inductance. Another factor concerning the board layout is the diameter of vias, as they also contribute to the net inductance. The use of larger diameter via holes is preferable in order to minimize the associated inductance. All of the aforementioned factors will contribute to the net inductance and, therefore, must be carefully managed in the early stages of the design.

Effects of net impedance

The magnitude of a capacitor's impedance is equal to $\sqrt{(\text{ESR})^2 + (X_L - X_C)^2}$. As seen by this relationship, a capacitor's impedance is significantly influenced by its net reactance ($X_C - X_L$). This will serve as a good guideline for usability across the frequency band of interest. Knowing the magnitude of the impedance, especially at the lowest and highest frequency, is an important factor for all broadband applications. Ideally, the designer will be looking to achieve reasonably low impedance at both band edges.

The design philosophy suggested here is to simply select a large enough value of capacitance such that the corresponding impedance is low enough to provide a good through path at the lowest operating frequency. For example, a capacitor that exhibits a maximum impedance of 1 ohm at the lowest frequency represents 2 percent of the total impedance referenced to a 50-ohm network, which should provide an acceptable impedance criterion for most applications. If low impedance cannot be achieved across the desired frequency range using one capacitor, then it will be necessary to use multiple capacitors by selecting staggered capacitance values in order to meet the low impedance requirements throughout the entire passband. The

impedance of each capacitor will have to be low enough to provide for a good RF path over successive frequency segments. For a given capacitor, the impedance will become progressively lower as the frequency is increased reaching its lowest value at F_{SR} and will start to gradually increase at frequencies above F_{SR}, as seen in Figure 7.

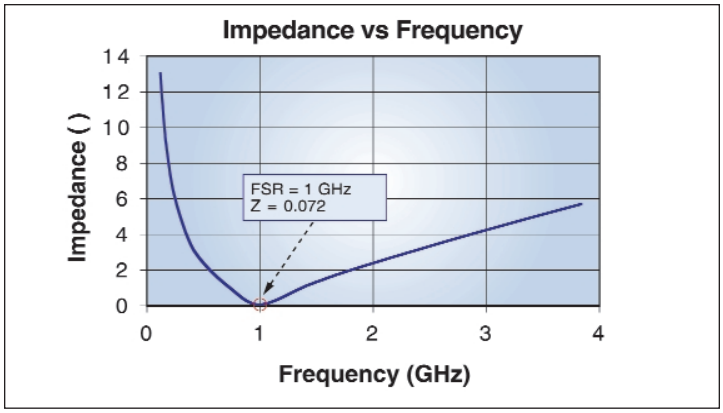
A high capacitance value will generally exhibit a suitably low impedance required for low frequency coverage as stated above; however, the capacitor's ESR should also be known at all frequencies within the passband, especially for frequencies above the capacitor's series resonant frequency. At the frequency where the electrode thickness is equal to or greater than one skin depth, the ESR will increase as the square root of f. Accordingly, the ESR will rapidly increase with increasing frequencies and will become a dominant factor in the net impedance.

Note that the net impedance below F_{SR} is capacitive and is dominated by 1 / ωC, therefore yielding a hyperbolic curve for frequencies less than F_{SR}. Conversely, the net impedance above F_{SR} is inductive and is dominated by ωL, therefore yielding a linear line segment for frequencies greater than F_{SR}. As illustrated by the impedance chart in Figure 7, the 100 pF capacitor would be suitable for most coupling applications from about 450 MHz through 1.8 GHz. For bypass and matching applications, the usability over frequency based on the impedance would be from about 450 MHz to 1 GHz. Frequencies in excess of 1 GHz are inductive and require S-parameter data to further assess the usable frequency range above F_{SR}.

Multiple capacitor approach

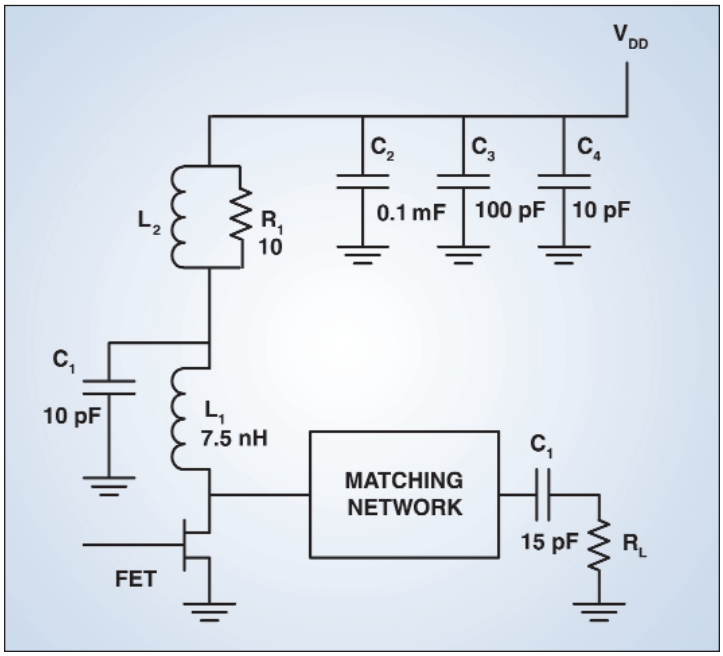
All of the guidelines outlined above for the single capacitor approach remain valid for the multiple capacitor scenario, however, the implementation of two or more capacitors will usually provide a more efficient solution while allowing for operation over a wider frequency spectrum. Small value resistors and inductors, as well as lossy ferrite beads, are sometimes used in conjunction with multiple capacitors that are connected in parallel, as they serve to electrically separate the capacitors as well as damping in-band resonances. At microwave frequencies, the inductance of a section of microstrip trace, typically in the order of 1 nH per 100 milliinches, may be used to isolate the capacitors in this configuration. In many instances, the capacitor's inherent parasitic elements will represent a significant contribution to the overall circuit and should always be included.

Broadband bypassing is a critical design matter that requires serious attention. Figure 8 shows a 1.9 GHz cellular FET amplifier with emphasis on the drain bias network. The circuit elements depicted in this figure will serve to suppress RF energy from getting onto the V_{DD} supply line, while providing high impedance at the drain in order to maintain optimum in-band RF gain. It also functions to keep noise generated by the power supply from appearing on the drain of the FET. High-speed switching environments created by switch mode power supplies (SMPS) will generate noise on V_{DD} supply lines.



▲ **Figure 7. Impedance versus frequency for an ATC100A101 (100 pF).**

The instantaneous current generated with fast rising and falling switch pulse edges can easily cause the V_{DD} supply line to ring. Since the losses within an SMPS are inversely proportional to switching frequencies, today's designs have spiraled these frequencies upward for a more efficient operation. RF energy generated from a typical SMPS operating anywhere from frequencies of 100 kHz to hundreds of megahertz must be prevented from appearing on the drain circuit. Spurious emissions generated by the SMPS consist of innumerable spectral components, which are generated by harmonics and intermodulation products of switched pulse edges. The resultant noise can easily include frequencies of up to several hundred MHz. The RF noise generated by SMPS switching is continuous and will generally occur up to frequencies equal to 0.35 / P_E, where P_E = pulse rise or fall time in seconds. For example, a switched pulse with a rise and fall time of 1.5 ns will yield spurious spectral components up to 233 MHz.



▲ **Figure 8. Diagram of a 1.9 GHz cellular FET amplifier with emphasis on the broadband drain bias network.**

Broadband drain bypass bias network

As illustrated in Figure 8, the FET's drain bias network consists of series inductive elements having an impedance of ωL and shunt capacitive elements with an impedance of $1 / \omega C$. Proper selection of these circuit elements in this bias network is essential, as they will serve to de-couple RF energy from the V_{DD} supply line to ground over a wide range of frequencies.

Since the capacitors exhibit a small parasitic inductance, there is an associated series (self) resonant frequency where

$$F_{SR} = \frac{1}{2\pi\sqrt{L_s C_0}}$$

At F_{SR}, the magnitude of the inductive and capacitive reactances are equal, and hence the net impedance ($\sqrt{(\mathrm{ESR})^2 + (X_L - X_C)^2}$) is equal to a small ESR value, typically expressed in milliohms. Accordingly, the designer will ideally select a capacitor that has an F_{SR} at or close to the desired "bypass frequency." This preference is based on establishing a low impedance path with minimal or zero net reactance, thereby making it ideal for bypassing applications.

As previously mentioned, it is essential that the capacitor's ESR and Q be taken into account at or near the parallel resonant frequency (F_{PR}) for all applications. F_{PR} usually occurs at more than twice F_{SR} for edge-mounted multilayer ceramic capacitors. At this frequency, the capacitor's impedance is likely to be high and inductive ($R + jX_L$) and may not provide an adequate RF path to ground. To alleviate this, the multiple capacitor approach uses two or more capacitors connected in parallel. They are selected such that their self-resonant frequencies are staggered in order to cover a wide range of frequencies with reasonably low loss. The number of required capacitive elements depends on the loss and impedance characteristics of each element over the intended frequency band segments.

From Figure 8, it can be seen that the inductors are in series with the drain and are not directly connected to reference RF ground. Accordingly, they rely on the by-pass capacitors C_1 through C_4 to obtain a low impedance path to ground. As a rule, inductor L_1 will have a reactance of at least 10 times higher than that of the transistor's drain impedance, whereas L_2 will be as large as possible. One caveat while selecting L_2 is to ensure that it is capable of handling the DC drain current with minimal IR drop. The combination of L_1 and C_1 will greatly suppress the in-band 1.9 GHz carrier frequency energy from appearing on the V_{DD} supply line. Inductor L_1 will act as a block at this frequency, while capacitor C_1 will serve to further suppress in-band RF energy by bypassing it to ground. L_2, C_2, C_3 and C_4 will suppress RF energy at frequencies below the 1.9 GHz carrier frequency, where the gain of the amplifier may be much higher. C_1's capacitance value is selected such that its F_{SR} is close to the amplifiers operating frequency.

Since C_1 is a shunt element, and the impedance is low at its F_{SR}, the RF energy at the operating frequency will be bypassed to ground. Capacitor elements C_2, C_3 and C_4 are staggered in value and are selected so that the impedance and inductive reactance of each will be low at successive frequency segments in order to offer continuous bypassing of frequencies below the amplifier's operating band. The use of ferrite beads may also be used in between the capacitive elements. Their inherently low Q offer good rejection of power supply noise over a wide range of frequencies, and they will also tend to isolate the effects of individual capacitive element.

Conclusion

This article has illustrated the various considerations for selecting capacitors for broadband applications. It has highlighted the frequency dependent properties of capacitors in relation to the parasitic elements and their implications to the various functional applications. Most important, it has been strongly suggested that capacitive elements be selected only after carefully and thoroughly evaluating both the circuit design requirement and the electrical and mechanical characteristics of the capacitor under consideration. ■

Author information

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