A 1 kW, 500 kHz FRONT-END CONVERTER FOR A DISTRIBUTED POWER SUPPLY SYSTEM

Loveday H. Mweene Chris A. Wright Martin F. Schlecht

Laboratory for Electromagnetic and Electronic Systems
Massachusetts Institute of Technology

ABSTRACT

The analysis, design, and performance of a prototype high power density converter suitable for use in the front-end of a distributed power supply system is presented. It delivers 1 kW to a regulated 40V distribution bus from the rectified utility. Its switching frequency is 500 kHz, and it uses a phase-shifted PWM technique to avoid primary side switching losses.

INTRODUCTION

This paper presents the analysis, design, and performance of a prototype high density converter that could be used as the front-end of a distributed power supply system. It accepts, as its input, the full range of the rectified utility (190V< V_{in} <380V), and it delivers 1 kW to a regulated 40V distribution bus. The switching frequency of the converter is 500 kHz, so its transformer (which has been designed to meet safety isolation requirements) and its filter elements are very small. The converter's efficiency at full load approaches 90%.

The converter's topology is a standard power MOSFET H-bridge that drives a transformer. The output of this transformer is rectified by a full bridge of Schottky diodes, as shown in Fig. 1. The switches of this forward converter are operated in a fixed frequency, PWM mode.

Given the inherent speed of majority carrier power devices, the switching frequency of a square-wave converter is limited by its parasitic reactive elements. For the converter discussed here, the dominant parasitic elements are the transformer's leakage inductor, the MOSFETs' output capacitors, and the rectifiers' junction capacitors.

Of these three groups of parasitic elements, the leakage inductor does not result in a direct switching loss. The double-ended nature of the H-bridge topology instead allows the leakage energy to be returned to the input. It is only important that the circulated leakage energy be made a small fraction (e.g. less than 10%) of the total energy delivered to the load each cycle. Doing so avoids excessive current stress for the MOSFETs and voltage stress for the rectifiers.

In contrast, the energy stored in the parasitic capacitors of a traditionally operated square-wave converter is dissipated each cycle, contributing to the switching losses. For a standard H-bridge converter operating under the conditions described here, the rectifier capacitors would cause a significant but tolerable amount of dissipation (about 2% of the output power). However, losses due to the MOSFET capacitors (an additional 4%) would be unnacceptable. Furthermore, since a MOSFET that is turning on must first pick up the load current before its voltage can collapse, significant switching losses would occur through this mechanism, as well.

To avoid these MOSFET switching losses, the converter of this paper is controlled with a special gate drive pattern that permits full recovery of the MOSFETs' capacitive energy. At the same time this drive scheme gives zero-voltage switching for the MOSFETs. This technique was used in [1] to measure transformer losses and in [2] to achieve a 250W, multiple output converter. In the second reference the drive technique was called "phase-shifted PWM". The purpose of this paper is to discuss the detailed operation of a converter using this technique.

PHASE-SHIFTED PWM

In the traditional operation of an H-bridge, the MOSFETs are turned on in opposite corner pairs (Q_1-Q_4 or Q_3-Q_2) to present the reflected input voltage to the output filter. Then, to achieve the freewheeling portion of the cycle, all of the MOSFETs are turned off, forcing the primary current to zero. The load current freewheels through the rectifiers, and the magnetizing current circulates through the loop formed by the secondary winding and the recitifers.

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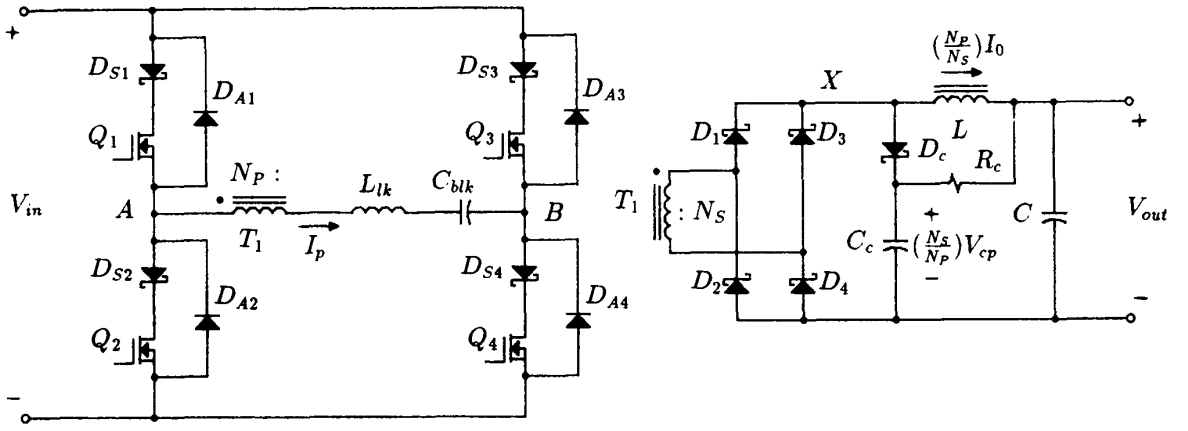


Figure 1: Schematic of the Power Circuit

In comparison, the phase-shifted PWM technique leaves two MOSFETs (either the top two or the bottom two) on during the freewheeling period. The load and magnetizing currents can therefore continue to flow in the primary winding. In fact, their commutation to the secondary side is resisted by the leakage inductance, and the total resistance of the transformer, the MOSFETs, and the rectifiers is not large enough to force a significant commutation during the freewheeling period.

Given this alternate method of control, the zero-voltage switching feature that results can be explained as follows. If Q_1 and Q_4 are on, and then Q_1 is turned off, the load and magnetizing current that had been flowing through Q_1's channel commutate to the parasitic capacitance of node A. This capacitance is the incremental parallel combination of the output capacitors of Q_1 and Q_2, the transformer's capacitance, and the reflected junction capacitors of the two off-state rectifiers, D_2 and D_3. The voltage at node A falls as the current discharges these combined capacitors until it reaches the bottom rail, where it is clamped by the antiparallel diode of Q_2. The waveforms of Fig. 2 show this transition.

As long as the negative gate drive for Q_1 is strong enough to avoid the Miller effect, this transition is completely lossless. Fortunately, the parasitic capacitance at node A acts as a snubber to make this condition easy to achieve.

At any time during the freewheeling period, Q_2 can be turned on losslessly with zero volts across it. It is only necessary to make sure this transition is sufficiently delayed with respect to the turn-off of Q_1 to avoid disrupting the lossless discharge of node A.

At the end of the freewheeling period, Q_4 is turned off, and the current flowing in the primary winding commutates to the parasitic capacitance of node B. This capacitance is the parallel combination of the capacitors from Q_3, Q_4, and the transformer's capacitance, but not from the rectifiers (which all remain on during this transition).

As the voltage across the transformer becomes negative, the secondary-side current starts to commutate from the D_1-D_4 path to the D_2-D_3 path. For a period of time all four rectifiers are on, and the voltage across the secondary is essentially zero. The voltage at node B (and, correspondingly, the transformer voltage) therefore appears across the leakage inductance, which has been drawn on the primary side in Fig. 1 for clarity in the following discussion.

An oscillation between the leakage inductance and the parasitic capacitance at node B ensues, according to the incremental model of Fig. 3. Note that the magnetizing inductance in this model has been replaced with a current source, I_m, since the transition under discussion is completed in a time too short for the magnetizing current to change significantly. If this oscillation were left to decay, both the final capacitor voltage and the final leakage inductor current would be zero.

The capacitor voltage starts at zero and the inductor current starts at I_o+I_m. The amplitude of the undamped current ring is therefore $I_o + I_m$, and the amplitude of the undamped voltage ring is

$$V_{osc} = (I_o + I_m)\sqrt{\frac{L_{lk}}{C_B}} \qquad (1)$$

By proper component selection, this voltage amplitude can be made larger than the input voltage ($V_{osc} > V_{in}$), so that the oscillation drives node B to the top rail. The antiparallel diode of Q_3 then turns on and clamps the voltage until the leakage inductance current falls below zero. During this clamping interval Q_3 can be turned on with zero switching losses.

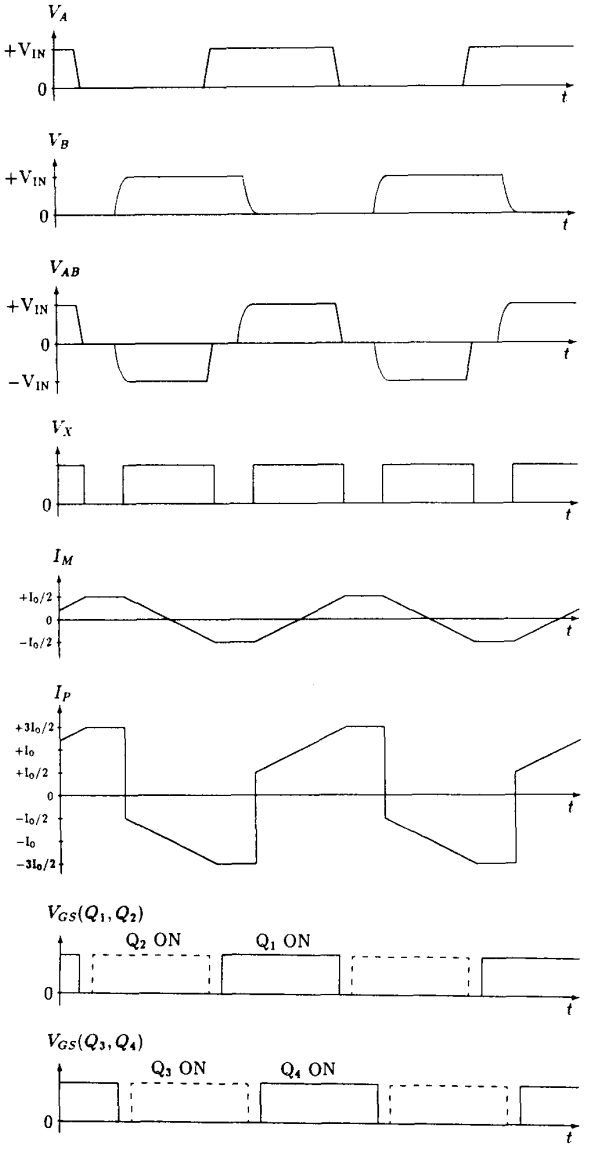


Figure 2: Waveforms for a 70% Duty Ratio

Once MOSFETs Q_2 and Q_3 are on, the transformer voltage is held at $-V_{in}$, regardless of the direction of the current. This negative voltage drives to completion the commutation of the secondary current from rectifiers D_1-D_4 to D_2-D_3. This point marks the end of the first half of the switching period.

The switching sequence in the second half of the period follows the reverse order of the sequence in the first half. First, Q_2 is turned off to let node A charge to the top rail, and Q_1 is turned on during the freewheeling period. Q_3 is then turned off, the voltage at node B rings to the bottom rail, and Q_4 is turned on during the clamping interval. Thus at no time is a MOSFET turned on or off with a non-zero voltage across it.

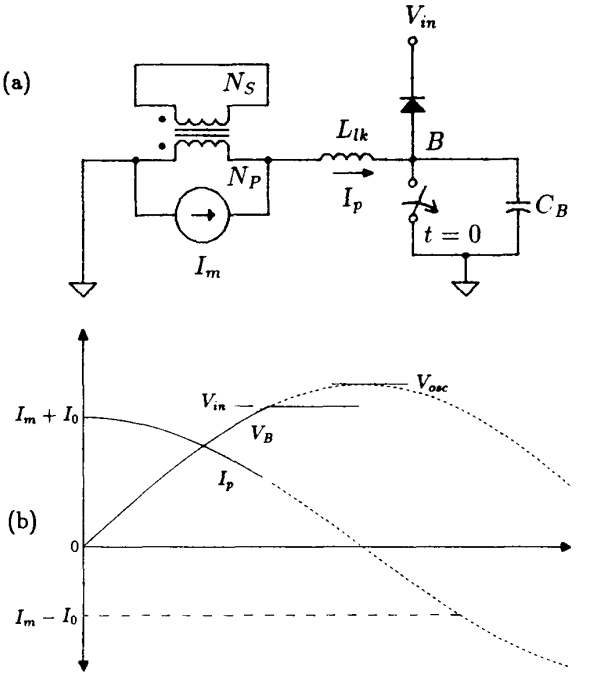


Figure 3: Incremental Model and Waveforms for Transition of Node B

As can be seen from the timing diagram of Fig. 2, all four MOSFETs are driven with a 50% duty ratio in this control scheme. The drives for Q_1 and Q_2 are opposite square-waves, with a sufficient dead time at each transition to permit the lossless charging of node A to be completed. Similarly, the drives for Q_3 and Q_4 are also opposite square-waves with dead times. To control the duty ratio of the H-bridge, the drives for the left and right legs are simply shifted in time with respect to one another. If the two drives are 180 degrees out-of-phase (meaning Q_4 is on whenever Q_1 is on), the duty ratio is 100%. If they are in phase (meaning Q_3 is on whenever Q_1 is on), the duty ratio is zero.

SPECIAL ISSUES

This section discusses several important details of the phase-shifted PWM operation that influence the converter's design and operation over the full load range.

First, note that during the transition of node A, the current flowing in the capacitor is always $I_o + I_m$, as

though it were driven by a current source. Therefore, given enough time, the voltage always reaches the new rail, but the length of time for this voltage transition is load dependent. If the magnetizing current is made large enough to complete this transition under light load within the shortest freewheeling period encountered, then the transition will always be lossless. If the new switch must be turned on before the rail is reached, however, then losses will occur. Since the capacitive losses are proportional to V^2, they will be negligibly small as long as the node voltage moved at least half way, and because these switching losses will occur under light load conditions, they can easily be handled by the heat removal system designed for full load dissipation.

Second, note that during the transition of node A, the voltage across the transformer has an average value of $V_{in}/2$ (assuming linear capacitors). The same is approximately true for the transition of node B. Even if these transitions were to occur simultaneously, therefore, the transformer voltage would effectively be zero for one half of the transition time, as depicted in Fig. 4. This limits the maximum duty ratio achievable. At light load, where only the magnetizing current drives the transitions, this loss of duty ratio is particularly significant.

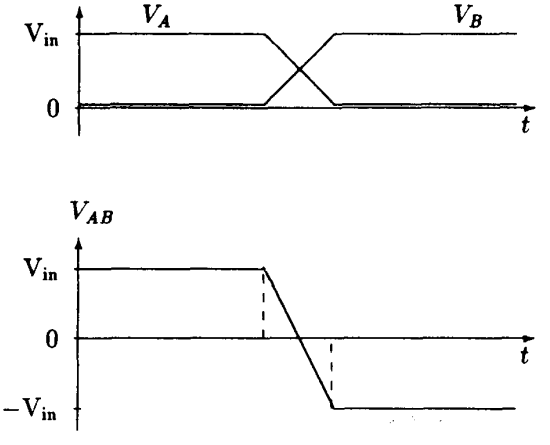


Figure 4: Duty-Ratio Lost Due to Transition Time

Third, if the amplitude of the voltage ring during the transition of node B is not large enough, the node voltage will not reach its new rail. The new MOSFET must then be turned on with a voltage across it. To minimize this voltage, the dead time between the off transition of the old MOSFET and the on transition of the new MOSFET should be

$$t_{dt} = \frac{\pi}{2}\sqrt{L_{lk}C_B} \qquad (2)$$

or one quarter of the oscillation period. The sensitivity of this timing is eased due to the peaking of the sinusoid, but since t_{dt} is quite short, typically 50 ns, care must be taken to be accurately time these signals. This value of dead time is guaranteed to turn the MOSFET on during the clamping interval as long as the node voltage rings high enough.

Fourth, the description of the transition of node B presented in the last section and depicted by the model of Fig. 3 assumed that all four rectifiers were on. This condition exists only until the leakage inductor current equals $I_m - I_o$, however. As Fig. 3b shows, the inductor's current rings around zero. When it reaches zero for the first time, the voltage at node B is at a peak, and Q_3 is turned on to end the oscillation. As long as I_m is less than I_o, therefore, the transition proceeds as described.

When, at light loads, I_m is greater than I_o, however, the transition follows the prescribed oscillation only until the leakage current reaches $I_m - I_o$, at which point rectifiers D_1-D_4 turn off and the secondary current is held constant by the output inductor. From that point on, the current charging the parasitic capacitor at node B is fixed at $I_m - I_o$.

Finally, since it is impossible to exactly balance the positive and negative volt-seconds across the transformer, it is necessary to place a relatively large capacitor in series with the primary, as shown in Fig. 1. The voltage across this capacitor during the freewheeling period can aid the commutation of the load and magnetizing current to the secondary side. As a result, the transition of node B may be greatly affected.

For instance, even if the capacitor voltage does not have a dc component, its ac voltage will be in the positive half of its cycle during the freewheeling period of Q_2-Q_4. This voltage therefore adds to the resistive and junction drops that appear across the leakage inductance. Any decrease in the primary current caused by this capacitor voltage directly reduces the starting current for the oscillation of node B. If the capacitor voltage is large enough to drive the primary current to zero, then there will be no current to charge node B losslessly, and a square-wave type switching loss will occur when Q_3 is turned on. This is a particular problem at light load where the primary current is already low.

The problem described above can be avoided by making the blocking capacitor large enough to ensure that there is only a small ac voltage across it. However, doing so does not solve the similar problem caused by the dc component of the capacitor voltage. In this case, the dc voltage aids the commutation during one freewheeling period and resists it during the other. It is therefore important to keep the gate drive timing balanced so that this dc voltage does not become too large.

CHOICE OF MAGNETIZING CURRENT

All of the issues discussed in the previous section

demonstrate how the lossless transitions are either slowed down or completely lost if the sum of the magnetizing and load currents is not large enough. For a given circuit design and output voltage, the magnetizing current always has the same value at the transitions, no matter what the input voltage. This is because the average of the positive volt-seconds (which is equal in magnitude to the average of the negative volt-seconds) placed across the transformer is proportional the output voltage.

The load current, however, can vary by a large amount. Therefore, to keep the sum of these currents large enough under light load conditions, it is necessary to have a relatively large magnetizing current. For instance, we could choose the peak magnetizing current to equal one half the maximum load current. The sum of the two would then vary by only a factor of 3 from full load to zero load.

The magnetizing current can be adjusted by changing the size of the transformer gap. The volume of the transformer core, its peak magnetic field, its core losses, and its leakage inductance are unaffected by this change.

What is affected is the rms value of the current carried by the MOSFETs and the primary winding. Figure 5 shows the sum of the magnetizing and load currents for the cases of 100% and 50% duty ratio, under the conditions suggested above. For the 100% case, the square of the rms current is

$$I^2_{rms}(d = 100\%) = \frac{13}{12} I_o^2 \qquad (3)$$

and for the 50% case, the square of the rms current is

$$I^2_{rms}(d = 50\%) = \frac{5}{3} I_o^2 \qquad (4)$$

For the 100% duty ratio case, the dissipation in the MOSFETs and primary winding is increased very little by the large magnetizing current. For the 50% duty ratio case the increase is larger, but still acceptable.

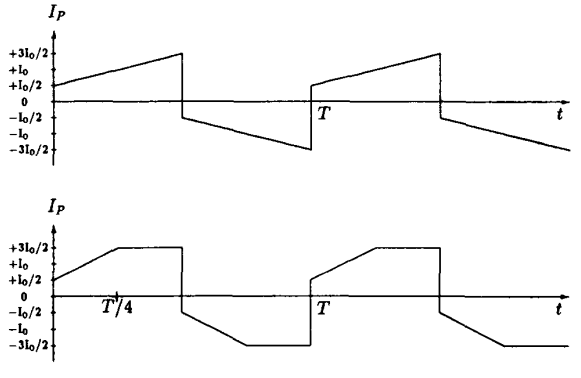


Figure 5: Primary Side Current for 100% and 50% Duty Ratios

CHARGING THE RECTIFIER CAPACITANCE

The one switching loss that the phase shifted PWM technique does not avoid is the charging loss that results from the rectifer capacitance. Actually, as described above, the capacitors of the rectifers that were off are losslessly discharged when node A makes its transition. However, after node B makes its transition to end the freewheeling period and the current in the secondary changes direction, the two previously conducting rectifiers must make a step change in voltage. Losses proportional to $\frac{1}{2}CV^2$ result, as explained below.

Figure 6 shows the incremental model appropriate for this portion of the cycle, with all pertinent components reflected to the primary side of the transformer. The capacitor is the parallel combination of the two rectifier junction capacitances. The inductor is the transformer's leakage inductance, and the resistor represents the losses throughout the circuit.

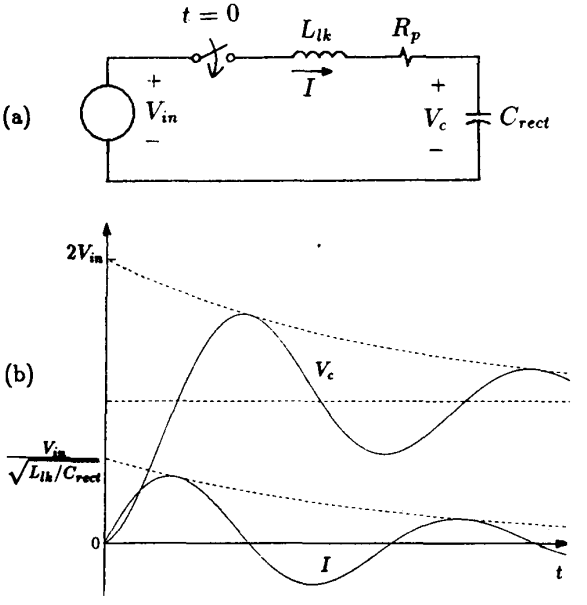


Figure 6: Incremental Model and Waveforms for Charging of the Rectifier Capacitance

Both the inductor current and the capacitor voltage of this incremental model start at zero. The oscillation that results causes the capacitor to ring around V_{in}, with a peak value that is twice as high. The amplitude of the current is V_{in} divided by the characteristic impedance.

Once the oscillation decays, the capacitor is charged to V_{in}. The energy that was drawn from the voltage source is QV_{in}, where Q is the final charge on the capacitor. If this capacitor were linear, $Q = C_{rect}V_{in}$, and an energy equal to $\frac{1}{2}C_{rect}V_{in}^2$ would have been lost.

The rectifier capacitors are nonlinear, however; they vary inversely with the square root of their voltage. If we define C_o as the value of the combined rectifier capacitors at V_{in}, then the total charge in these capacitors is

$$Q = \int_0^{V_{in}} \left(C_o \sqrt{\frac{V_{in}}{V}} \right) dV = 2C_o V_{in} \qquad (5)$$

and the total energy stored in them is

$$E_{rect} = \int_0^{V_{in}} \left(C_o \sqrt{\frac{V_{in}}{V}} \right) V\, dV = \frac{4}{3}\left(\frac{1}{2} C_o V_{in}^2\right) \qquad (6)$$

The energy lost during the charging process is therefore

$$E_{diss} = QV_{in} - \frac{4}{3}\left(\frac{1}{2} C_o V_{in}^2\right) = \frac{8}{3}\left(\frac{1}{2} C_o V_{in}^2\right) \qquad (7)$$

Clamping the Oscillation

Because the voltage stress on the rectifiers is already high (80V for a 40V output if the duty ratio is 50%), it is important to prevent the oscillation from increasing this stress by a factor of two if Schottky diodes are to be used. A voltage clamp is therefore needed across the rectifier bridge, as in Fig. 1. Figure 7 shows the incremental model and waveforms (assuming a linear rectifier capacitor) that result once this clamp is installed.

The energy that flows into this clamp can be computed as follows. Defining α as the angle of the oscillation cycle from when the capacitor voltage passes through V_{in} until the capacitor voltage reaches the primary-referred clamp voltage V_{cp}, then

$$\alpha = \sin^{-1}\left(\frac{V_{cp} - V_{in}}{V_{in}}\right) \qquad (8)$$

The leakage inductor current at the end of this period is

$$I(\alpha) = \frac{V_{in}\cos\alpha}{\sqrt{L_{lk}/C_{rect}}} \qquad (9)$$

This current flows into the clamp voltage, decreasing linearly with time, until it reaches zero. The duration of the clamping action is

$$\Delta t = \frac{L_{lk} I(\alpha)}{V_{cp} - V_{in}} \qquad (10)$$

and the energy flowing into the clamp is therefore

$$E_{cp} = \frac{I(\alpha) V_{cp}}{2}\Delta t = \frac{1}{2} L_{lk} I^2(\alpha)\left(\frac{V_{cp}}{V_{cp} - V_{in}}\right) \qquad (11)$$

This expression can be rewritten as

$$E_{cp} = \frac{1}{2} C_{rect} V_{in}^2 \left(\frac{(1+u)^2(1-u)}{u}\right) \qquad (12)$$

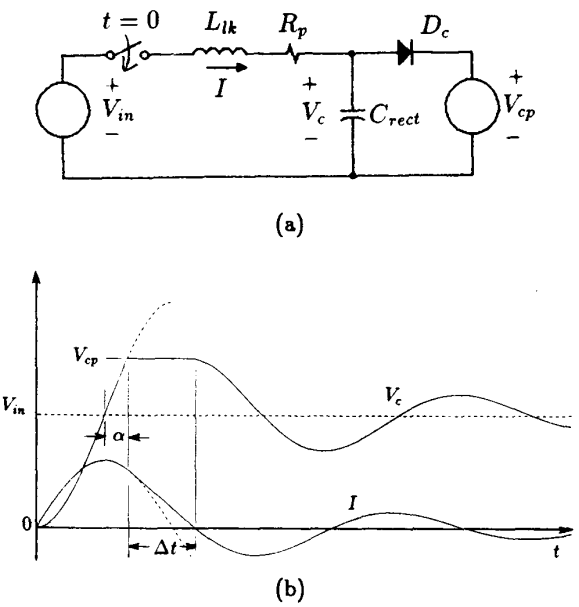


Figure 7: Incremental Model and Waveforms for Charging of the Rectifier Capacitance with Clamp Added

where

$$u = \frac{V_{cp} - V_{in}}{V_{in}} \qquad (13)$$

Thus energy delivered to the clamp equals the energy stored in the rectifier capacitors times a correction factor. Figure 8 shows how this correction factor varies with u.

To illustrate the use of this correction factor, assume that $V_{cp} = \left(\frac{N_p}{N_s}\right) 100V$. If $V_{in} = \left(\frac{N_p}{N_s}\right) 60V$ when the input voltage is in the middle of its range, $u = 2/3$, and

$$E_{cp} = \frac{1}{2} C_{rect} V_{in}^2 \left(\frac{25}{18}\right) \qquad (14)$$

This is only about 33% more energy than would have been lost without the clamp. On the other hand, when the input voltage is at the top of its range and $V_{in} = \left(\frac{N_p}{N_s}\right) 80V$, then $u = 1/4$ and

$$E_{cp} = \frac{1}{2} C_{rect} V_{in}^2 \left(\frac{75}{16}\right) \qquad (15)$$

This is a 4.7 times increase in energy, which can result in a substantial loss.

Not all the energy flowing into the clamp must be lost, however. If the clamp charge is discharged to the 40V output, then (with the assumptions made above) only 60% of the clamp energy calculated above is lost. The rest is delivered to the load.

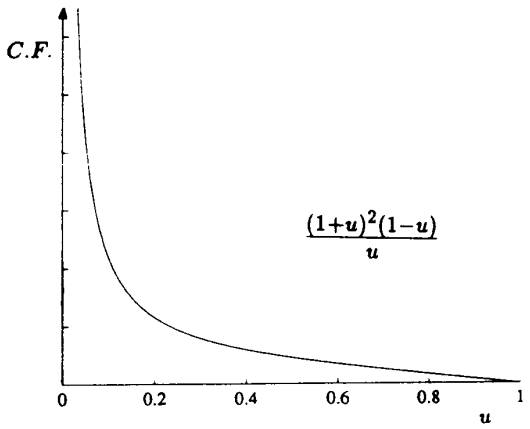


Figure 8: Correction Factor to Determine Clamp Energy

As a final point, once the clamping action is finished, the voltage across the capacitor in Fig. 7 returns to V_{in}. It does this by ringing with the leakage inductance, and as this oscillation decays, the additional energy lost is:

$$E = \frac{1}{2} C_{rect} (V_{cp} - V_{in})^2 \qquad (16)$$

If this oscillation does not decay before the end of the conduction period, it can affect the transition time of node A. The primary side current will be the sum of the load current, the magnetizing current, and this oscillation current. If the oscillation current is an appreciable fraction of the load current, the sum at the start of the transition can vary significantly depending on where in the oscillation cycle it begins.

Note that the loss analysis given above does not account for the nonlinear nature of the rectifier capacitors, as the issues are the same. The higher the clamp voltage, the less energy dissipated, but the higher the voltage stress on the rectifier.

THE CONTROL CIRCUIT

The control circuit for the prototype converter, shown in Fig. 9, is based on two standard high frequency PWM control ICs available from Unitrode, the UC3823 and the UC3901. The UC3901 senses the output voltage, compares it against a reference voltage, and produces a square-wave with an amplitude that is proportional to the error. The square-wave is passed through an isolation transformer and rectified to provide the feedback signal for the UC3823. This signal determines the duty ratio of the output of the UC3823. The UC3823 also provides soft-start and over-current protection features.

To translate the output of the UC3823 into the four gate drive signals needed for the H-bridge, TTL logic gates and delay lines, and one comparator, were used. The flip-flops divide the basic clock frequency by two, and they create one square-wave timed to the rising edge of the UC3823 output and one timed to its falling edge. The first (along with its inverse) is used to drive Q_1 and Q_2; the second is used to drive Q_3 and Q_4. The delay lines provide the required dead time between one square-wave gate drive signal and its inverse. The comparator sets the initial state of the flip-flops.

The actual gate driver (one of which is shown in the schematic of Fig. 9) is a DS0026 buffered by external MOSFETs driving a transformer, with the transformer output clamped by zener diodes. A large capacitor is used in series with the primary of the transformer to withstand the dc component of the drive voltage. Note that since the duty cycle of the gate drive signal is a square-wave, the voltage across the blocking capacitor remains constant at half the control voltage, independent of the effective duty ratio of the power converter.

One advantageous feature of the transformer drive for all four MOSFETs is that the gate drive goes negative when the MOSFET is off. This greatly improves the drive's ability to avoid the Miller effect. The energy lost driving the gates this way is four times higher, however, because the voltage swing is twice as large as normal.

Compensation of the Control

If the input bus capacitor is very large, the incremental model of the power circuit is a duty ratio controlled voltage source applied to an L-C filter that is in series with the load. In designing the compensation of our prototype, we treated the load as an incremental current source. If the load is composed of point-of-load converters, however, incrementally each of them will have a negative resistance in parallel with the input capacitors. There will also be inductance between the front-end and load converters, and the number of converters installed may vary. The eventual compensation of the front-end converter and the total distributed supply is therefore a more complicated process than we have accomplished here.

Assuming a current source load, Fig. 10 shows the transfer function (duty ratio to output voltage) of the power circuit. It also shows the transfer function we designed into the control circuit and the total loop transmission.

Since the output ripple is at 1 MHz, it would be possible to get the ripple attenuation required with an output filter tuned to 50 kHz. However, we wanted the loop transmission's cross-over to occur above the filter's resonance. Otherwise, the cross-over frequency must be much lower than the filter's resonant frequency and it is possible for the resonant peak to cause the loop transmission to pass through unity more than once. Bandwidth

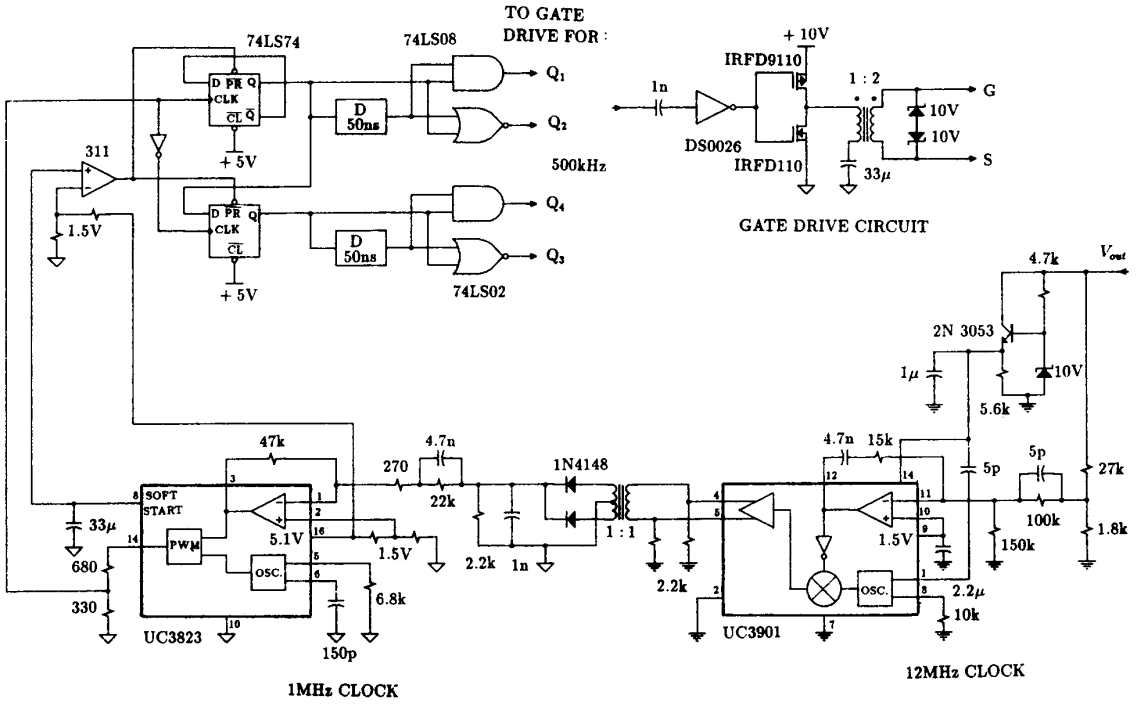


Figure 9: Control Circuit

limitations in the control circuitry forced us to place the cross-over frequency in the region of 50 kHz. As a result, the filters were tuned to a resonant frequency of 5 kHz. These filter elements are much larger than they could otherwise have been, a tradeoff which requires further investigation.

THE PROTOTYPE CONVERTER

Figure 11 shows the prototype power circuit constructed using the topology of Fig. 1 and the components listed in Table 1. The transformer was split into two separate parts to maintain a low profile. The primary windings of each part are connected in series, and the secondary windings are connected in parallel after their rectifier bridges (two diodes were needed for each bridge location to handle the current anyway, so the total number of output rectifiers remains unchanged). This connection guarantees that both the voltage and the current split equally between the two transformers.

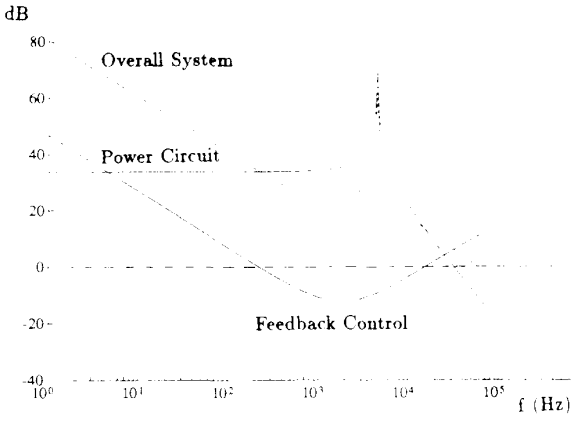
The schematic of Fig. 1 shows that each MOSFET has a series Schottky diode and an antiparallel bipolar diode. This was done to avoid conduction in the relatively slow body diode of the MOSFET in favor of a faster external diode. Our ultimate goal is to remove these additional

Part	Type	Part	Type
D_{1-4}	MBR10100	C_{blk}	1μF
D_C	50SQ100	C	47μF
D_{A1-A4}	MUR840	C_c	4.7μF
D_{S1-S4}	USD620	T_1 core	LP2232
Q_{1-4}	IRF350	L_{lk}	2μH
R_c	120Ω	L	26μH

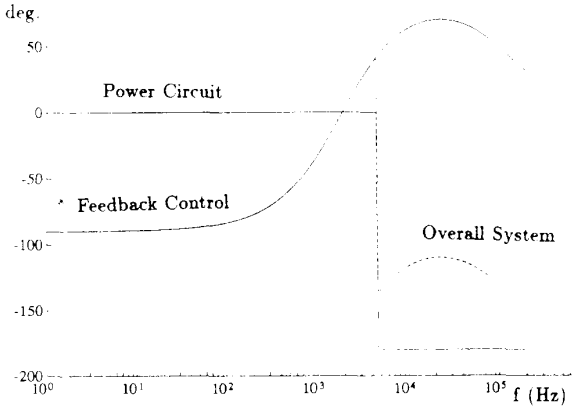
Table 1: Parts List for Prototype Power Circuit

parts, but we have not fully investigated the reliability of using the body diode in this manner. Furthermore, once these additional parts are removed, the body diode's recovery time will preclude any further increase in the switching frequency.

Figure 12 shows various operating waveforms from the experimental circuit. Figure 12a shows that the the drain-to-source voltage, V_{DS}, of Q_2 falls to zero prior to turn-on of the gate. Similarly, the turn-off transition shows that the channel has turned off, evidenced by the end of the plateau region on V_{GS}, before the drain-source voltage begins to rise. Figure 12b shows the voltages of nodes A and B of the bridge for a duty cycle of 75%.



(a) Magnitudes



(b) Phases

Figure 10: Frequency Responses

For the same duty cycle, the corresponding transformer voltage is shown in Fig. 12c. These bridge voltage measurements had to be made with the closed loop control disabled because the instrumentation affected the stability of the controller. Finally, the transformer's primary current at full power (1kW) is shown in Fig. 12d for an input voltage of 250V, where the current scale is 4A/div.

Figure 13 shows the response of the output voltage to a 40% step change in rated load current, from 15A to 25A. The lower trace in the Figure is the synchronizing signal used to control a high-speed MOSFET-switched load. The response to this load transient is the upper trace in the Figure, showing a 2V spike on the 40V dc output. Note that the absence of ringing in the transient response confirms the adequate stability provided by the controller compensation.

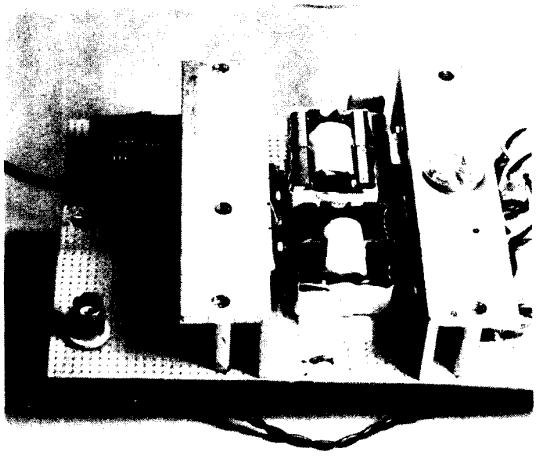


Figure 11: Prototype Power Circuit

Table 2 gives the measured efficiencies (±1%) at full load (1 kW) for a range of input voltages. Of the approximately 120W lost, 40W are due to the 0.8V forward drop of the 100V Schottky rectifiers. Another 20W are lost in the clamp circuit for the rectifiers. The switches of the H-bridge have approximately 45W of conduction losses, and each transformer dissipates about 2.5W. The control circuit requires 10W, most of which goes to the gate drives.

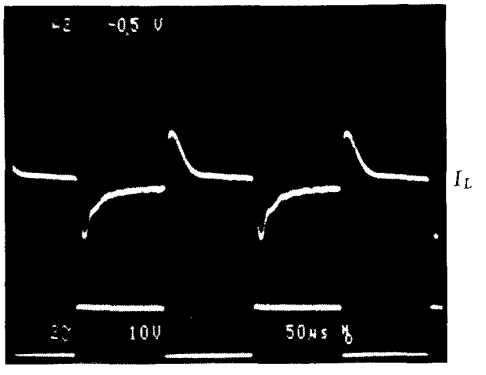


Figure 13: Transient Response of Prototype Power Circuit

CONCLUSIONS

The phase-shifted PWM control technique permits a 1 kW off-line converter to be operated efficiently in the 1 MHz range. While it is necessary to make the magnetizing current relatively large (e.g. one half the maximum

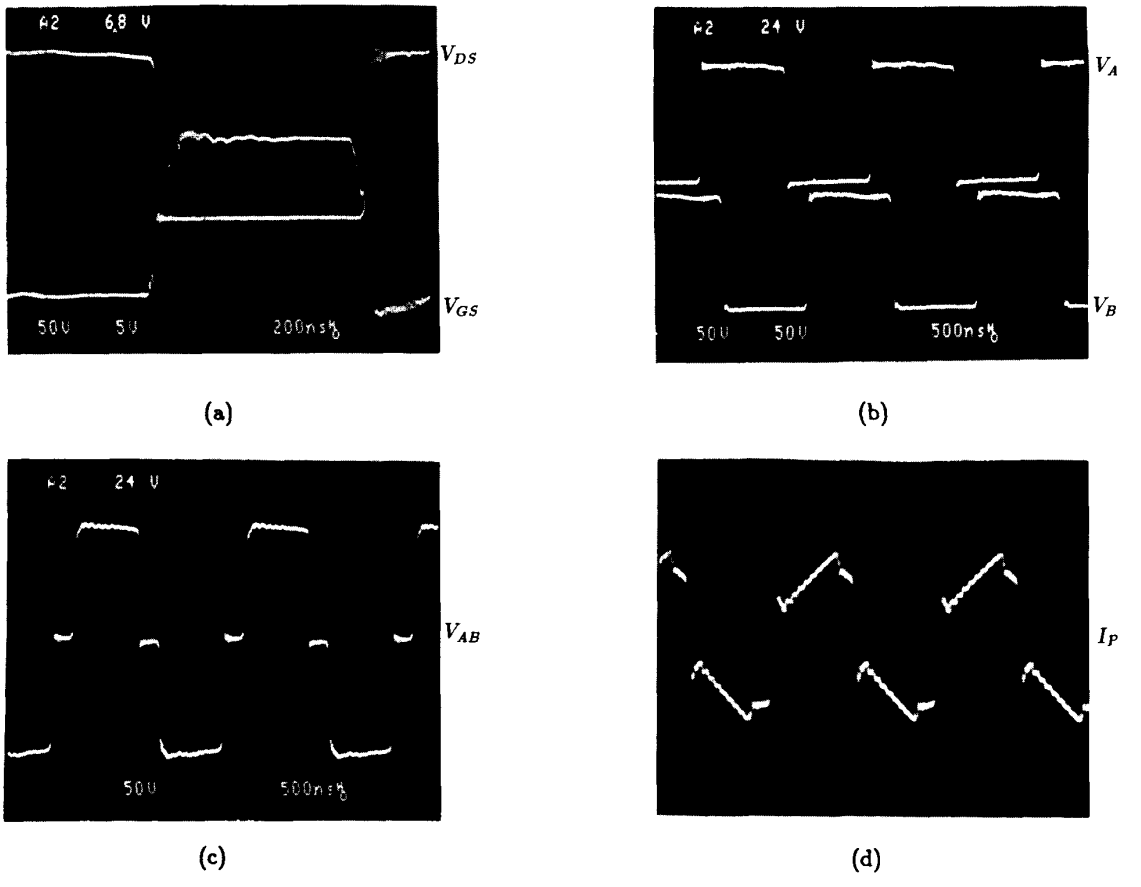


Figure 12: Waveforms from Prototype Power Circuit

load current) to ensure that the converter achieves lossless transitions over the full range of load current, the additional losses caused by this current are tolerable. The dominant losses are in the rectifier stage (due to both conduction and switching mechanisms). Better Schottky diodes (or synchronous rectifiers) and an energy recovering clamp circuit would therefore significantly improve the overall conversion efficiency.

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	Input Voltage volts	Duty Ratio %	Efficiency %
High Line	380	43	87
Mid Line	250	65	89
Low Line	200	85	90

Table 2: Measured Efficiency of Prototype Power Circuit

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