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An Asymmetrical Half Bridge Flyback Converter with Zero-Voltage and Zero-Current Switching

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***Abstract*—In this paper, the analysis and design of an asymmetrical half bridge flyback DC-DC converter is presented, which can minimize the switching power loss by realizing the Zero-Voltage-Switching (ZVS) during the transition between the two switches and the Zero-Current-Switching (ZCS) on the output diode. As a result, high efficiency can be achieved. The principle of the converter operation is explained and analyzed. In order to ensure the realization of ZVS in operation, the required interlock delay time between the gate signals of the two switches, the transformer leakage inductance, and the ZVS range of the output current variation are properly calculated. Experimental results from a 8V/8A, 200kHz circuit are also presented, which verify the theoretical analysis.**

I. Introduction

To realize high switching frequency and high efficiency at the same time, the soft switch technology is introduced, which aims to reduce the switching power loss by turning on/off the switch when the voltage across it and/or the current through it is zero at the switching instant.

Among the topologies used in the soft switch technology, the asymmetrical half bridge converter is investigated due to its simple circuit configuration and the high flexibility. In this converter, the two switches build a half bridge, the resonance between the parasitic capacitance of the switch and the leakage inductance of the transformer is utilized to achieve the zero voltage across the switch, and there is no need to insert additional components to produce resonance. This simple configuration of the half bridge converter also enables the cost to be reduced with the smallest number of components. Moreover, the half bridge converter has the advantage of high flexibility. Based on the half bridge topology, a family of the soft switch converters can be developed [1]. If a center taped transformer is used in the circuit, the converter could function as a forward type converter [2], [3]; or with a complementary polarity transformer, the flyback type converter is available [4], [5], [6].

During the resonance, the peak resonant voltage and the peak resonant current do not go beyond the input voltage and the output current, and the device stress level is low. The resonance process happens only during the transition between the two switches, this maintains the low conduction power loss. Another advantage of this converter is that the simple constant frequency pulse width modulation (PWM) control method can be utilized.

In the asymmetrical half bridge flyback converter, the two switches in the half bridge operate in asymmetrical mode, which means that the two switches turn on/off complementarily and their duty ratios are D and $(1 - D)$ respectively. Between the transition of the two switches, a small dead time is introduced. During the dead time, a partial resonance process happens, which makes it possible to turn on and off the switch at zero voltage. The output diode is turned on and off at zero current. Therefore, both ZVS and ZCS are achieved in this converter. As a result, the switching power loss in the circuit can be minimized, and the value of the dv/dt and di/dt in the fast switching transitions is limited.

In the previous publications [4], [5], [6], the asymmetrical half bridge flyback converter has been analyzed in the steady state, the voltage transfer ratio has been investigated, and the realization process of the ZVS has been analyzed in detail.

During the resonance process which realizes ZVS, the energy stored in the transformer leakage inductance must be large enough to discharge the voltage across the switch to zero. Once the voltage across the switch reaches zero, the switch should be turned on properly, otherwise, the resonance process will continue and cause the voltage larger than zero again, which prevents achieving the ZVS. From the analysis, it can be seen that there are four parameters which can influence the realization of the ZVS: the transformer leakage inductance, the parasitic capacitance of the switch, the interlock delay time between the gate signals of the two switches, and the load current. Therefore, if we want to maintain the ZVS transition during the variation of the output current, the transformer leakage inductance and the interlock delay time should be designed properly. On the other hand, with a known transformer leakage inductance value, the range of the output current variation should be selected carefully such that the ZVS transition is maintained during the converter operation. Such information is not available in the past work.

In this paper, the detailed analysis of the circuit topology and design process will be presented. The design of the transformer leakage inductance, the ZVS range of the output current variation, and the interlock delay time between the gate signals of the two switches to ensure the ZVS transition will be described. A 8V/8A, 200kHz experimental converter is built and tested, the results are utilized to verify the theoretical analysis.

II. Principle of Operation

Fig.1 is the topology of an asymmetrical half bridge flyback converter.

To simplify the analysis of the circuit operation, the following assumptions are provided:

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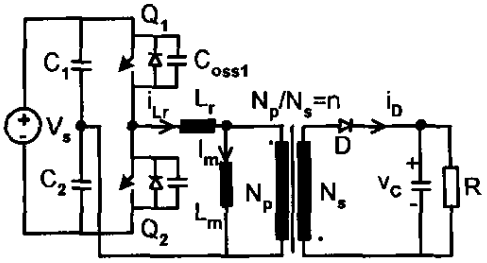

Fig. 1. The asymmetrical half bridge flyback converter

- C_1 and C_2 are large enough so that V_{C1} and V_{C2} are almost constant (ripple neglected), which equal to $(1-D)V_s$ and DV_s respectively,
- the transformer secondary side leakage inductance is neglected,
- the output capacitance of the two switches are constant during operation, and satisfy $C_{oss1} = C_{oss2} = C_{oss}$,
- L_m is large enough so that I_m is ripple free,
- C is large enough so that V_o is ripple free,
- all elements of the circuit are lossless.

Fig.2 shows the theoretical waveforms of the AHBC, and the

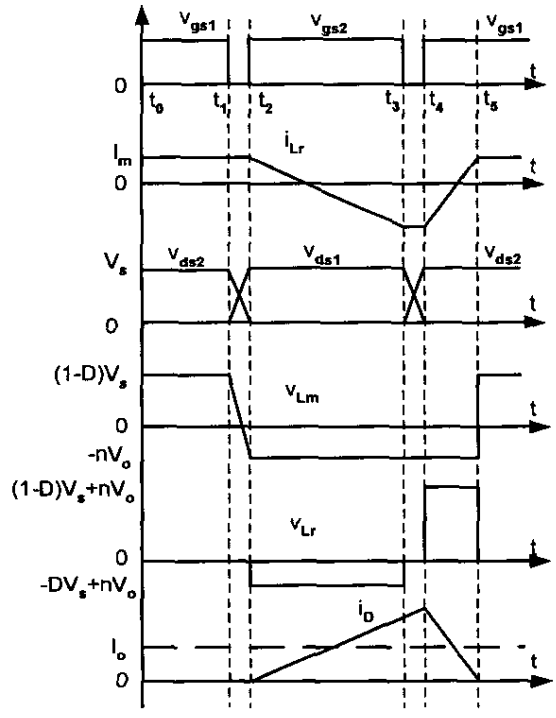

Fig. 2. Waveforms explaining basic operation of the converter

following is the description of each stage in detail:

Stage 1: [Fig.3(a)] (t_0–t_1)

Switch Q_2 is off, Q_1 conducts the primary side current i_{Lr}, which is also the current flowing through the transformer magnetizing inductance L_m, $v_{Lm} = (1-D)V_s$. The voltage across

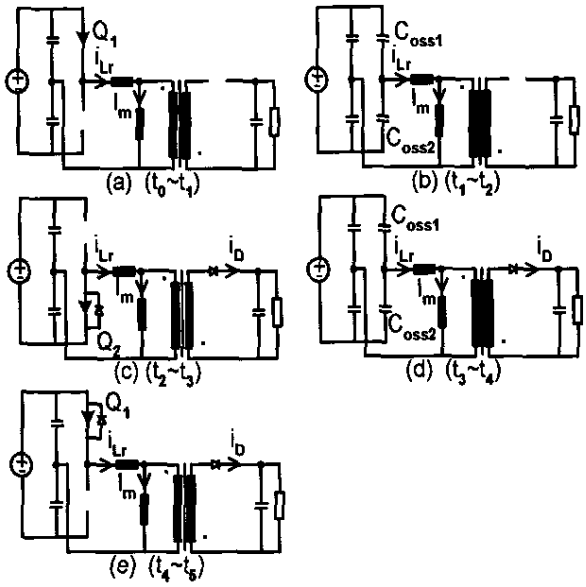

Fig. 3. Equivalent circuits for each stage in operation

Q_1 is zero, and $v_{ds2} = V_s$. The output diode D is off, $i_D = 0$.

Stage 2: [Fig.3(b)] (t_1–t_2)

At t_1, Q_1 turns off, the primary side current i_{Lr} flows through the two switches output capacitors C_{oss1} and C_{oss2}, charging C_{oss1} and discharging C_{oss2}. Since C_{oss1}, C_{oss2} and L_r are very small compared to L_m, i_{Lr} almost keeps constant, the charging and discharging processes are about linear. At t_2, v_{ds2} decreases to zero.

Stage 3: [Fig.3(c)] (t_2–t_3)

i_{Lr} flows through the body diode of Q_2, the output diode D turns on at zero current, the voltage across the magnetizing inductance $v_{Lm} = -nV_o$, $v_{Lr} = -DV_s + nV_o$, i_{Lr} begins to decrease linearly, $i_D = n(I_m - i_{Lr})$ increases linearly. Q_2 can be turned on at zero voltage. After i_{Lr} becomes negative, it flows through Q_2.

Stage 4: [Fig.3(d)] (t_3–t_4)

At t_3, Q_2 turns off, i_{Lr} now flows through C_{oss1} and C_{oss2}, discharging C_{oss1} and charging C_{oss2} linearly. At t_4, v_{ds1} decreases to zero.

Stage 5: [Fig.3(g)] (t_4–t_5)

i_{Lr} flows through the body diode of Q_1, Q_1 can be turned on at zero voltage. $v_{Lr} = (1-D)V_s + nV_o$, i_{Lr} begins to increase linearly. After i_{Lr} becomes positive, it will go through Q_1. i_D decreases linearly. At t_5, i_D decreases to zero, the output diode D turns off naturally at zero current. Another switching cycle repeats.

III. DC ANALYSIS

A. Simplified voltage transfer ratio

Since the zero voltage transition between the two switches are very small compared to the static operation period, it can be neglected in the DC analysis first. If we also neglect the influence of the transformer leakage inductance, by applying the

volt-seconds balance to the transformer magnetizing inductance L_m, we can easily derive the simplified voltage transfer ratio. When Q_2 on, D on, the voltage across L_m is $-DV_s$, which should be equal to the reflected output voltage $-nV_o$. Therefore,

$$\frac{V_o}{V_s} = \frac{D}{n}. \tag{1}$$

Actually, due to the existence of the transformer leakage inductance L_r, the volt-seconds applied to the transformer is reduced, and this will influence the output voltage. In the next subsection, we will derive the revised voltage transfer ratio which considers the influence of L_r.

B. Revised voltage transfer ratio

Neglecting the influence of the ZVS transition between the two switches and applying the volt-seconds balance to the transformer magnetizing inductance L_m, we can achieve

$$(1-D)V_s\Delta t_1 + (-nV_o)[\Delta t_3 + \Delta t_5] = 0, \tag{2}$$

$$\Delta t_1 = DT - \Delta t_5, \tag{3}$$

$$\Delta t_3 = (1-D)T, \tag{4}$$

$$\Delta t_5 = \frac{L_r[I_m - i_{Lr}(t_3)]}{(1-D)V_s + nV_o}. \tag{5}$$

$$V_o = \frac{(1-D)V_s\Delta t_1}{n(T-\Delta t_1)}. \tag{6}$$

Δt_i is the time period of stage i (i=1, ..., 5), and $i_{Lr}(t_3)$ is the value of the primary side current at time t_3.
$i_{Lr}(t_3)$ can be calculated approximately:

$$i_{Lr}(t_3) = I_m - \frac{DV_s - nV_o}{L_r}(1-D)T. \tag{7}$$

Then Δt_1 and Δt_5 can be calculated accordingly:

$$\Delta t_1 = \frac{nV_o}{(1-D)V_s + nV_o}T, \tag{8}$$

$$\Delta t_5 = \frac{DV_s - nV_o}{(1-D)V_s + nV_o}(1-D)T. \tag{9}$$

And, since the average value of i_D is the output current I_o,

$$I_o = \frac{n[I_m - i_{Lr}(t_3)](T-\Delta t_1)}{2T}. \tag{10}$$

Therefore, the revised output voltage can be derived:

$$V_o = \frac{(1-D)V_s}{n} * \frac{nD(1-D)V_s - 2L_rf_sI_o}{n(1-D)^2V_s + 2L_rf_sI_o}. \tag{11}$$

From Eqn.11, it can be seen that if $L_r = 0$, the revised voltage transfer ratio is just same as the simplified voltage transfer ratio shown in Eqn.1.

IV. Design Considerations

A. Transformer leakage inductance L_r

The advantage of the asymmetrical half bridge flyback converter is the realization of the zero voltage transition between the two switches during the operation. To ensure the zero voltage transition, the transformer leakage inductance L_r should be designed properly. At stage 4 [Fig.2 and Fig.3(d)], the energy stored in L_r must be large enough to discharge v_{ds1} from V_s to zero and charge v_{ds2} from zero to V_s. Therefore,

$$\frac{1}{2}L_ri_{Lr}(t_3)^2 > \frac{1}{2}C_{oss1}V_s^2 + \frac{1}{2}C_{oss2}V_s^2. \tag{12}$$

The average value of the primary side current i_{Lr} should be zero, so that the voltage across the two input capacitor C_1 and C_2 can keep constant. Therefore, from

$$I_m = i_{Lr} + i_D/n, \tag{13}$$

we can get:

$$I_m = I_o/n. \tag{14}$$

From Eqn.7, Eqn.11 and Eqn.14,

$$L_r \geq 2C_{oss}\left(\frac{nXV_s}{2n(1-D)V_sI_o - XI_o}\right)^2. \tag{15}$$

$$X = n(1-D)^2V_s + 2L_rf_sI_o. \tag{16}$$

The above equation can be solved by matlab or other mathematical tools. First, we can define the following function:

$$y = L_r - 2C_{oss}\left(\frac{nXV_s}{2n(1-D)V_sI_o - XI_o}\right)^2, \tag{17}$$

then assume a range of L_r, plot the curve of y in Matlab. After that, we can check if a suitable L_r value can be achieved such that y is larger than zero. If not, the assumed L_r range should be enlarged, and then repeat the process until a suitable L_r value is available.

B. ZVS range of the output current I_o

If the value of the transformer leakage inductance is already known, Eqn.17 can also be used to calculated the ZVS range of the output current. First we can assume a range on the output current I_o, and then use Eqn.17 to plot the curve of y vs. I_o. The ZVS transition is possible for those values of I_o where the corresponding y is greater than zero.

C. The gate signal interlock delay time t_{id} design

To realize the zero voltage transition between the two switches, the interlock delay time t_{id} between the gate signals of the two switches should also be designed properly.
In stage 2 [Fig.2 and Fig.3(b)], the interlock delay time t_{id1} between Q_1 off and Q_2 on should be large enough for v_{ds2} decreasing to zero, and its maximum limit is when the primary side current i_{Lr} reaches zero during stage 3 [Fig.2 and Fig.3(c)]. In stage 4 [Fig.2 and Fig.3(d)], the interlock delay time t_{id2} between Q_2 off and Q_1 on should be large enough for v_{ds1} decreasing to zero, and its maximum limit is when i_{Lr} reaches zero during stage 5 [Fig.2 and Fig.3(e)]. If the switch is still not turned on after i_{Lr} reaches zero, The resonance between

L_r, C_{oss1} and C_{oss2} will continue, and accordingly, v_{ds1} or v_{ds2} will increase from zero again. As a result, when the switch turns on, ZVS is not achieved.

In stage 3 [Fig.2 and Fig.3(c)], when i_{Lr} changes from I_m to zero, the transition time is t_{r3}, and in stage 5 [Fig.2 and Fig.3(e)], when i_{Lr} changes from $i_{Lr}(t_3)$ to zero, the time is t_{r5}. Therefore, the interlock delay time setting should satisfy:

$$\Delta t_2 \le t_{id1} \le t_{r3}, \tag{18}$$

$$\Delta t_2 = \frac{2C_{oss}V_s}{I_m}, \tag{19}$$

$$t_{r3} = \frac{L_r I_m}{DV_s - nV_o}, \tag{20}$$

$$\Delta t_4 \le t_{id2} \le t_{r5}, \tag{21}$$

$$\Delta t_4 = \frac{-2C_{oss}V_s}{i_{Lr}(t_3)}, \tag{22}$$

$$t_{r5} = \frac{-L_r i_{Lr}(t_3)}{(1-D)V_s + nV_o}. \tag{23}$$

Applying Eqn.14, Eqn.7, and Eqn.11,

$$\Delta t_2 = \frac{2nC_{oss}V_s}{I_o}, \tag{24}$$

$$t_{r3} = \frac{X}{2nf_sV_s}, \tag{25}$$

$$\Delta t_4 = \frac{2nC_{oss}XV_s}{2n(1-D)V_sI_o - XI_o}, \tag{26}$$

$$t_{r5} = \frac{2n(1-D)L_rV_sI_o - L_rXI_o}{n^2(1-D)^2V_s^2}. \tag{27}$$

If we want to design a suitable interlock delay time t_{id1} and t_{id2} to maintain the zero voltage transition under different load cases from I_{omin} to I_{omax}, first, the four transition time could be calculated by using matlab or other mathematical tools in the range of the output current I_o. From the calculated values, the limits for the interlock delay time could be set, and then we can design t_{id1} and t_{id2} according to their limits.

V. Experiment Results

An experimental circuit is built to verify the above analysis, its specifications are as follows:

- input voltage: $V_s = 45V$,
- output voltage: $V_o = 8V$,
- maximum output current: $I_{omax} = 8A$,
- switching frequency: $f_s = 200kHz$, $D = 0.4$.

The circuit parameters are listed as:

- $C_1 = C_2 = 0.47\mu F$, $C = 440\mu F$,
- output schottky diode: MBR1035, $V_F = 0.57V$,
- switches: IRF530, $R_{DS(on)} = 0.16\Omega$.
  $C_{oss(eff)} = 380pF$ ($V_{ds} = 0V$ to $50V$).
  $C_{oss(max)} = 1300pF$.
- transformer core: TDK ETD34,
- $n = N_p/N_s = 2$, $L_m = 370\mu H$, $L_r = 1.43\mu H$.

Fig.4 shows the experimental waveforms of the voltage across the transformer primary side V_{pri} and the voltage across the secondary side V_{sec}.

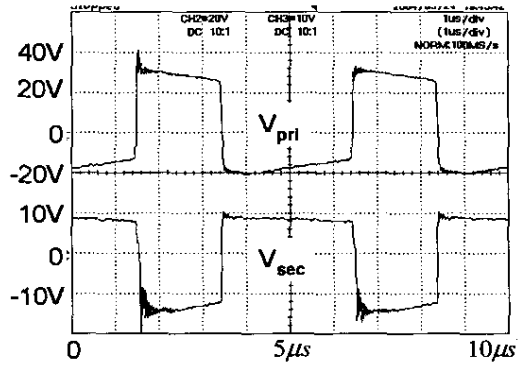

Fig. 4. Experimental waveforms of V_{pri} and V_{sec}

Fig.5 shows the experimental waveforms of the transformer primary side current i_{Lr} and the current flowing through the output diode i_D. It can be seen that the diode is turned on and turned off at zero current.

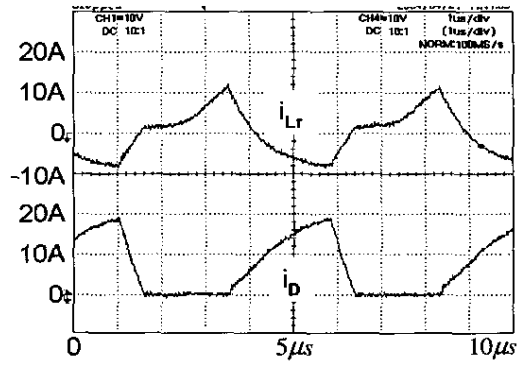

Fig. 5. Experimental waveforms of i_{Lr} and i_D

A. Transformer leakage inductance L_r

From the above analysis, the design consideration for the transformer leakage inductance L_r has been provided (Eqn.15). According to the circuit specifications and parameters, the required L_r value to realized ZVS from 50% (4A) to maximum output current (8A) is calculated and plotted according to Eqn.17, the result is shown in Fig.6. It can be seen that to realize the ZVS transition (y larger than zero), L_r must be larger than $0.1\mu H$. In the experiment circuit, the transformer leakage inductance is measured to be $1.43\mu H$, which has already met this requirement.

In the actual operation, the output capacitance of the switch is not constant but changes according to the voltage across the switch, therefore, the actual transformer leakage inductance required may be different from the theoretical values calculated above. To leave a safety margin, in the calculation, we can use the maximum value of the output capacitance $1300pF$ instead of the effective value $380pF$. As a result, the new calculated L_{rmin} is $0.25\mu H$. With the transformer leakage inductance of $1.43\mu H$ in the experiment, the requirement is still satisfied.

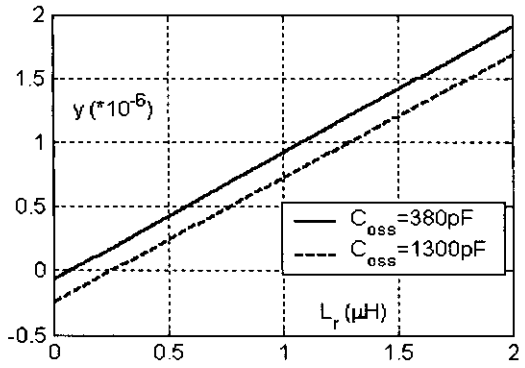

Fig. 6. Transformer leakage inductance requirement

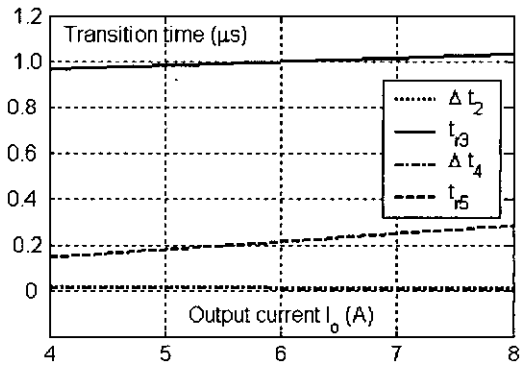

Fig. 8. Transition time requirement

Therefore, the zero voltage transition is ensured. This can be verified from the switching waveforms achieved in the experiment.

B. ZVS range of the output current I_o

Since $L_r = 1.43uH$, based on Eqn.17, the ZVS range of the output current can be calculated. From the curve y vs. I_o shown in Fig.7, it can be seen that when I_o is larger than 0.9A, the ZVS transition can be realized.

After considering the safety margin and using 1300pF as the output capacitance value of the switch, we can get the result that the ZVS range is when I_o larger than 1.8A.

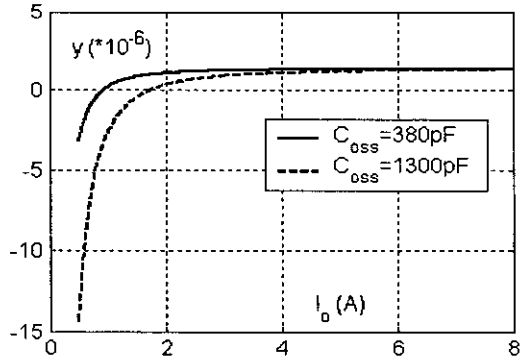

Fig. 7. ZVS range of the output current

C. Interlock delay time t_{id}

How to set t_{id} properly has been covered in the above analysis. The minimum limit is when the voltage across the switch parasitic capacitance v_{ds1} or v_{ds2} decreases to zero, and the maximum limit is when the transformer primary side current i_{Lr} reaches zero.

Based on Eqn.24–Eqn.27, the transition time Δt_2, t_{r3}, Δt_4, t_{r5} needed from 50% to maximum output current are calculated, and shown in Fig.8.

Then the needed interlock delay time t_{id1} and t_{id2} could be found out.

$$t_{id1min} = max\{\Delta t_2\} = 16ns, \tag{28}$$

$$t_{id1max} = min\{t_{r3}\} = 0.96\mu s, \tag{29}$$

$$t_{id2min} = max\{\Delta t_4\} = 8ns, \tag{30}$$

$$t_{id2max} = min\{t_{r5}\} = 150ns. \tag{31}$$

It can be seen that the maximum limit for the transition from Q_1 to Q_2 is very large, almost $1\mu s$, therefore, there will be no problem in this transition. What we need to consider carefully is only the transition from Q_2 to Q_1. According to the interlock delay time calculated above, to ensure the zero voltage transition between the two switches from 50% to maximum output current, t_{id1} and t_{id2} are both set to be $100ns$.

Again, to leave a safety margin, in the calculation, we can use the maximum value of the output capacitance, $1300pF$. As a result, the new t_{id1min} is $55ns$, and the new t_{id2min} is $28ns$. Although the new limit is more critical, with $t_{id1} = t_{id2} = 100ns$, the requirement is still satisfied. Therefore, the zero voltage transition is ensured. This can be verified from the switching waveforms shown below.

Fig.9 shows the zero voltage transition between the two switches at the maximum output current case. In the figures, -2div is the ground for both two waveforms. The gate threshold voltage of the switch IRF530 is 4V, it can be seen that when two switches are turned on/off, the voltage across the switch is almost zero, therefore the zero voltage transition is successfully realized. These switching waveforms also verify the above theoretical analysis on the required transformer leakage inductance (Eqn.15) and the interlock delay time (Eqn.18 and Eqn.27).

To investigate the influence of the improper interlock delay time setting to the ZVS realization, t_{id2} is deliberately increased to 350ns, which has already exceeded its maximum limit t_{id2max} calculated in Eqn.31. The switching waveforms of Q_1 turning on are shown in Fig.10. It can be seen that due to the too large interlock delay time, when Q_1 is turned on, v_{ds1} has already increased from zero to a large value, the ZVS transition is not achieved.

D. Efficiency and loss analysis

The efficiency of the experiment circuit is measured from $6W$ output power to maximum output power $64W$, and shown

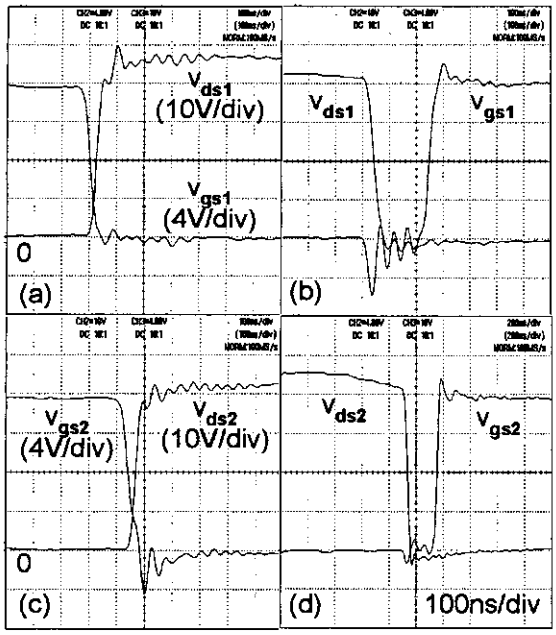

Fig. 9. ZVS transition intervals of Q_1 and Q_2 at maximum output current — (a) Q_1 off, (b) Q_1 on, (c) Q_2 off, (d) Q_2 on. ('0': -2div, the ground of all waveforms.)

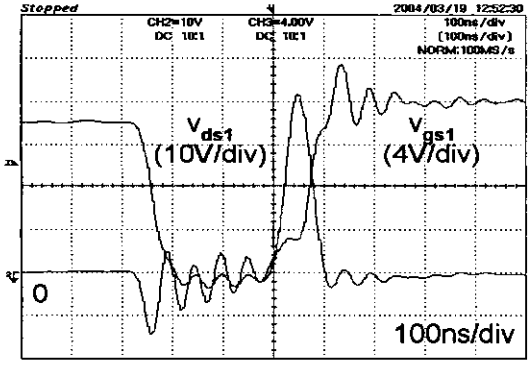

Fig. 10. non-ZVS transition caused by improper setting of t_{1d}. ('0': -2div, the ground of the waveforms.)

in Fig.11. The highest efficiency is achieved at $25W$ output power, 87.3%.

Since the two switches are turned on and off at zero voltage, and the output diode is turned on and off at zero current, the switching loss in the circuit is minimized to be almost zero, and it can be neglected in the loss analysis.

When the converter works with the full load, the achieved efficiency in the experiment is about 81%, and the power loss is $15W$. The conduction loss in the circuit can be calculated:

$$P_{\mathrm{Q1,COND}} = \frac{R_{\mathrm{DS(on)}}}{T}[\int_{t_4}^{t_5} i_{\mathrm{Lr}}^2 dt + I_{\mathrm{m}}^2(DT - \Delta t_5)], \quad (32)$$

$$P_{\mathrm{Q2,COND}} = \frac{R_{\mathrm{DS(on)}}}{T}\int_{t_2}^{t_3} i_{\mathrm{Lr}}^2 dt, \quad (33)$$

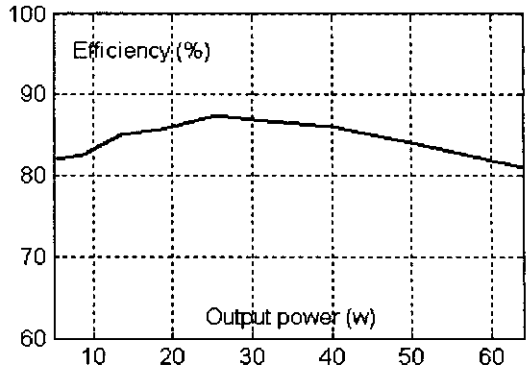

Fig. 11. Measured efficiency

$$P_{\mathrm{D,COND}} = V_{\mathrm{F}} I_{\mathrm{o}}[(1-D) + \frac{\Delta t_5}{T}]. \quad (34)$$

Therefore, the total conduction loss is calculated as:

$$P_{\mathrm{COND}} = 2.06 + 4.78 + 3.12 = \underline{9.96W}. \quad (35)$$

The calculated conduction loss is about $9.96W$, this amount accounts about 12.6% of the input power. The remaining $5.04W$ power loss is consumed by the transformer and the ESR of the capacitors in the circuit.

VI. Conclusion

In this paper, an asymmetrical half bridge flyback converter has been analyzed in detail. With the analysis, some design considerations which have not been covered in previous research are clearly discussed and presented. The advantage of this converter is its ability to realize the zero voltage transition between the two switches and the zero current switching on the output diode and its high versatility to function as different type of converters. To make sure that the zero voltage transition really happens during the operation of the converter, the required transformer leakage inductance value, the ZVS range of the output current variation, and the interlock delay time for the gate signals of the switches are properly calculated. From the experimental switching waveforms, the method of the calculation is verified to be correct and applicable. In the asymmetrical half bridge flyback converter, the zero voltage transition between two switches are realized, and the output diode is turned on and off at zero current. As a result, the switching power loss in the circuit is largely reduced, and high efficiency is achieved.

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