A 1.9 kW FB-ZVS PHASE SHIFTED HIGH POWER DENSITY DC/DC CONVERTER FOR OFF-LINE APPLICATIONS

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ABSTRACT

This paper describes the main design efforts that have been done during the design of a high power density **1.9 kW DC/DC** converter prototype for off-line applications. It was selected a Phase Shifted ZVS Full Bridge topology because it helps to achieve high efficiency and high power density. It has been paid a great attention to the design of the magnetic elements, specially to thermal constraints, because they are the major limitation for the reduction of their size. It is shown that a small increment in the power losses of that components can pay back an impressive reduction in their volume. Solutions for improving heat evacuation outside the transformer are presented and a discrete elements based model is given for calculating the temperature of the hottest spot of the transformer and for the study of its thermal stability.
An special method for constructing large current toroids for output filter inductance is also presented.
The control functions are performed by a UC 3825 PWM controller from UNITRODE and a logic circuit implemented into an EPLD (Erasable Programmable Logic Device) from ALTERA, which synthesizes the Phase Shifted control waveforms and the time delays that must be left for allowing for the resonant transitions to take place.

INTRODUCTION

Modern telecommunication exchange powering systems are based in distributed architecture, both for AC/DC battery chargers and for DC/DC converters for electronic voltage generation.
Each battery charger is composed of a boost power factor corrector converter, a back-up capacitor stack and a DC/DC step down converter. This double stage scheme is nowadays the unique way for achieving both high power factor at the mains and tight regulation in the DC bus for battery charging, allowing for constant current charging or constant voltage operation.
This paper deals with three aspects concerning the design of the later DC/DC converter, for which a **ZVS PWM FB** topology has been selected[1]:

I. Review of thermal constraints in the design of the power transformer.
II. Construction of the output filter inductance.
III. Proprietary circuit designed for controlling Phase Shifted ZVS converters.

I. POWER TRANSFORMER

The transformer must be designed for complying with the **IEC - 950** standard, and for a maximum input power, which is:

$$P_{in} = P_{out} \cdot 1.20/0.93 = 2452 \text{ W} \approx 2500 \text{ W}^2.$$

The transformer can be calculated by the Area Product method, which can be followed at ref. **[1]**. The limiting factor

[1] For a description of this topology refer to **[6]** or **[7]**.
[2] Considering **20 %** overload and just for this calculation a full load efficiency of **93%**.

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of this method is the total power losses allowed for the transformer, which is ultimately determined by the assumption of natural convection cooling. Application of this method gives a required area product (**AP**) value of **29.5 cm⁴** at **150 kHz**. The smallest standard core suited for this application that fulfills this condition is the **EC 90** with an area product of **AP(EC 90) = 65.33 cm⁴**, which was considered too large. We concluded that the limit for power losses imposed by natural convection cooling could not be accepted. Instead, it was considered that accomodating **2500 W** into the only **13.1 cm⁴** of the **EC 70** core would be very successful, since there is a **66 %** reduction from calculated needs and an **80 %** reduction compared to the **EC 90** core.

We thought that heat dissipation could be improved packaging the transformer inside an aluminum case and filling that case with an epoxy bonding material, which can provide good insulating characteristics and very high thermal conductivity, and then attaching the set to the converter's heat sink. A thermal model has been developed for this set, in order to:

1. Predict the maximum power losses allowable for an **EC 70** based transformer.
2. Calculate the thermal stability margins existing for it.

Simplified heat transfer model.

Fig. 1 represents to scale the cross section of the encapsulated **EC 70** transformer standing on a heat sink by one of its columns. It has been divided up into **44** discrete elements, carefully selected for exploiting symmetry and emphasizing that the main heat stream is going to flow to the heat sink. Ferrite is represented by elements whose first number is **1**. N° **2** is reserved for those elements forming the coil, and n° **3** refers to bonding material parts.

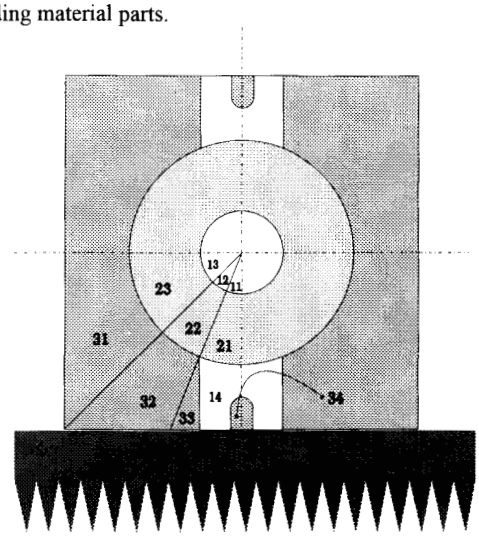

FIG 1

The complex problem of calculating how much power can generate a transformer for the hottest spot not surpassing **130°C** for a given set of boundary conditions must be simplified. These are some of the assumptions that were done:

1. The central volume can be solved as one of very large length (2D problem)
2. Thermal resistivities:

   copper (ρ_{Cu}) ~ **0.01**·ferrite (ρ_1)

   ferrite (ρ_1) ~ **0.2**·bonding materials (ρ_3)

   THEN:

2.1. Each copper turn acts as an isothermal

   ⇒ hottest point: center.

2.2. Coil modeled as a crown with resistivity given by

   $$\rho_2 = (1-K_W)\cdot\rho_3$$

   (K_W is the window utilization factor ; refer to **[1]** for definition).

3. Conservative approach: radial heat flow (1D problem).

If each element of fig. 1 is represented by two thermal resistors and a current source applied at the mass center of each element, as plotted in fig. 2 below, it is obtained the equivalent electrical model for one half of the transformer cross section shown in fig. 3, in which the elements of fig. 1 have been characterized by the following geometric values[3]:

- l_e: equivalent length
- A_e: equivalent cross section (for heat flow)
- **S**: surface (for volume and power calculation)
- **R1, R2**: equivalent thermal resistance (fig. 2)
- **P**: equivalent power (fig. 2)

[3] It can be shown that the center of application of power losses for the elemens **21**, **22**, **23**, in which the coil has been divided into lay at a very similar radius value for all of them.

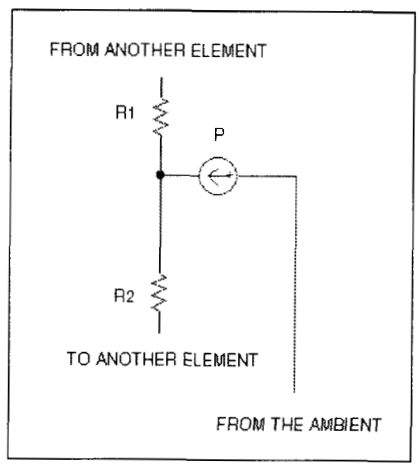

FIG 2

The enclosure used for the transformer has been modeled considering convection and radiation heat transmission, according to the models described in ref. **[2]**, which allow to

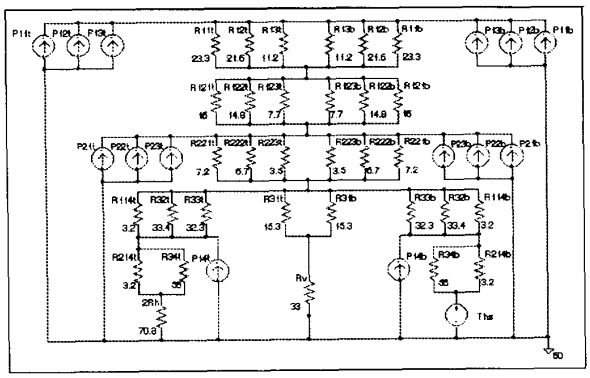

FIG 3

element	l_e (mm)	A_e (mm²)	R1 (°C/W)	R2 (°C/W)	S (mm²)	P (W)
11	8.2	70.5	23.3	-	12.7	$14.4 \cdot 10^{-3} \cdot P_c$
12	8.2	76	21.6	-	13.7	$15.5 \cdot 10^{-3} \cdot P_c$
13	8.2	146	11.2	-	26.4	$29.9 \cdot 10^{-3} \cdot P_c$
14	11.66	363	3.2	3.2	93	$106 \cdot 10^{-3} \cdot P_c$
21	14.05	261	16	7.2	80.7	$60 \cdot 10^{-3} \cdot P_{cu}$
22	14.05	283	14.8	6.7	87.3	$65 \cdot 10^{-3} \cdot P_{cu}$
23	14.05	544	7.7	3.5	168	$125 \cdot 10^{-3} \cdot P_{cu}$
31	17.03	1117	15.3	-	418	0
32	20.19	605	33.4	-	268.6	0
33	7.7	239	32.3	-	40.5	0
34	6.4	114	56	-	16	0

TABLE 1

calculate film coefficients (h_c), radiation coefficients (h_r) and thus thermal resistances:

plane	h_c (W/°Cmm²)	h_r (W/°Cmm²)	h (W/°Cmm²)	R (°C/W)
horizontal	$6.8 \cdot 10^{-6}$	$2.08 \cdot 10^{-6}$	$8.87 \cdot 10^{-6}$	**35.4**
vertical	$7.42 \cdot 10^{-6}$	$2.08 \cdot 10^{-6}$	$9.5 \cdot 10^{-6}$	**33**

TABLE 2

The heat sink has been modeled as a voltage source,which is the thermal focus electric equivalent.

The circuit of fig. 3 has to be solved for core losses, **Pc**, and for copper losses, **Pcu**. It has been supposed a maximum ambient temperature of **60 °C**, and a hottest spot temperature of **130 °C**. The solutions can be calculated by hand or using a circuit simulator as **PSPICE**[4].

The precedent method has also been applied to the heads of the transformer.

When both models are solved independently, it can be obtained the following results:

MODEL	Pc_{max} (W)	Pcu_{max} (W)
columns	27.05	19.23
heads	56.8	-

TABLE 3

However, if both models are connected by means of axial thermal resistors, a complete half of the tranformer can be simulated, showing the cooling effect that the heads produce at the central column. Fig. 4 below represents the Safe Operating Area (or **SOA**) obtained for the transformer.

The inner triangle represents the allowed area in which the transformer can be operated with all of its points under **130 °C**, as obtained with the columns model, whereas the largest triangle represents the same concept when heads cooling is included. The intermediate triangle, defined by Pc_{max} **= 31.3 W** and Pcu_{max} **= 25.5 W**, represents a correction accounting for the thermal gradient existing between the successive column sections.

Influence of temperature in core losses.

Core losses density is a function measured in **mW/cm³**. It can be considered a function of three variables: frequency, flux density and temperature, for sinusoidal excitation of the transformer.

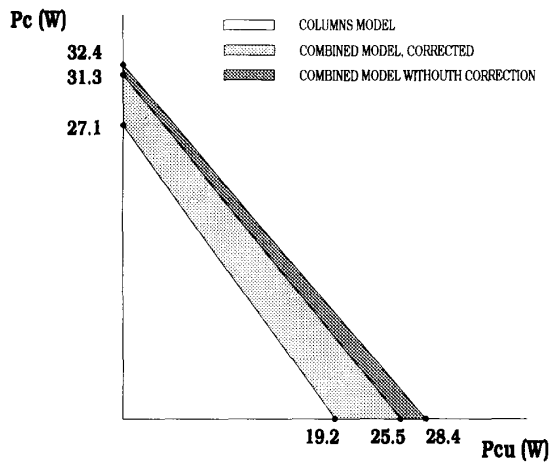

FIG 4

Ferrite's manufacturers use to give some curves showing its dependence with temperature for some combinations of values of frequency and flux density.

These curves are very different from one material to another and also are highly dependent on the value of frequency and flux, but they use to have a similar shape resembling a parabola.

A more complex model can be obtained if the losses injected by each source in any of the precedent models are proportional not only to the volume of the element involved, but also to the temperature of the node. For evaluation of the influence

[4] As the center of application of **Pc** and **Pcu** are separated by a small thermal impedance, it is possible to solve the circuit for the extreme cases **Pc = 0** and **Pcu = 0**, and then consider that worst case conditions are found at the straight line given by:

$$\frac{Pc}{Pc_{max}} + \frac{Pcu}{Pcu_{max}} = 1$$

The largest deviation from this equation is found at the neighbourghood of point $0.5Pcu_{max}$, $0.5Pc_{max}$, and it has been checked to be under + 5%.

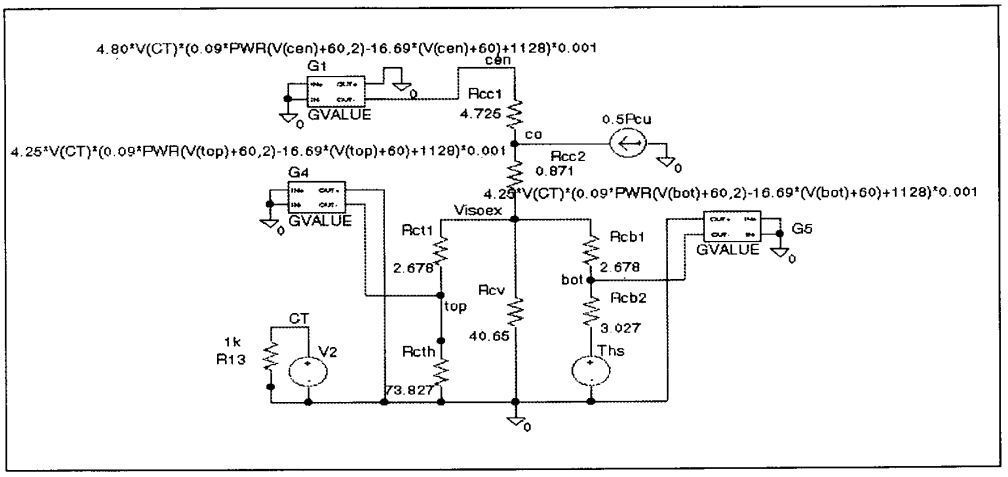

FIG 5

modul. factor	I_{G1} cen. col.	I_{G1}/I_{G5} nom. 1+1.13	I_{G4} top col.	I_{G4}/I_{G5} nom. 1+1	I_{G5} bot. col.	Pc (W)	Pcu (W)	ΣP (W)
1.5167	3.506	1.517	2.585	1.119	2.311	**25.0**	**0**	**25.0**
1.2628	2.917	1.514	2.169	1.126	1.927	**20.9**	**3.2**	**24.1**
1.0105	2.328	1.508	1.747	1.131	1.544	**16.8**	**6.4**	**23.2**
0.7560	1.746	1.508	1.318	1.138	1.158	**12.6**	**9.6**	**22.2**
0.5049	1.163	1.503	0.886	1.145	0.774	**8.4**	**12.8**	**21.2**
0.2523	0.584	1.505	0.447	1.152	0.388	**4.3**	**16.0**	**20.3**
0	0	-	0	-	0	**0**	**19.2**	**19.2**

TABLE 4

of this parameter it can be useful the simplified model of the central columns formerly explained.

A material that can be appropriated for this high frequency application is **PC 40** from **TDK**. The curve of core losses versus temperature at **100 kHz** and **200 mT** of flux density can be approximated by the following expression in the interval of interest, that ranges from **50 °C** to **130 °C**[5]:

$$\rho_{Pc}(t) = 0.09t^2 - 16.69t + 1128 \quad mW/cm^3$$

The losses generated in each element are consequently expressed as: $P_{1i} = k \cdot \rho_{Pc}(t_{1i}) \cdot V_{1i} \cdot 10^{-3} \quad W$

where $\mathbf{V_{1i}}$ represents the volume of the element **1i** and k is a modulating factor that links the sources with the transformer operating point, which is the same for all of them.

Fig. 5 is a schematic diagram that represents the current sources as dependent both of temperature of the element and of the modulating factor.

Plotting these points to the same scale of fig. 4, it is obtained the figure 6:

Table 4 above shows the relative losses share between columns, referred to bottom column losses for comparison:

Thermal stability.

The precedent considerations show that it is not possible to make a reliable transformer design ignoring the feedback existing between temperature and core losses.

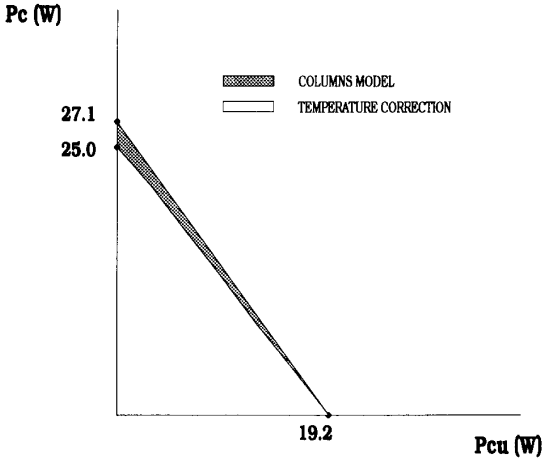

FIG 6

Thermal stability is guaranteed if a small perturbation in the losses produces an increment in the temperature of the hottest spot that implies back an increment in losses smaller than the perturbation. Mathematically:

$$\mathbf{R_{h\to a}} < \frac{1}{\left(dP_{1i}/dT\right)_{T=T_0}}$$ where $\mathbf{R_{h\to a}}$ is the thermal impedance existing between the hottest spot and the ambient, and $\mathbf{P_{1i}}$ are the hottest element losses versus temperature function.

In the model shown before, the extreme conditions satisfy:

[5] Unfortunately the same curve at **150 kHz** was not available

$$1/\left(dP_{1c}/dt\right)_{t=t_c} = 13.2 \quad > \quad 10.29 = R_{h\to a}$$

so that the operating conditions are stable.

Runaway temperature.

The stability criterion can be used for defining the runaway temperature:

$$T_{runaway}: \quad \left(dP_{1i}/dT\right)_{T=T_{runaway}} = \frac{1}{R_{h\to a}}$$

This new point of view lets make a prediction for total power deliverable if the condition of maximum temperature of **130 °C** is relaxed and substituted by the runaway temperature.

Simulation of this conditions leads to a maximum for core losses of **Pc = 30.7 W** at a center temperature of t_c = **146 °C**.

The usefulness of this calculation is that it permits to know ***how safe*** is **130 °C** as a temperature limit, and that if the transformer is operated under these conditions there is a safety margin of **16 °C**.

As a conclusion of this paragraph, it must be emphasized the importance of the heat sink, as a component essential for achieving very low impedances to the flow of heat, and thus for obtaining high power dissipation and ***stable*** solutions.

We can reinforce this conclusion obtaining the result of the simulation without a heat sink (natural convection cooling):

For this purpose we can substitute the heat sink model by a very large thermal resistance, which can reflect the inability of the bottom surface for evacuating heat.

The result obtained is that it would be possible to extract only **Pc = 7.1 W** with an absolute maximum temperature at the center of t_c = **128 °C**.

It should be noted that these values are in good agreement with the conventional solutions; for example the procedure described in **[1]** recommends a maximum temperature rise of **40 °C** and suggests a thermal resistance from hottest spot to air of **8.9 °C/W** for an **EC 70** transformer, thus allowing for total losses of **4.5 W**; but if it were allowed for reaching t_c = **128 °C** it would dissipate **7.85 W**.

A last hypothesis that can be simulated is the opposite to that of the precedent paragraph: replacing the plane that is on top of the transformer by another heat sink at the same temperature than the bottom one.

The solution is that temperature could rise to an absolute maximum value of t_c = **150 °C** with power losses in excess of **40 W**.

Experimental verification.

At the moment of writing this paper it has not been possible to fully evaluate all the conclusions exposed here.

It has been prooved that it is possible to evacuate more than **20 W** from an **EE 55/28/21**core attached to the heat sink with a thick finned aluminum clamp, with **47 °C** of temperature increment over the ambient.

II. OUTPUT FILTER INDUCTANCE.

It has been developed an structure called **Compact Toroid** (or simply **CT**, henceforth) formed by three elements, as it shown in figure 8: a printed circuit **P**, some turn pieces **D** and the core **T**.

The printed circuit consists in some pads distributed around two concentric crowns and some traces connecting one pad from each crown to another pad of the other crown, in such a way that when the turn pieces are soldered to the pads, they form the winding.

Fig 7, top, illustrates enlarged one of the turn pieces with the circular slot to carry the core inside it (bottom):

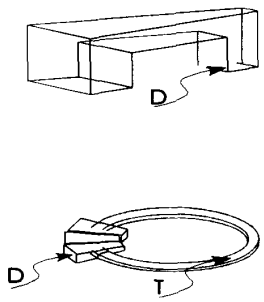

FIG 7

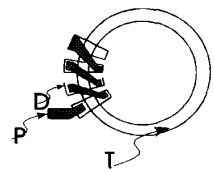

FIG 8

Best results are obtained if the **CT** is implemented over a metallic substrate. In this case it is easier to use thick copper traces, which help to reduce copper losses and if the metallic substrate is attached to the heat sink of the converter, the inductance would be thermically coupled to a stable temperature focus, allowing for a different design trade off between size and losses[6].

An immediate consequence of substituting copper wire by turn pieces is that now we can design the windings taking into account **6** independent parameters that define the turn pieces and the copper traces, which can be combined for achieving an optimum solution.

The adjective "compact" given to this particular implementation refers to the possibility of designing the inductance with almost full use of the window, with the unique limit of isolation of the turn pieces and manufacturability of the traces, what implies that only a small circle in the center of the inductance can not be used.

Another advantage of this solution is that it interfaces very well with the other elements of the circuit, making innecesary the use of connectors. The inductor is connected to the output rectifiers and there are great currents involved and great values of **di/dt** are expected to be found in the loop formed by the rectifiers, the inductance and the output capacitor. This implementation makes it possible to connect these elements very close to each other, thus minimizing parasitics.

It is easy to notice that if a positioning element is added to the turn piece, it would be possible to mount the inductor automatically. The complete process would begin with the application of the soldering paste and would finish with an oven curing, as is it done with all **SMT** components.

[6] Refer to transformer design considerations.

Conventional versus Compact comparison.

Large current toroids are difficult to be wound, because of the lack of flexibility of the conductors that have to be used. The use of Litz wire for their construction is highly recommended since it makes easier winding the conductor around the core. Nevertheless it is difficult to get a tight fitting between winding and core, and a great part of the winding area can not be used. Also, the total height of the toroid is somewhat increased.

Consequently, the resulting conductor is longer than what is really needed and copper losses are increased. Use of more than one layer of conductors of smaller section simplifies winding but at the expense of worsening the electrical properties of the inductance. It is also neccesary to add some kind of connectors to the ends of the wire, and packaging the inductor into a case is greatly recommended for simplify handling and attachment. Last, such big toroids can not be automatically wound.

A comparison between a wired toroid -or simply **WT**, henceforth- and a compact toroid has been carried out for our particular application. No heat sink cooling has been used for the **CT**, what would have given a much smaller core size and apparent volume.

The following table shows the main parameters and performances of both solutions at **30 A** of output current. Central columns give relative figures when comparison makes sense.

TABLE 5

PARAMETER	WIRED TOROID			COMPACT TOROID
Core used (MPP, Magnetics)	55438			55076
Permeability μ	125	-	-	60
Core's weight (g) (related to its cost)	182	100 %	27 %	49
N° of turns	8	-	-	18
Inductance (μH)	18	-	-	18.14
Core losses (W)	1.83	100 %	40 %	0.73
Copper losses(W)	1.03 Litz 330*0.2	100 %	153 %	1.58 0.5 mm trace thick
Total losses (W)	2.85	100 %	81 %	2.30
Apparent volume (cm^3)	76	100 %	32 %	24
Layout area (cm^2)	26	100 %	54 %	14
Height (mm)	29.1	100 %	48 %	14
Used window area(cm^2)	1.63	-	-	1.7
Used wind. area / Available wind. area	38 %	100 %	124 %	47 %
temperat. rise (°C)	6.3	100 %	377 %	23.8

CT is made over a core weighting **27 %** of that weighted by the **WT** core. The **CT** core's permeability is smaller, so it is much less lossy than its **WT** counterpart, but some of this advantage is lost because of copper losses, which are higher, as it could be expected comparing the number of turns.

CT's layout area and height are one half of that required by the **WT** solution, so the volume is slightly under one third of **WT**'s.

CT's window utilization factor is only a quarter higher than that achieved by **WT** and such modest improvement is due to the large number of turns used for making it. If **8** turns were mounted over an identical core of permeability **μ = 300** it would be obtained a rather than optimal **19 μH** inductance that will use **67 %** of the available window area, which nearly doubles the window profitability of **WT**. (That hypothetical lossy inductance would saturate at 5 amps).

The last row of the table compares the predicted full load temperature rise over ambient temperature with natural convection cooling. It should be thought that the **CT**'s much higher temperature increment is a great disadvantage, but in fact **24 °C** over the ambient is a conservative value, whereas the **6 °C** temperature increment of the **WT** proofs that it is a rather than optimal design, directly pointing to the problem of finding an optimal solution for conventional wired toroids with standard Litz wire gauges. The total low losses required lead to large cross section wires, which badly fit the core shape and badly profit its window area, which is proportional to the power handled by the inductance.

(The results presented in this comparison should not be generalized: the particular benefits obtainable with a **CT** solution should be individually calculated for each case, being specially apparent for high levels of current). The structure called Compact Toroid is patent pending.

III. PROPRIETARY PHASE SHIFTED ZVS CONTROLLER

A **P**hase **S**hifted PWM Peak Current Mode **C**ontroller (PSC) can be designed combining some building blocks that are used for making switched mode power supply controllers (SMPSC) and three special blocks:

1. **The core PSC controller**. It is the circuit that generates the signals for activating the four switches. They are obtained from the PWM pulses and the clock pulses. Its most simple - though unreliable- implementation could be a pair of toggle flip-flops.
2. **Two delay blocks**. They have to generate the delay that must exist to allow for resonant transitions to take place. The two nodes of the power circuit have got different transition behaviour, so it is necessary to provide for different delays to the switches governing their voltage.

It was considered that the most effective solution for building up a prototype could be using all the internal circuitry of a commercial SMPS controller that could be of some worth, limiting the design effort to the three said blocks. The SMPSC selected for this application was the **UC 3825**, because it is a high frequency design, allowing for switching frequencies up

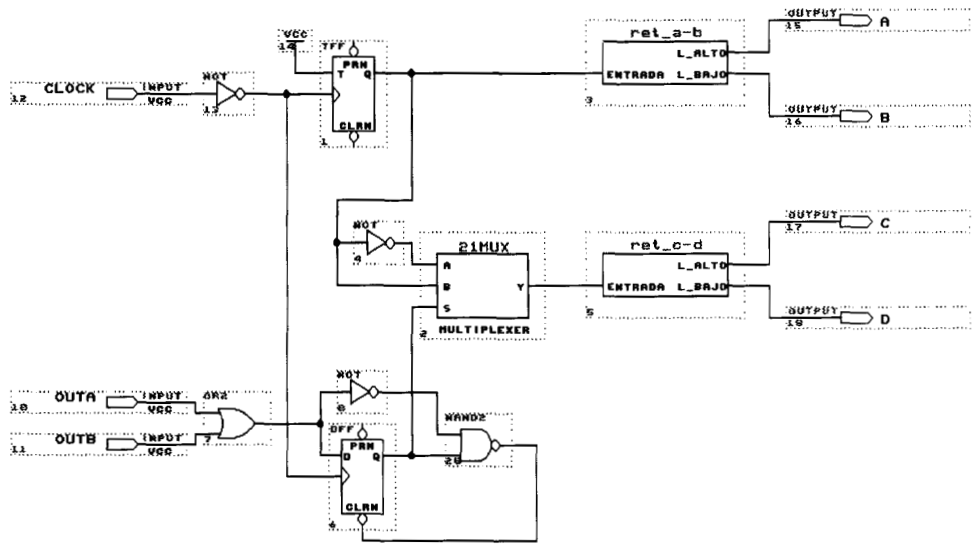

FIG 9

to 1 **MHz**, and it has very fast propagation delays and fully latched logic.

For implementing the special blocks it was selected an erasable programmable logic device (**EPLD**), because it can contain many logic functions in just one chip, and this component can be programmed and erased as many times as necessary, greatly simplifying the circuit debug, because the board layout need not be changed if the blocks are redesigned.

For this application it was selected the family **5000** from **ALTERA**, because its internal architecture is based on modular blocks called **LABs**, or Logic Array Blocks, internally linked through a network called **PIA**, or Programmable Interconnect Array. This **PIA** provides a cross point switch for logic communication and yield a predictable uniform delay, instead of the routing-dependent random delay typical of other programmable gate arrays.

Core Phase Shifted control circuit.

This module must generate the control signals that activate the power bridge switches' drivers.

Fig. 9 is a schematic diagram of the circuit designed for meeting all the requirements, called **FASE8**.

Both bistables are triggered by the **clock** signal. The **T** flip-flop act as a frequency divider and the **D** flip-flop really controls a two channel multiplexer that selects either following the logic value of the **T** flip-flop or its inverse. The later implies power transfer and the former implies no voltage difference at the primary, though the four switches will remain toggling.

The latching character of the circuit is due to the asynchronous pulses generated by the **NAND** gate fedback to the **clear** input of the flip-flop. Once the output of the flip-flop goes low it can not change its state until a **clock** edge comes again.

PWM comparator output pulses are given to the circuit through the pins called **OUTA** and **OUTB**.

In absence of **PWM** pulses the **D** flip-flop stays fixed at low level and both legs follow the same sequence, i.e., phase shift is **0°**.

The outputs of the circuit are given to two delay blocks, called **ret_a-b** and **ret_c-d**, which connect to the driver circuit.

Fig. 10 is a plot of a simulation of the previous circuit, showing the most important signals and their relations:

- The inputs are:
  - **CLOCK**, sharp edges obtained conforming the homonymous signal of the **UC 3825**
  - **OUTA** and **OUTB,** generated at the **UC 3825** as **PWM** pulses.
- The outputs are:
  - **A** and **B,** are the high side and low side driving signals for the switches of one leg of the bridge.
  - **C** and **D,** same as before, for the other leg.
- Internal signals:
  - Signals beginning with **:6** concern to the **D** flip-flop.
  - Signals beginning with **:1** refer to the **T** flip-flop.

During the first half cycle, signal **OUTB** is high, so the diagonal switches **A** and **D** are active, and power flows from the

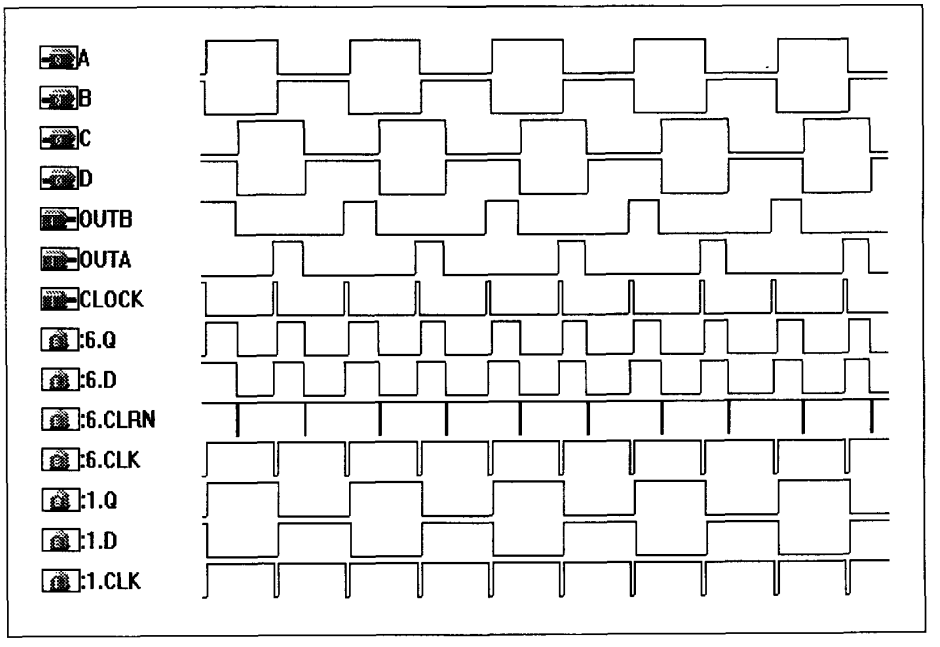

FIG 10

source to the load. When the **OUTB** signal goes to zero the feedback over the **NAND** gate generates a brief clearing pulse over the **D** flip-flop, changing its state, and turning off the switch **D**. The delaying block **ret_c-d** starts the count, allowing for the resonant transition with both **C** and **D** switches opened and when it finishes the high-side switch **C** is closed, and takes place the primary current freewheeling subcycle through switches **A, C** and the anti parallel diode across **C**.

Another power transfer interval will happen with the next **CLOCK** pulse and the **OUTA** signal, which will toggle the **T** flip-flop, immediately turning off the switch **A** and triggering the **ret_a-b** delaying block. While this block is performing its task, both switches of leg **A-B** are opened, and the resonant transition towards **ZVS** develops. After that brief instant, the switch **B** is closed and the power is transferred through the **C-B** diagonal. After a resonant transition comes another primary freewheeling subcycle through switches **B** and **D** plus its anti parallel diode[7].

The predicted waveforms shown in fig. 10 were experimentally confirmed to be correct in the prototype.

Programmable delay generator.

As it is possible to specify the internal **LABs** that are going to implement the logic functions and moreover it is possible to assign the last to the "atomic" elements constituting each **LAB**, the so called macrocells, it is possible to build up a delay generator based in cascaded asynchronous gate transitions. The inexistence of transmission lines inside the chip is also a good help for achieving highly repetitive delays.

The selected component is the **EPM 5064**, which includes 64 macrocells, that can be configured to form up to 84 flip-flops, up to 128 latches and 36 signal pins, though it is possible to implement the circuit in smaller members of the **5000** family.

For other **PLD** families the asynchronous design could have to be converted into a synchronous design. In that case it could be necessary to use a very high frequency retriggerable clock for slicing up the power converter clock cycle into a great deal of units. One delay generator could be triggered by a signal phase-locked to the power converter clock signal, and the other generator should better be cycle-by-cycle retriggered by the asynchronous **PWM** comparator signal.

Each delay generator must produce very short pulses of durations ranging from **30 ns** to **300 ns**, for the values of the components used in our power circuit. The pulses should have sharp edges, and should be repetitive and predictable.

The delay generator stage controls the driving signals of a pair of **MOSFETs**, arranged as one leg of the bridge.

In order to minimize the number of flip-flops used, it has been selected a counter structure for them. After a triggering signal comes, the **MOSFET** of the leg that was closed and conducting current is disabled, and a counting process began.

During this time both switches of the leg are opened, thus allowing for the resonant transition to happen. The counter flip-flop array sweeps up in an asynchronous fashion until the count equals the externally programmed value. When that

[7] The pulses **OUTB** shown in fig. 10 are all equal, but the length of pulses **OUTA** is intentionally decreasing for testing the ability of the controller when there is any slight difference between secondary windings, output diodes, etc., which produces a tiny mismatch between their respective ramps.

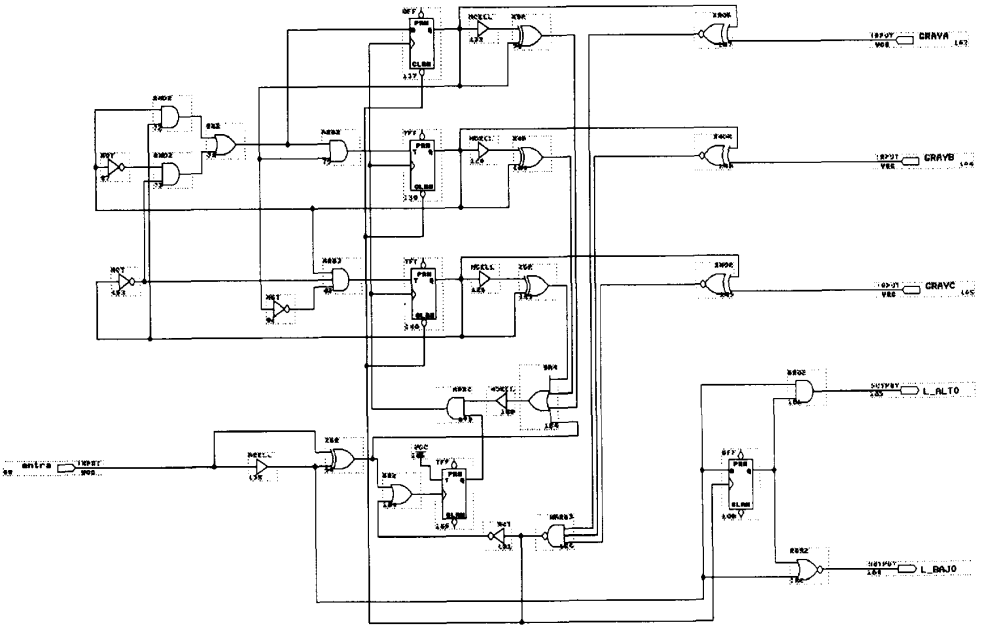

FIG 11

event occurs, the **MOSFET** that was initially in the off state is activated.

Fig. 11 is an schematic diagram of a delay generator used, called **ret3ff**. The count begins when a high level appears in the pin called **entra**, which turns off the **MOSFET** that was conducting current and generates a short pulse that activates the counter. The counting process is self-sustained by the feedback existing from the **XOR** gates and the four input **OR** gate until the values of the counter flip-flops are the same to that of the input pins **GRAYA**, **GRAYB** and **GRAYC**. In that moment all the outputs of the **XNOR** gates are at high level and the three input **NAND** gate in which they converge generates a pulse that:

1. Stops the counting process.
2. Resets the counter flip-flops.
3. Enables the **MOSFET** that was off before signal **entra** changed its state.

The outputs of the circuit are **L_ALTO** and **L_BAJO**, which are respectively connected to the driver inputs for high side **MOSFET** and low side **MOSFET** of the leg. The other output pins do not play any role in the circuit but showing the internal signals of the circuit, which would otherwise be unobservable.

The presented counter structure is very useful, because it gives seven[8] delay options linearly scaled. The pitch between these values can be varied from about **15 ns** to hundreds of nanoseconds simply delaying the feedback signal of the counter, what implies a great flip-flop economy. It is also possible to improve the time resolution further than the limit of **15 ns**, but not with the counter circuit implemented over this family of components.

The delay values are selected by three external micro switches (four in the case of the **ret3fver** delay generator). As the required delay value depends on the operating conditions, it should be adjusted in the prototype changing the combination of the micro switches. For this purpose the counter has been designed with a **GRAY** structure so that each increment or decrement in the desired delay value needs the change of just one micro switch.

Table 6 shows the delay values expressed in nanoseconds obtained with different delay generators that has been synthesized.

It should be mentioned that the delays obtained with this method are very stable and they have very low jitter, which is originated by random deviations in the period of the power converter clock signal.

[8] If a wider range of values is desired, it is possible to increase it simply adding more flip-flops to the counter, as it is shown in the delay generator **ret3fver**, which has been synthesized with a four bit counter so that it can provide for **15** different delay values, instead of the 7 values that the other delay generators can deliver.

GRAY CODE DCBA	ret3	ret3ff	ret3ffm	ret3fver
0000	-	-	-	-
0001	35	40	53	82
0011	46	61	83	156
0010	62	84	115	212
0110	75	111	142	282
0111	87	127	172	354
0101	102	150	200	416
0100	117	175	230	480
1100	-	-	-	550
1101	-	-	-	618
1111	-	-	-	686
1110	-	-	-	750
1010	-	-	-	808
1011	-	-	-	880
1001	-	-	-	942
1000	-	-	-	1000

TABLE 6

CONCLUSIONS

The conventional practice of cooling the power transformer by natural convection is considered improper for achieving high power density converters. An alternative solution mainly based on heat conduction to the heat sink is presented, which dramatically reduces transfomer size requirements.

A method for calculating the safe operating area of heat sink attached transformers is given, including perverse thermal feedback considerations and runaway temperature calculation.

It has been presented the Compact Toroid, a new approach for constructing large current toroids for applications in which **DC** component is dominant. This implementation intrinsically achieves lower copper losses compared to large current wound toroids; it can profit from most of the window area of the core, it can be automatically mounted with **SMT** techniques and it can be easily cooled in appropriate substrates, leading to smaller inductance size. Its total height can be greatly reduded, as far as it is really limited only by the core's height.

Last, a proprietary Phase Shifted control circuit has been presented, which incorporate two digitally programmable delay generators for resonant transition timing, which can be operated in a closed loop fashion for improving **ZVS** control.

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