# Analysis and Design of an Auxiliary Commutated Full Bridge DC/DC Converter Topology Including the Effect of Leakage Inductance

Dheeraj K. Jain
Dept. of Electrical & Computer Eng.
Concordia University
Montreal, PQ, Canada, H3G 1M8

Praveen K. Jain
Dept. of Electrical & Computer Eng.
Queen's University, Walter Light Hall
Kingston, ON, Canada K7L 3N6

Haibo Zhang
Cistel Technology Inc.
210, Colonnade Road, Suite 200
Ottawa, ON, Canada K2E 7L5

**Abstract: This paper presents the analysis and design of an auxiliary commutated full bridge dc/dc converter topology including the effect of leakage inductance of the output transformer. In applications where the transformer has high turns-ratio between the primary and secondary windings, the value of leakage inductance is relatively high. This high value of leakage inductance, however, is not large enough to achieve the zero voltage switching (ZVS) of the converter over the entire range of operating load conditions, but can be effectively used in minimizing the circulating current of the auxiliary commutation circuit used for achieving ZVS. The operating principle of the circuit is demonstrated and the steady state analysis is performed. Based on the analysis, a criterion for optimal design is given.**

## 1.0 Introduction

Full-bridge dc/dc converters are extensively applied in medium to high power dc/dc power conversion. High efficiency, high power density, high reliability and low EMI are some of the most desirable features for these converters, particularly for computer and telecommunication applications.

For power levels up to 3 kW, the full bridge converters now employ MOSFET and use Phase-Shift Modulation (PSM) to regulate the output voltage. In most of these converters, Zero Voltage Switching (ZVS) is achieved by placing a snubber capacitor across each of the switches and either by inserting an inductor in series with the transformer or by connecting an inductor in parallel to the power transformer [1-5]. In a practical full- bridge configuration, the snubber capacitor may be the internal drain-to-source capacitor of the MOSFET, the series inductor may be the leakage inductor and the parallel inductor may be the magnetizing inductor of the power transformer. This makes the power circuit of these converters simple. However, the full-bridge converter with series inductor losses its ZVS capability at no-load (or light-load), and the converter with the parallel inductor losses it's ZVS under short circuit. The loss of ZVS under these two extreme conditions results in (i) increased size of heat sink due to switching losses particularly at higher switching frequencies, (ii) higher EMI due to high di/dt of the snubber discharging current, and (iii) reduced reliability due to reverse recovery current of the body diodes. Moreover, the converter with series inductor reduces the effective duty ratio because of the voltage drop across the series inductor, resulting in higher primary current and larger output inductor.

An alternative full-bridge converter topology to overcome the aforementioned drawbacks has been developed for high power IGBT full-bridge circuits [6-7]. An auxiliary circuit controlled by bi-directional switches is employed at each leg of the full-bridge to achieve ZVS of the main switches. For low-power applications operating at high frequency, this topology is rather complicated in both power and control circuitry.

Auxiliary commutated ZVS full bridge converter topologies suitable for low power applications ($\leq$ 3 kW) have been reported [8-9]. In these converter topologies an auxiliary circuit comprising of an inductor at each leg of the bridge is employed. These converter topologies provide ZVS of all the switches under all operating conditions including open and short circuits. Reference [10] has presented analysis of such converters for the detailed design.

In applications where the transformer has high turns-ratio between the primary and secondary windings, the value of leakage inductance is relatively high. The high value of leakage inductance, however, is not large enough to achieve the zero voltage switching (ZVS) of the converter over the entire range of operating load conditions, but can be effectively used in minimizing the circulating current of the auxiliary commutation circuit used for achieving ZVS. This paper presents the analysis and design of an auxiliary commutation full bridge dc/dc converter topology including the effect of leakage inductance of the transformer. Trade-off in selecting the auxiliary circuit components is given to optimize the performance of the overall converter. Detailed simulation of the converter is presented to verify the analysis and to demonstrate the key features.

0-7803-7512-2/02/$17.00 ©2002 IEEE

## 2.0 Description of Circuit

Fig. 1 shows the auxiliary commutated full-bridge converter topology to be discussed. It consists of two functional sub-circuits. One sub-circuit is the PSM conventional full bridge converter, which is referred to as the power circuit hereafter. The other is an auxiliary network shown inside the dotted area in Fig.1.

The power circuit employs the following devices:

(i) $S_1$, $S_2$, $S_3$, and $S_4$, four MOSFET switches,
(ii) $T_{fr}$, the power transformer with a turns ratio of k,
(iii) $S_{R1}$ and $S_{R2}$, two synchronous rectifiers,
(iv) $L_1$, $L_2$ and $C_o$, the output filter, and
(v) $R_o$, the load.

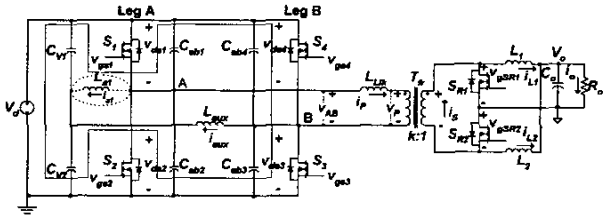



Fig. 1 The proposed ZVS full bridge converter topology

The auxiliary circuit is comprised by eight passive devices, i.e.,

(i) $C_{sb1}$, $C_{sb2}$, $C_{sb3}$, and $C_{sb4}$, four drain-to-source snubber capacitors, each across one switch,
(ii) $C_{V1}$ and $C_{V2}$, a capacitive voltage divider, and
(iii) $L_{a1}$ and $L_{aux}$, two auxiliary inductors.

Phase shift pulse width modulation is used as the control technique for output regulation and the externally driven technique (EDT) is used for the synchronous rectifier switches. Together with the auxiliary circuits, the leakage inductance of the transformer, PSM control and EDT, zero voltage switching is achieved for all the switches of full-bridge converter as well as the synchronous rectifier.

For the gating signals, shown in Fig. 2, the Leg A of the inverter terminates while Leg B initiates the power transfer cycle. Leg A achieves the natural ZVS commutation for the considerably reduced load current and auxiliary inductor $L_{a1}$ is designed to achieve ZVS at no-load. On the other hand, Leg B losses natural ZVS commutation at the considerably higher value of the load current and largely depends upon auxiliary inductor $L_{aux}$. In applications where there is always some minimum load current (around 20%), there is no need of connecting the inductor $L_{a1}$.

## 3.0 Steady State Analysis

Since conventional full bridge converters have been extensively discussed in the literature, the analysis of its operation will not be repeated in this paper. Only the operation of the auxiliary circuit is analyzed below.

To simplify the steady state analysis, the following assumptions are made:

(i) the input dc voltage, $V_d$, and the output voltage $V_o$, are constant,
(ii) the converter outputs a constant power $P_o$,
(iii) all components and devices have ideal properties and characteristics,
(iv) there is a very short dead time, $t_d$, between the ON states of the two switches on each leg of the bridge,
(v) the phase shift angle between the conduction of diagonal switches of the bridge is θ, in degree,
(vi) $C_{sb1}$ and $C_{sb2}$ have equal capacitance, and so do $C_{sb3}$ and $C_{sb4}$,
(vii) $C_{V1}$ and $C_{V2}$ have equal capacitance, and they are large enough such that their voltages can be considered constant during steady state operation.

The proposed converter has the following two modes of operation.

### *3.1 Mode 1*

This mode occurs at heavy loads and the converter has ten distinct operating intervals during a single switching cycle. The opearting principle can be illustratd with key waveforms shown in Fig. 2. In the last interval of previous cycle when both $S_2$ and $S_4$ were on, the primary current of $T_{fr}$ saw a constant voltage, $-V_d$, and $S_{R1}$ was on and $S_{R2}$ was off. At the end of this interval the primary current reached at its peak value $I_{ppk}$. At the beginning of this interval when $S_2$ is turned-off and no other switching action takes place. The current flowing through $S_2$ is the primary peak current $I_{ppk}$ which is flowing through leg A starts to charge $C_{sb2}$ and discharge $C_{sb1}$. During this interval $T_{fr}$ starts to see a zero voltage which is given by dead time ($t_d$). During this interval none of the secondary rectifier switches $S_{R1}$ and $S_{R2}$ are turned-on so the current is freewheeling in both inductors. As this interval is small the primary current ($i_p$) remains constant. Within this interval the voltage across switch $S_1$, which is given by $v_{ds1}$ falls to zero volts and voltage across switch $S_2$, which is given by $v_{ds2}$ reaches to $V_d$. Now $S_1$ has ZVS condition for turn-on. In the next interval, $S_1$ is

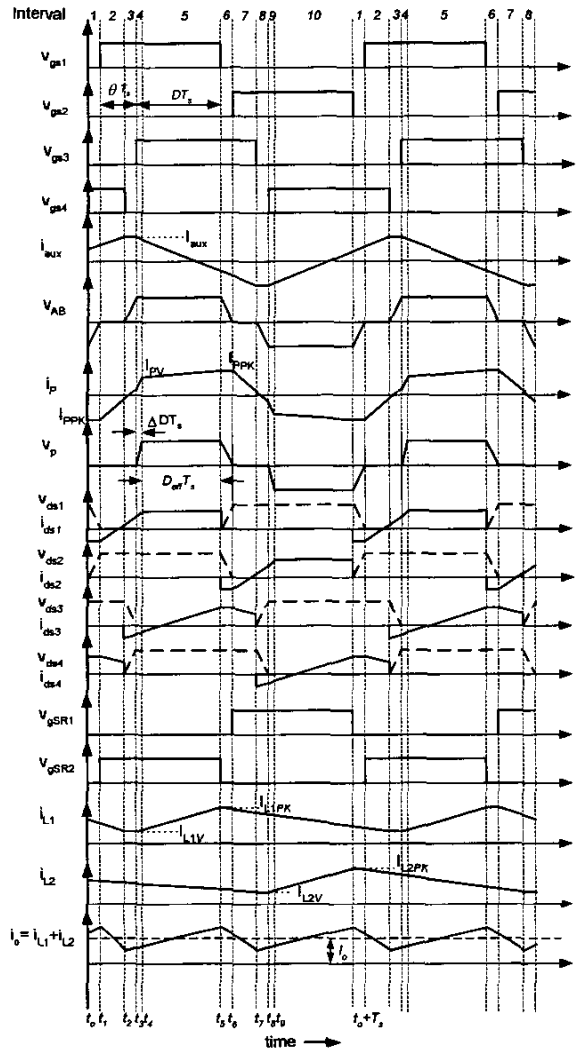



Fig. 2 Key waveforms for the proposed converter topology in Mode 1. The dead time and switching transient are exaggerated

turned-on in ZVS condition. As both $S_1$ and $S_4$ are on, the primary winding of $T_{fr}$ sees zero voltage. During this interval $S_{R2}$ is turned-on. At the beginning of Interval 3, $S_4$ is turned-off, the auxiliary current flowing through $L_{aux}$ reaches to its peak, which is given by $I_{aux}$. In this interval primary current is still flowing in the negative direction due to the energy stored in $L_{Lk}$. This primary current helps auxiliary current to charge the snubber capacitor $C_{sb4}$ and discharging snubber capacitor $C_{sb3}$. The duration of this interval is given by dead time. At the beginning of next interval, $S_3$ is turned-on under ZVS condition. During this interval $i_{aux}$ starts to decrease linearly and the primary current starts to reverse the direction from negative to positive. At the beginning of interval 5, the primary side has positive current and both diagonal switches $S_1$ and $S_3$ are on. Thus the power transfer from primary side to secondary side is there and load current is equally shared between $L_1$ and $L_2$. The rest five intervals are similar to first five intervals.

### *3.2 Mode 2*

This mode occurs at light loads and the converter has twelve distinct operating intervals during a single switching cycle. The operating principle can be illustratd with key waveform shown Fig. 3. In the last interval of previous cycle when both $S_2$ and $S_4$ were on, the primary current of $T_{fr}$ saw a constant voltage, $-V_d$, and $S_{R1}$ was on and $S_{R2}$ was off. At the end of this interval the primary current reached at its peak value $I_{ppk}$. At the beginning of this interval when $S_2$ is turned-off and no other switching action takes place. The current flowing through $S_2$ is the primary peak current $I_{ppk}$ which is flowing through leg A starts to charge $C_{sb2}$ and discharge $C_{sb1}$. During this interval $T_{fr}$ starts to see a zero voltage which is given by dead time ($t_d$). During this interval none of the secondary rectifier switches $S_{R1}$ and $S_{R2}$ are turned-on so the current is freewheeling in both inductors. As this interval is small the primary current ($i_p$) remains constant. Within this interval the voltage across switch $S_1$, which is given by $v_{ds1}$ falls to zero volts and the voltage across switch $S_2$, which is given by $v_{ds2}$ reaches to $V_d$. Now $S_1$ has ZVS condition for turn-on. In the next interval, $S_1$ is turned-on in ZVS condition. As both $S_1$ and $S_4$ are on, the primary winding of $T_{fr}$ sees zero voltage. During this interval $S_{R2}$ is turned-on. In this interval primary current discharge the leakage inductance ($L_{Lk}$) very fast and changed the direction from negative to positive. During the beginning of next interval no switching action takes place and the primary current remains constant for the rest of interval. In the beginning of Interval 4, $S_4$ is turned-off, the auxiliary current flowing through $L_{aux}$ reaches to its peak, which is given by $I_{aux}$. During this interval, auxiliary current is enough to charge the snubber capacitor $C_{sb4}$ and discharging snubber capacitor $C_{sb3}$. The duration of this interval is very small which is given by dead time. In this interval, the primary side of the transformer starts to see the positive voltage. At the beginning of next interval, $S_3$ is turned-on under ZVS condition. During this interval $i_{aux}$ starts to decrease linearly. The primary side has positive current and both diagonal switches $S_1$ and $S_3$ are on. Thus the power transfer from primary side to secondary side is there and load current is equally shared between $L_1$ and $L_2$. At the beginning of

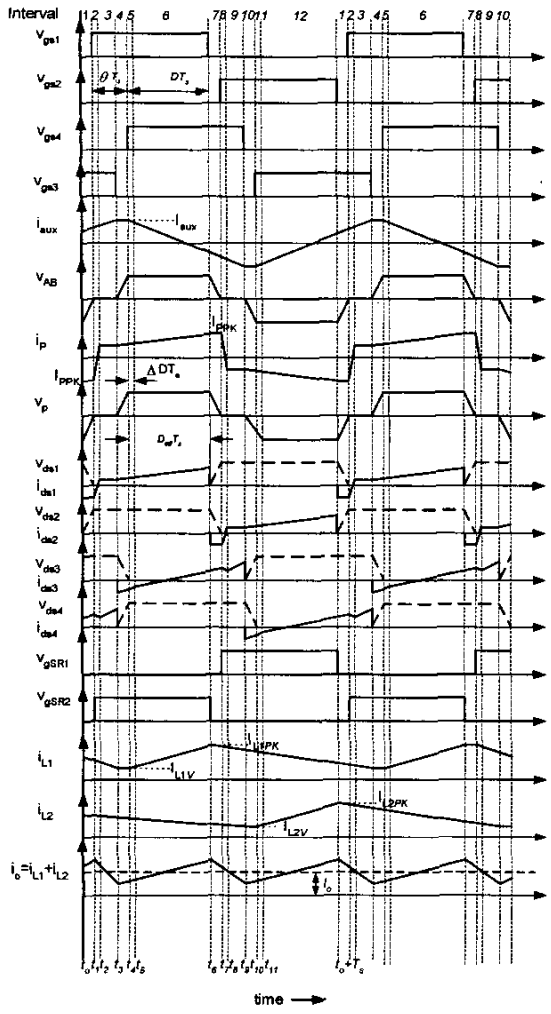



Fig. 3 Key waveforms for the proposed converter topology in Mode 2. The dead time and switching transient are exaggerated.

interval 6, no switching action takes place so there will be no effect on the power transfer. The rest six intervals are similar to first six intervals.

### 3.3 *Analysis*

The basic design equations has been derived using [1], [10], [11] and [12] and given in Table I. In these equations, $D_{eff}$ is effective duty ratio, D is primary duty cycle, $\Delta D$ is the loss in duty cycle due to transformer leakage inductance ( $L_{Llk}$ ), $I_{aux}$ is peak current in auxiliary inductor, $I_{ppk}$ and $I_{pv}$ are the primary peak and valley current respectively, $I_{L1pk}$ and $I_{L1v}$ are the peak and valley current of the output inductor $L_1$.

| | |
|---|---|
| 1 | $k = \frac{V_d \cdot D_{eff}}{V_o}$ |
| 2 | $D_{eff} = \frac{D}{\left[1 + \frac{L_{Llk} \cdot f_s}{k^2 \cdot R_o}\right]}$ |
| 3 | $D = \frac{1}{2} - \frac{t_d}{T_s} - \theta$ |
| 4 | $\Delta D = \frac{I_o \cdot L_{Llk}}{k \cdot V_d \cdot T_s}$ |
| 5 | $D_{\max} = \frac{1}{2} - \frac{t_d}{T_s}$ |
| 6 | $I_{ppk} = \frac{I_{L1pk}}{k} = \frac{1}{2 \cdot k}[I_o + \frac{V_o}{L_1}(1 - D_{eff})T_s]$ |
| 7 | $I_{pv} = \frac{I_{L1v}}{k} = \frac{1}{2 \cdot k}[I_o - \frac{V_o}{L_1}(1 - D_{eff})T_s]$ |
| 8 | $I_{aux} = \frac{V_d}{4L_{aux}}(\frac{T_s}{2} - t_d)$ |

Table I: Basic design equations for analysis

Due to space limitation, only the switching transitions equations has been given. The detailed analysis of the proposed topology is given in [13]. It is well understood that the switching transition from one switch to another occurs in the dead time. The dead time is constant for both the switching transition intervals.

### 3.4 *Analysis Equations for Mode 1*

#### A. *Interval 1 ($t_o \le t < t_1$)*

At the beginning of this cycle, the primary current reached at its peak value $I_{ppk}$. The drain to source voltage of both switches in leg A are governed by,

$$v_{ds1}(t) = V_d - \frac{I_{ppk}}{2C_{sb1}}(t - t_o) \quad (1)$$

$$v_{ds2}(t) = \frac{I_{ppk}}{2C_{sb2}}(t - t_o) \quad (2)$$

In the meantime, the current that flows through $S_4$ only consist of $i_{aux}$, which is the current of the auxiliary inductor $L_{aux}$. It is found that

$$i_{aux}(t) = \frac{V_d}{2L_{aux}}(t - t_o - \theta \cdot T_s) + I_{aux} \quad (3)$$

*B. Interval 3 ($t_2 \le t < t_3$)*

When $S_4$ is off, $i_{aux}$ reaches its positive peak value $I_{aux}$ and remains constant during this interval and the value of primary current, which is decreasing during this interval, can be defined as:

$$I_p(t) = \frac{\frac{V_d}{L_{Lik}}(t_3 - t_4) + I_{pv} + I_{ppk}}{(t_3 - t_1)}(t - t_1) - I_{ppk} \quad (4)$$

Similar to Interval 1, it is found that

$$V_{ds3}(t) = V_d - \int_{t_2}^{t_3} \frac{I_{aux} - \frac{\frac{V_d}{L_{Lik}}(t_3 - t_4) + I_{pv} + I_{ppk}}{(t_3 - t_1)}(t - t_1) + I_{ppk}}{2C_{sb3}} dt \quad (5)$$

$$V_{ds4}(t) = \int_{t_2}^{t_3} \frac{I_{aux} - \frac{\frac{V_d}{L_{Lik}}(t_3 - t_4) + I_{pv} + I_{ppk}}{(t_3 - t_1)}(t - t_1) + I_{ppk}}{2C_{sb4}} dt \quad (6)$$

*3.5 Analysis Equations for Mode 2*

*A. Interval 1 ($t_o \le t < t_1$)*

This interval is same as of Mode 1 so it is not repeated here.

*B. Interval 2 ($t_1 \le t < t_2$)*

At the beginning of this interval, $S_1$ is turned-on in ZVS condition. So, $S_1$ will achieve zero turn-on losses. Hence, $S_1$ consists of primary current which is governed by

$$I_p(t) = \frac{V_d}{L_{Lik}}(t - t_1) - I_{ppk} \quad (7)$$

The current passing through $S_4$ only has auxiliary current ($i_{aux}$) flowing through it, which is given by

$$i_{aux}(t) = \frac{V_d}{2L_{aux}}(t_1 - t) + I_{aux} \quad (8)$$

The duration of this interval is determined by the phase shift angle that is required to regulate the output voltage as well as by the dead time:

$$t_2 - t_1 = \frac{I_o \cdot L_{Lik}}{k \cdot V_d} \quad (9)$$

*C. Interval 4 ($t_3 \le t < t_4$)*

At the beginning of this interval, $S_4$ is turned-off and no other switching action takes place. The primary current starts to increase during this interval, which is given by:

$$I_p(t) = \frac{2I_{ppk} - \frac{V_d}{L_{Lik}}(t_2 - t_1)}{(t_6 - t_3)}(t - t_3) + \frac{V_d}{L_{Lik}}(t_2 - t_1) - I_{ppk} \quad (10)$$

Similar to Interval 1, it is found that

$$V_{ds3}(t) = V_d - \int_{t_3}^{t_4} \frac{I_{aux} - I_p(t)}{2C_{sb3}}(t - t_3) dt \quad (11)$$

$$V_{ds4}(t) = \int_{t_3}^{t_4} \frac{I_{aux} - I_p(t)}{2C_{sb4}}(t - t_3) dt \quad (12)$$

## 4.0 Design Curves

Based on the detailed analysis, characteristics curves for designing the converter are presented. Due to space limitation, only the following key design graphs are given. Fig. 4 shows the effective duty cycle $D_{eff}$ as a function of the leakage inductance for 100% and 20% of the rated output load current. This figure shows that the effective duty cycle reduces as the leakage inductance increases. The reduction in the effective duty cycle is more pronounced at higher load current. As the power transfer from input to the output is directly proportional to the duty cycle, the effect of higher leakage inductance is, therefore, reduction in the output power.

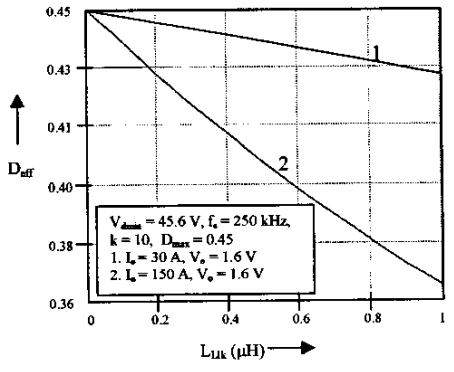



Fig. 4 Effective duty cycle ( $D_{eff}$ ) versus leakage inductance ( $L_{Lik}$ ).

For leg B, the primary current assists auxiliary current in discharging and charging the snubber capacitors across $S_3$

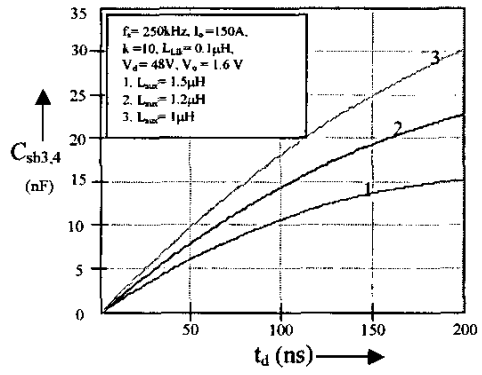



Fig. 5 Snubber capacitor ( $C_{sb3,4}$ ) versus dead time ( $t_d$ ) with leakage inductance ( $L_{Lk}$ =0.1μH) and k=10 for Leg B.

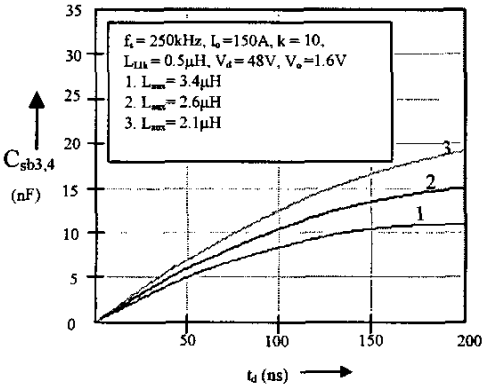



Fig. 6 Snubber capacitor ( $C_{sb3,4}$ ) versus dead time ( $t_d$ ) with leakage inductance ( $L_{Lk}$ =0.5μH) and k=10 for Leg B.

and $S_4$. That's why the value of auxiliary inductor is higher than the value where the leakage inductance ( $L_{Lk}$ ) is assumed to be zero. But the higher value of leakage inductance will reduce the effective duty cycle ( $D_{eff}$ ) and lower overall efficiency of the circuit.

Particularly, to successfully discharge the snubbers for leg B within the switching dead time $t_d$, the discharging current is required to be

$$I_{B\_discharge} \geq \frac{C_{sb3,4} \cdot V_d}{t_d} \tag{13}$$

By using equations (4) through (6), $I_{B\_discharge}$ for $S_3$ or $S_4$ is given by

$$I_{B\_discharge} = \frac{1}{2}\left( \frac{V_d}{4 \cdot L_{aux}}\left(\frac{T_s}{2} - t_d\right) - \frac{\frac{V_d}{L_{Lk}}(t_3 - t_4) + I_{pv} + I_{ppk}}{(t_3 - t_1)}(t - t_1) + I_{ppk} \right)$$

(14)

Using equations (13) and (14) the graphs shown in Fig. 5 and 6 has been plotted to determine the value of snubber capacitor ( $C_{sb3,4}$ ) as a function of the minimum dead time $t_d$, which is required to achieve the ZVS of the main inverter switches, for the various auxiliary and leakage inductance. It is observed from these figures that for the same dead time and snubber capacitor, the value of auxiliary inductance is higher for the higher value of leakage inductance. For example, Fig. 5 shows that for $L_{Lk}$=0.1 μH, $t_d$=200 ns and $L_{aux}$=1.5 μH, the required value of the snubber capacitor is 15 nF. Now, if we examine Fig. 6, which is given for $L_{Lk}$=0.5μH, it is observed
that for the same values of $t_d$ and $C_{sb3,4}$, the required value of $L_{aux}$ is now equal to 2.6 μH. Therefore, there is a direct effect of the leakage inductance on the selection of auxiliary circuit parameters.

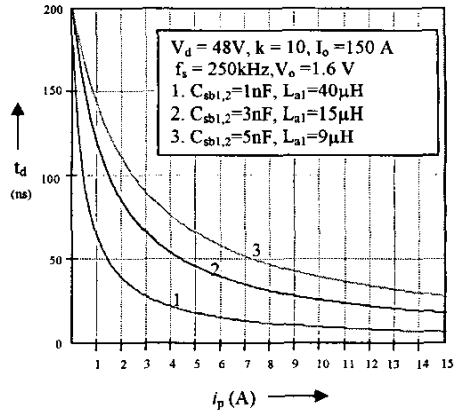



Fig. 7 Dead time ( $t_d$ ) versus primary current ( $i_p$ ) with k=10 for Leg A.

No-load condition is going to be the worst condition for Leg A. For the successful discharge of the snubber capacitors with in the dead time, the discharging current required is

$$I_{A\_discharge} \geq \frac{C_{sb1,2} \cdot V_d}{t_d} \tag{15}$$

The discharging current for switches in Leg A has a magnitude determined by

$$I_{A\_discharge} = \frac{I_{ppk}}{2} \tag{16}$$

For the applications where output current reduces less than 20%, an auxiliary inductor is added in Leg A. Now the peak value of this primary current ( $I_p$ ) is given by

$$I_P = I_{a1} + I_{ppk} \tag{17}$$

where, $I_{a1}$ is the peak value of the current passing through $L_{a1}$ and is given by

$$I_{a1} = \frac{V_d}{4 \cdot L_{a1}} \left(\frac{T_s}{2} - t_d\right) \tag{18}$$

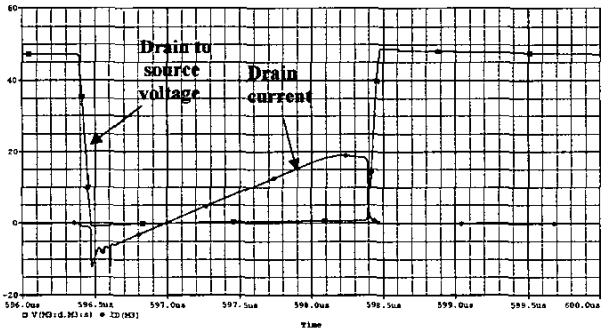
The graph plotted between primary current and dead time in Fig. 7 shows the different values of auxiliary inductor $L_{a1}$ and snubber capacitor $C_{sb1,2}$ required to achieve ZVS condition, from no load to full load, within the dead time $t_d$. ZVS can be achieved for any load with the expense of small increase in conduction losses.

## 5.0 Simulation Results

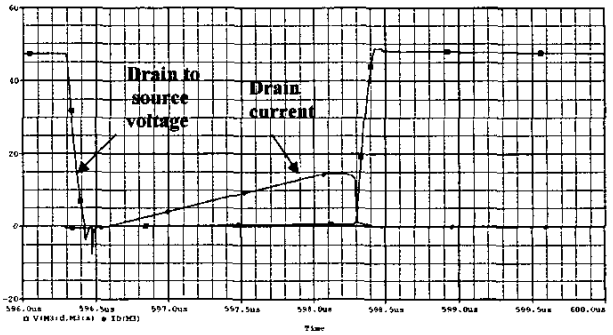
Simulation of the proposed converter topology is performed with the ORCAD software. Table II shows the principal parameters used in the simulation.

| parameter | Value/parameter | parameter | value/parameter |
|---|---|---|---|
| $V_{d\min} / V_{d\max}$ | 45.6V/50.4V | $t_d$ | 200ns |
| k | 10:1 | $C_{V1}, C_{V2}$ | 8μF, each |
| $V_o$ | 1.6V | $I_o$ | 150A |
| $S_1, S_2, S_3, S_4$ | IRFP150 | $S_{R1}, S_{R2}$ | IRL3803 |

Table II Principal parameter of the simulation circuit

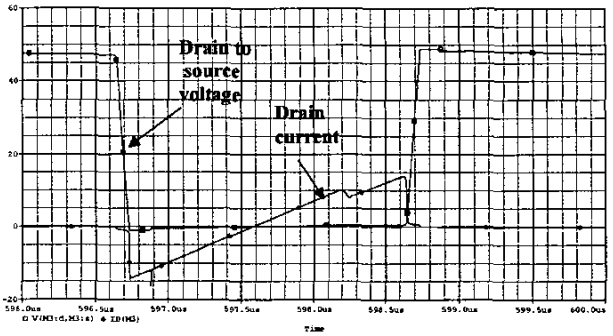



8 (a)

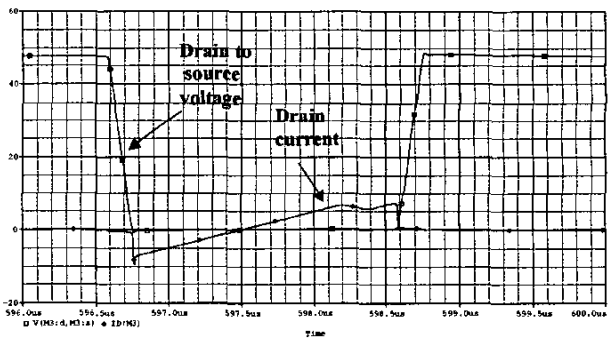



8 (b)

Fig. 8: Simulation results for Leg B (a) at $L_{Lik}$ =0.1μH (b) at $L_{Lik}$ =0.5μH with $C_{sb3,4}$ =15nF at Full Load




9 (a)




9 (b)

Fig. 9: Simulation results for Leg B (a) at $L_{Lik}$ =0.1μH (b) at $L_{Lik}$ =0.5μH with $C_{sb3,4}$ =15nF at 20% Load

Fig. 8 and Fig. 9 shows the voltage and current waveforms of the switches under full load and 20% load current respectively for Leg B. It is seen that ZVS is achieved at both turn-on and turn-off. As explained earlier, Leg B is the critical leg of the inverter where natural ZVS is lost at

considerably higher load current, therefore, the voltage and current waveforms for the switches of this Leg are only shown in Fig. 8 and Fig. 9.

For the applications where output current reduces less than 20%, an auxiliary inductor is added in Leg A. Simulation result for Leg A shown in Fig. 10 has been performed by using characterstics curve shown in Fig. 7.

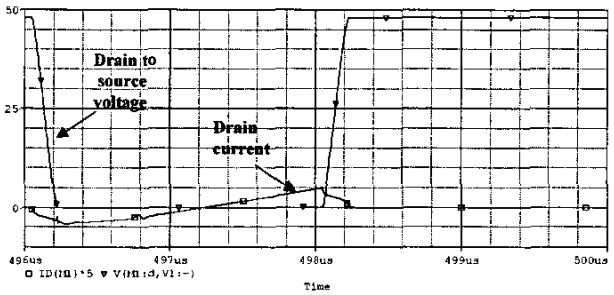



Fig. 10: Simulation result for Leg A at $L_{Llk}$ =0.5μH, $L_{al}$ =40μH with $C_{sb1,2}$ =1nF at 1% load.

## 6.0 Conclusions

In this paper an auxiliary commutated full-bridge inverter has been analyzed which includes the effect of transformer's leakage inductance to optimize the performance. It is shown that the leakage inductance has positive influence in reducing the circulating current caused by the auxiliary circuit to achieve the zero voltage switching. In addition, a current doubler rectifier circuit using externally driven synchronous switches further reduces the conduction losses in the rectifying stage. The optimized converter topology is expected to find applications in designing low-voltage and high-current point-of-use power supplies for servers.

## 7.0 References

[1] J. A. Sabate, V. Vlatkovic, R. Ridley, F. C. Lee and B.H. Cho "Design considerations for high- voltage, high-power, full-bridge, zero-voltage-switched, PWM converter," IEEE APEC '90 Records, pp. 275-284.

[2] R. A. Fisher, K. Ngo and M. Kuo, "A 500 kHz, 250 W dc/dc converter with multiple outputs controlled by phase-shifted PWM and magnetic amplifiers," Proceedings of High Frequency Power Conversion Conference, 1988, pp. 100-110.

[3] M. Walters and W. Polivka, "A high density modulator power processor for distributed military power systems," IEEE APEC '88 Records, pp. 403-412.

[4] L. H. Mweene, C. A. Wright and M. F. Schelcht, "A 1 kW, 500 kHz front-end converter for a distributed power supply system," IEEE PESC'89 Records, pp. 423-432.

[5] R. L. Steigerwald, "A review of soft-switching techniques in high performance dc power supplies", IEEE IECON'95 Records, pp. 1-7.

[6] R. W. Dedoncker and J. P. Lyons, "The auxiliary resonant commutated pole converter," IEEE IAS'90 Records, pp. 1228-1235.

[7] R. Teichmann and S. Bernet, "Investigation and comparison of auxiliary resonant commutated pole converter topologies," IEEE PESC'98 Records, pp. 15-23.

[8] O. D. Patterson, D. M. Divan, "Pseudo-resonant full bridge dc/dc converter," IEEE PESC'87, pp. 424-430.

[9] M. Nakaoka, S. Nagai, Y. J. Kim, Y. Ogino and Y. Murakami, "The state-of-the-art phase-shifted zvs-pwm series & parallel resonant dc-dc power converters using internal parasitic circuit components and new digital control," IEEE PESC'92, pp. 62-70.

[10] Praveen Jain, Wen Kang, Harry Soin and Youhao Xi, "Load and Line Independent Zero Voltage Switching Full Bridge DC/DC Converter Topology," *proceeding of* INTELEC'98, pp. 22-29.

[11] Laszlo Balogh, "Design Review: 100W, 400KHz, dc/dc converter with current doubler synchronous rectification achieves 92% efficiency," *Unitrode Power Supply Design Seminar*, 2.1-2.25, 1996.

[12] David J. Hamo, "A 50W, 500kHz, full-bridge, phase-shift, ZVS Isolated DC to DC converter using the HIP4081A," *Intersil*, No. AN9506, April 1995.

[13] Dheeraj K. Jain, "Analysis and design of an auxiliary commutated full bridge dc/dc convverter for low voltage and high current applications," *M.A.Sc. Thesis*, In the Department of Electrical and Computer Engineering, Montreal, Canada, December 2001.