Optimum Design Considerations for a High Efficiency ZVS Full Bridge DC-DC Converter

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Abstract: **This paper focuses on the ZVS operation and design considerations for a ZVS DC-DC full bridge converter. With the proposed circuit diagram the efficiency can be improved comparing with a conventional phase shift full bridge (PSFB), and the voltage ringing across the rectifier diodes can be reduced significantly by clamp circuits. A 1.2kW(50V/24A) prototype with a efficiency of 95% is made to verify the theoretical analysis .**

I INTRODUCTION

The phase shift ZVS full bridge(FB) converter is widely used in high power applications because of it's high power density, low EMI, and simply control strategy[1,2]. In a conventional PSFB converter, the leakage inductance or series inductance must be large enough to ensure the ZVS for the lagging leg switches[3-4]. However a large series inductance will bring out large duty cycle loss and voltage ringing across the rectifier diodes. Some improvements have been proposed to reduce the duty cycle loss and suppress the voltage ringing[5-11]. Two clamp diodes and a series inductor are added to extend ZVS range and relax the voltage ringing across the rectifier diodes[3,4]. But the duty loss is still large because of the large series inductor and it still can't achieve ZVS at very light load. Some converters utilizing the magnetizing current of transformer[13] or paralleled inductor, and other assistant current source[8] to improvement ZVS for the switches of the lagging leg. With the assistant current source it can achieve ZVS without increasing duty loss if the leakage inductance of the transformer is small, and ZVS is independent of the input voltage.

However if the series inductance or leakage inductance is very small, during the passive to active transition period, the reflected load current opposes the magnetizing current in the transformer and sinks the current from the assistant current source before the parasitic capacitor of MOSFET fully discharged or charged[12]. Hence ZVS fails if the assistant current is not larger than the reflected load current at full load condition. To achieve ZVS at heavy load the magnitude of assistant current source must be higher than the reflected full load current, which results in high conduction loss especially in high power level.

A family of FB converters, which can achieve ZVS from full load to no load by adding a series coupled inductor were proposed in [9,10]. However these converters suffer from the same drawbacks as of other current source assistant converters mentioned above. An improved PSFB converter as shown in Fig.1 was proposed in [12], which can solve these problems mentioned above by adding two auxiliary coupled inductors L_{lk1}, L_{lk2} and two clamp diodes Dc1 ,Dc2, but the ZVS condition and the designing of the key parameter weren't given in [12]. This paper discusses the ZVS operation condition and the optimal design considerations to achieve high efficiency and full load range ZVS. The operation principle of the proposed converter will be given in the next section. The design consideration will be given in the third section.

II OPERATION PRINCIPLE OF THE PROPOSED CONVERTER

A. The Circuit Diagram of the Improved Converter

As shown in Fig.1 the circuit consists of two half bridges with coupled primary windings. The two inductors Lr1, Lr2 and two small auxiliary inductors L_{lk1} and L_{lk2} are coupled respectively.

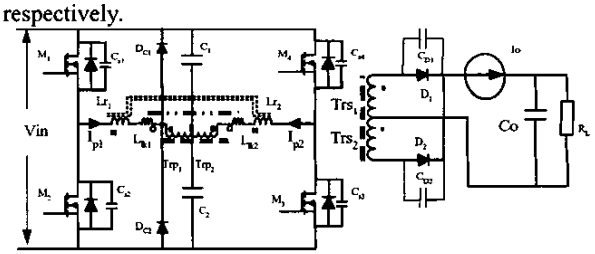

Fig.1 The circuit diagram of the improved ZVS PSFB DC-DC converter

Trp_1 and Trp_2 are the primary windings of the transformer with same turn count, and Trs_1, Trs_2 are secondary windings. N_{Trp1}:N_{Trs1} =n1. L_{r1} and L_{r2} are coupled inductors with the same turns. L_{lk1} and L_{lk2} are small inductors in series of the transformer winding and L_{lk1}=L_{lk2}.

To relax the voltage ringings across the output rectifier diodes two clamp diodes Dc1, Dc2 are added as shown in Fig.1. Because the inductor Lr1 and Lr2 are coupled, the needed clamp diodes can be reduced to two. The two primary windings of the transformer are connected in opposite manner as shown in Fig.1. Therefore the current through the midpoint of transformer is the sum of two winding currents, and the primary side peak current control method can be employed. To simplify the analysis a large block capacitor is neglected, which is in series with the

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transformer winding in the experimental circuit to block the DC bias of the transformer. Due to the large inductance of Lo, the inductor Lo can be seen as a current souse Io.

B. The Operation Stages in a Half Switching Cycle

To simplify the analysis the parasitic capacitance of the transformer is replaced by the junction capacitor C_{D1} and C_{D2} shown in Fig.1. Because the detailed analysis of every operation stages of half switching cycle has been discussed in [12], the stages are explained simply in this paper. Fig.2 is the key waveforms in one switching cycle and Fig.3 is the equivalent circuits of the corresponding stages.

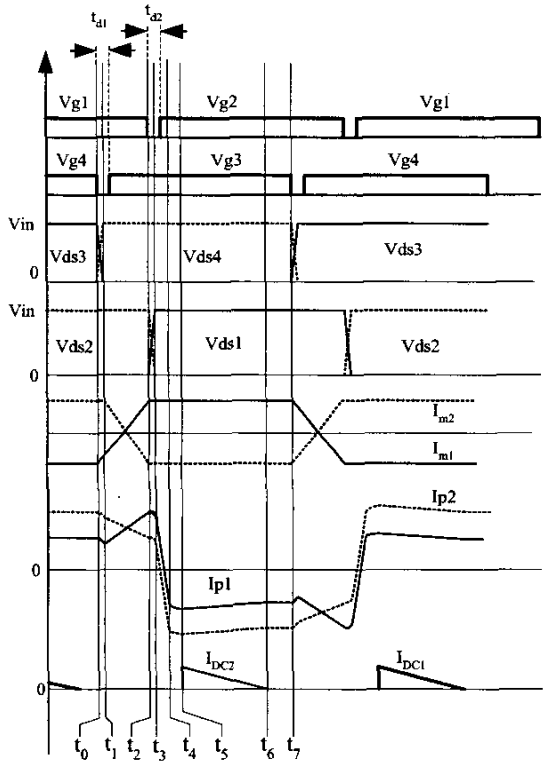
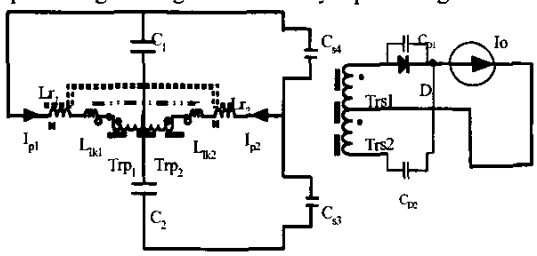


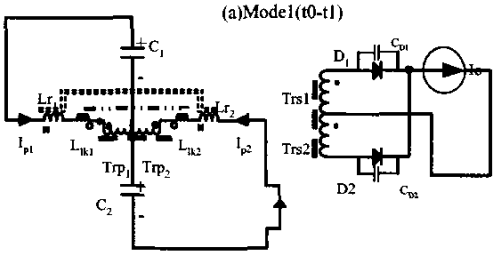
Fig.2 The key waveforms of the converter in one switching cycle

Mode1(t_0-t_1): Before the time t_0 the switches M1, M4 are on. The voltages across T_{rp1} and T_{rp2} are both half of input voltage Vin, the energy is transferred to the load. At t0 M4 turns off, due to the junction capacitance of M4 the voltage across M4 is almost clamped at zero, therefore switching off loss is reduced. During this interval the capacitors C_{s3}, C_{s4} are discharged and charged respectively until the voltage across C_{s4} reaches V_{IN}.

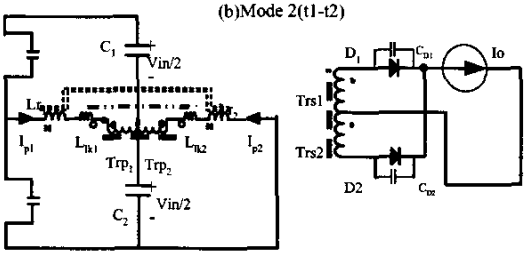
Mode2(t_1-t_2): During this interval the current I_{p2} flows through the anti-paralleled diode of M3 when the voltage across C_{s3} reaches zero. M3 is switched on when the anti-paralleled diode is on. The voltage across transformer is clamp at zero because the rectifier diodes both D1 and D2 are on. The coupled inductors L_{r1} and L_{r2} are charged by the input voltage during this interval by input voltage.



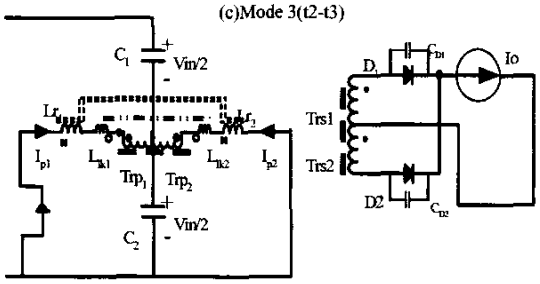
(a)Mode1(t0-t1)



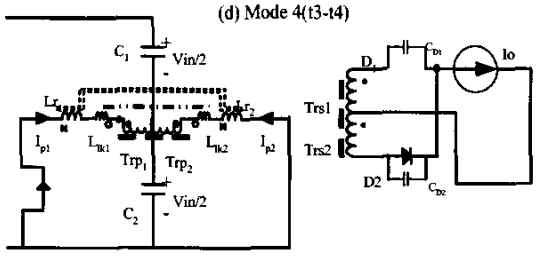
(b)Mode 2(t1-t2)



(c)Mode 3(t2-t3)



(d) Mode 4(t3-t4)



(f) Mode 5(t4-t5)

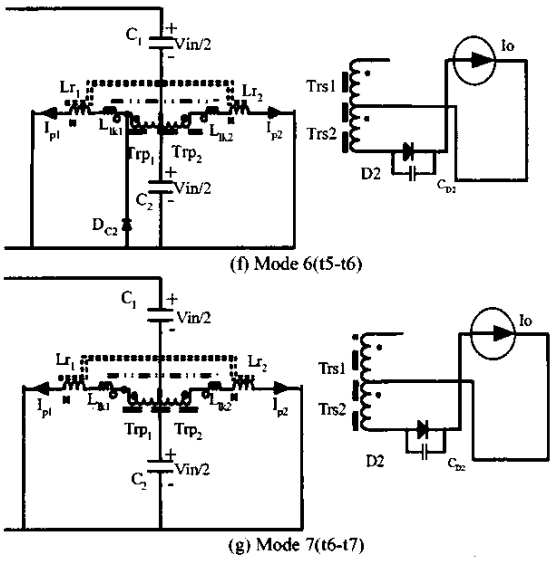


Fig.3 The seven equivalent circuits of operation modes in half switching cycle

Mode3(t_2-t_3): At t_2 M1 is switched off, then the storage energy in L_{lk1},$L_{lk2}$and L_{r1},L_{r2} will charge and discharge the capacitors C_{s1} and C_{s2} respectively. This period ends when the capacitor C_{s1} is charged fully until the drain to source voltage of M1 reaches Vin.

Mode4(t3-t4): At t3 the anti-paralleled diode of M2 is on because the voltage across C_{s2} is discharged to zero. After t3, the M2 switches on and ZVS is achieved. Because the D1 and D2 are still conducting and the voltage across the series coupled inductors L_{lk1} and L_{lk2} are $V_{IN}/2$.

Mode5(t4-t5): When the current I_{p1} of primary reaches the value -(Io/n1-Im) at t4, the diode D1 cuts off. Then the capacitor C_{D1} will interact with the inductance L_{lk1} and L_{lk2}. This period ends when the voltage across the capacitor C_{D1} reaches at 2Vin/(n1) while the voltages across the primary winding Trp1 and Trp2 of the transformer reach Vin/2 respectively.

Mode6(t5-t6): At t_5 the clamp diode D_{C2} conducts after the voltage across the transformer winding reaches Vin/2. The transition of lagging leg switches is finished. The current difference between the inductance Llk1 and the current of the winding Trp1 flows through the clamp diode. Owing to the clamping diode D_{C1} the voltage across diode D1will be clamped at 2Vin/n1. This period ends when the clamping diode cuts off because the difference current decreases to zero. During this interval the energy is transferred to the load.

Mode7(t6-t7): After the clamp diode cuts off, the current of the inductance L_{lk1} will be equal to the current of the winding Trp1. During this interval the energy is still transferred to the load. This period ends at t7, when the switch M3 switches off. Then the next operation mode will be similar to mode 1.

The next half switching cycle is similar to the analysis mentioned above except the opposite polarity of the currents through the transformer windings and voltages across the transformer windings.

III Analysis and Optimal Design Considerations

A. The ZVS Range

The leading leg ZVS range: To achieve the ZVS operation in overall load range of all switches the coupled inductors should be designed appropriately. The simplified equivalent circuits of the leading leg (M3,M4) and the lagging leg transitions(M1,M2) are shown in Fig.4 and Fig.5 respectively.

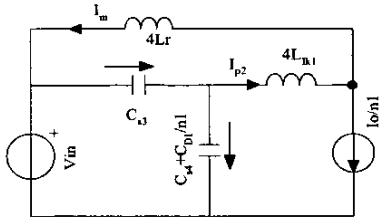


Fig.4 The leading leg transition equivalent circuit

Before the transition of the leading leg, the magnetizing current Im of the coupled inductor Lr1, and the currents Ip1 and Ip2 can be described as equations (1)-(3). The current ripple of the filter inductor is considered in the current Ip1 and Ip2. Due to the large inductance of the inductor Lr1, the current Im can be seen as a current source during the transition periods of the leading leg and the lagging leg.

$$I_m = \frac{1}{2}\frac{Vin\times(1-D)}{4Lr1\times 2\times fs} \quad (1)$$

$$I_{p2}(t_0) = I_m + (Io/n1) + \Delta Io/(2*n1) \quad (2)$$

$$I_{p1}(t_0) = (Io/n1) + \Delta Io/(2*n1) - I_m, \quad (3)$$

where D is the operation duty cycle of the converter, ΔIo is the current ripple of the output current, and fs is the switching frequency, Io is the load current.

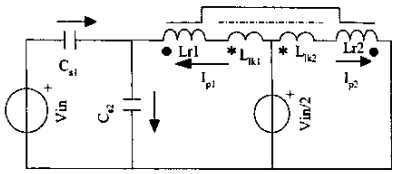
ZVS switching for the leading leg switches is achieved easily because of the large filter inductance of Lo. At heavy load condition, it can be seen as a current source and the capacitor Cs is charged easily by this current source. Even at very light load, Io is almost zero and the current source Im still flows through the leading leg switches because of the large inductance of Lr1 and Lr2. Therefore the parasitic capacitors of the MOSFETs will be fully charged linearly by the current source Im during the dead time between the leg switches. In fact when the load current is null the duty cycle will be very small, and the current source Im described in (1) will be much larger than the reflected load current. Therefore the most difficult ZVS condition is at critical continuous condition because the duty is still larger while the reflected load current is small. Hence to achieve ZVS for the leading leg switches at full load range, the inductance Lr1 must match the equation (4).

$$Lr1 \le \frac{(1-D\max)}{16fs\cdot(\frac{(Cs+C_{D1}/n1)}{td1}-\frac{(Vin/n1-Vo)\cdot D\max}{Lo\cdot n1})} \quad (4)$$

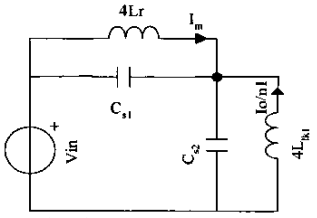
where t_{d1} is the dead time between the leading leg switches shown in Fig.2, and Dmax is the maximum duty cycle of the critical continuous mode of the output current.

The lagging leg ZVS range: The ZVS operation condition of lagging leg switches is critical, and it determines the ZVS operation of the proposed converter.

The currents and voltages of the key components during t1 and t2 are presented in equations (5)-(8). Fig.5 shows the simplified equivalent circuits of the transition period of the lagging leg.



(a) equivalent circuit



(b). Simplified circuit from (a)

Fig.5 The transition equivalent circuit of lagging leg

$$I_{p2}(t) = I_{p2} - I_{m2}(t) \quad (t1<t<t2) \quad (5)$$

$$I_{p1}(t) = I_{p1} + I_{m1}(t) \quad (t1<t<t2) \quad (6)$$

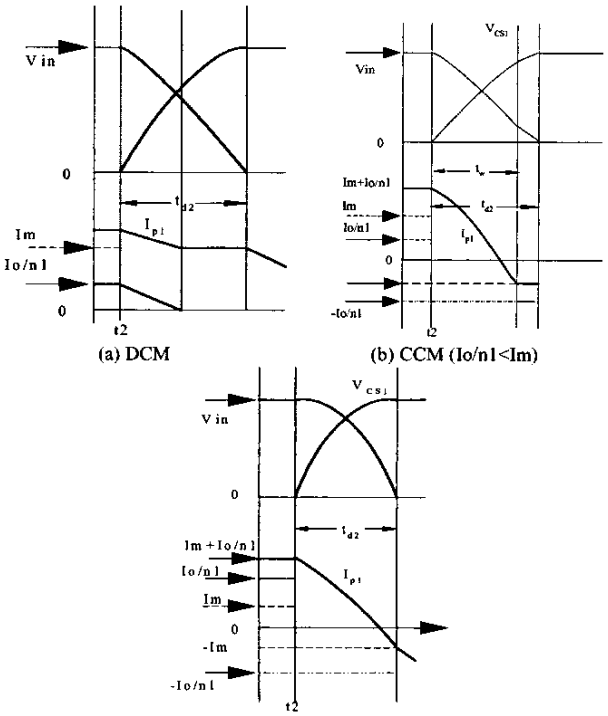
$$I_{m1}(t) = \frac{Vin\times(t-t1)}{4Lr1} - I_m \quad (t1<t<t2) \quad (7)$$

$$I_{m2}(t) = \frac{-Vin\times(t-t1)}{4Lr} + I_m \quad \text{if } (t1<t<t2), \quad (8)$$

where $I_{m1}(t)$ and $I_{m2}(t)$ are the magnetizing current of the coupled inductance Lr1 and Lr2 respectively before the lagging leg transition, and $(t2-t1)\approx(1-D)T$. Therefore the current $Ip1(t2)=(Io/n1+Im)$.

The transition of lagging leg switches can be divided into three stages according to the relationship between the load current Io and the current source Im as shown in Fig.6.

Before calculating the ZVS condition, we suppose the dead time t_{d2} =Tc/4 where $Tc=2\pi\sqrt{8\cdot L_{lk1}\cdot Cs1}$.



(a) DCM (b) CCM (Io/n1<Im)

(c) CCM (Io/n1>Im)

Fig.6 The key current and voltage of the lagging leg transition period at different output current modes

When the transition begins at t2, the voltage across the capacitance Cs1 and current through the inductor L_{lk1} can be described as (9) and (10).

$$v_{Cs1}(t) = ZrI_{p1}(t2)\sin\omega r(t-t2) \quad \text{if } (t2<t<t3) \quad (9)$$

$$I_{p1}(t) = \text{Im} - I_{p1}(t2)\times\cos\omega r(t-t2) \quad \text{if } (t2<t<t3) \quad (10)$$

where $Zr=\sqrt{\frac{2L_{lk1}}{Cs}}$, $\omega r=\frac{1}{\sqrt{8L_{lk1}\times Cs}}$ and $I_{p1}(t2)$=Im, if the current $Io\approx 0$.

To analysis the ZVS condition at very light load current the current ripple flowing in the filter inductor Lo can't be neglected. The operation mode will vary with the load current because the current of filter inductor can't remain constant at light load condition due to current ripple. Equation (11) describes the magnitude of the voltages across the capacitors Cs3, Cs4 with the certain dead time t_{d2} without considering the input voltage clamp. From Fig.7 corresponding to (11) we can see that when the maxim voltage of Cs3 and Cs4 can be higher than Vin, ZVS switching of lagging leg switches can be achieved. With different leakage inductance L_{lk1} the voltage magnitude in function of load current Io is different, and lager L_{lk1} results in higher magnitude voltage.

$$V_{CS1}(Io)\begin{cases} Zr\cdot Ip1(Io)\cdot\sin(\omega r\cdot td2) & if(n1\cdot \mathrm{Im}+\Delta Io/2)<Io<Io_{\max} \\ Zr\cdot Ip1(Io)\cdot\sin(\omega r\cdot td2)+\dfrac{(\mathrm{Im}-Io/n1+\Delta Io/2n1)\cdot(td2-tw)}{2\cdot Cs1} & if(\Delta Io/2)<Io<(n1\cdot \mathrm{Im}+\Delta Io/2) \\ Zr\cdot Ip1(Io)\cdot\sin(\omega r\cdot td2)+\dfrac{\mathrm{Im}2(Io)\cdot(td2-tw)}{2\cdot Cs1} & if\,0<Io<\Delta Io/2 \end{cases} \quad (11)$$

$$\mathrm{Im}2(Io)=\frac{Vin\cdot(1-\frac{8\cdot n1\cdot Lo\cdot Io}{Vin-2n1\cdot Vo})\cdot T}{8\cdot Lr1} \qquad if\,0<Io<\Delta Io/2 \quad (12)$$

where Im2(Io) is the magnetizing current in function of load current Io because the duty cycle varies with load current at DCM mode, Lo is the output filter inductance, and Vo is the output voltage.

From the above equations we can see that another factor which influences the ZVS condition is the inductance Lr1. Lower inductance Lr1 results in larger magnetizing current which assists to achieve ZVS for all switches. From the equations (1),(10) and (11), we can obtain curves of the inductance Lr1 in function of Io as shown in Fig.8, from which we can see that design of the inductance Lr1 must match the critical DCM mode condition of load current because the most difficult condition of ZVS is at the critical DCM mode.

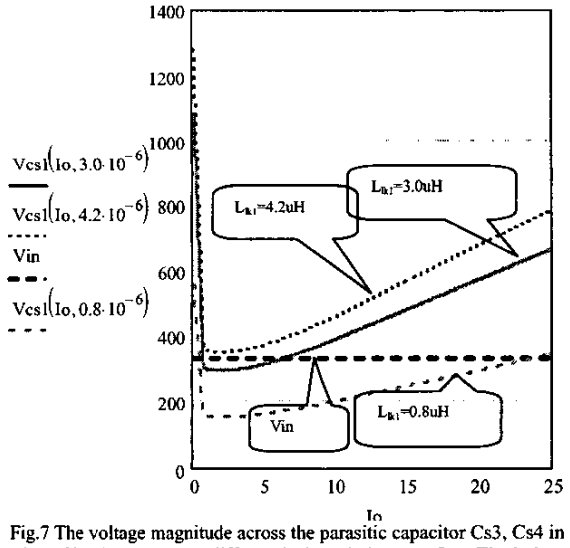


Fig.7 The voltage magnitude across the parasitic capacitor Cs3, Cs4 in function of load current Io at different leakage inductance L_{lk1}. The inductor Lr1=30uH and Lo=40uH.

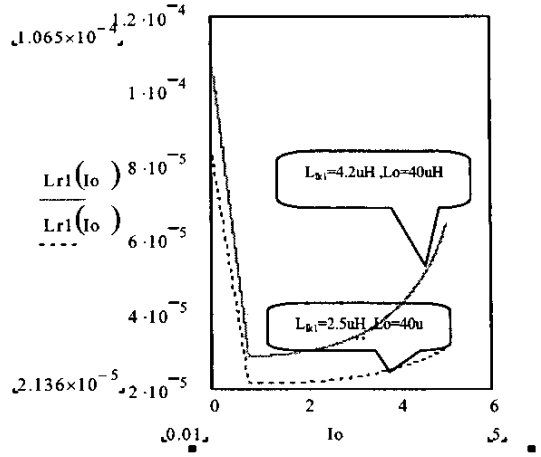


Fig.8 The function diagram of inductance Lr1 Vs load current at different leakage inductance L_{lk1}.

From the key waveforms shown in Fig.6, transition of the lagging leg switches is similar to the conventional PSFB with assistant current source to achieve ZVS. But the energy stored in the inductance L_{lk1} is larger than the conventional PSFB at light load, and the assistant current source will increase with the increase of duty cycle. Hence with appropriate inductance Lr1, the inductance L_{lk1} can be reduced and the duty cycle loss will be smaller than the conventional PSFB .

B. Conduction Loss of the Primary Switches

In the experiment the MOSFETs of leading leg and lagging leg are IXYH20N50 and IRFP460 respectively. The conduction loss can be calculated according to equation (13)-(18). Fig.9 shows the conduction loss in function of the inductance Lr1. From Fig.9 we can see that the conduction loss will increase with the reducing of the inductance of Lr1. The calculation results are based on the inductance L_{lk1}=4.2uH.

$$Plead1=\int_0^{D\max\cdot T}(\mathrm{Im}+Io/2n1)^2\cdot Rdslead\cdot dt\cdot fs \quad (13)$$

$$Plead2=\int_{D\max T}^{T}(\mathrm{Im}+Io/2n1-\frac{Vin(t-D\max T)}{4Lr1})^2\cdot Rdslead\,dt\cdot fs \quad (14)$$

$$Plead=2\cdot(Plead1+Plead2) \quad (15)$$

$$Plag1=\int_0^{D\max\cdot T}(-\mathrm{Im}+Io/2n1)^2\cdot Rdslag\cdot dt\cdot fs \quad (16)$$

$$Plag2 = \int_{D\max T}^{T} (-\mathrm{Im} + Io/2n1 + \frac{Vin(t - D\max \cdot T)}{4Lr1})^2 \cdot Rdslag \cdot dt \cdot fs \quad (17)$$

$$Plag = Plag1 + Plag2 \quad (18)$$

where Rdslead=0.3, Rdslag=0.25.

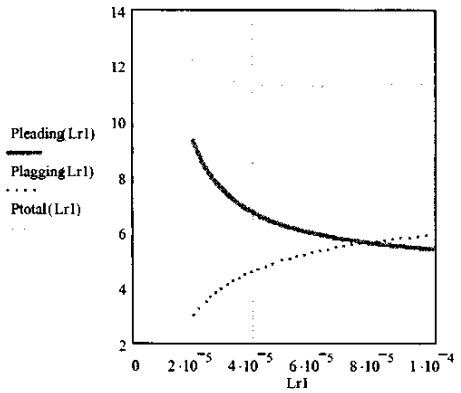


Fig.9 The calculated conduction loss in function of the inductance Lr1.

C. Duty Cycle Loss

The duty loss is in proportional to the inductance L_{lk1}. From the analysis in last paragraph, the larger inductance L_{lk1} will be helpful to achieve ZVS, and the smaller inductance Lr1 is also helpful to reduce conduction loss. However the duty loss will increase with the increasing inductance L_{lk1} and the conduction loss of primary will increase with the reducing of the inductance Lr1. Therefore a trade off between the inductances L_{lk1} and Lr1 must be make in designing an optimized DC-DC converter.

D. Measures to Suppress the Voltage Ringing Across the Rectifier Diodes

To restraint the voltage ringings across the rectifiers caused by the leakage inductance of the transformer, another clamp circuit can be employed especially when the leakage inductance is large, and can't be neglected. The experimental circuit is shown in Fig.10. An auxiliary winding of the transformer with four clamp diodes consists of this clamp circuit which is clamp to the input. With this clamp circuit the clamp diodes Dc1 and Dc2 can be removed. The turn number of the auxiliary winding is $(2N_{Trp1}-1)$ where N_{Trp1} is the turn number of transformer winding T_{rp1}. Therefore the voltage of the transformer winding can be clamped at a certain value which is a little higher than the voltage Vin/2 as shown in equation (15).

$$V_{clp} = \frac{1}{2} \frac{Vin \times N_{Trp1}}{(2 \times V_{Trp1} - 1)} \quad (15)$$

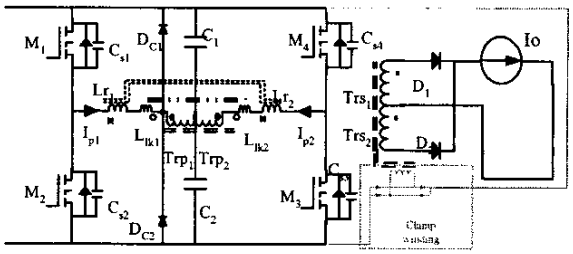


Fig.10 The experimental circuit with an auxiliary clamp circuit

IV Experimental Results

To verify the analysis, an 1.2kW(50V/24A) prototype is implemented based on above optimum design. Fig.11 and Fig.12 show the voltage waveforms of the drive signal and drain to source voltages of all MOSFETs. ZVS switching is achieved at full load and light load for all switches. The current waveforms of transformer are shown in Fig.13. At light load condition (Io=1A), the current of the transformer is still large because of the current source I_{Lr1} is larger than heavy load condition. Therefore the conduction loss is larger than conventional PSFB converter at light load.

Fig.14 shows the voltages across the rectifier diode with and without the clamp circuit respectively. Either auxiliary winding or two clamp diodes have the same clamp effect in suppressing the voltage ringing. The voltage spike is clamp at about 150V, and schottky diodes with 200V break down voltage can be employed at the rectifier diodes.

The measure efficiency diagram is shown in Fig.15. The efficiency at full load is above 95%. The parameters the key components of the prototype are listed in table 1.

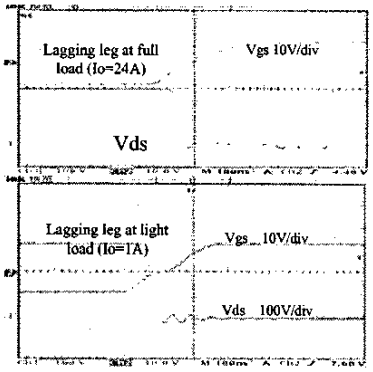
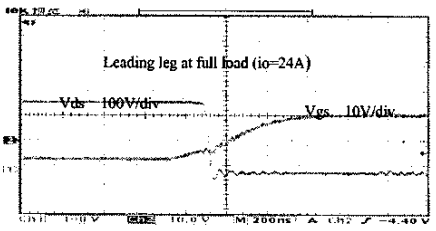


Fig.11 The measured waveforms of driving and drain to source voltages of the lagging leg switches at full load and light load respectively.



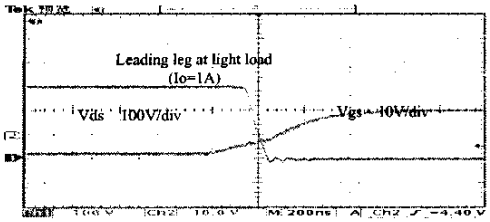
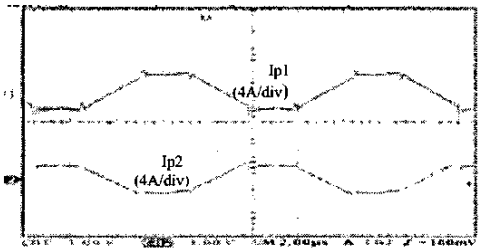


Fig.12 The measured waveforms of driving and drain to source voltages of the leading leg switches at full load and light load respectively



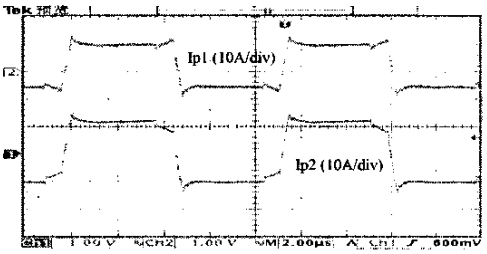


Fig.13 Measured current of the transformer at full load (bottom) and light load (top) respectively.

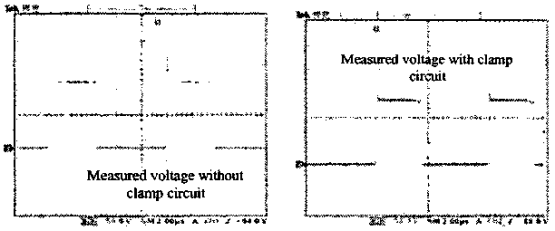


Fig.14 Measured voltages acrosss the rectifier diode without and with clamp circuit respectively. (50V/div)

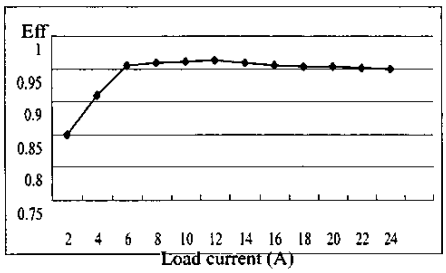


Fig.15 The measure efficiency Vs load current without considering the driving and control circuits loss.

TABLE I

THE MAIN COMPONENTS PAREMETER OF THE EXPERIMENTAL CIRCUIT

Component	type	Component	Value
M1,M2	IRFP460	Lr1,Lr2	42uH
M3,M4	IXFH20N50	L_{lk1},L_{lk2}	4.2uH
D_{C1},D_{C2}	FR157	n1	10:4
D1,D2	MBR20200CT	T1 Core: EE55/TDK	

V CONCLUSION

The detailed analysis of an improved PSFB converter is presented, and it is helpful to make an optimized DC-DC power supply with high efficiency and low EMI. An 1.2kW (105kHz) prototype is made to verify the analysis. By making a trade off between the conduction loss and ZVS condition, the efficiency of the converter is higher than 95% at full load is achieved. Two clamp circuits shown in Fig.10 are added to suppress the voltage ringings across the rectifier diodes.

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