

TWO-DIMENSIONAL FINITE ELEMENT SIMULATION AND STRESS ANALYSIS OF A FULL BRIDGE DC-DC POWER CONVERTER

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Abstract – The power MOSFETs used in DC-DC converters undergo excessive electrical and thermal stress as a result of higher switching frequency operation for size and cost reduction. The next generation of power MOSFETs have to be designed and optimized at the application level, which involves identification of tradeoffs among critical circuit and device performance and reliability parameters. This paper presents the results obtained from measurements and two-dimensional (2-D) finite element simulations conducted to evaluate the various electrical stresses applied to a power MOSFET in a 350V – 3.5V, 225A full-bridge (FB) phase-shifted ZVS DC-DC converter. MOSFETs were found to fail under no-load converter operation in the field.

INTRODUCTION

Recent advances in power semiconductor device technology have resulted in a remarkable growth in power electronics. Because of the lack of interaction between circuit designers and device manufacturers, many of the devices available in the commercial market today are not optimized to meet the performances and reliability requirements of the power electronic applications in which they will be eventually used. For example power semiconductor devices are not optimized for resonant converter applications. The next generation of power semiconductor devices have to be designed and optimized at the application level, which involves identification of tradeoffs among critical circuit and device performance and reliability parameters (1).

Presently system-level and device-level optimization is accomplished through an expensive and time-consuming approach, which includes examination of a range of parameters and experimental determination of the best product, which opposes the purpose of optimization and product cost reduction. Therefore a circuit and device design methodology must be used, where the device meets the design specifications while accounting for

application-specific switching stresses. Simulation techniques significantly reduce the development time while allowing a wider range of parameter variation.

There has been a continuous effort to increase the power density, and operation frequencies of power converters. Higher operation frequencies result in smaller size, and therefore greater electrical and physical interaction. In spite of slightly inferior on-state performance compared to bipolar devices, silicon power MOSFETs are extensively used in medium-voltage power supplies because of their simplicity of operation, and faster switching. In conventional hard-switched FB DC-DC converter topology higher switching frequency results in smaller reactive components size, but increases MOSFET switching losses, heat sink requirement or number of paralleled devices, and over-voltage stress as a result of parasitic inductance and body diode reverse recovery. Zero voltage switching (ZVS) is one of the possible solutions for operation at higher frequencies in order to increase the converter power density. In a full bridge topology, ZVS can be achieved by use of the parasitic intrinsic MOSFET body diode, which reduces the switching losses, and heat sink requirements. The two legs of the bridge are operated with a phase shift, which allows zero voltage turn on of the MOSFETs by use of the energy stored in the transformer leakage inductance to discharge the output capacitance of the MOSFETs before turning them on.

Recently, power MOSFET failures have been reported in the ZVS FB DC-DC converter topology (2,3). This paper presents the results obtained from a study conducted to evaluate the various electrical stresses applied to a power MOSFET in a 350V - 3.5V, 225A FB ZVS DC-DC converter. For the converter under study MOSFETs were found to fail under no-load converter operation. Normal operation of the FB ZVS DC-DC converter creates conditions that cause forward and reverse recovery of the MOSFET body diode. Body diode recovery introduces an additional stress on the MOSFET. The intrinsic body diodes of similar rated (500V-20A) MOSFETs from

different manufacturers were tested for forward recovery and reverse recovery performance. It is observed that the peak reverse recovery current of these diodes is much greater than that of the conventional diodes for the same operating conditions. Lifetime control is used in power diodes to improve the switching performance, while no such attempt is made in case of commercial power MOSFETs.

SIMULATION AND MODELING

A simulation infrastructure for optimal system design is shown in Fig. 1a. Knowledge of internal charge dynamics in the device is very important for analyzing the device performance under stress conditions. An advanced finite element numerical simulator can be used to study the electrical characteristics of the device. The device is represented by a two-dimensional (2-D) mesh structure and semiconductor device equations are solved at each node in the mesh to present an accurate picture of the internal carrier dynamics during switching and conduction. The effects of the 3-D geometry on the device electrical characteristics can be investigated by use of 3-D simulators. Circuit simulators, which are normally used for power electronic circuits use compact circuit models of active devices. It is difficult to develop an accurate model for power semiconductor devices because of their complex structures. Also these models differ significantly from the small-signal models. Therefore circuit models based on physical behavior are developed after performing 2-D process and device simulation. Lumped circuit models can be used to interface between device and circuit simulators, which is inaccurate. The solution is to perform 2-D mixed device and circuit simulation and solve the internal semiconductor equations under boundary conditions imposed by external circuit elements. Parasitic effects can also be incorporated into these simulations. By solving the heat generation and diffusion equations simultaneously with semiconductor equations, the heating effects can be modeled. An optimum device can be developed for a specific application by tradeoff between process, device and circuit performance and reliability parameters. This process is very slow because of complex mixed-mode simulations. Circuits with few components can be modeled and the actual circuit must be reduced to a behavioral circuit that produces similar device stresses.

In order to study the performance of a commercial power MOSFET, the structure shown in Fig. 1b, was used in the simulator, which solves the basic semiconductor equations consistently throughout the device. In order to

obtain the results in a realistic amount of time, a mesh is defined comprising of nodes. The coupled semiconductor equations, such as Poisson's equation, the continuity equations for electrons, and holes, and the current density equations are solved at each grid point for basic quantities such as electric field, electrostatic potential, carrier concentrations, and drift and diffusion currents. In order to obtain performance characteristics, a set of external conditions in the form of voltages or currents applied to device contacts are specified, which are used as boundary conditions to solve the device equations. For a given set of external stimuli, the simulator calculates a solution through an iteration scheme in which the coupled set of equations are solved iteratively until a solution is reached. The mesh design is critical, and therefore must be well conditioned so that it should be dense in the regions where electrical quantities such as electric field and potential have steep gradients, and sparse in the regions where quantities remain relatively constant. The grid should also be dense in the channel region. The 2-D simulation results of power MOSFET performance under static conditions in Fig. 2 show a good match with the measured values.

CIRCUIT OPERATION

A FB ZVS DC-DC converter, which uses circuit parasitics to achieve resonant switching is shown in Fig. 3a (4). Various electrical stresses are applied to the MOSFET during a switching cycle. The two legs of the converter are operated with a phase-shift, which causes a resonant discharge of the output capacitance of the MOSFETs by utilizing the energy stored in the transformer leakage inductance (L_{lk}) and determines the converter duty cycle. Larger leakage inductance increases the load range at which the converter operates with ZVS but decreases the effective duty cycle at the secondary of the transformer. Energy transfer occurs during active states, when diagonally opposite MOSFETs conduct for example M_1 and M_4 . For approximately half of the switching period M_3 and M_2 will be under a forward blocking voltage stress with the input voltage applied across the drain-source, with gate-source shorted. When M_4 is turned off, the energy stored in the output inductors charges the output capacitance of M_4 and discharges the output capacitance of M_3 , which causes the anti-parallel body diode of M_3 to conduct. A passive state begins and no energy is transferred to the load. M_3 can now be turned on under zero voltage.

FORWARD RECOVERY STRESS

When the body diode of M_3 starts to conduct its forward voltage rises to peak forward recovery voltage, which is higher than the final steady state voltage drop. The excess charge in the drift region requires time to build up to its final value and before this time period the resistance of the diode is very high. High level injection increases the conductivity of the lightly doped drift region of the body diode and greatly enhances the current handling capability (5). To determine the static forward voltage drop the transition from low level injection to high level injection is taken into account. During the period in which the excess carrier distribution grows in the drift region, there is no conductivity modulation of the drift region until the space charge is discharged to its thermal equilibrium value. Therefore there is a voltage overshoot before the drift region becomes shorted by the large amount of carrier injection. The duration of the space charge layer discharge and the growth of the excess-carrier distribution in the drift region is governed by both the intrinsic properties of the body diode and the external circuit in which the MOSFET is used. A large value of di/dt minimizes the time needed to discharge the space charge layer. On the other hand a large value of forward current and of carrier lifetime in the drift region will lengthen the time needed for the excess-carrier portion of the transient to be completed. This establishes an inherent trade-off between shorter turn-on transient and higher on-state losses. During the forward recovery time t_{fr} , the power dissipation in the body diode is much higher than predicted from its static characteristics, which is an additional stress on the MOSFETs to be used in the converter. As is shown in Fig. 3b after the diode forward recovers and a steady state voltage of V_F is reached across the device, M_3 is turned on under ZVS and the current is shared between the channel and body diode. When M_1 is turned off similar situation happens for M_2 and its body diode goes under forward recovery and M_2 is turned on under ZVS. This causes the current to decrease and change direction and after reverse recovery of the body diodes of M_2 and M_3 another active state continues to transfer energy to the transformer secondary.

Similar rated devices (500V-20A) from different manufacturers were tested in the forward recovery test circuit of Fig. 4a, where M_3 is the device under test. By turning on M_4 current ramps up in the inductor in parallel with M_3 . By adjusting the duration of the gate pulse the forward current was adjusted for five different values and three different di/dt values were chosen as shown in Fig. 4b. The measurements were performed at four different temperatures. Test results which indicate the variation of forward recovery energy loss as a function of temperature for similarly rated MOSFETs (A-E) and IGBT(V) are

shown in Fig. 4c. The results show that IGBT with its anti-parallel diode, which is optimized for reverse recovery shows the worst performance under forward recovery.

Rigorous 2-D device simulations were performed to understand the internal plasma dynamics during transient switching conditions. The MOSFET structure obtained from simulation of device performance under static conditions as is shown in Fig. 5a, was used in a 2-D mixed device and circuit simulator, in which semiconductor equations are solved within the device under boundary conditions imposed by external circuit elements (6). Three similar structures were used in order to study the dynamics of the device under forward recovery in FB ZVS DC-DC converter. The finite element simulation results are shown in Fig. 6 c, d, and e at three different time instants indicated in Fig. 3b. Current flow through the channel and body diode of MOSFETs M_3 and M_4 are shown at t_1 , which corresponds to the beginning of the forward recovery. Instant t_2 is during the conduction of the body diode and t_3 is when the MOSFET is also conducting the reverse current in its third quadrant of operation. Figure 5b shows the 2-D simulation results of the current through MOSFETs M_3 and M_4 and the drain-source voltage of M_3 during forward recovery of its body diode, by considering the effect of parasitic drain and source lead inductances.

REVERSE RECOVERY STRESS

Under normal operating conditions during a passive to active transition reverse recovery of the body diode occurs, when the drain-source voltage is low due to conduction of the channel. Therefore the reverse recovery energy loss is significantly reduced, and therefore this is not a stressful reverse recovery. Under no-load condition the phase shifted full bridge topology has to operate with extremely short active intervals (7). For very narrow pulses the normal current-mode control can not be maintained and is replaced by the duty-ratio mode control. This means that the current symmetry in the transformer primary is no longer ensured and some dc current component may build up. This current can be caused by unsymmetry in duration of positive and negative voltage pulses across primary, which is a result of unequal delays in the driving signals. A net dc voltage attempts to appear across the primary winding, which causes a unidirectional current.

Similar rated devices (500V-20A) from different manufacturers were tested in the reverse recovery test circuit of Fig. 6a, where M_1 is the device under test. By

turning on M_2 current ramps up in the inductor in parallel with M_1 . By adjusting the duration of the gate pulse the forward current was adjusted for two different values as shown in Fig. 6b. The measurements were performed at four different temperatures. Test results, which indicate the variation of peak reverse recovery current and reverse recovery energy of various devices as a function of forward current, are shown in Fig. 7a, and 7b at 60°C. The results show that IGBT (device V) with its anti-parallel diode, which is optimized for reverse recovery shows the best performance under reverse recovery. MOSFET B failed under this testing condition as is shown in Fig. 6c.

The MOSFET structure obtained from simulation of device performance under static conditions was used in the 2-D mixed device and circuit simulator. Two similar structures were used in the reverse recovery test circuit of Fig. 7a. A good match was obtained between the measured and simulated results as is shown in Fig. 7c.

FB ZVS DC-DC CONVERTER TEST CIRCUIT

In order to study the MOSFET switching performance in FB ZVS DC-DC converter, the test circuit of Fig. 8a was designed. Circuit operation can be described by use of the gating signals and waveforms in Fig. 8b, and c. When M_3 is turned on during interval I, the L_{lk} inductor current increases linearly through M_3 and the body diode of M_{aux} to a final maximum value determined by the pulse width of M_3 gate signal and the upper half of the input voltage source. Period II begins when M_3 is turned off, during which the energy stored in L_{lk} discharges the output capacitance of M_4 and charges the output capacitance of M_3 . As a result M_3 is turned off under hard switching and the body diode of M_4 starts conducting when its output capacitance is completely discharged. The inductor current freewheels through the body diode of M_{aux} and M_3 and the lower half of the input voltage source. When M_4 and M_{aux} are turned on during period III, their channel conducts the inductor current in the negative direction. The inductor current increases linearly to a final value determined by the pulse width of M_{aux} gate signal and the lower half of the input voltage source. Therefore M_4 is turned on under ZVS. When M_{aux} is turned off, the inductor current freewheels through M_4 and diode D_2 . Figure 9 shows the 2-D simulation results of FB ZVS DC-DC converter test circuit. The simulated and measured turn-off and on-state performance are compared in Fig. 9a, and b.

CONCLUSION

This paper presents various electrical stresses in FB ZVS DC-DC converters with a detailed study of the MOSFET body diode recovery stress under normal and low load operating conditions. Experimental results show the variation of forward recovery energy loss, peak reverse recovery current, and reverse recovery energy loss at different current levels and temperatures. The duration of the forward recovery, reverse recovery, the peak forward recovery voltage, and the peak reverse recovery current is governed by both the intrinsic properties of the body diode and the external circuit in which the MOSFET is used. The next generation of power MOSFETs have to be designed and optimized at the application level, which involves identification of tradeoffs among critical circuit and device performance and reliability parameters. Simulation techniques significantly reduce the development time, while allowing a wider range of parameter variation. Two-dimensional finite element simulation results showed the dynamics of the device under forward recovery, and reverse recovery in the FB ZVS DC-DC converter. The experimental results are supported by detailed two-dimensional numerical simulation results. A test circuit is designed to study the MOSFET switching performance in FB ZVS DC-DC converter. The simulated and measured turn-off and on-state performance is compared in this circuit.

REFERENCES

1. S. Abedinpour, and K. Shenai, "Power Electronics Technologies for the New Millennium," in *Proc. IEEE Int. Caracas Conf. Devices, Circuits, and systems (ICCDCS)*, 2000, pp. P 111-1, P 111-9.
2. L. Sao, R. Redl, K. Dierberger, "High-voltage MOSFET behavior in soft-switching converter: analysis and reliability improvements," in *Proc. IEEE Int. Telecommunications Energy Conf. (INTELEC)*, 1998, pp. 30-40.
3. H. Aigner, K. Dierberger, and D. Grafham, "Improving the full-bridge phase-shift ZVT converter for failure-free operation under extreme conditions in welding and similar applications," in *Proc. IEEE Industrial Applications Society Annual Meeting*, 1998, vol. 2, pp. 1341-1348.
4. J. A. Sabate et al., "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," in *Proc. IEEE Applied Power Electronics Conf. (APEC)*, 1990, pp. 275-284.
5. B. J. Baliga, *Power semiconductor devices*, PWS Co., 1996.

6. *Atlas users Manual*, Silvaco International, Santa Clara, CA.
7. A. Pietkiewiz, and D. Tolik, "Operation of high power soft-switched phase-shifted full-bridge dc-dc converter

under extreme conditions," in *Proc. IEEE Int. Telecommunications Energy Conf. (INTELEC)*, 1994, pp. 142-147.

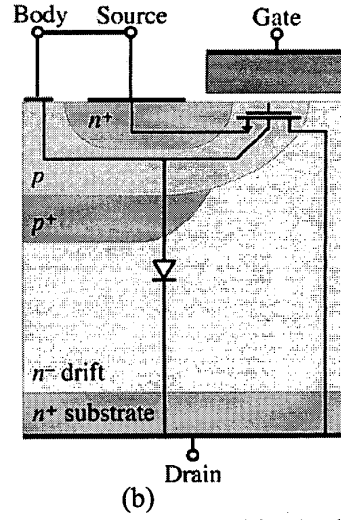
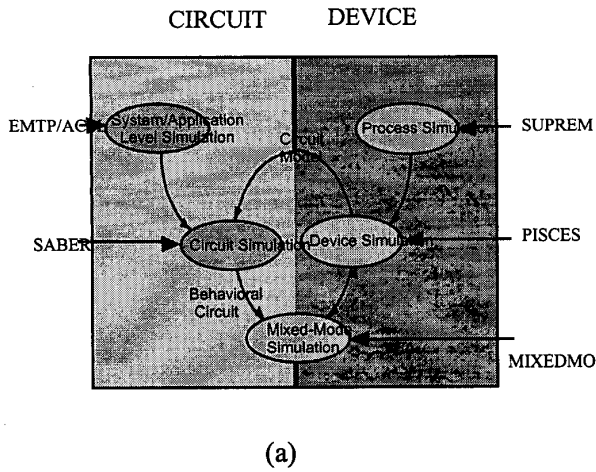


Fig. 1 (a) Framework for power system optimization, and (b) split-source MOSFET structure used for simulation.

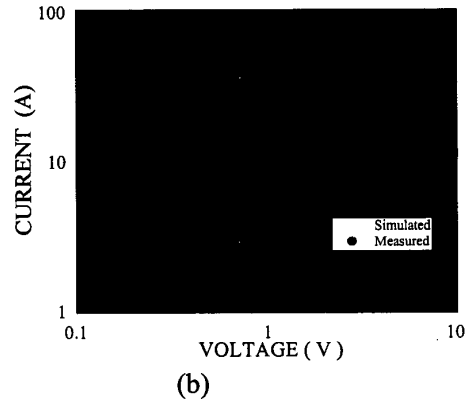
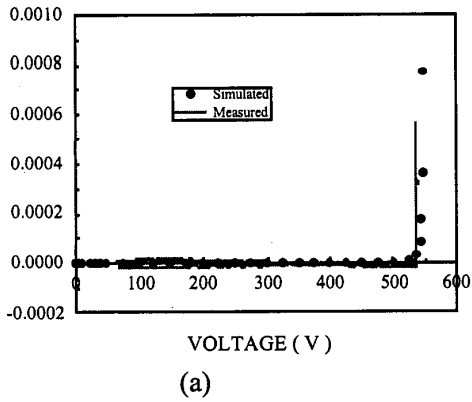


Fig. 2 2-D simulation results (a) breakdown performance, and (b) drain current vs. drain-source voltage.

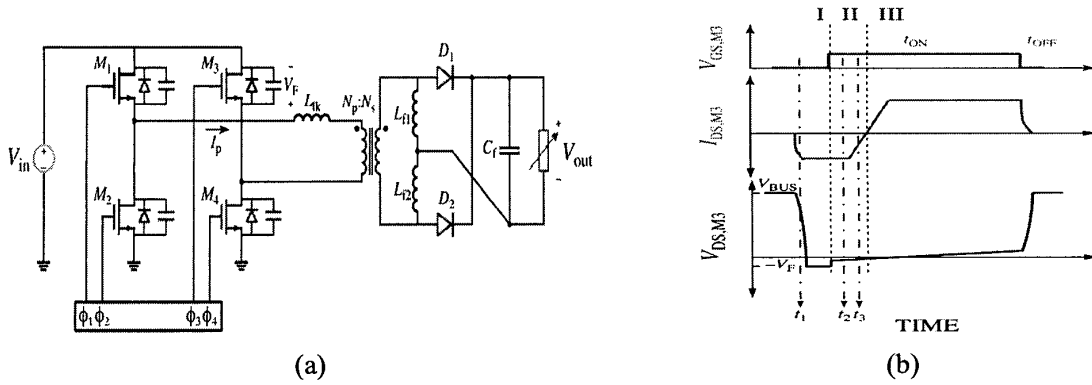


Fig. 3 Full bridge ZVS DC-DC converter (a) circuit, and (b) waveforms.

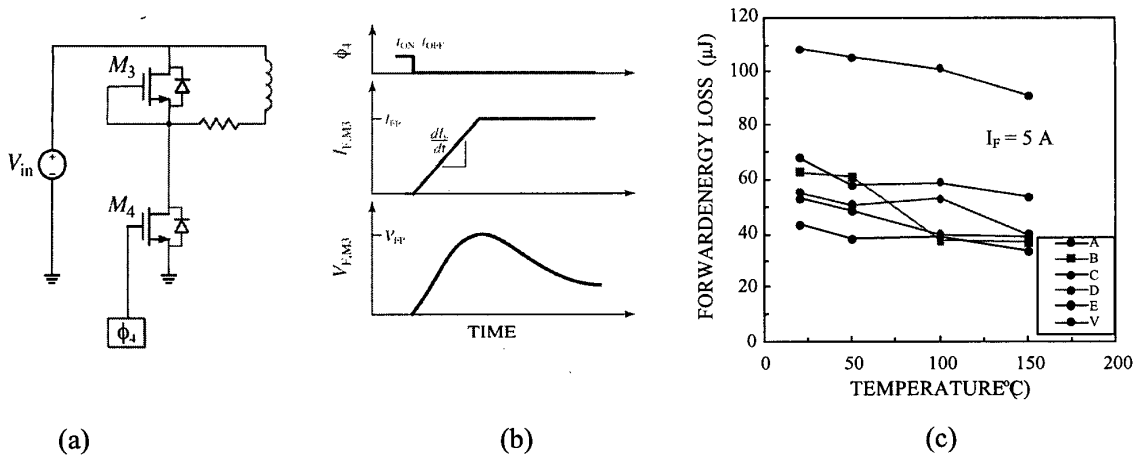


Fig. 4 Forward recovery test circuit, (b) measurement procedure, and (c) measurement results.

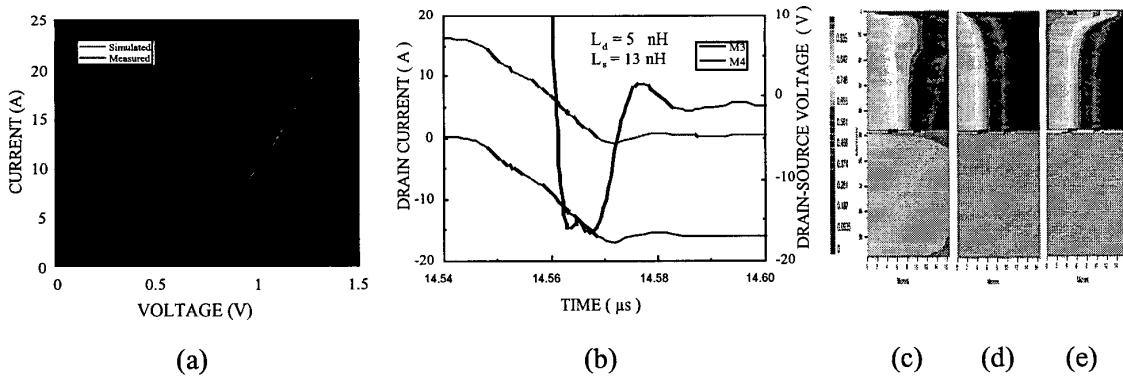


Fig. 5 2-D simulation results (a) body diode static iv, (b) forward recovery transition.(c)@ t_1 , (d) @ t_2 , and (e)@ t_3 .

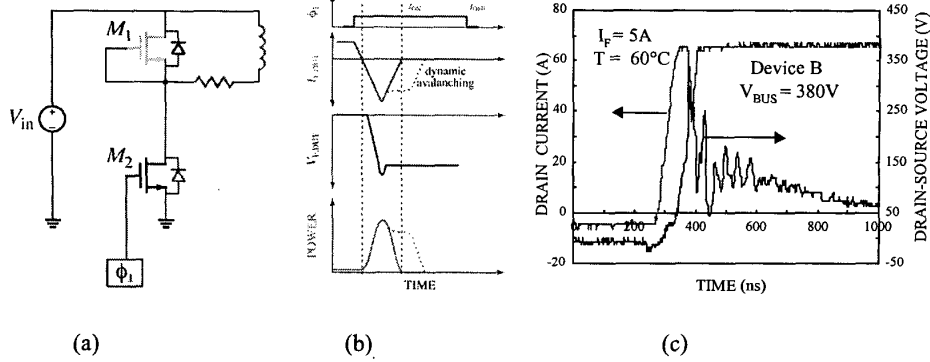


Fig. 6 Reverse recovery (a) test circuit, (b) waveform, and (c) device failure.

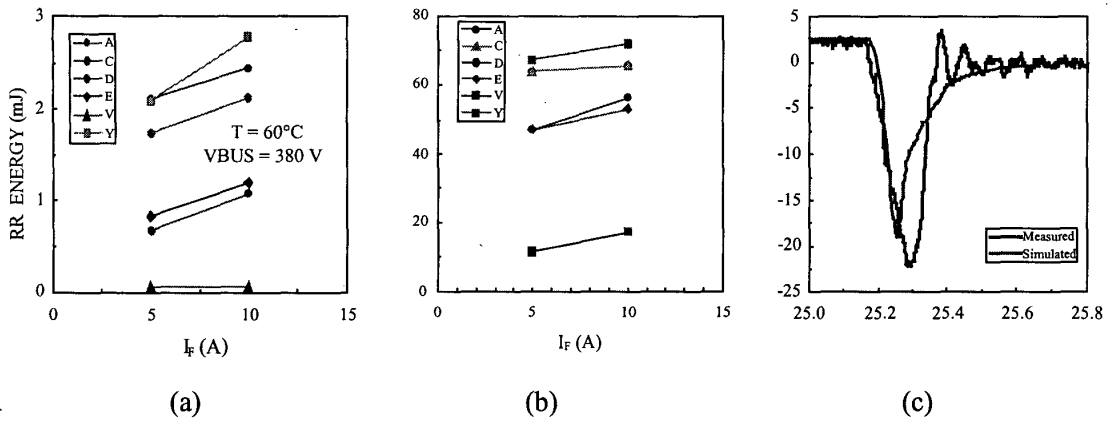


Fig. 7(a) Variation of peak reverse recovery (RR) current, (b) RR energy loss vs. forward current for similarly rated MOSFETs (A-E) and IGBT (V), and (c) measurement and 2-D simulation results for MOSFET A.

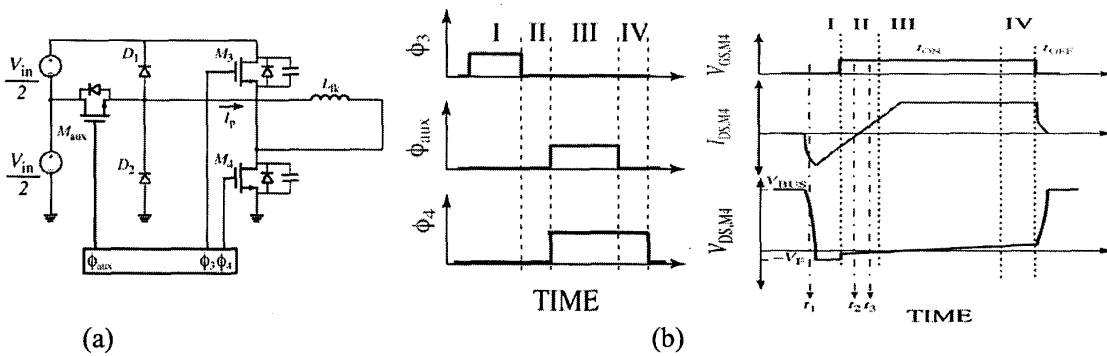


Fig. 8 FB ZVS DC-DC converter (a) test circuit, and (b) waveforms.

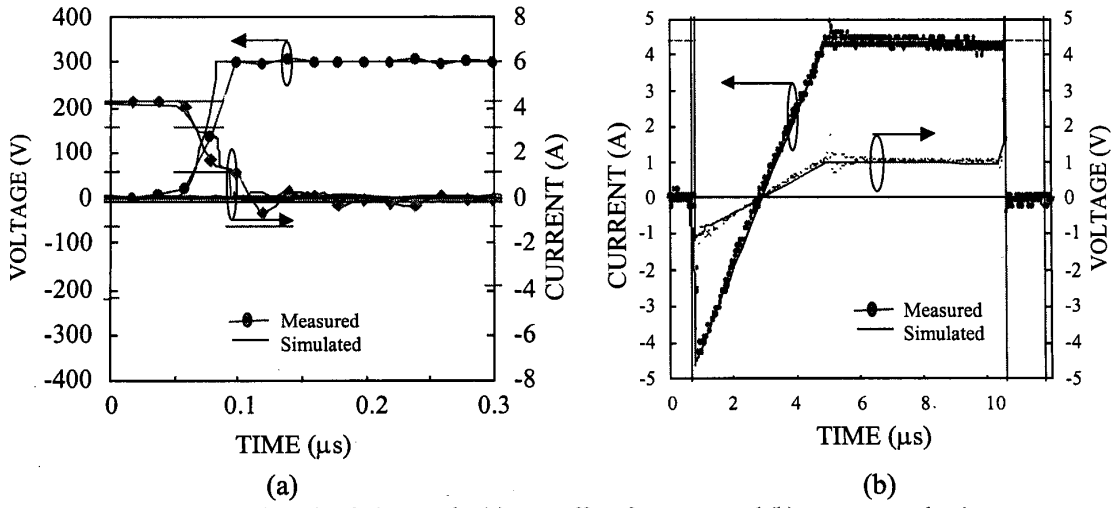


Fig. 9 2-D simulation results (a) turn-off performance, and (b) on-state conduction.