The Zero-Voltage-Switching Parallel-Resonant DC Link (PRDCL) Inverter with Minimized Conduction Loss

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Abstract—**This paper presents a Parallel-Resonant DC Link (PRDCL) circuit for soft switching main power devices with a single auxiliary power device for low conduction loss in single or three-phase inverter and converter applications. The proposed resonant network with one auxiliary power device is activated whenever it is needed to change the status of power devices connected to a DC link. The proposed resonant network is designed to force the DC link voltage to drop to zero before any power devices in the DC link are turned on. The auxiliary switch in the proposed resonant network is also turned on in a Zero-Voltage-Switching (ZVS) condition. Therefore, the switching losses caused in all power devices in a full-bridge converter and resonant circuit can be effectively eliminated. In addition, there is no conduction loss in the auxiliary power device because the resonant circuit is not activated if there is no status change in the power devices connected in the DC link. Furthermore, the resonant swing voltage in the DC link is well restricted within a predefined voltage level so that the required voltage rating of all power devices in the DC link is nicely constrained. The detailed modes of operation and experimental results are provided to verify the operation.**

1. INTRODUCTION

There is a growing interest in using a resonant DC link (RDCL) inverter for soft-switching technique to eliminate the switching losses caused in all power devices across a DC link. The basic concept of RDCL inverter is that a resonant tank or circuit in a DC link is used to make the DC link voltage zero and keep it at zero for a short switching transition time whenever power devices across the DC link need to have their status changed.

A simple method of a resonant DC link inverter based on this basic concept is to use a free resonant circuit in the DC link by using passive components, L and C [3-5]. However, the major problem with an RDCL inverter is the high voltage stress on the power devices because the voltage swing by natural resonance can be two or three times higher than the supplied DC voltage, V_{dc}.

To clamp this resonant voltage swing, an actively clamped resonant DC link (ACRDCL) inverter [1-2] was proposed. Since only one power device is used, the ACRDCL inverter is interesting to many high efficiency power conversions. Based on an ACRDCL inverter, the trials are being conducted Pulse-Width-Modulation (PWM). Specifically the Synchronized Resonant DC Link (SRDCL) inverter [6] makes it possible to realize the continuous variation of the resonant output pulse width by controlling the turn ON time of S7 in Fig. 2 [6]. However, a resonant current must flow S7 to extend output pulse width as shown in Fig. 2 [6]. This is not desirable for a high efficiency PWM operation.

Another method for a PWM operation based on an ACRDCL inverter is to change the switch status to provide a current path to the three-phase output at [7]. The DC link voltage waveform does not change the basic operation of conventional ACRDCL inverter, but the three-phase output voltage waveform can be Pulse-Width-Modulated.

However, the peak DC link voltage of an ACRDCL inverter is larger than Vdc and increase greatly when the resonant inductor current abruptly decreases as shown in the experimental results in Fig. 6 [19] and Fig. 3(a) [20]. To clamp this DC link voltage, the two types of Source Voltage Clamped Resonant Link (SVCRL) inverters employ just one power device as proposed in [19-20]. By using SVCRL inverters, the PWM or Pulse-Density-Modulation (PDM) is implemented as described in the paper.

There are other approaches soft switching the power devices in the DC link [8-9]. The proposed methods are useful for making a commutation of power devices by every one resonant cycle. Therefore, it is very useful in a SCR inverter to eliminate a commutation circuit in each SCR leg. A sort of PDM technique [8] is proposed based on controlling the number of each resonant pulse depending on load current. Nevertheless, it is difficult to have a high resolution PWMed output. To have a high resolution of PWM output, a rest time control method of resonant cycle [10] is proposed. However, the method needs three power devices in a resonant DC link stage.

To make a resonance in DC link, a Transformer-assisted Quasi-Resonant DC Link (TQRDCL) inverter is proposed in [10-14]. The DC link voltage is well clamped by properly designing the inductor size of L_{r1} and L_{r2}. However, it needs at least three power devices to make a resonance in the DC link [10-11]. A method for eliminating four power devices based on a TQRDCL inverter by using three-phase double full bridge inverters is proposed in [13]. The four power devices in each three-phase full bridge converters are used for making a resonance in DC link as well as input and output conversion.

An improved version of TQRDCL is proposed by employing just two power devices in [14]. The proposed method does not require any voltage or current sensing devices to ensure resonant operation and is capable of PWM operation. New RDCL inverters without an assisting transformer are proposed in [15-16]. However, the numbers

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of two or three power devices are still required. It is not desirable in light of system cost.

To clamp the DC link voltage, a resonant DC link dual converter with a voltage clamp circuit is proposed [17]. The DC link voltage is freely resonated, but the DC link voltage around a peak is clamped by controlling the turn on or off time of the clamping switch. Although the clamp circuit part is the same as the proposed PRDCL inverter, the purpose of the clamp circuit is to clamp the DC link voltage only. The C_c and C_r consist of a resonant component with L_r. The clamping switch is controlled to make the clamping capacitor voltage V_{Cc} at *T3* equal to V_{Cc} at *T4*. Hence, it is needed to sense the C_c voltage. Furthermore, since the resonance depends on the passive component sizes with the load current, there is no way to make a PWM feature. The resonance is always fixed. To be a ZVS for power devices converter and inverter parts, sensing the DC link voltage is essential.

Other simple RDCL inverters that use only one power device are proposed in [18-20]. Nevertheless, the auxiliary power device is placed into a power current flowing line. Hence, there are always conduction losses in resonant mode as well as simple conduction mode.

To reduce conduction loss in a resonant DC link inverter, the auxiliary power device of the resonant network should not be placed into the power flowing line. This paper proposes a new parallel resonant DC link (PRDCL) circuit, which does not use an auxiliary power device in the power flowing line. Whenever it is necessary to turn off the main devices in the inverter leg, the PRDCL network with an auxiliary power device intervenes to make the DC line a zero voltage condition.

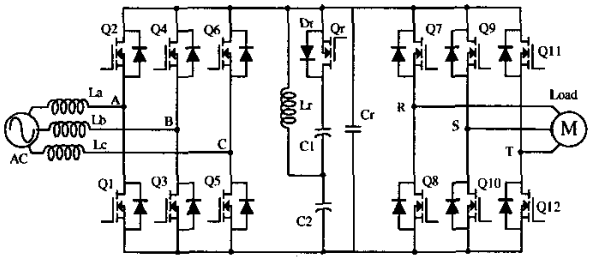


Fig. 1 Proposed resonant DC Link inverter.

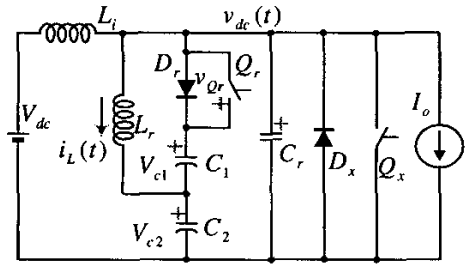
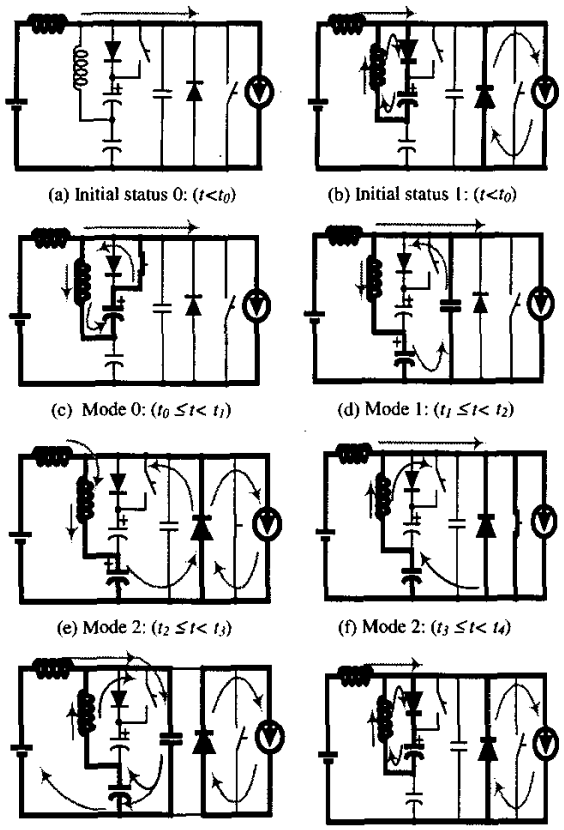


Fig. 2 Simplified equivalent circuit of proposed PRDCL inverter.



(a) Initial status 0: ($t<t_0$) (b) Initial status 1: ($t<t_0$)

(c) Mode 0: ($t_0 \le t< t_1$) (d) Mode 1: ($t_1 \le t< t_2$)

(e) Mode 2: ($t_2 \le t< t_3$) (f) Mode 2: ($t_3 \le t< t_4$)

(g) Mode 3: ($t_4 \le t< t_5$) (h) Mode 4: ($t_5 \le t< t_6$)

Fig. 3 Detailed operating modes of proposed RDCL inverter

2. PROPOSED PRDCL INVERTER

The proposed main PRDCL inverter is shown in Fig. 1 and can be considered as an equivalent circuit as shown in Fig. 2. The power devices in a full-bridge inverter and converter can be replaced by an equivalent switch Q_x. This implies that the short circuit state can be obtained by closing both the power devices of one or more positive and negative inverter or converter legs. The three input inductors, L_a, L_b, and L_c, with the input source voltage, v_{ac}, can be replaced by a rectified DC voltage source, V_{dc}, with one inductor, L_i, as shown in Fig. 2. The resonant capacitor, C_r, includes the drain to source output capacitors of all inverter and converter power devices.

Assume that Q_r and Q_x are ideal switches and there is no core saturation in resonant inductor. At ($t < t_0$) there are two initial conditions, Status 0 and Status 1, depending on a existing PWM time slot of T_7 as shown in Figs. 3(a), (b), and 4. Assume that the PRDCL inverter is operated from the initial status 0 as shown in Fig. 3(a) and Q_r is turned off.

If the switching period is defined as $T = t_7 - t_0$, and the turn on time of Q_x is defined as $Q_{x,ON}=T_4= t_4 - t_3$, then the C_1 and C_2 voltages can be considered as constant voltage sources. With these conditions, the DC link voltage $v_{dc}(t < t_0) =V_{dc}$, $V_{c1} =V_{dc}$, and $i_{Lr}(t < t_0) = 0$. The load current flows from

source to load side directly. Since there is no intervention by the resonant circuit consisting of Q_r, D_r, L_r, C_r, C_1, and C_2, there are no power losses caused by the resonant circuit. The resonant frequency of $f_r = 1/[2\pi\sqrt{(L_rC_r)}]$ is very fast, so the V_{c1} and V_{c2} across voltages of C_1 and C_2 can be considered as constant voltage sources in resonant mode. The operation can be divided into five modes of operation, based on the switching time of the power device and resonant cycle.

A. *Detailed Modes of Operation:*

Mode 0 ($t_0 \le t < t_1$): This mode starts when resonant switch Q_r is turned on at $t = t_0$ as shown in Fig. 4. The inductor current, $i_{Lr}(t)$, is now increased as (1) and flows through C_1, Q_r, and L_r as shown in Fig. 3(c). Since V_{c1} can be a constant voltage source during $T_2 = t_1 - t_0$, then the resonant inductor current is linearly increased. If Q_r is conducting, the DC link voltage can be written as the following:

$$i_{Lr}(t) = \frac{V_{c1}}{L_r}t\,, \tag{1}$$

$$I_1 \equiv i_{Lr}(t_1) = \frac{V_{c1}}{L_r}(t_1 - t_0), \tag{2}$$

$$v_{Qx}(t_0 \sim t_1) = V_{c1} + V_{c2}\,. \tag{3}$$

This mode is finished when Q_r is turned off at $t = t_0$.

Mode 1 ($t_1 \le t < t_2$): If Q_r is turned off at $t = t_1$, a resonant cycle is now initiated by L_r and C_r. The DC link voltage, $v_{dc}(t)$, or $v_{Qx}(t)$ is decreased with a resonant fashion. This resonant time, T_2, can be calculated with the initial inductor current value of $i_{Lr}(t_1) = I_1$ as:

$$v_{dc}(t) = v_{Qx}(t) = (V_{c1} + V_{c2})\cos\omega_r(t - t_1)\,, \tag{4}$$

$$T_2 \equiv t_2 - t_1 = \frac{\pi}{2}\sqrt{L_rC_r}\,, \tag{5}$$

where $\omega_r = 2\pi\sqrt{(L_rC_r)}$ is a resonant frequency. If $v_{Qx}(t)$ becomes zero, $v_{Qr}(t) = V_{c1} + V_{c2}$. The inductor current is still in the positive direction. This mode is finished when the DC link voltage $v_{Qx}(t)$ drops to zero at $t = t_2$ as shown in Fig. 3(d).

Mode 2 ($t_2 \le t < t_4$): Since the inductor current is still positive, the anti-parallel diode, D_x, will be conducted as shown in Fig. 3(e). Note that Q_x should be turned on with the zero-voltage-switching (ZVS) condition when D_x is conducted by the positive resonant inductor current. Otherwise, the resonant inductor will begin to recharge C_r and Q_x will not be able to be switched under a ZVS condition. As shown in Fig. 3(f), if Q_x is already turned on during ($t_2 \le t < t_3$), the inductor current $i_{Lr}(t)$ becomes negative polarity and decreases linearly by the voltage, V_{c2} as shown in Fig. 3(f). This mode is finished if Q_x is turned off at $t = t_4$. The Q_x current can be written as

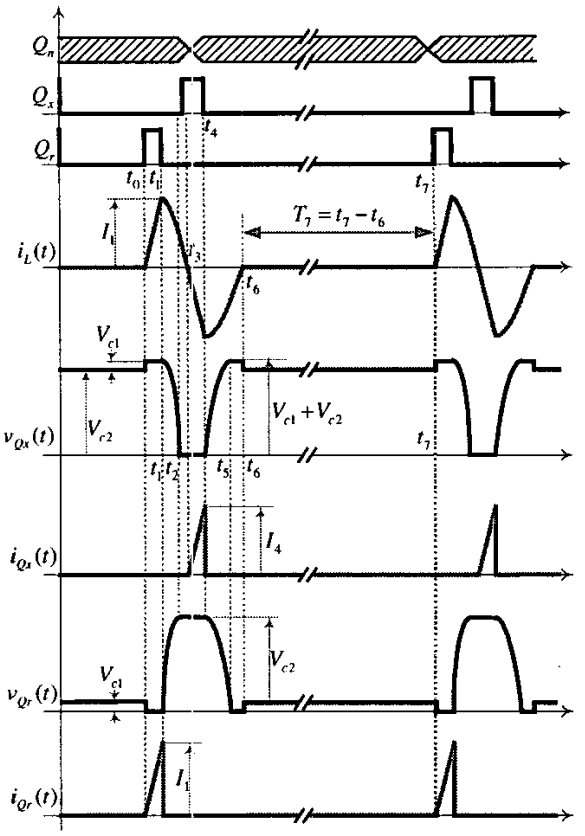


Fig. 4 Key operating waveforms of proposed PRDCL inverter.

$$i_{Qx}(t) = \frac{V_{c2}}{L_r}(t - t_3), \tag{6}$$

$$I_4 \equiv i_{Qx}(t_4) = \frac{V_{c2}}{L_r}(t_4 - t_3)\,. \tag{7}$$

Mode 3 ($t_4 \le t < t_5$): Since the current polarity, $i_{Lr}(t)$ is negative and Q_x is already turned off, the DC link voltage, $v_{Qx}(t)$, is now increased due to the resonance between L_r and C_r, as shown in Fig. 3(g). If $v_{Qx}(t)$ reaches $(V_{c1} + V_{c2})$ at $t = t_2$, this mode is finished.

$$v_{Qx}(t) = (V_{c1} + V_{c2})\sin\omega_r(t - t_4)\,.$$

Mode 4 ($t_5 \le t < t_6$): This mode starts with the turned-off condition of both Q_r and Q_x. The extra resonant inductor current flows through L_r, D_r, and C_1 as shown in Fig. 3(h). If Q_r is turned on after $i_L(t)$ is decreased to zero at $t = t_6$, there will be a time slot of T_7 as shown in Fig. 5 and Status 0 in Fig. 3(a). Otherwise if Q_r is turned on while $i_L(t)$ flows into D_r, then a new switching cycle is started from Status 1 as shown in Fig. 3(b).

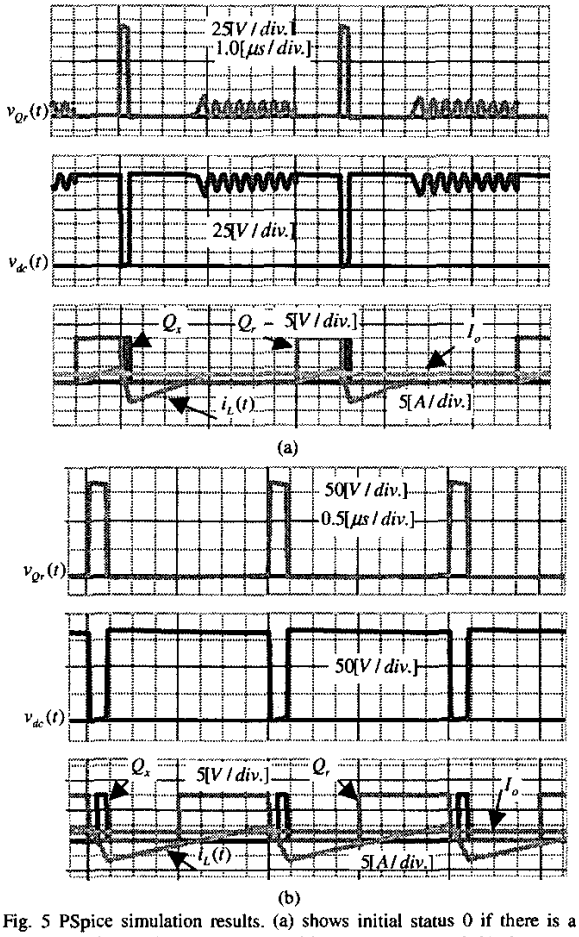


Fig. 5 PSpice simulation results. (a) shows initial status 0 if there is a discontinuous inductor current with T = 10.0 [us] and (b) shows no initial status 0 with T = 4.0 [us].

B. *Simulation and Experimental Results.*

The PSpice simulation is carried out with the parameters of L_r=20 [uH], $C_1 = C_2$ = 1.0 [uF], V_{dc} = 150 [V], $Q_{x,ON}$ = 0.3 [us], $Q_{r,ON}$ = 2 [us], and the output capacitance of C_{oss} = 150[pF] for MOSFET IRF840B from Fairchild Semiconductor. If the switching cycle T = 10[us], then there is the initial status 0 as shown in Figs. 3(a) and 5(a). If T=4.0 [us], then the inductor current is continuous and there is no initial status 0 as shown in Fig. 3(a). As can be seen in Fig. 5(a), Q_x is turned on after the DC link voltage $v_{dc}(t)$ becomes zero. From the simulation results, the Q_r switch is switched on with a quasi-ZVS switching condition. It means that Q_r is turned on when the drain to source voltage of Q_r still exists as V_{c1} as shown in Fig. 5(a). However, the voltage of V_{c1} is very small, here V_{c1} = 20V, compared with V_{c2} = 150[V]. Hence, the switching losses caused by the quasi-ZVS condition are very small. To have a complete ZVS for both Q_r and Q_x, the inductor current must be continuous.

The practical experiments are carried out using FMS7401, a dedicated microcontroller for a power control application, developed by Fairchild Semiconductor. The main block consists of 1 [Kbytes] EEPROM with six channel A/D converters including an internal oscillator. It can control 8-bit resolution PWM output with 250[KHz] switching frequency.

For a fast output transient response of the power system, the inner current-control-loop can be implemented by using internal analog comparator with current sensing OP amplifier. There is current sensing amplifier having a gain of 16 provided a digital leading edge blanking circuit. An outer voltage control loop can be realized by using an adjustable voltage reference in software digitally.

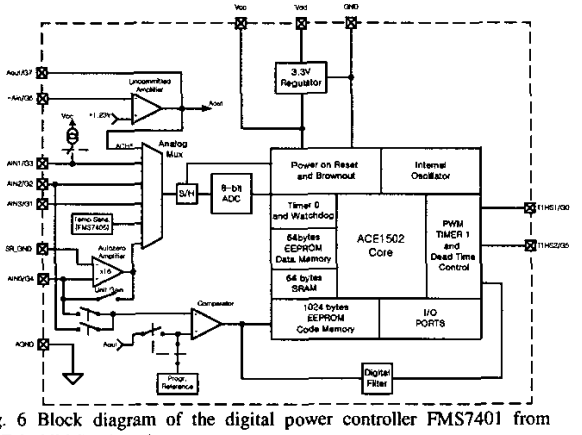


Fig. 6 Block diagram of the digital power controller FMS7401 from Fairchild Semiconductor.

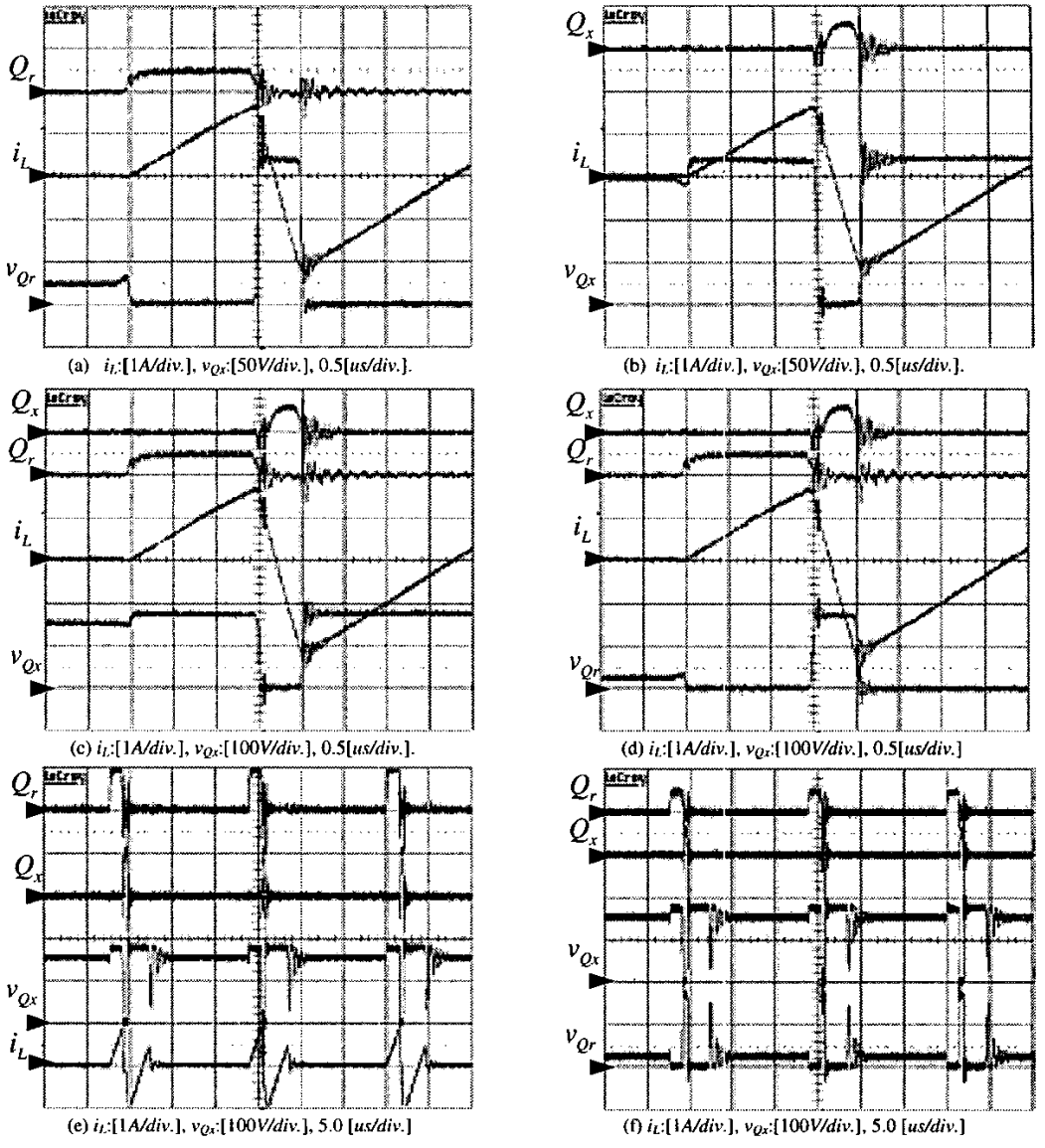
The power device turning times are set to $Q_{x,ON}$ = 0.3 [us], $Q_{r,ON}$ = 1.5 [us], and the dead-time between Qx and Q_r is set to 0.2[us] by adjusting two-PWM control registers and the internal dead time control register in FMS7401. The switching cycle is set to T=16 [us].

Table 1: PRDCL inverter parameters.

L_r	20 [uH]
L_i , L_o	1.4 [mH]
C_1, C_2	1.0 [uF], 250 [V]
Q_r, Q_x	FQAF13N50 (500[V] 9.6[A])
V_{dc}	150[V]

High and low side gate drives are used for driving N-channel MOSFETs such as FQAF13N50 from Fairchild Semiconductor, which has a typical output capacitance of C_{oss} = 245 [pF]. Hence, resonance cycle time T_2 based on the parameters in Table1 can be calculated by using (5) as T_2 = 0.11 [us]. First, Q_r is turned on during $T_1 = t_1 - t_0$ and then turned off. Then, mode 1 is initiated as shown in Fig. 3(d) for T_2. After T_2, the DC link voltage becomes zero. Hence, the Q_x can be switched on with ZVS condition.

Fig. 7(a) shows that Q_r is turned on while the v_{Qr} voltage is not completely at a zero condition. This is a quasi-resonant mode if there is an initial status 0 as described in Fig. 3(a). Nevertheless, the switching losses would be almost zero because the inductor current starts from zero with a slope.



(a) i_L:[1A/div.], v_{Qx}:[50V/div.], 0.5[us/div.].
(b) i_L:[1A/div.], v_{Qx}:[50V/div.], 0.5[us/div.].
(c) i_L:[1A/div.], v_{Qx}:[100V/div.], 0.5[us/div.].
(d) i_L:[1A/div.], v_{Qx}:[100V/div.], 0.5[us/div.]
(e) i_L:[1A/div.], v_{Qx}:[100V/div.], 5.0 [us/div.]
(f) i_L:[1A/div.], v_{Qx}:[100V/div.], 5.0 [us/div.]

Fig. 7 Experimental results of proposed PRDCL inverter.

Fig. 7(b) shows that the drain voltage of Q_x, v_{Qx} is zero before turning on gate signal is applied to Q_x. Hence Q_x is switched on without switching losses. As can be expected from the calculation of resonant time in (5), the experiment result of T_2 time can be identified by the time from high level to ground of v_{Qx} in Fig. 7(b). It is about 0.1[us] and well matched with the calculation value of 0.11[us].

From Fig.7 (a), the obtained C_1 and C_2 voltage levels, V_{c1} and V_{c2}, can be calculated as 20[V], 150[Vdc], respectively. It can be also found in Fig. 7(a).

The Q_x and Q_r timing relation are shown in Figs. 7(c) and 7(d). As can be seen, the $Q_{r,ON}$=1.5[us], $Q_{x,ON}$ =0.3[us], and the dead-time between Q_x and Q_r is about 0.2[us]. The Figs. 7(e) shows a discontinuous inductor current with the initial status 0. Fig. 7(f) shows experimental results of gate signals Q_x and Q_r with their drain voltages of v_{Qx} and v_{Qr}.

From the experimental results, the DC link voltage is well clamped within (V_{c1} + V_{c2}) because the DC link voltage exceeds the (V_{c1} + V_{c2}), then a current path through C_1 and C_2 is provided.

3. CONCLUSION

Inn this paper, new parallel resonant DC link inverter using one resonant switch is proposed to overcome the drawback of the efficiency degradation because a resonant power device is placed into a load current flowing path. All

switches are switched on under the ZVS condition when the switching cycle is initiated from the initial status 1. If the initial status 0 is employed in order to make PWM output, the load current flows directly from source to load side without any intervention by the resonant circuit in the initial status 0. Hence, there is no conduction loss caused by the load current. In the initial status 0, the resonant switch Q_r is switched on with non-zero voltage level, V_{c1}. It is quasi-resonant mode. Nevertheless, the switching losses can be very small because the inductor current or Q_r current starts from zero level.

If the initial status 0 is not employed for a PDM operation, then Q_x and Q_r are completely switched on under the ZVS condition. Experimental results are provided. It can be expected that the proposed PRDCL inverter is very useful for a high efficiency power converter.

REFERENCES

[1] D.M Divan and G. Skibinski, "Zero Switching–Loss Inverters for High Power Applications," *IEEE Proceeding of Industry Application Society pp. 627-634.* 1987.

[2] D.M. Divan, "Static Power Conversion Method and Apparatus Having Essentially Zero Switching Losses and Clamped Voltage Levels," *United States Patent, US4864483, Sep. 5,* 1989.

[3] S.K. Sul and T.A. Lipo, "Field Oriented Control of an Induction Machine in a High Frequency Link Power System," *IEEE-PESC Conf. Rec.*, pp. 1084–1090, 1988.

[4] D.M. Divan, "The Resonant DC Link Converter–A New Concept in Static Power Conversion," *IEEE Trans. on Industry Applications, Vol.25, No. 2, March, pp. 317–325,* 1989.

[5] S.K. Sul and T.M. Lipo, "Design and Performance of a High-Frequency Link Induction Motor Drive Operating at Unity Power Factor," *IEEE Trans. on.Industry Applications, Vol.26, No.3, May,* pp. 434–439, 1990.

[6] D.M. Divan, L. Malesani, P. Tenti, and V. Toigo, "A Synchronized Resonant DC Link Converter for Soft-Switched PWM," *IEEE Tran. On Industry Application, Vol.29, No.5, Sept.* pp. 940–948, 1993.

[7] G. Venkataramanan and D.M Divan, "Pulse Width Modulation with Resonant DC Link Converters," *IEEE Tran. On Industry Applications, Vol.29, No.1, Jan.* pp. 113–120, 1993.

[8] J.S. Lai and B.K Bose, "An Induction Motor Drive Using an Improved High Frequency Resonant DC Link Inverter," *IEEE Trans. on.Power Electronics, Vol.6, No.3, July,* pp. 504–513, 1989

[9] M.T. Aydemir, P.Caldeir, T.A. Lipo, E.R.C. da Silva, and G. Ledwich, "Utilization of a Series Resonant DC Link for a DC Motor Drive," IEEE Trans. On Industry Application Vol.29, No.5, Sept. pp. 949–958, 1993.

[10] H. Yonemori, K. Hayashi, and M. Nakaoka, "A Novel Space-Voltage Vector Modulation Modulated Sinewave Three-Phase Inverter with High-Frequency Transformer-Coupled Resonant DC Link," *IEEE-PESC Conf. Rec.*, pp. 651–658, 1994.

[11] K. Yurugi, H.Yonemori, K.Hayasi, and M.Nakaoka, "Next Generation Space Voltage Vector ZVT-PWM AC-DC Active Power Converter with Auxiliary Transformer-Assisted Resonant DC Link," *IEEE PESC Conf. Rec.* pp. 644–650, 1994.

[12] H. Yonemori, M. Yoshida, and M. Nakaoka, "Three-Phase ZVS-PWM Inverter System with Transformer-Assisted Quasi-Resonant DC Link and its Feasible Comparative Evaluations," *IEEE-PESC Conf. Rec.*, pp. 171–176, 1996.

[13] A. Julian, D.M. Divan, T.A. Lipo, F. Nozari, and P.A. Mezs, "Double Bridge Resonant DC Link Converter with Variable Input and Output Frequency," *IEEE Proc. of Applied Power Electronics Conf., APEC'96.* pp. 181–186, 1996.

[14] A.S. Ba-Thunya and H.A. Toliyat, "A New High Frequency Transformer Assisted ZVS Quasi-Resonant DC-Link PWM Inverter with Minimum Voltage Stress on the Switched," *IEEE PESC Conf. Rec.*, 1999.

[15] J.B. Bell, R.M. Nelms, and M.T. Shephered, "Design of a ZVS PWM Inverter for A Brushless DC Motor in an EMA Application," *IEEE Proc. of Applied Power Electronics Conf., APEC'95.* pp. 399–405, 1995.

[16] W. Yi, H.L. Lie, Y.C. Jung, J.G. Cho, and G.H, Cho, "Program-Controlled Soft Switching PRDCL Inverter with New Space Vector PWM Algorithm," *IEEE-PESC Conf. Rec.*, pp. 313–318, 1992.

[17] S. Kondo, S.H. Yang, S. Takizawa, and F. Harashima, "Resonant DC Link Dual Converter System for Motor Drives," *Proc. of IEEE IAS'91*, pp. 789-794, 1991.

[18] Y. Jang and R.W. Eriction, "Design and Experimental Results of a 6KW Single-Switch Three-Phase High Power Factor Rectifier Using Multi-Resonant Zero Current Switching," *Proc. of IEEE Applied Power Electronics Conf., APEC'96.* pp. 524–530, 1996.

[19] In-Hwan Oh, Y.S. Jung, and M.J. Youn, "A Source Voltage-Clamped Resonant Inverter for a PMSM Using a Predictive Current Control Technique," *IEEE Transaction on Power Electronics*, Vol.14, No.6, pp. 1122–1132, Nov. 1999.

[20] In-Hwan Oh, and M.J. Youn, "A Simple Soft-Switched PWM Inverter Using Source Voltage Clamped Resonant Circuit," *IEEE Transaction on Industrial Electronics*, Vol.46, No.2, pp. 468–471, April. 1999.

[21] T.S. Wu, M.D. Bellar, A. Tchamdjou, J. Mahdavi, and M. Ehsani, "A Review of Soft–Switched DC-AC Converters," *IEEE Proc. of Industry Application Society, IAS'96* , pp. 1133–1144, 1996.

[22] **FMS7401** Digital Power Controller (DPC) data sheet, Fairchild Semiconductor, http://www.fairchildsemi.com/ds/FM/FMS7401.pdf, 2004.