SG6848 **AN6848**

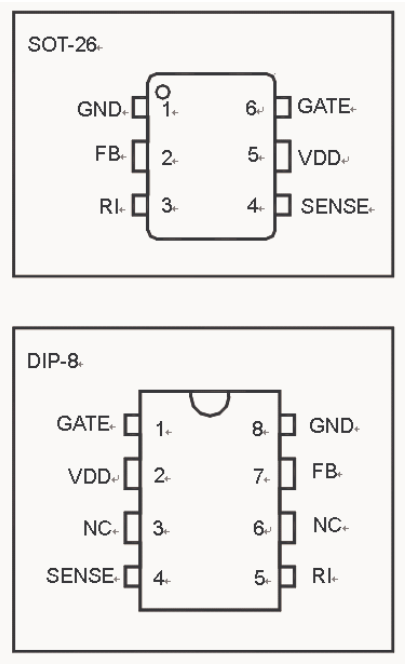
ABSTRACT

The present application note describes a detailed design strategy for a high efficiency, compact flyback converter. Design considerations and mathematical equations are presented. Finally, the guidelines for printed circuit board layout are also given.

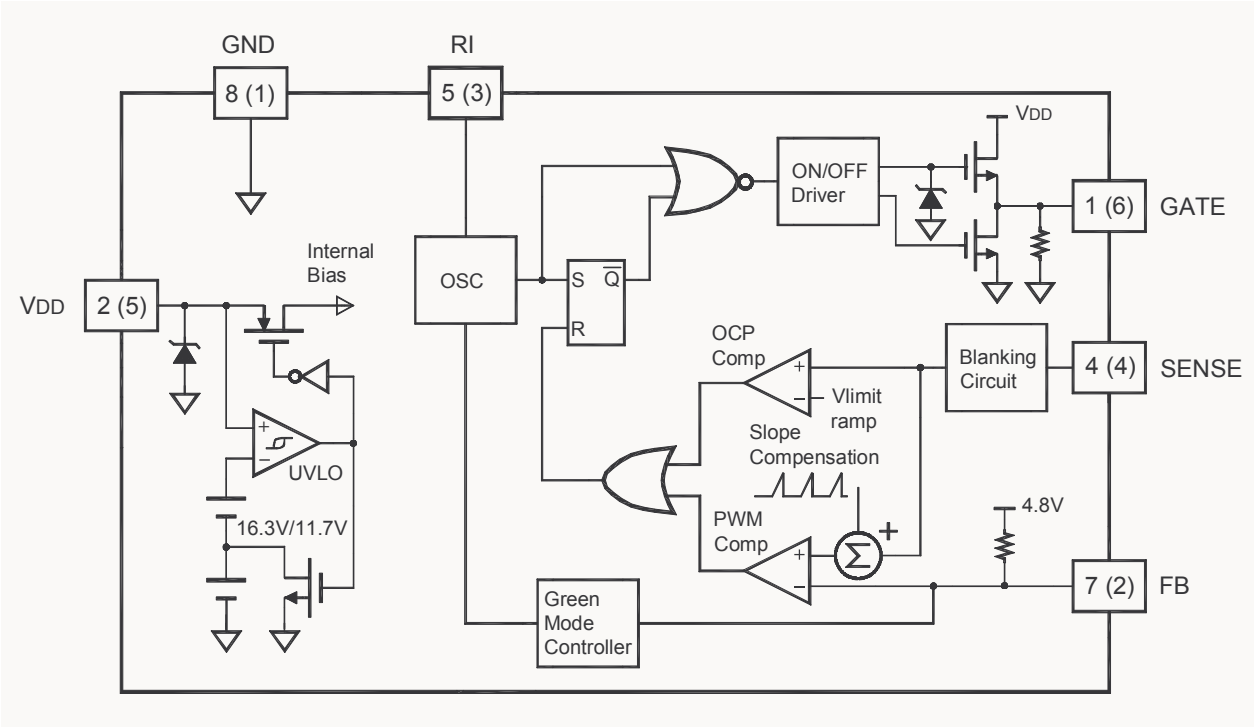
FEATURES

- Green-mode operation with linearly decreasing PWM frequency
- Low start up current, 5uA
- Low operation current, 2mA
- Leading-edge blanking
- Constant output power limiting for universal input
- Built-in synchronized slope compensation
- Current mode operation
- Cycle-by-cycle current limiting
- Under voltage lockout (UVLO)
- Programmable PWM frequency
- Clamped gate output voltage 17V
- Few external components
- SOT-26 and DIP-8 packages available

PIN CONFIGURATION



BLOCK DIAGRAM



DIP-8 pin assignment. Number in parenthesis is SOT-26 pin assignment.

Description

This highly integrated PWM controller provides several special enhancements designed to meet the low standby-power needs of low-power SMPS. To minimize standby power consumption, the proprietary green-mode function provides off-time modulation to linearly decrease the switching frequency under light-load conditions. This green-mode function enables the power supply to easily meet even the strictest power conservation requirements.

The BiCMOS fabrication process enables reducing the start-up current to 5uA, and the operating current to 2mA. To further improve power conservation, a large start-up resistance can be used. Built-in synchronized slope compensation ensures the stability of peak current mode control. Proprietary internal compensation provides a constant output power limit over a universal line input range (90Vac to 264Vac). Pulse-by-pulse current limiting ensures safe operation even during short-circuits.

To protect the external power MOSFET from being damaged by excessive supply voltage, the SG6848's output driver is clamped at 17V. SG6848 controllers can be used to improve the performance and reduce the production cost of power supplies. The SG6848 is the best choice for replacing linear and RCC-mode power adapters. It is available in 8-pin DIP and 6-pin SOT-26 packages.

Start-up Circuitry

When the power is turned on, the input rectified voltage, Vdc, charges the hold-up capacitor C1 via a start-up resistor R_{IN}. As the voltage of VDD pin reaches the start threshold voltage $V_{TH(ON)}$, SG6848 activates the entire power supply.

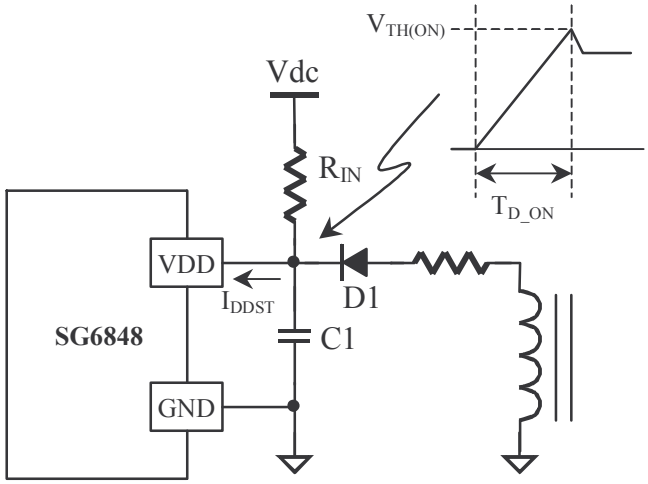


Figure 1. Circuit of providing power to SG6848

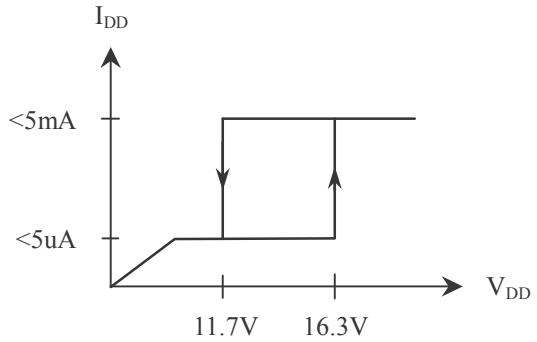


Figure 2. UVLO specification

The maximum power-on delay time is determined as follows,

$$V_{TH(ON)} = (V_{dc} - I_{DDST} \cdot R_{IN}) \left[1 - e^{-\frac{T_{D\_ON}}{R_{IN} \cdot C1}} \right] \qquad (1)$$

where

I_{DDST} is the start-up current of SG6848;

T_{D_ON} is the power-on delay time of the power supply.

Due to the low start-up current, a large R_{IN} such as 1.5Mohm can be used. Also with a hold-up capacitor of 10uF/50V, the power-on delay T_{D_ON} is less than 2.8S for 90Vac input.

The FB input

This pin is designed for feedback control and to activate the green-mode function. Figure 3 is a typical feedback circuit mainly consisting of a shunt regulator and an opto-coupler. R_1 and R2 form a voltage divider for the output voltage regulation. R3 and C1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB}= 47ohm, C_{FB}= 1nF) placed from the FB pin to GND can increase stability. The maximum source current on the FB pin is 2mA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. Thus, the value of the biasing resistor Rb is determined as follows,

$$\frac{V_o - V_D - V_Z}{Rb} \cdot K \geq 2mA \qquad (2)$$

where V_D is the drop voltage of a photodiode, about 1.2V;

V_Z is the minimum operating voltage of the shunt regulator. Typical value is 2.5V;

K is the current transfer rate (CTR) of the opto-coupler.
For an output voltage Vo=5V, with CTR=100%, the maximum value of Rb is 650ohm.

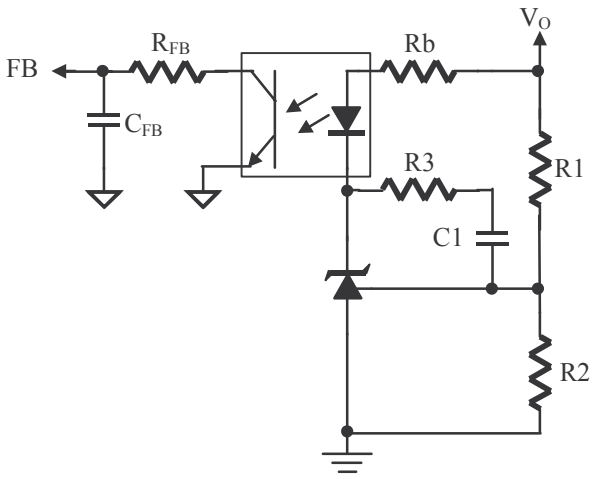


Figure 3. Feedback circuit.

Oscillator & Green Mode Operation

One external resistor, R_i, connected between RI and GND pins is used to program the PWM frequency of the SG6848. The approximated formula is:

$$F_{OSC}(KHz) = \frac{6650}{R_i(Kohm)} \qquad (3)$$

The recommended F_{OSC} is from 50 to 100KHz.

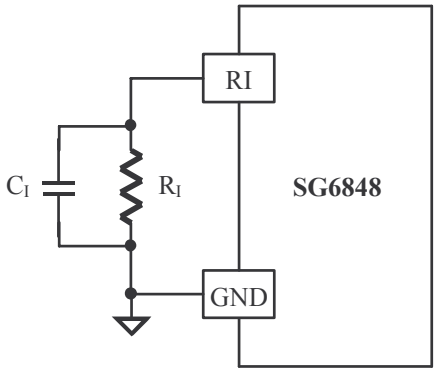


Figure 4. Setting PWM frequency

The patented green-mode function provides off-time modulation to reduce the PWM frequency at light-load and no-load conditions. The sink current of the FB pin determines the green mode operation as shown in Fig.5. At light load, the sink current of the FB pin will increase. When the sink current is larger than 1mA, the PWM frequency decreases in order to reduce the power consumption of the power supply at light-load and in no-load conditions.

For lightening surge tests, a small capacitor (not over 50pF) connected from the RI pin to GND is recommended. This added capacitor also improves stability, especially at light load and high input line voltage conditions.

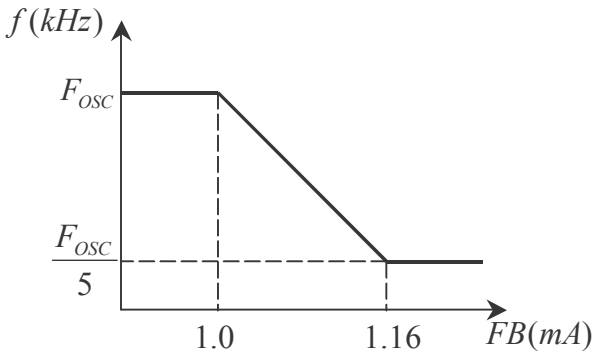


Figure 5. PWM frequency vs. FB current.

Built-in Slope Compensation

A flyback converter can be operated in either discontinuous current mode (DCM) or continuous current mode (CCM). There are many advantages to operating the converter in CCM. With the same output power, a converter in CCM exhibits smaller peak inductor currents than one in DCM. Therefore, a small-sized transformer and a low-rated MOSFET can be applied. On the secondary side of the transformer, the rms output current of DCM can be up to twice that of CCM. Larger wire gauge and output capacitors with larger ripple current ratings are required. DCM operation

also results in higher output voltage spikes. A large LC filter must also be added. Therefore, a flyback converter in CCM achieves better performance with lower component cost.

Despite the above advantages of operating in CCM, there is one concern – stability. Operating in CCM, the output power is proportional to the average inductor current, while the peak current is controlled. This causes a well-known sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent this oscillation. The SG6848 introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. The sensed voltage together with this slope compensation signal (V_{SLOPE}) is fed into the non-inverting input of the PWM comparator. The resulting voltage is compared with the FB signal to adjust the PWM duty cycle, such that the output voltage is regulated. Therefore, users can use the SG6848 to design a cost-effective, highly efficient and compact sized flyback power supply operating in CCM without adding any external components.
The positive ramp added is,

$$V_{SLOPE} = V_{SL} \cdot D \qquad (4)$$

where
V_{SL} = 0.33V;

D = Duty cycle

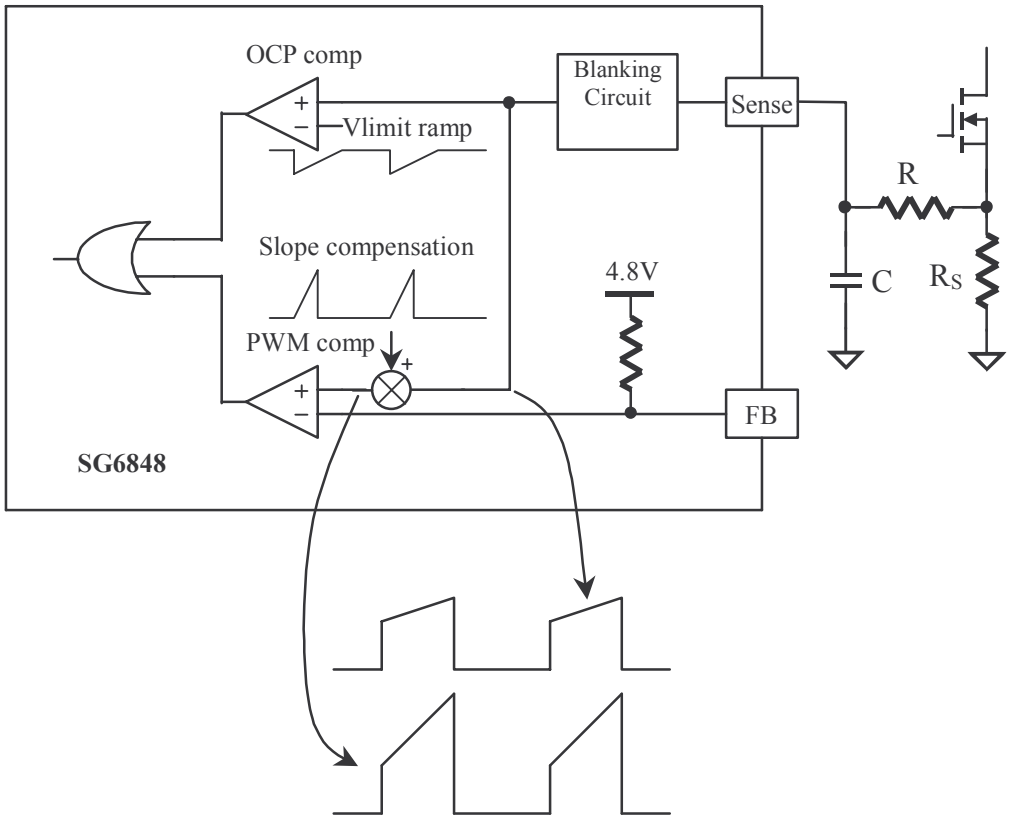


Figure 6. Synchronized slope compensation

Constant Output Power Limit

The maximum output power of a flyback converter can generally be determined from the current-sense resistor R_S. When the load increases, the peak inductor current increases accordingly. When the output current arrives at the protection value, the OCP comparator dominates the current control loop. OCP occurs when the current-sense voltage

reaches the threshold value. The output GATE driver is turned off after a small propagation delay, td. The delay time results in unequal power-limit level under universal input. In the SG6848, a saw-tooth power-limiter is designed to solve the unequal power-limit problem. As shown in Figure 7, the power limiter is designed as a positive ramp signal and is fed to the inverting input of the OCP comparator. This results in a lower current limit at high-line inputs than at low-line inputs. However, with fixed propagation delay, td, the peak primary current would be the same for various line input voltages. Therefore the maximum output power can practically be limited to a constant value within a wide input voltage range without adding any external circuitry.

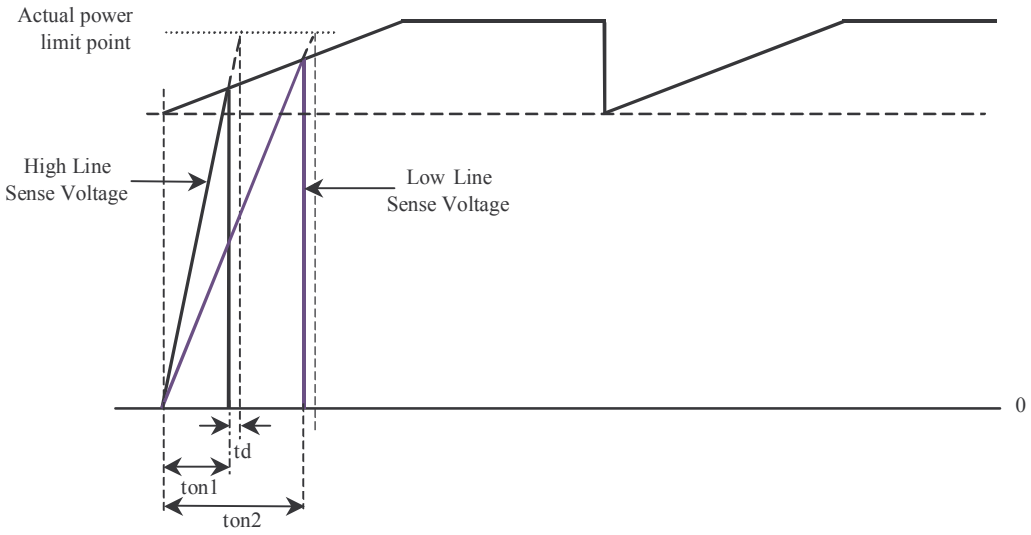


Figure 7. Constant power limit compensation

Short Circuit Protection

When the output of a flyback power supply is shorted, the primary VDD will decrease due to the coupling polarity between the aux winding and the secondary winding of a transformer. When V_{DD} drops below UVLO level of the SG6848, the power supply will enter hiccup operation mode and hence limit the output power. However, it is possible that the V_{DD} voltage remains higher than the UVLO level even if the output is shorted. This happens when the coupling between the aux and the primary winding is too good. Therefore, the construction of the transformer becomes a dominant factor. The recommended construction layout is to increase the insulation thickness for the aux winding and place the primary aux winding in one side of the bobbin. For low output voltage applications, using a low dropout voltage diode and a larger secondary winding also help.

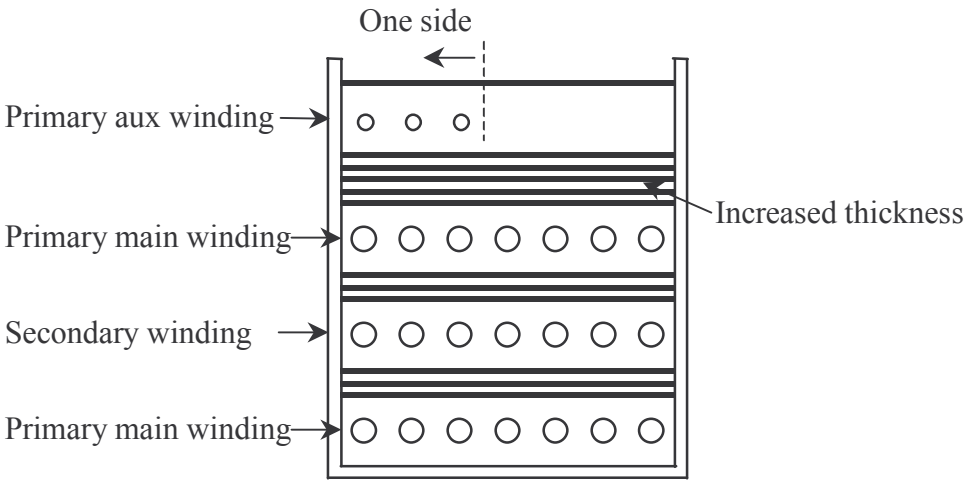


Figure 8. Transformer Construction

Leading Edge Blanking

A voltage signal proportional to the MOSFET current develops on the current-sensing resistor, R_S. Each time the MOSFET is turned on, a spike, which is induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode, inevitably appears on the sensed signal. Inside the SG6848, a leading edge blanking time of about 270 nsec. is introduced to avoid premature termination of the MOSFET by the spike. Therefore, only a small-value RC filter (e.g. 100ohm + 470pF) is required between the SENSE pin and R_S. Still, a non-inductive resistor for the R_S is recommended.

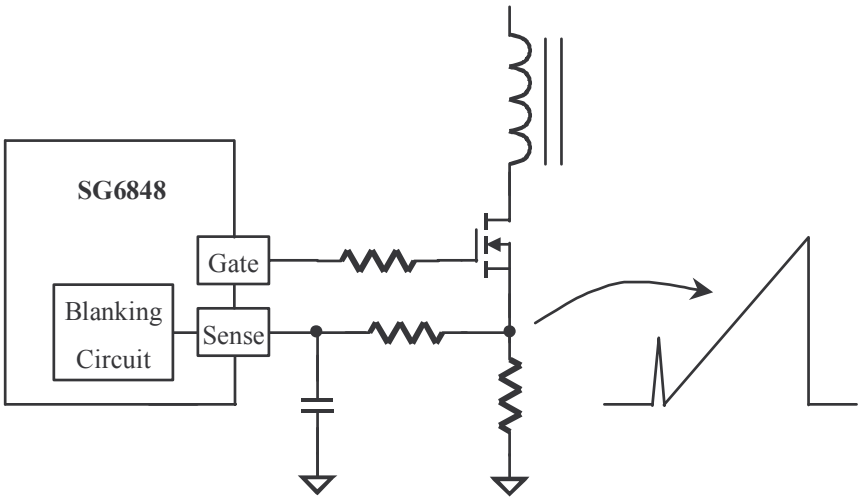


Figure 9. Turn on spike

Gate Drive

The SG6848's output stage is a fast totem pole driver that can drive a MOSFET gate directly. It is also equipped with a voltage clamping Zener diode to protect the MOSFET from damage caused by undesirable over-drive voltage. The output voltage is clamped at 17V. An internal pull-down resistor is used to avoid a floating state of the gate before startup. A gate drive resistor in the range of 47 to 100 ohm is recommended. This resistor limits the peak gate drive current and provides damping to prevent oscillations at the MOSFET gate terminal.

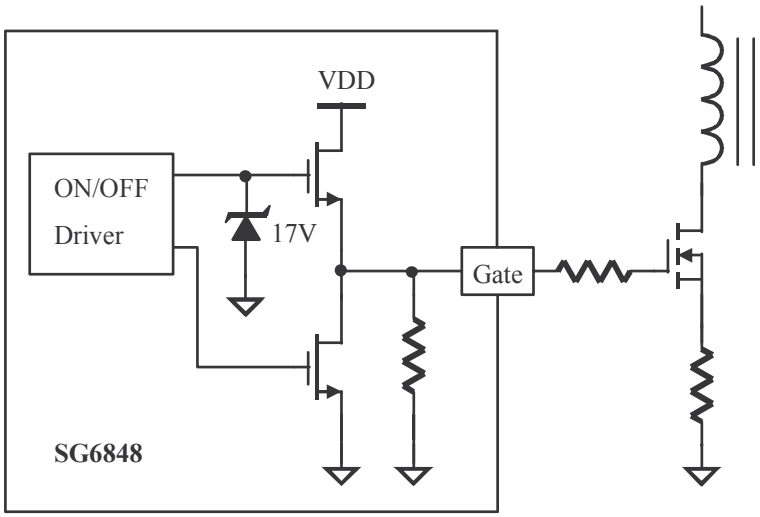


Figure 10. Gate drive

Lab Note

Before reworking or soldering/de-soldering on the power supply, it is suggested to **discharge the primary capacitors by an external bleeding resistor**. Otherwise the PWM IC may be destroyed by external high voltage during soldering or de-soldering.

This device is sensitive to ESD discharge. To improve the production yield, the production line should be ESD protected in accordance to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1.

Printed Circuit Board (PCB) Layout

High frequency switching current/voltage make PCB layout a very important design issue. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge/ESD tests. Here, we give some common guidelines:

(A) In order to get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C1 first, and then to the switching circuits.

(B) The high frequency current loop is in **C1 – Transformer – MOSFET – R_S – C1**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High voltage traces related to the drain of the MOSFET and the RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, it's better to connect this heatsink to ground.

(C) As indicated by 3, the ground of control circuits should be connected first before any other circuitry.

(D) As indicated by 2, the area enclosed by the **transformer aux winding, D1, and C2** should also be kept small. Place C2 close to the SG6848 for good decoupling.

(E) Two suggestions for ground connections, with different pro and cons, are offered.

I. GND3→2→4→1: This should avoid common impedance interference for the sense signal.

II. GND3→2→1→4: This should be better for ESD tests, where the earth ground is not available on the power supply. Regarding the ESD discharge path, the charges go from secondary through the transformer's stray capacitance to GND2 first. Then the charges goes from GND2 to GND1 and back to the mains. It should be noted that control circuits should not be placed in the discharge path. Point discharges for common choke can decrease the high frequency impedance and help increase ESD immunity.

(F) Should a Y-cap between primary and secondary be required, it is suggested to connect this Y-cap to the **positive terminal of C1 (Vdc)**. If this Y-cap is connected to primary GND, it should be connected to the **negative terminal of C1 (GND1)** directly. The Point discharge of this Y-cap also helps with ESD. However, the distance between these two points should be at least 5mm according to safety requirements.

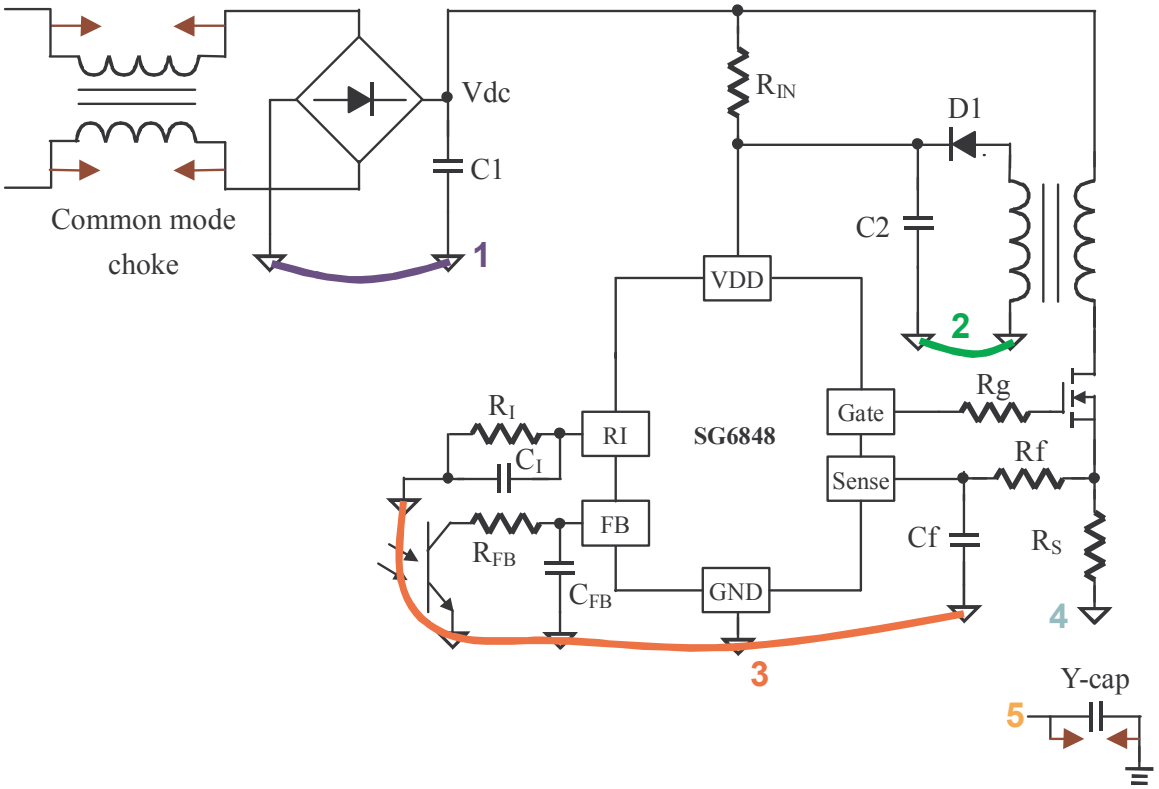


Figure 11. Layout considerations