Designing Switching Voltage Regulators With the TL494

Patrick Griffith *Standard Linear & Logic*

ABSTRACT

The TL494 power-supply controller is discussed in detail. A general overview of the TL494 architecture presents the primary functional blocks contained in the device. An in-depth study of the interrelationship between the functional blocks highlights versatility and limitations of the TL494. The usefulness of the TL494 power-supply controller also is demonstrated through several basic applications, and a design example is included for a 5-V/10-A power supply.

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Introduction

Monolithic integrated circuits for the control of switching power supplies have become widespread since their introduction in the 1970s. The TL494 combines many features that previously required several different control circuits. The purpose of this application report is to give the reader a thorough understanding of the TL494, its features, its performance characteristics, and its limitations.

The Basic Device

The design of the TL494 not only incorporates the primary building blocks required to control a switching power supply, but also addresses many basic problems and reduces the amount of additional circuitry required in the total design. Figure 1 is a block diagram of the TL494.

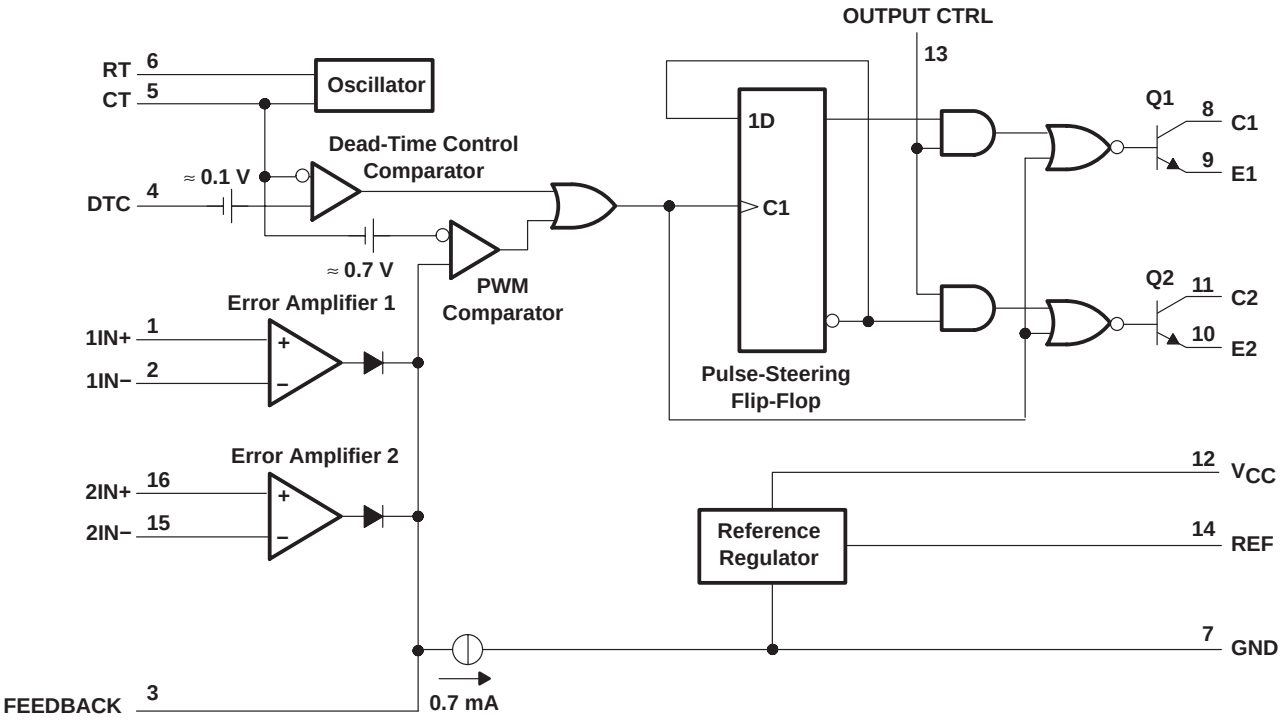


Figure 1. TL494 Block Diagram

Principle of Operation

The TL494 is a fixed-frequency pulse-width-modulation (PWM) control circuit. Modulation of output pulses is accomplished by comparing the sawtooth waveform created by the internal oscillator on the timing capacitor (C_T) to either of two control signals. The output stage is enabled during the time when the sawtooth voltage is greater than the voltage control signals. As the control signal increases, the time during which the sawtooth input is greater decreases; therefore, the output pulse duration decreases. A pulse-steering flip-flop alternately directs the modulated pulse to each of the two output transistors. Figure 2 shows the relationship between the pulses and the signals.

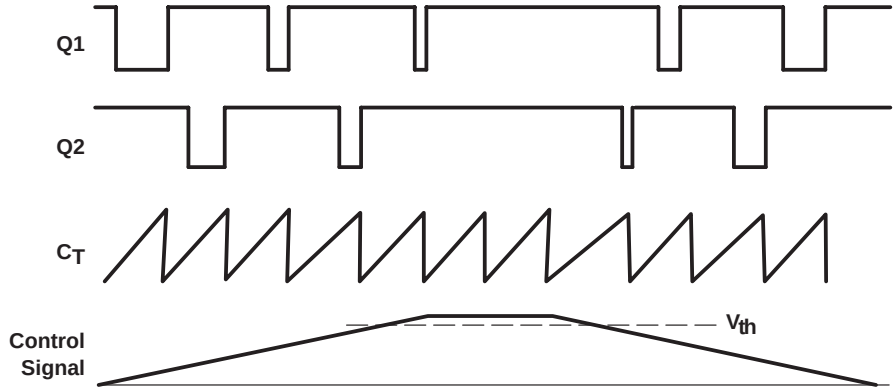


Figure 2. TL494 Modulation Technique

The control signals are derived from two sources: the dead-time (off-time) control circuit and the error amplifier. The dead-time control input is compared directly by the dead-time control comparator. This comparator has a fixed 100-mV offset. With the control input biased to ground, the output is inhibited during the time that the sawtooth waveform is below 110 mV. This provides a preset dead time of approximately 3%, which is the minimum dead time that can be programmed. The PWM comparator compares the control signal created by the error amplifiers. One function of the error amplifier is to monitor the output voltage and provide sufficient gain so that millivolts of error at its input result in a control signal of sufficient amplitude to provide 100% modulation control. The error amplifiers also can be used to monitor the output current and provide current limiting to the load.

5-V Reference Regulator

The TL494 internal 5-V reference regulator is shown in Figure 3. In addition to providing a stable reference, it acts as a preregulator and establishes a stable supply from which the output-control logic, pulse-steering flip-flop, oscillator, dead-time control comparator, and PWM comparator are powered. The regulator employs a band-gap circuit as its primary reference to maintain thermal stability of less than 100-mV variation over the operating free-air temperature range of 0°C to 70°C. Short-circuit protection is provided to protect the internal reference and preregulator, 10 mA of load current is available for additional bias circuits. The reference is internally programmed to an initial accuracy of ±5% and maintains a stability of less than 25-mV variation over an input voltage range of 7 V to 40 V. For input voltages less than 7 V, the regulator saturates within 1 V of the input and tracks it (see Figure 4).

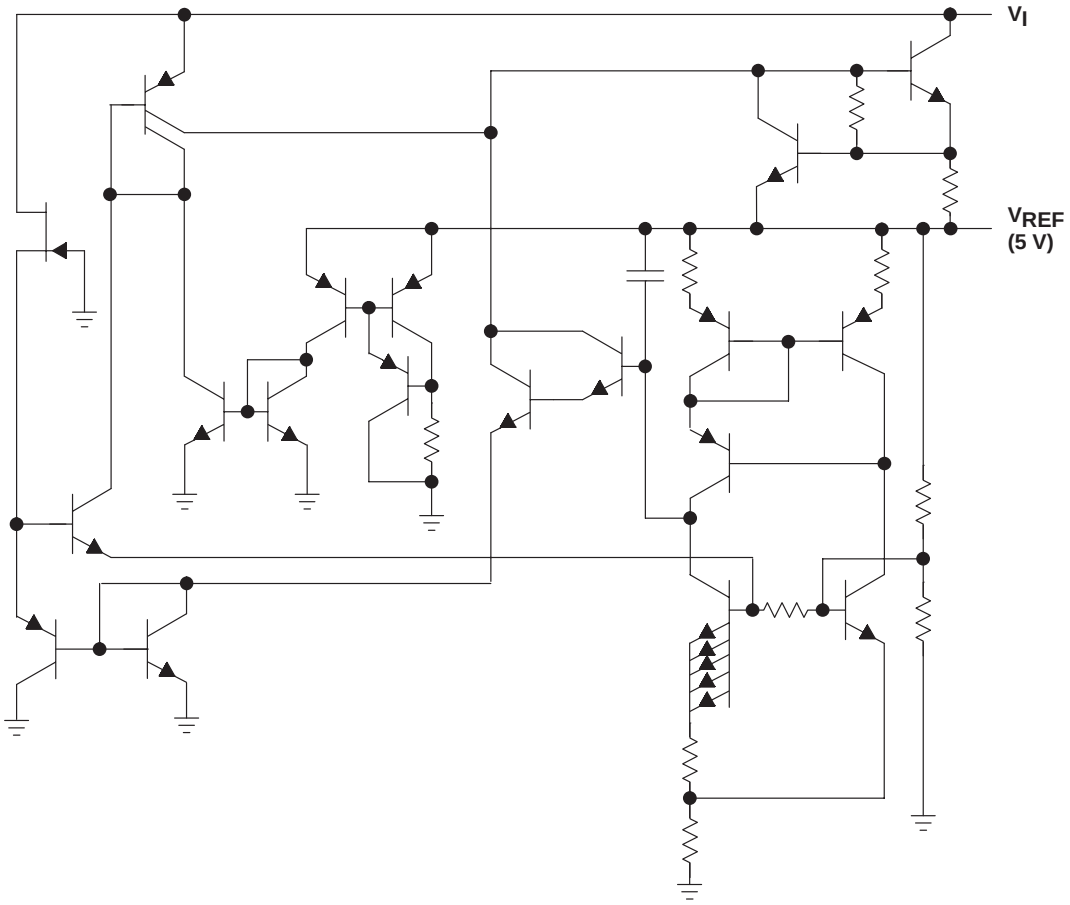


Figure 3. 5-V Reference Regulator

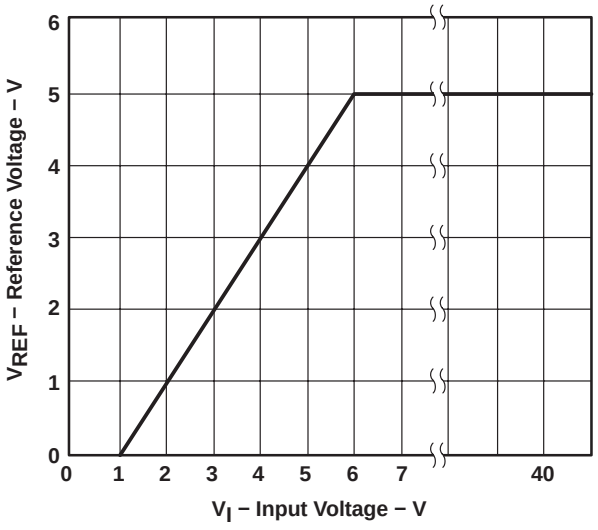


Figure 4. Reference Voltage vs Input Voltage

Oscillator

A schematic of the TL494 internal oscillator is shown in Figure 5. The oscillator provides a positive sawtooth waveform to the dead-time and PWM comparators for comparison to the various control signals.

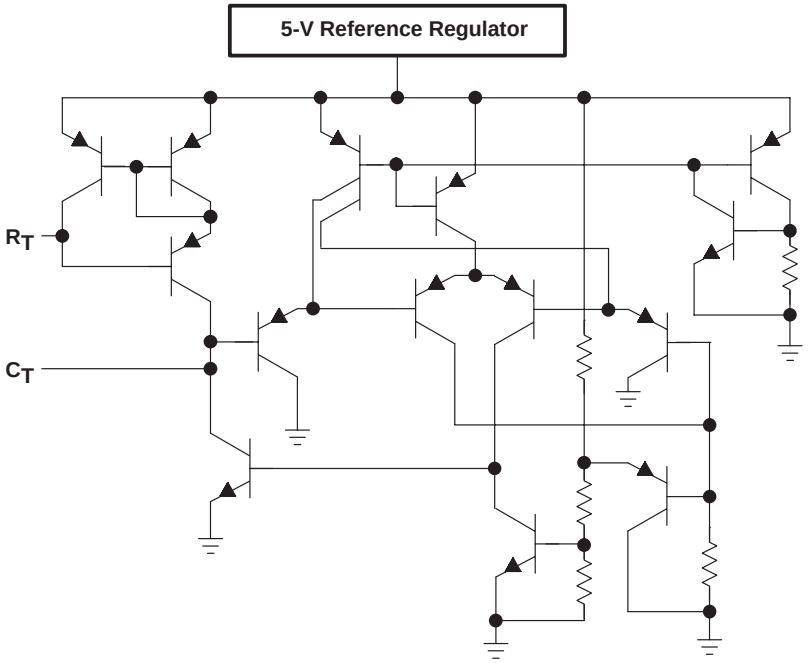


Figure 5. Internal-Oscillator Schematic

Operation Frequency

The frequency of the oscillator is programmed by selecting timing components R_T and C_T. The oscillator charges the external timing capacitor, C_T, with a constant current; the value of which is determined by the external timing resistor, R_T. This produces a linear-ramp voltage waveform. When the voltage across C_T reaches 3 V, the oscillator circuit discharges it and the charging cycle is reinitiated. The charging current is determined by the formula:

$$I_{CHARGE} = 3\ V/R_T \quad (1)$$

The period of the sawtooth waveform is:

$$T = (3\ V \times C_T)/I_{CHARGE} \quad (2)$$

The frequency of the oscillator becomes:

$$f_{OSC} = 1/(R_T \times C_T) \quad (3)$$

However, the oscillator frequency is equal to the output frequency only for single-ended applications. For push-pull applications, the output frequency is one-half the oscillator frequency.

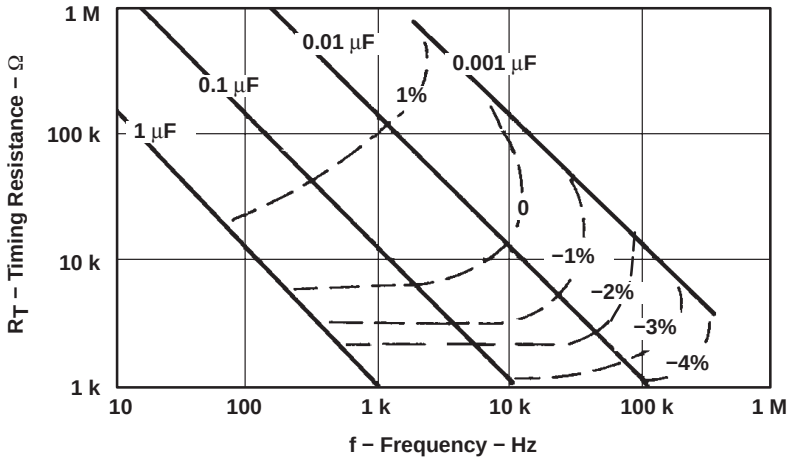
Single-ended applications:

$$f = 1/(R_T \times C_T) \quad (4)$$

Push-pull applications:

$$f = 1/(2R_T \times C_T) \quad (5)$$

The oscillator is programmable over a range of 1 kHz to 300 kHz. Practical values for R_T and C_T range from 1 kΩ to 500 kΩ and 470 pF to 10 μF, respectively. A plot of the oscillator frequency versus R_T and C_T is shown in Figure 6. The stability of the oscillator for free-air temperatures from 0°C to 70°C for various ranges of R_T and C_T also is shown in Figure 6.



NOTE: The percent of oscillator frequency variation over the 0°C to 70°C free-air temperature range is represented by dashed lines.

Figure 6. Oscillator Frequency vs R_T/C_T

Operation Above 150 kHz

At an operation frequency of 150 kHz, the period of the oscillator is 6.67 μs. The dead time established by the internal offset of the dead-time comparator (~3% period) yields a blanking pulse of 200 ns. This is the minimum blanking pulse acceptable to ensure proper switching of the pulse-steering flip-flop. For frequencies above 150 kHz, additional dead time (above 3%) is provided internally to ensure proper triggering and blanking of the internal pulse-steering flip-flop. Figure 7 shows the relationship of internal dead time (expressed in percent) for various values of R_T and C_T.

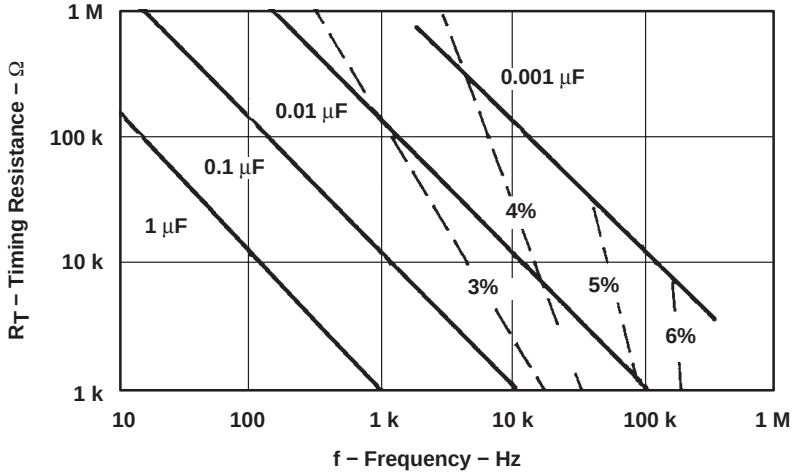


Figure 7. Variation of Dead Time vs R_T/C_T

Dead-Time Control/PWM Comparator

The functions of the dead-time control comparator and the PWM comparator are incorporated in a single comparator circuit (see Figure 8). The two functions are totally independent; therefore, each function is discussed separately.

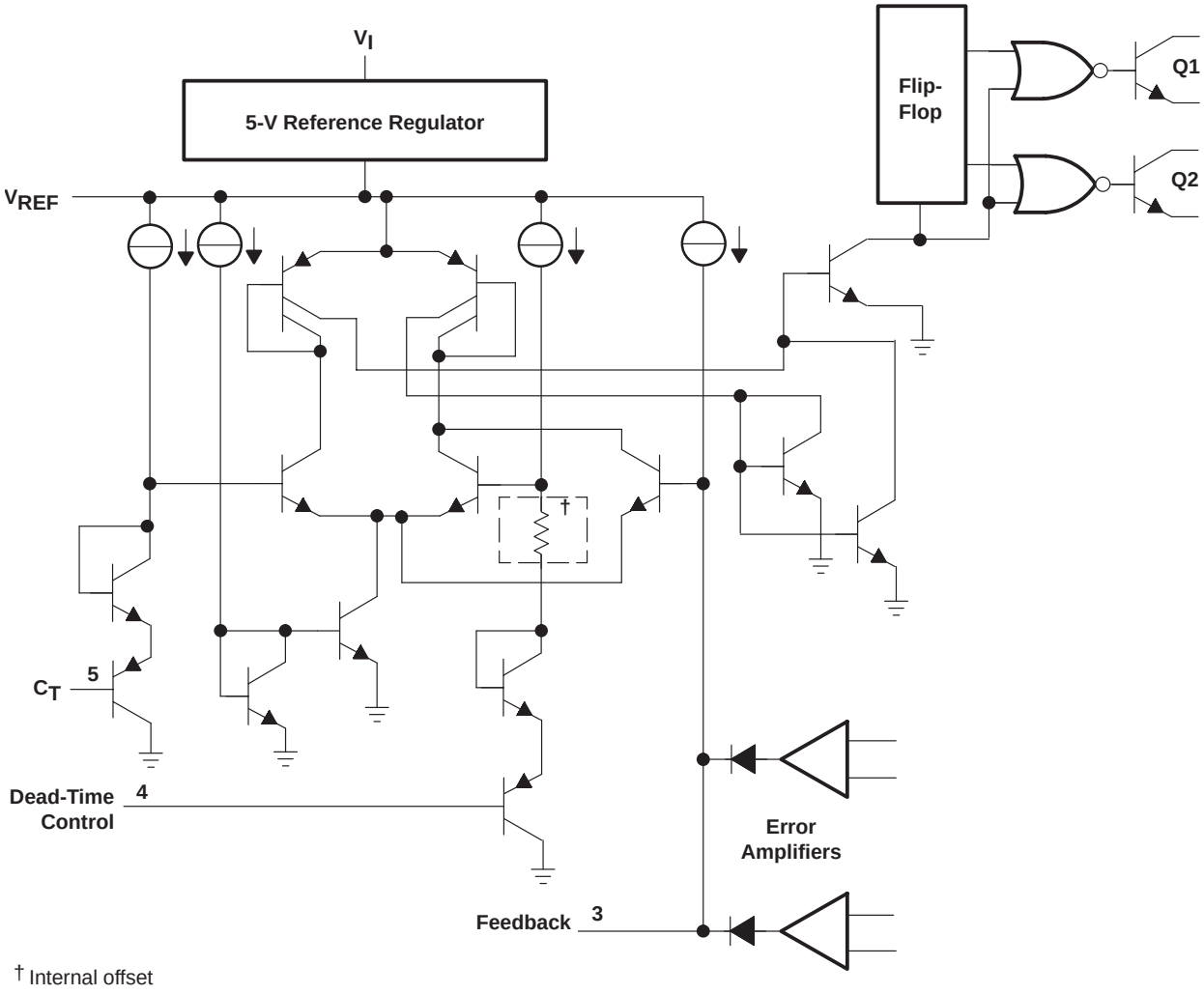


Figure 8. Dead-Time Control/PWM Comparator

Dead-Time Control

The dead-time control input provides control of the minimum dead time (off time). The output of the comparator inhibits switching transistors Q1 and Q2 when the voltage at the input is greater than the ramp voltage of the oscillator (see Figure 28). An internal offset of 110 mV ensures a minimum dead time of ~3% with the dead-time control input grounded. Applying a voltage to the dead-time control input can impose additional dead time. This provides a linear control of the dead time from its minimum of 3% to 100% as the input voltage is varied from 0 V to 3.3 V, respectively. With full-range control, the output can be controlled from external sources without disrupting the error amplifiers. The dead-time control input is a relatively high-impedance input (I_I < 10 μA) and should be used where additional control of the output duty cycle is required. However, for proper control, the input must be terminated. An open circuit is an undefined condition.

Comparator

The comparator is biased from the 5-V reference regulator. This provides isolation from the input supply for improved stability. The input of the comparator does not exhibit hysteresis, so protection against false triggering near the threshold must be provided. The comparator has a response time of 400 ns from either of the control-signal inputs to the output transistors, with only 100 mV of overdrive. This ensures positive control of the output within one-half cycle for operation within the recommended 300-kHz range.

Pulse-Width Modulation (PWM)

The comparator also provides modulation control of the output pulse width. For this, the ramp voltage across timing capacitor C_T is compared to the control signal present at the output of the error amplifiers. The timing capacitor input incorporates a series diode that is omitted from the control signal input. This requires the control signal (error amplifier output) to be ~0.7 V greater than the voltage across C_T to inhibit the output logic, and ensures maximum duty cycle operation without requiring the control voltage to sink to a true ground potential. The output pulse width varies from 97% of the period to 0 as the voltage present at the error amplifier output varies from 0.5 V to 3.5 V, respectively.

Error Amplifiers

A schematic of the error amplifier circuit is shown in Figure 9. Both high-gain error amplifiers receive their bias from the V_I supply rail. This permits a common-mode input voltage range from –0.3 V to 2 V less than V_I. Both amplifiers behave characteristically of a single-ended single-supply amplifier, in that each output is active high only. This allows each amplifier to pull up independently for a decreasing output pulse-width demand. With both outputs ORed together at the inverting input node of the PWM comparator, the amplifier demanding the minimum pulse out dominates. The amplifier outputs are biased low by a current sink to provide maximum pulse width out when both amplifiers are biased off.

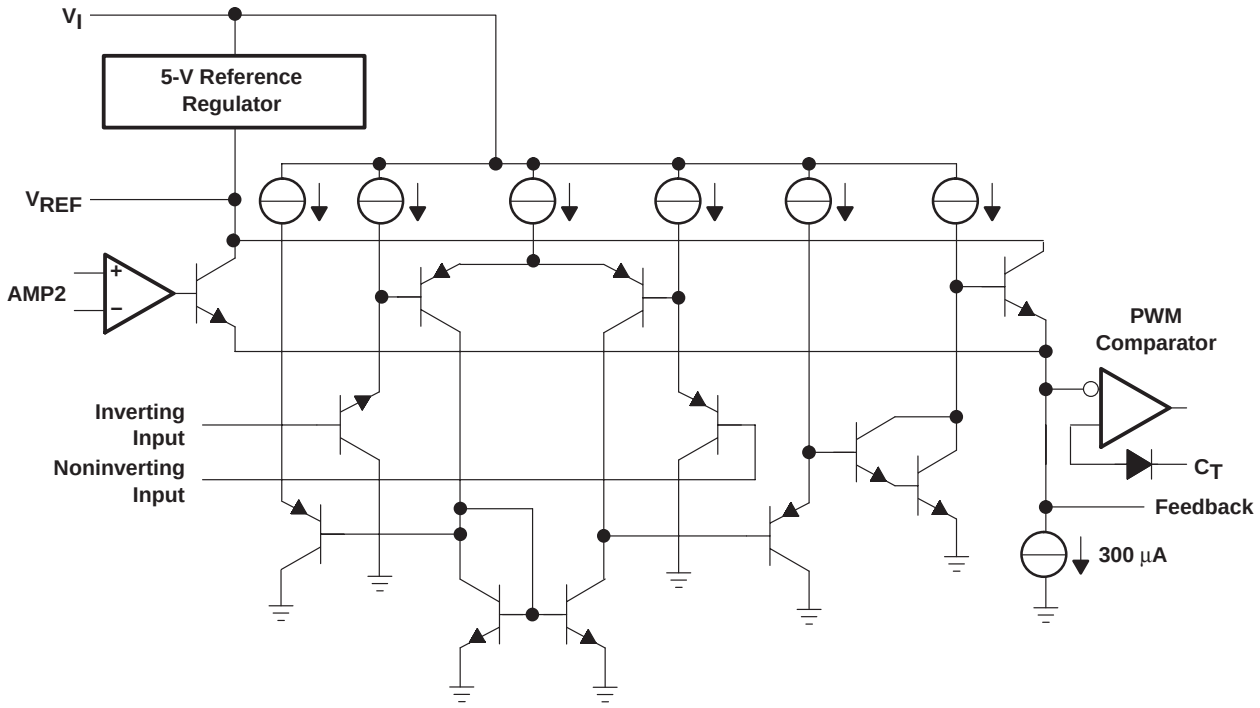


Figure 9. Error Amplifiers

Figure 10 shows the output structure of the amplifiers operating into the 300-μA current sink. Attention must be given to this node for biasing considerations in gain-control and external-control interface circuits. Because the amplifier output is biased low only through a current sink (I_{SINK} = 0.3 mA), bias current required by external circuitry into the feedback terminal must not exceed the capability of the current sink. Otherwise, the maximum output pulse width is limited. Figure 11 shows the proper biasing techniques for feedback gain control.

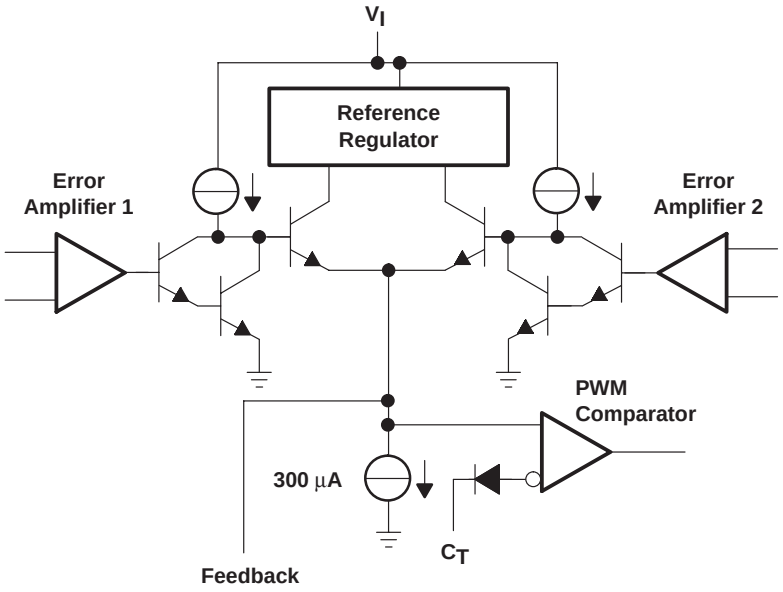


Figure 10. Multiplex Structure of Error Amplifiers

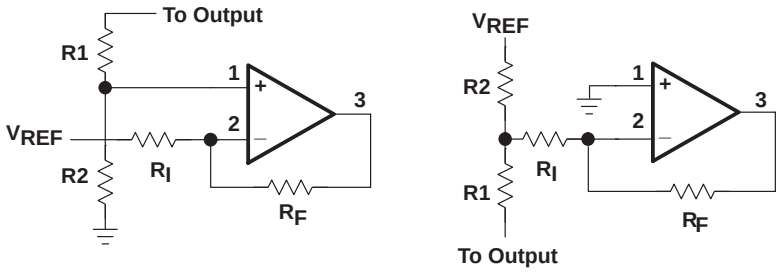


Figure 11. Error-Amplifier-Bias Configurations for Controlled-Gain Applications

Figure 12 shows a plot of amplifier transfer characteristics. This illustrates the linear gain characteristics of the amplifiers over the active input range of the PWM comparator (0.5 V to 3.5 V). This is important for overall circuit stability. The open-loop gain of the amplifiers, for output voltages from 0.5 V to 3.5 V, is 60 dB. A Bode plot of amplifier response time is shown in Figure 13. Both amplifiers have a response time of approximately 400 ns from their inputs to their outputs. Precautions should be taken to minimize capacitive loading of the amplifier outputs. Because the amplifiers employ active pullup only, the amplifiers' ability to respond to an increasing load demand can be degraded severely by capacitive loads.

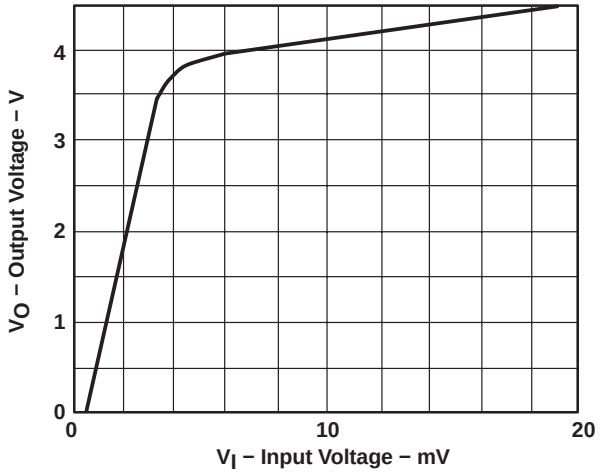


Figure 12. Amplifier Transfer Characteristics

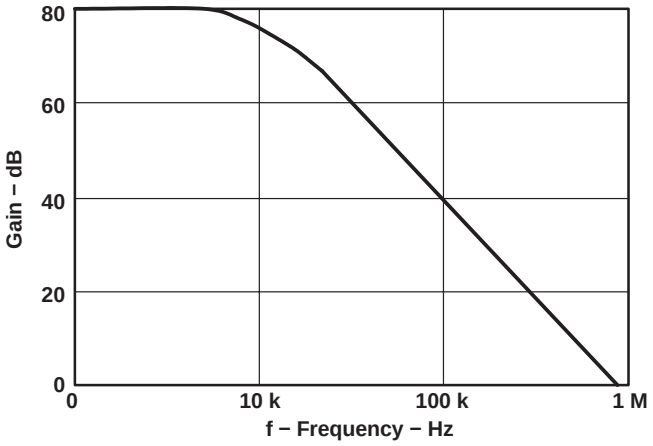


Figure 13. Amplifier Bode Plot

Output-Control Logic

The output-control logic is structured to provide added versatility through external control. Designed for either push-pull or single-ended applications, circuit performance can be optimized by selection of the proper conditions applied to various control inputs.

Output-Control Input

The output-control input determines whether the output transistors operate in parallel or push-pull. This input is the supply source for the pulse-steering flip-flop (see Figure 14). The output-control input is asynchronous and has direct control over the output, independent of the oscillator or pulse-steering flip-flop. The input condition is intended to be a fixed condition that is defined by the application. For parallel operation, the output-control input must be grounded. This disables the pulse-steering flip-flop and inhibits its outputs. In this mode, the pulses seen at the output of the dead-time control/PWM comparator are transmitted by both output transistors in parallel. For push-pull operation, the output-control input must be connected to the internal 5-V reference regulator. Under this condition, each of the output transistors is enabled, alternately, by the pulse-steering flip-flop.

FUNCTION TABLE

INPUT TO OUTPUT CTRL	OUTPUT FUNCTION
V_I = GND	Single-ended or parallel output
$V_I = V_{ref}$	Normal push-pull operation

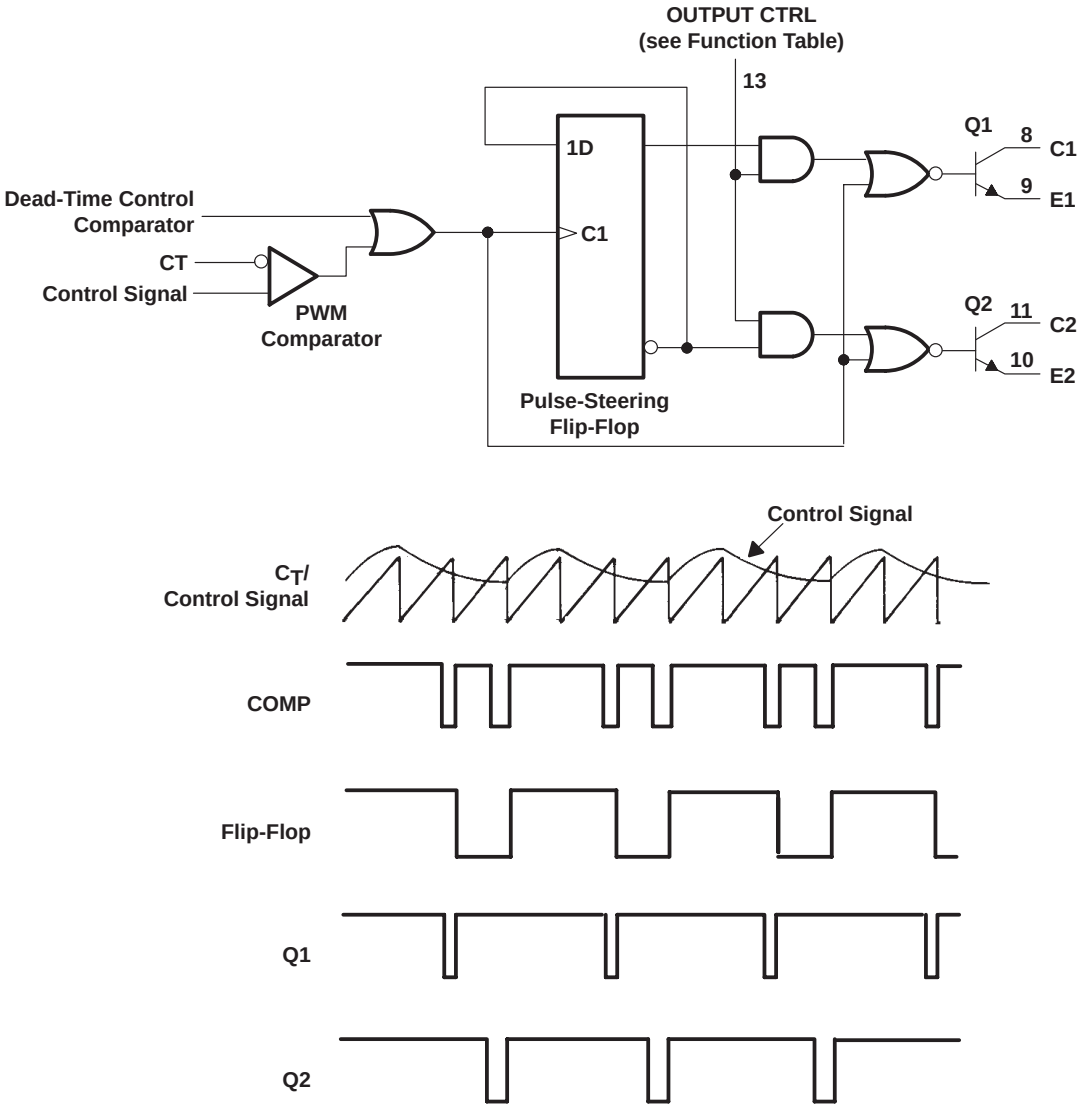


Figure 14. Output-Steering Architecture

Pulse-Steering Flip-Flop

The pulse-steering flip-flop is a positive-edge-triggered D-type flip-flop that changes state synchronously with the rising edge of the comparator output (see Figure 14). The dead time provides blanking during this period to ensure against the possibility of having both outputs on, simultaneously, during the transition of the pulse-steering flip-flop outputs. A schematic of the pulse-steering flip-flop is shown in Figure 15. Since the flip-flop receives its trigger from the output of the comparator, not the oscillator, the output always operates in push-pull. The flip-flop does not change state unless an output pulse occurred in the previous period of the oscillator. This architecture prevents either output from double pulsing, but restricts the application of the control-signal sources to dc feedback signals (for additional detail, see *Pulse-Current Limiting* in this application report).

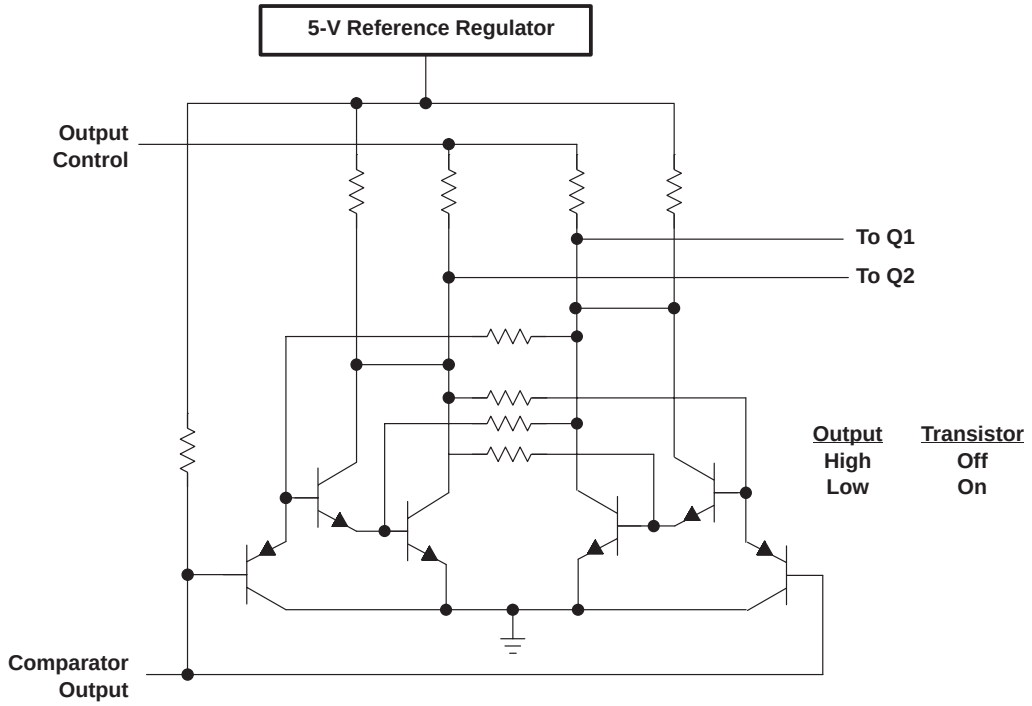


Figure 15. Pulse-Steering Flip-Flop

Output Transistors

Two output transistors are available on the TL494. The output structure is shown in Figure 16. Both transistors are configured as open collector/open emitter, and each is capable of sinking or sourcing up to 200 mA. The transistors have a saturation voltage of less than 1.3 V in the common-emitter configuration and less than 2.5 V in the emitter-follower configuration. The outputs are protected against excessive power dissipation to prevent damage, but do not employ sufficient current limiting to allow them to be operated as current-source outputs.

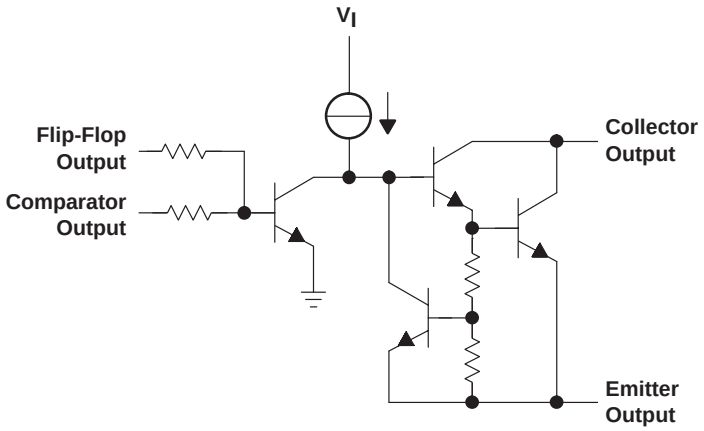


Figure 16. Output-Transistor Structure

Applications

Reference Regulator

The internal 5-V reference regulator is designed primarily to provide the internal circuitry with a stable supply rail for varying input voltages. The regulator provides sufficient drive to sustain up to 10 mA of supply current to additional load circuitry. However, excessive loading may degrade the performance of the TL494 because the 5-V reference regulator establishes the supply voltage of much of the internal control circuitry.

Current Boosting the 5-V Regulator

Conventional bootstrap techniques for three-terminal regulators, such as the one in Figure 17, are not recommended for use on the TL494. Normally, the bootstrap is programmed by resistor R_B so that transistor Q1 turns on as the load current approaches the capability of the regulator. This works very well when the current flowing into the input (through R_B) is determined by the load current. This is not necessarily the case with the TL494. The input current not only reflects the load current but includes the current drawn by the internal control circuit, which is biased from the reference regulator as well as from the input rail itself. As a result, the load current drawn by the reference regulator does not control the bias of shunt transistor Q1.

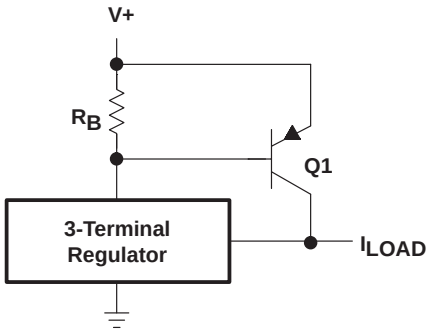


Figure 17. Conventional Three-Terminal Regulator Current-Boost Technique

Figure 18 shows the bootstrapping technique that is preferred for the TL494. This technique provides isolation between any bias-circuit load and the reference regulator output and provides a sufficient amount of supply current, without affecting the stability of the internal reference regulator. This technique should be applied for bias circuit drive only because regulation of the high-current output is solely dependent on the load.

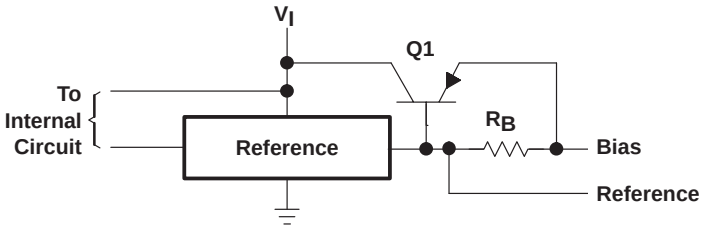


Figure 18. TL494 Reference Regulator Current-Boost Technique

Applications of the Oscillator

The design of the internal oscillator allows a great deal of flexibility in the operation of the TL494 control circuit.

Synchronization

Synchronizing two or more oscillators in a common system easily is accomplished with the architecture of the TL494 control circuits. Since the internal oscillator is used only for creation of the sawtooth waveform on the timing capacitor, the oscillator can be inhibited as long as a compatible sawtooth waveform is provided externally to the timing capacitor terminal. Terminating the R_T terminal to the reference-supply output can inhibit the internal oscillator.

Master/Slave Synchronization

For synchronizing two or more TL494s, establish one device as the master and program its oscillator normally. Disable the oscillators of each slave circuit (as previously explained) and use the sawtooth waveform created by the master for each of the slave circuits, tying all C_T pins together (see Figure 19).

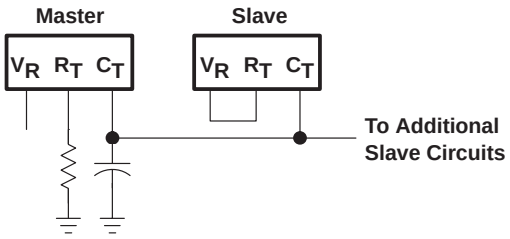


Figure 19. Master/Slave Synchronization

Master Clock Operation

To synchronize the TL494 to an external clock, the internal oscillator can be used as a sawtooth-pulse generator. Program the internal oscillator for a period that is 85% to 95% of the master clock and strobe the internal oscillator through the timing resistor (see Figure 20). Q1 is turned on when a positive pulse is applied to its base. This initiates the internal oscillator by grounding R_T, pulling the base of Q2 low. Q1 is latched on through the collector of Q2 and, as a result, the internal oscillator is locked on. As C_T charges, a positive voltage is developed across C1. Q1 forms a clamp on the trigger side of C1. At the completion of the period of the internal oscillator, the timing capacitor is discharged to ground and C1 drives the base of Q1 negative, causing Q1 and Q2 to turn off in turn. With the latch of Q1/Q2 turned off, R_T is open circuited, and the internal oscillator is disabled until another trigger pulse is experienced.

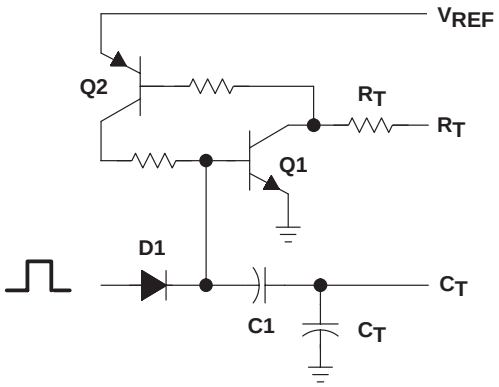


Figure 20. External Clock Synchronization

A common problem occurs during start-up when synchronizing the power supply to a system clock. Normally, an additional start-up oscillator is required. Again, the internal oscillator can be used by modifying the previous circuit slightly (see Figure 21). During power up, when the output voltage is low, Q3 is biased on, causing Q1 to stay on and the internal oscillator to behave normally. Once the output voltage has increased sufficiently ($V_O > V_{REF}$ for Figure 21), Q3 no longer is biased on and the Q1/Q2 latch becomes dependent on the trigger signal, as previously discussed.

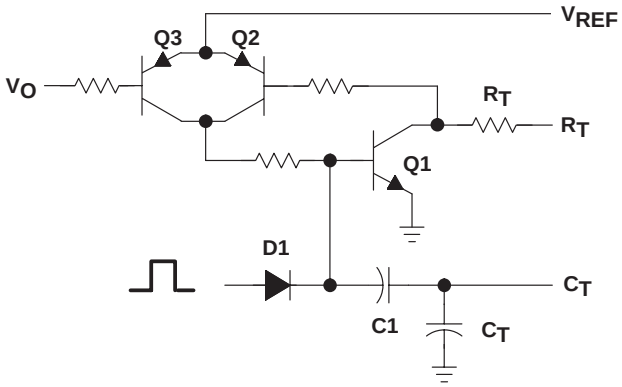


Figure 21. Oscillator Start-Up Circuit

Fail-Safe Operation

With the modulation scheme employed by the TL494 and the structure of the oscillator, the TL494 inherently turns off if either timing component fails. If timing resistor R_T opens, no current is provided by the oscillator to charge C_T. The addition of a bleeder resistor (see Figure 22) ensures the discharge of C_T. With the C_T input at ground, or if C_T short circuits, both outputs are inhibited.

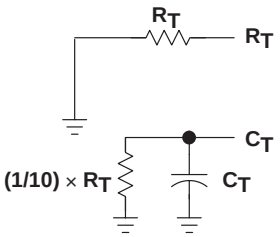


Figure 22. Fail-Safe Protection

Error-Amplifier-Bias Configuration

The design of the TL494 employs both amplifiers in a noninverting configuration. Figure 23 shows the proper bias circuits for negative and positive output voltages. The gain control circuits, shown in Figure 11, can be integrated into the bias circuits.

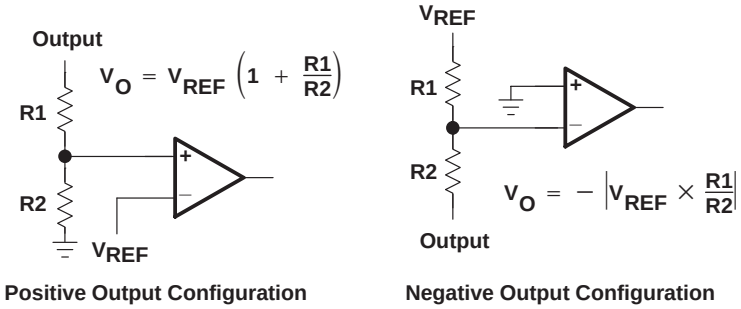


Figure 23. Error-Amplifier-Bias Configurations

Current Limiting

Either amplifier provided on the TL494 can be used for fold-back current limiting. Application of either amplifier is limited primarily to load-current control. The architecture defines that these amplifiers be used for dc control applications. Both amplifiers have a broad common-mode voltage range that allows direct current sensing at the output voltage rails. Several techniques can be employed for current limiting.

Fold-Back Current Limiting

Figure 24 shows a circuit that employs the proper bias technique for fold-back current limiting. Initial current limiting occurs when sufficient voltage is developed across R_{CL} to compensate for the base-emitter voltage of Q1, plus the voltage across R1. When current limiting occurs, the output voltage drops. As the output decays, the voltage across R1 decreases proportionally. This results in less voltage required across R_{CL} to maintain current limiting. The resulting output characteristics are shown in Figure 25.

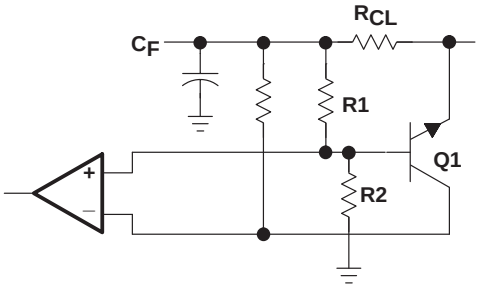
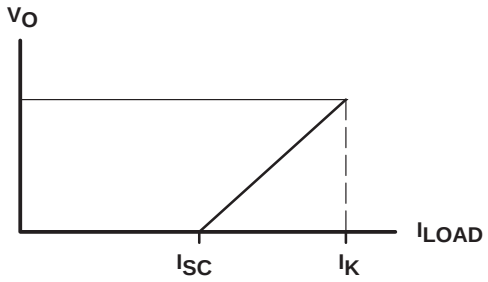


Figure 24. Fold-Back Current Limiting



$$I_K = \frac{V_O R1 + V_{BE(Q1)} (R1 + R2)}{R_{CL} \times R2}$$

$$I_{SC} = \frac{V_{BE(Q1)} (R1 + R2)}{R_{CL} \times R2}$$

Figure 25. Fold-Back Current Characteristics

Pulse-Current Limiting

The internal architecture of the TL494 does not accommodate direct pulse-current limiting. The problem arises from two factors:

- The internal amplifiers do not function as a latch; they are intended for analog applications.
- The pulse-steering flip-flop sees any positive transition of the PWM comparator as a trigger and switches its outputs prematurely, i.e., prior to the completion of the oscillator period.

As a result, a pulsed control voltage occurring during a normal on-time not only causes the output transistors to turn off but also switches the pulse-steering flip-flop. With the outputs off, the excessive current condition decays and the control voltage returns to the quiescent-error-signal level. When the pulse ends, the outputs again are enabled and the residual on-time pulse appears on the opposite output. The resulting waveforms are shown in Figure 26. The major problem here is the lack of dead-time control. A sufficiently narrow pulse may result in both outputs being on concurrently, depending on the delays of the external circuitry. A condition where insufficient dead time exists is a destructive condition. Therefore, pulse-current limiting is best implemented externally (see Figure 27).

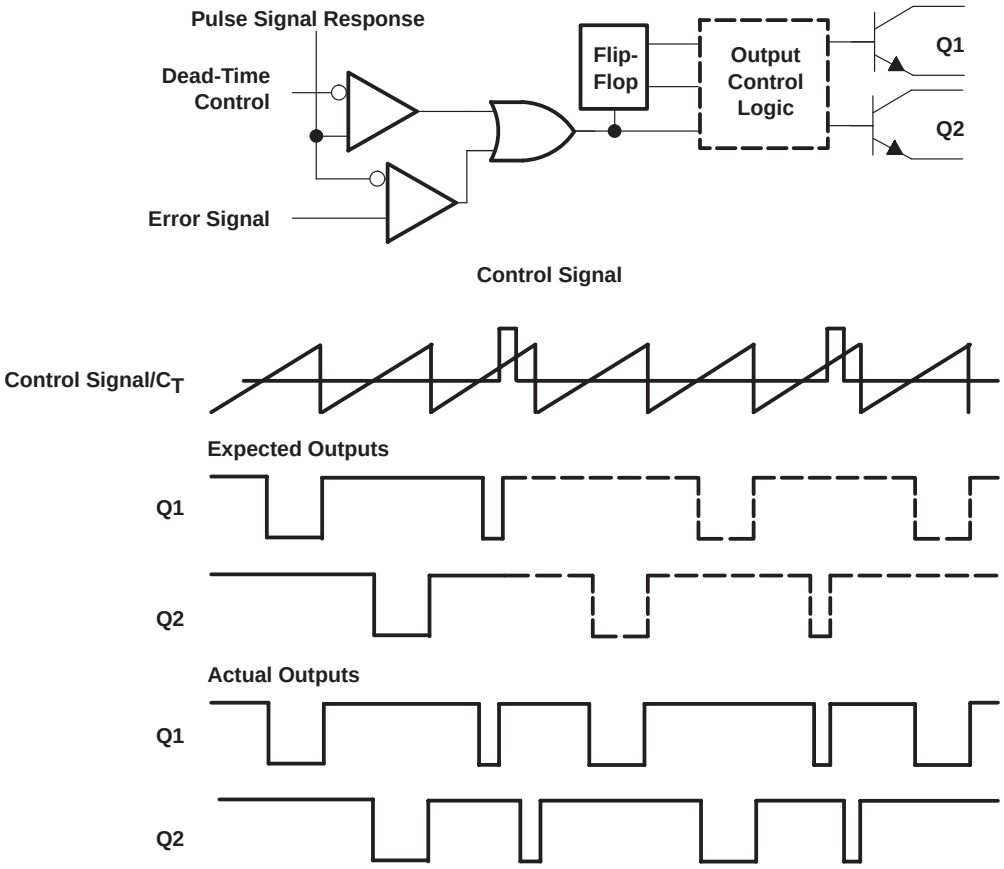


Figure 26. Error-Signal Considerations

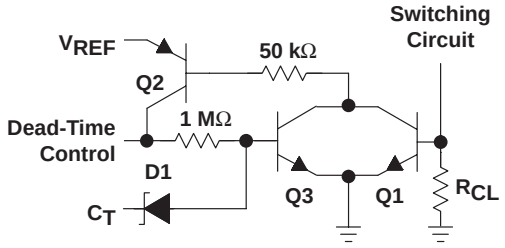


Figure 27. Peak-Current Protection

In Figure 27, the current in the switching transistors is sensed by R_{CL}. When there is sufficient current, the sensing transistor Q1 is forward biased, the base of Q2 is pulled low through Q1, and the dead-time control input is pulled to the 5-V reference. Drive for the base of Q3 is provided through the collector of Q2. Q3 acts as a latch to maintain Q2 in a saturated state when Q1 turns off, as the current decays through R_{CL}. The latch remains in this state, inhibiting the output transistors, until the oscillator completes its period and discharges C_T to 0 V. When this occurs, the Schottky diode (D1) forward biases and turns off Q3 and Q2, allowing the dead-time control to return to its programmed voltage.

Applications of the Dead-Time Control

The primary function of the dead-time control is to control the minimum off time of the output of the TL494. The dead-time control input provides control from 5% to 100% dead time (see Figure 28).

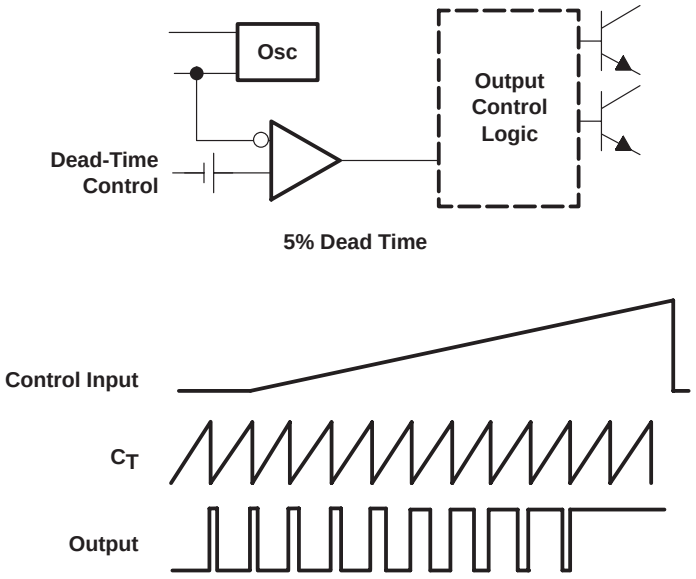


Figure 28. Dead-Time Control Characteristics

Therefore, the TL494 can be tailored to the specific power transistor switches that are used to ensure that the output transistors never experience a common on time. The bias circuit for the basic function is shown in Figure 29. The dead-time control can be used for many other control signals.

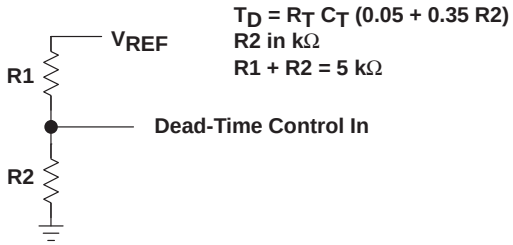


Figure 29. Tailored Dead Time

Soft Start

With the availability of the dead-time control, input implementation of a soft-start circuit is relatively simple; Figure 30 shows one example. Initially, capacitor C_S forces the dead-time control input to follow the 5-V reference regulator that disables both outputs, i.e., 100% dead time. As the capacitor charges through R_S, the output pulse slowly increases until the control loop takes command. If additional control is to be introduced at this input, a blocking diode should be used to isolate the soft-start circuit. If soft start is desired in conjunction with a tailored dead time, the circuit in Figure 29 can be used with the addition of capacitor C_S across R1.

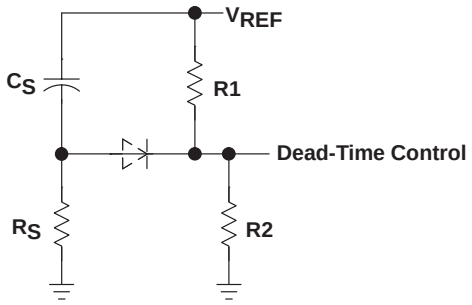


Figure 30. Soft-Start Circuit

The use of a blocking diode for soft-start protection is recommended. Not only does such circuitry prevent large current surges during power up, it also protects against any false signals that might be created by the control circuit as power is applied.

Overvoltage Protection

The dead-time control also provides a convenient input for overvoltage protection that may be sensed as an output voltage condition or input protection. Figure 31 shows a TL431 as the sensing element. When the supply rail being monitored increases to the point that 2.5 V is developed at the driver node of R1 and R2, the TL431 goes into conduction. This forward biases Q1, causing the dead-time control to be pulled up to the reference voltage and disabling the output transistors.

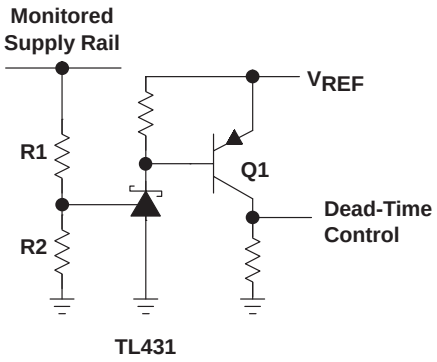


Figure 31. Overvoltage-Protection Circuit

Modulation of Turnon/Turnoff Transition

Modulation of the output pulse by the TL494 is accomplished by modulating the turnon transition of the output transistors. The turnoff transition always is concurrent with the falling edge of the oscillator waveform. Figure 32 shows the oscillator output as it is compared to a varying control signal and the resulting output waveforms. If modulation of the turnoff transition is desired, an external negative slope sawtooth waveform (see Figure 33) can be used without degrading the overall performance of the TL494.

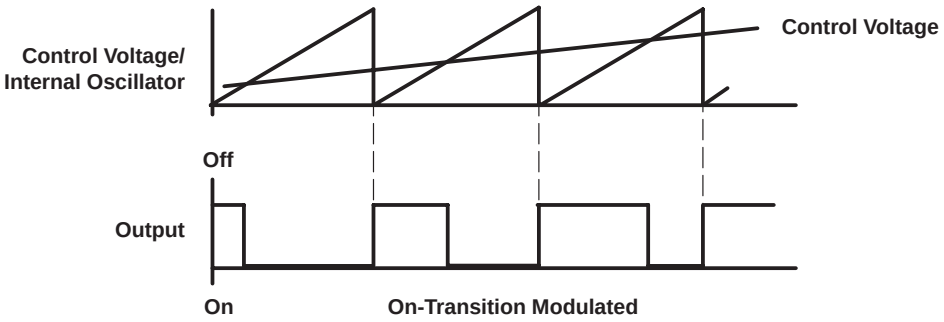


Figure 32. Turnon Transition

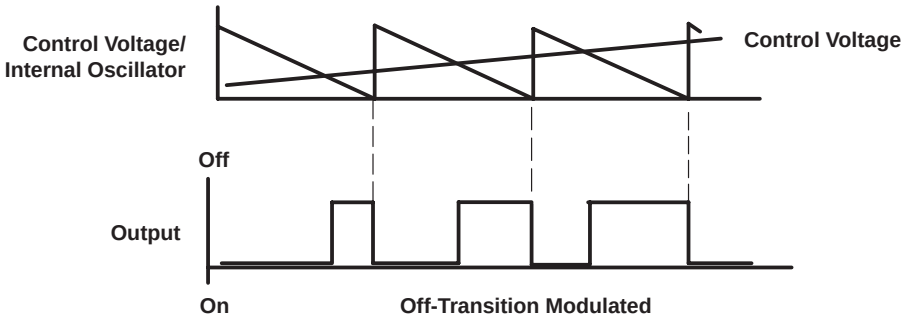


Figure 33. Turnoff Transition

Design Example

The following design example uses the TL494 to create a 5-V/10-A power supply. This design is based on the following parameters:

V_O = 5 V
V_I = 32 V
I_O = 10 A
f_{OSC} = 20-kHz switching frequency
V_R = 20-mV peak-to-peak (V_{RIPPLE})
ΔI_L = 1.5-A inductor current change

Input Power Source

The 32-V dc power source for this supply uses a 120-V input, 24-V output transformer rated at 75 VA. The 24-V secondary winding feeds a full-wave bridge rectifier followed by a current-limiting resistor (0.3 Ω) and two filter capacitors (see Figure 34).

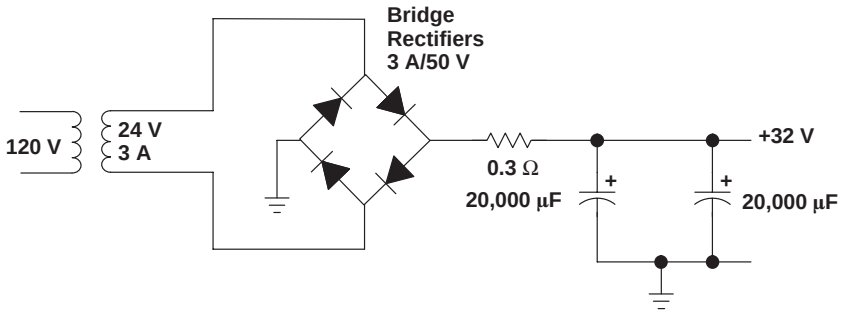


Figure 34. Input Power Source

The output current and voltage are determined by equations 6 and 7:

$$V_{RECTIFIER} = V_{SECONDARY} \times \sqrt{2} = 24\ V \times \sqrt{2} = 34\ V \quad (6)$$

$$I_{RECTIFIER(AVG)} \sim (V_O/V_I) \times I_O \sim 5\ V/32\ V \times 10\ A = 1.6\ A \quad (7)$$

The 3-A/50-V full-wave bridge rectifier meets these calculated conditions. Figure 35 shows the switching and control sections.

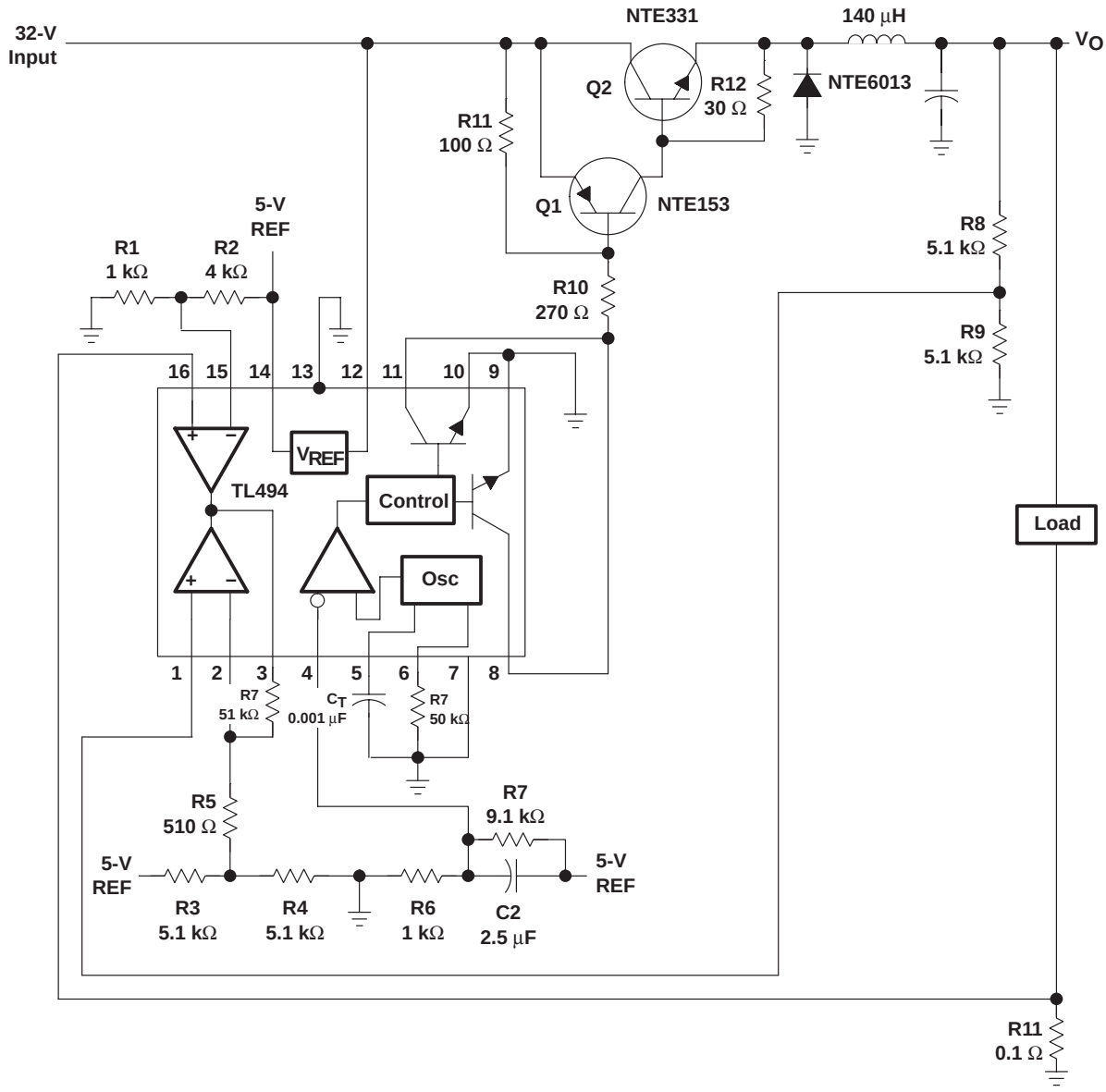


Figure 35. Switching and Control Sections

Control Circuits

Oscillator

Connecting an external capacitor and resistor to pins 5 and 6 controls the TL494 oscillator frequency. The oscillator is set to operate at 20 kHz, using the component values calculated by equations 8 and 9:

$$f_{OSC} = 1/(R_T \times C_T) \quad (8)$$

Choose C_T = 0.001 μF and calculate R_T:

$$R_T = 1/(f_{OSC} \times C_T) = 1/[(20 \times 10^3) \times (0.001 \times 10^{-6})] = 50\ k\Omega \quad (9)$$

Error Amplifier

The error amplifier compares a sample of the 5-V output to the reference and adjusts the PWM to maintain a constant output current (see Figure 36).

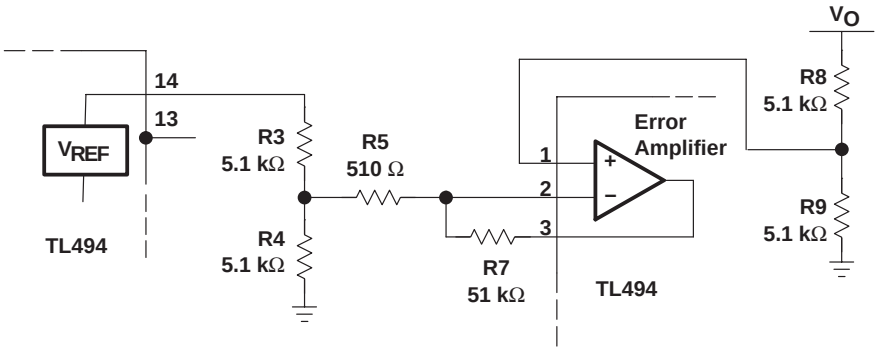


Figure 36. Error-Amplifier Section

The TL494 internal 5-V reference is divided to 2.5 V by R3 and R4. The output-voltage error signal also is divided to 2.5 V by R8 and R9. If the output must be regulated to exactly 5.0 V, a 10-kΩ potentiometer can be used in place of R8 to provide an adjustment.

To increase the stability of the error-amplifier circuit, the output of the error amplifier is fed back to the inverting input through R7, reducing the gain to 100.

Current-Limiting Amplifier

The power supply was designed for a 10-A load current and an I_L swing of 1.5 A; therefore, the short-circuit current should be:

$$I_{SC} = I_O + (I_L/2) = 10.75\ A \tag{10}$$

The current-limiting circuit is shown in Figure 37.

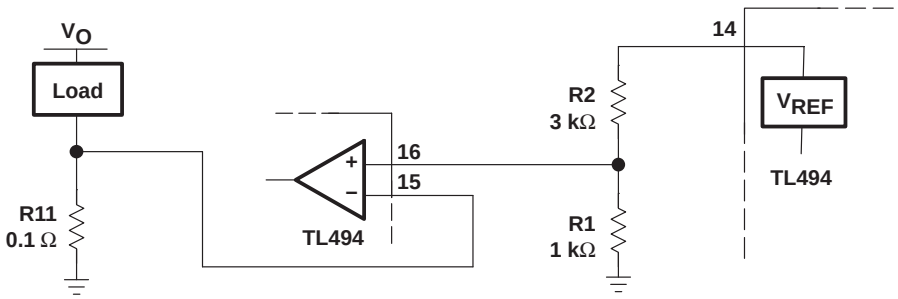


Figure 37. Current-Limiting Circuit

Resistors R1 and R2 set the reference of about 1 V on the inverting input of the current-limiting amplifier. Resistor R11, in series with the load, applies 1 V to the noninverting terminal of the current-limiting amplifier when the load current reaches 10 A. The output-pulse width is reduced accordingly. The value of R11 is:

$$R11 = 1V/10\ A = 0.1\ \Omega \tag{11}$$

Soft Start and Dead Time

To reduce stress on the switching transistors at start-up, the start-up surge that occurs as the output filter capacitor charges must be reduced. The availability of the dead-time control makes implementation of a soft-start circuit relatively simple (see Figure 38).

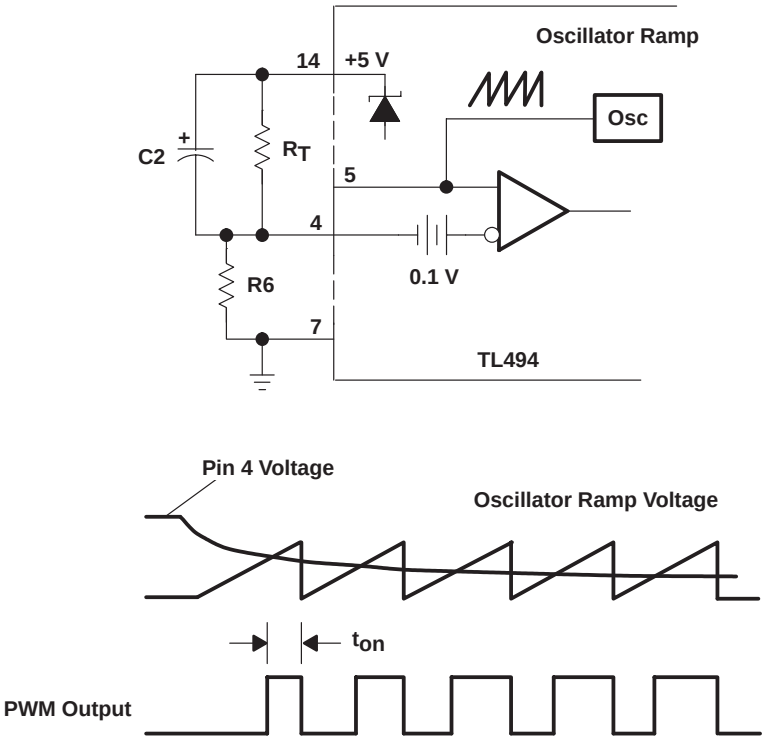


Figure 38. Soft-Start Circuit

The soft-start circuit allows the pulse width at the output to increase slowly (see Figure 38) by applying a negative slope waveform to the dead-time control input (pin 4).

Initially, capacitor C2 forces the dead-time control input to follow the 5-V regulator, which disables the outputs (100% dead time). As the capacitor charges through R6, the output pulse width slowly increases until the control loop takes command. With a resistor ratio of 1:10 for R6 and R7, the voltage at pin 4 after start-up is 0.1×5 V, or 0.5 V.

The soft-start time generally is in the range of 25 to 100 clock cycles. If 50 clock cycles at a 20-kHz switching rate is selected, the soft-start time is:

$$t = 1/f = 1/20\ kHz = 50\ \mu s\ per\ clock\ cycle \tag{12}$$

The value of the capacitor then is determined by:

$$C2 = soft{-}start\ time/R6 = (50\ \mu s \times 50\ cycles)/1\ k\Omega = 2.5\ \mu s \tag{13}$$

This helps eliminate any false signals that might be created by the control circuit as power is applied.

Inductor Calculations

The switching circuit used is shown in Figure 39.

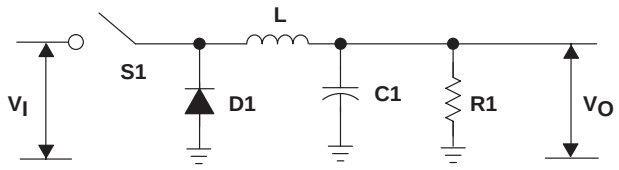


Figure 39. Switching Circuit

The size of the inductor (L) required is:

d = duty cycle = V_O/V_I = 5 V/32 V = 0.156
f = 20 kHz (design objective)
t_{on} = time on (S1 closed) = (1/f) × d = 7.8 µs
t_{off} = time off (S1 open) = (1/f) – t_{on} = 42.2 µs
L $\simeq (V_I - V_O) \times t_{on}/\Delta I_L$
$\simeq$ [(32 V – 5 V) × 7.8 µs]/1.5 A
$\simeq$ 140.4 µH

Output Capacitance Calculations

Once the filter inductor has been calculated, the value of the output filter capacitor is calculated to meet the output ripple requirements. An electrolytic capacitor can be modeled as a series connection of an inductance, a resistance, and a capacitance. To provide good filtering, the ripple frequency must be far below the frequencies at which the series inductance becomes important. So, the two components of interest are the capacitance and the effective series resistance (ESR). The maximum ESR is calculated according to the relation between the specified peak-to-peak ripple voltage and the peak-to-peak ripple current.

$$ESR(max) = \Delta V_{O(ripple)}/\Delta I_L = V/1.5\,A = 0.067\,\Omega \quad (14)$$

The minimum capacitance of C3 necessary to maintain the V_O ripple voltage at less than the 100-mV design objective was calculated according to equation 15:

$$C3 = \Delta I_L/(8f\Delta V_O) = 1.5\,A/(8 \times 20 \times 10^3 \times 0.1\,V) = 94\,\mu F \quad (15)$$

A 220-mF, 60-V capacitor is selected because it has a maximum ESR of 0.074 Ω and a maximum ripple current of 2.8 A.

Transistor Power-Switch Calculations

The transistor power switch was constructed with an NTE153 pnp drive transistor and an NTE331 npn output transistor. These two power devices were connected in a pnp hybrid Darlington circuit configuration (see Figure 40).

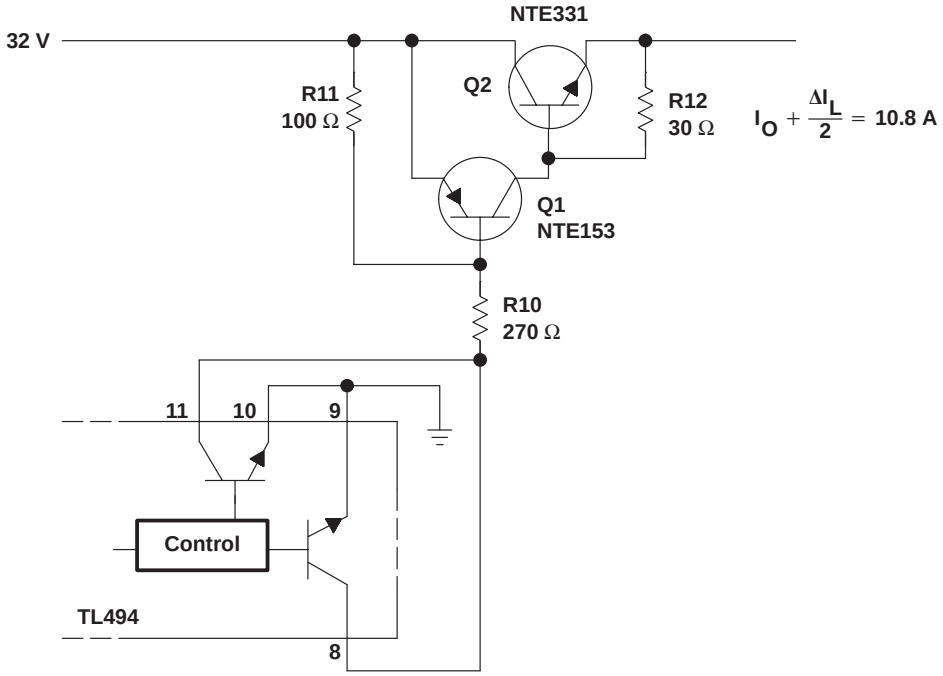


Figure 40. Power-Switch Section

The hybrid Darlington circuit must be saturated at a maximum output current of $I_O + \Delta I_L/2$ or 10.8 A. The Darlington h_{FE} at 10.8 A must be high enough not to exceed the 250-mA maximum output collector current of the TL494. Based on published NTE153 and NTE331 specifications, the required power-switch minimum drive was calculated by equations 16–18 to be 144 mA:

$$h_{FE}(Q1) \text{ at } I_C \text{ of } 3 \text{ A} = 15 \tag{16}$$

$$h_{FE}(Q2) \text{ at } I_C \text{ of } 10.0 \text{ A} = 5 \tag{17}$$

$$i_B \geq [I_O + (I_L/2)] / [h_{FE}(Q2) \times h_{FE}(Q1)] \geq 144 \text{ mA} \tag{18}$$

The value of R10 was calculated by:

$$R10 \leq \{V_I - [V_{BE}(Q1) + V_{CE}(TL494)]\}/[i_B] = [32 - (1.5 + 0.7)]/(0.144) \tag{19}$$

$$R10 \leq 207\ \Omega$$

Based on these calculations, the nearest standard resistor value of 220 Ω was selected for R10. Resistors R11 and R12 permit the discharge of carriers in switching transistors when they are turned off.

The power supply described demonstrates the flexibility of the TL494 PWM control circuit. This power-supply design demonstrates many of the power-supply control methods provided by the TL494, as well as the versatility of the control circuit.

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