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A Comprehensive Analysis of Current-Mode Control for DCM Buck-Boost Converters

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***Abstract*—Comprehensive analyses for the buck–boost, pulsewidth-modulation dc–dc converters applying peak current current-mode control are given. The analysis provides closed-form solutions for steady-state output, small-signal loop gain, and conducted susceptibility. It also proves that the state-space averaged model developed for converter using a single-loop voltage-mode control is valid for a current-mode-controlled converter.**

***Index Terms*—Conducted susceptibility, current-mode control, loop gain, sensitivity.**

I. Introduction

By nature, signals in current forms have advantages over voltage form, since voltage is an accumulation of electron flux and therefore is slow in time as far as control mechanism is concerned. This understanding spawned in the late 1970s a new tide in switch-mode power supply design, namely, the current-mode control [1]. However, by adding a current loop, the conventional concept of loop gain is blurred, since multiple loops exist and make it difficult to identify the main loop [2].

The current-mode control techniques, in addition to introducing difficulties in loop identification, also create new territories for analysis. [1] and [2] developed current programmed model using state-space averaging and resulted in a very complicated y-parameter base. Reference [3] considered current-mode control as a sort of conductance control and suggested such a converter as a current source. Reference [4] introduced the sampled-data control concept and additional gain factor that was claimed to improve theoretical loop gain prediction. Reference [5] attempted to improve the average-current current-mode model. However, given streams of studies for current-mode operation, most existing reports either did not provide a model that was easy to use or employed a mathematical procedure that produced questionable results. With this in mind and using an actual design as the base, this paper presents a complete analysis for the flyback converter in the discontinuous conduction mode (DCM) with peak-current current-mode control.

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II. Closed-Loop Steady State

A. Closed-Form Output Equation

Refer to Fig. 1(a), where the schematic of a flyback converter is shown. At steady state, that is, under constant load and constant line input, the closed-loop output is given as

$$v_O = \frac{M_{10}\cdot M_{11}\cdot\{M_8+M_9[M_6+M_7(M_3\cdot M_1+M_5)]\}}{1+M_{10}\cdot M_{11}\cdot M_9\cdot M_7(M_3\cdot M_2-M_4)}$$

$$M_1 = \left(1+\frac{R_5}{R_4}\right)A\cdot V_{\rm ref}$$

$$M_2 = \left(1+\frac{R_5}{R_4}\right)A\cdot\frac{R_2}{R_1+R_2}$$

$$M_3 = h_{FE}\frac{R_7}{-(R_7\cdot R_6+(1+h_{FE})R_8(R_7+R_6))}$$

$$M_4 = -M_3$$

$$M_5 = h_{FE}\frac{(R_7+R_6)V_{be}}{-(R_7\cdot R_6+(1+h_{FE})R_8(R_7+R_6))}$$

$$M_6 = \frac{R_9}{R_9+R_{10}+R_{11}}V_r$$

$$M_7 = \frac{R_9(R_{11}+R_{10})}{R_9+R_{10}+R_{11}}$$

$$M_8 = \frac{1}{3}\left[\left(1+\frac{R_{12}}{R_{11}+R_{10}}\right)V_r - 2\cdot V_D\right]$$

$$M_9 = -\frac{1}{3}\cdot\frac{R_{12}}{R_{11}+R_{10}}$$

$$M_{10} = \frac{n\cdot L_p\cdot f_s}{V_b\cdot R_{13}}$$

$$M_{11} = \frac{N_s\cdot V_{\rm bus}}{N_p}\sqrt{\frac{R}{2\cdot L_s\cdot f_s}}.$$

The power stage gain M_{11} is given in [6] and [7].

B. Output Sensitivity

The closed-form solution gives designers the ability to evaluate many performance merits of a design analytically and numerically. Among them, load regulation, line regulation, and component sensitivities are the three most sought after figures. For instance, the load regulation sensitivity can be expressed as

$$S_R = \frac{\partial v_o}{\partial M_{11}}\frac{\partial M_{11}}{\partial R}.$$

III. AC Loop Gain

In order to study the small-signal behavior of the converter, the schematic of Fig. 1(a) is transformed into Fig. 1(b) in which the transfer functions of individual blocks are identified and derived as follows.

The first error amplifier gives

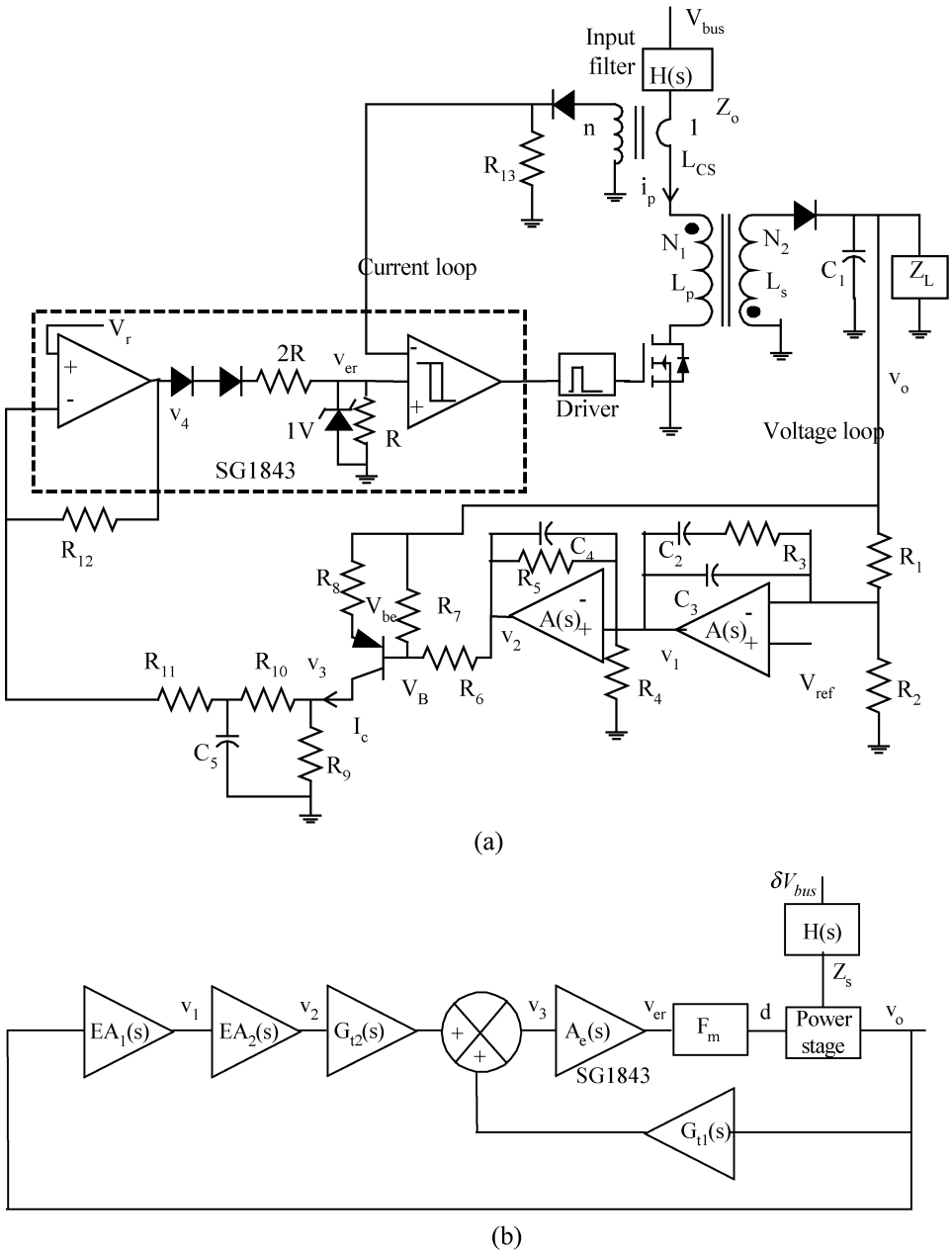
$$EA_1(s) = -\frac{R_2}{R_1+R_2}\cdot\frac{A(s)}{R_p\left[\frac{1}{R_p}+\frac{1+A(s)}{Z_{f1}(s)}\right]}$$

where $\mathrm{R_p} = \mathrm{R1//R2}$ and

$$A(s) = \frac{A}{\left(\frac{s}{2\cdot\pi\cdot f_p}+1\right)}.$$

The second-stage error amplifier gives

$$EA_2(s) = \frac{v_2}{v_1} = A(s)\left[1-\frac{A(s)}{Z_{f2}(s)\cdot\left(\frac{1+A(s)}{Z_{f2}(s)}+\frac{1}{R_4}\right)}\right].$$



(a)

(b)

Fig. 1. (a) Circuit schematic. (b) Small-signal block diagram.

The transistor stage gains are

$$G_{t1}(s) = \frac{\begin{vmatrix} \frac{1+h_f}{h_i} & -\left(\frac{1}{R_8}+\frac{1+h_f}{h_i}\right) \\ \frac{h_f}{h_i} & -\frac{h_f}{h_i} \end{vmatrix} \frac{1}{R_7} + \begin{vmatrix} \frac{1}{R_6}+\frac{1}{R_7}+\frac{1}{h_i} & \frac{-11}{h_i} \\ \frac{h_f}{h_i} & -\frac{h_f}{h_i} \end{vmatrix} \frac{1}{R_8}}{D_e}$$

$$G_{t2}(s) = \frac{\begin{vmatrix} \frac{1+h_f}{h_i} & -\left(\frac{1}{R_8}+\frac{1+h_f}{h_i}\right) \\ \frac{h_f}{h_i} & -\frac{h_f}{h_i} \end{vmatrix} \frac{1}{R_6}}{D_e}$$

$$D_e = \begin{vmatrix} \frac{1}{R_6}+\frac{1}{R_7}+\frac{1}{h_i} & \frac{-1}{h_i} & 0 \\ \frac{1+h_f}{h_i} & -\left(\frac{1}{R_8}+\frac{1+h_f}{h_i}\right) & 0 \\ \frac{h_f}{h_i} & -\frac{h_f}{h_i} & \frac{1}{Z_c(s)} \end{vmatrix}$$

$$A_e(s) = -\frac{1}{3}\cdot\frac{R_{12}}{R_{11}+\left(\frac{1}{R_{10}}+C_5\cdot s\right)^{-1}}\cdot\frac{(C_5\cdot s)^{-1}}{R_{10}+(C_5\cdot s)^{-1}}.$$

The PWM gain is

$$F_m = \frac{\partial D}{\partial v_{er}} = \frac{L_p\cdot f_s\cdot n}{R_s\cdot V_B} \quad F_v = \frac{\partial D}{\partial V_B} = \frac{-L_p\cdot f_s\cdot n\cdot V_{er}}{R_s\cdot V_B^2}.$$

By invoking the canonical model given in [6] and [7], the power stage duty-cycle-to-output transfer function can be shown to be

$$G_p(s) = \left[1 - g_2\frac{j_1}{j_2}\frac{r_1\cdot Z_s(s)}{r_1+Z_s(s)}\right]\frac{j_2}{\frac{1}{Z_L(s)}+\frac{1}{r_2}+C_1\cdot s}.$$

The loop gain is finally given as

$$T(s) = \frac{EA_1(s)\cdot EA_2\cdot G_{t2}(s)\cdot A_e(s)\cdot F_m\cdot G_{vd}(s)}{1-G_{t1}(s)\cdot A_e(s)\cdot F_m\cdot G_{vd}(s)}.$$

The theoretical loop gain as shown in Fig. 2(a) compares extremely well against the actual measurement of Fig. 2(b).

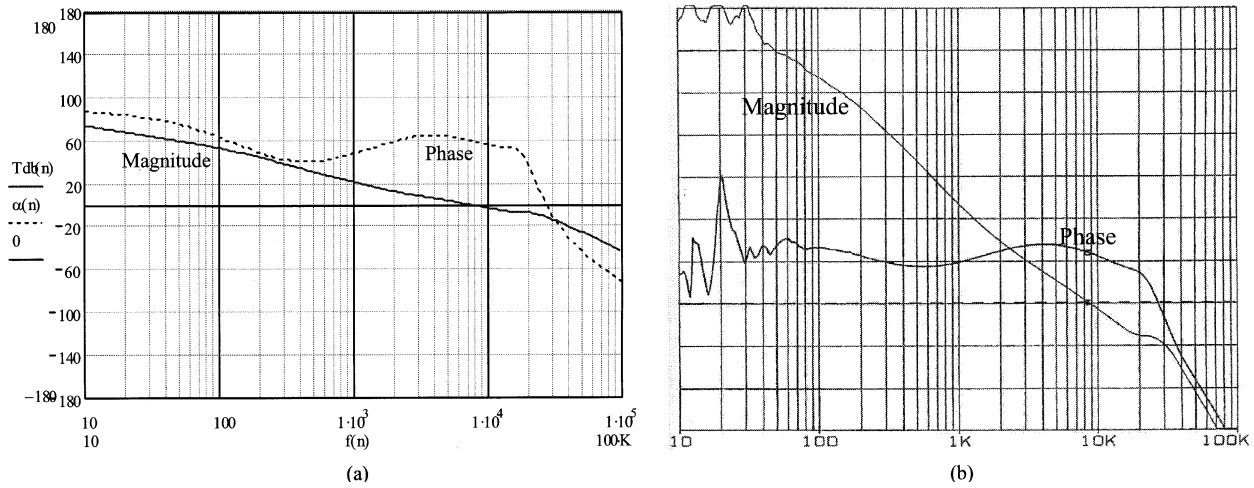


Fig. 2. Loop gain. (a) Theoretical. (b) Measurement 10 dB/div, 45°/div.

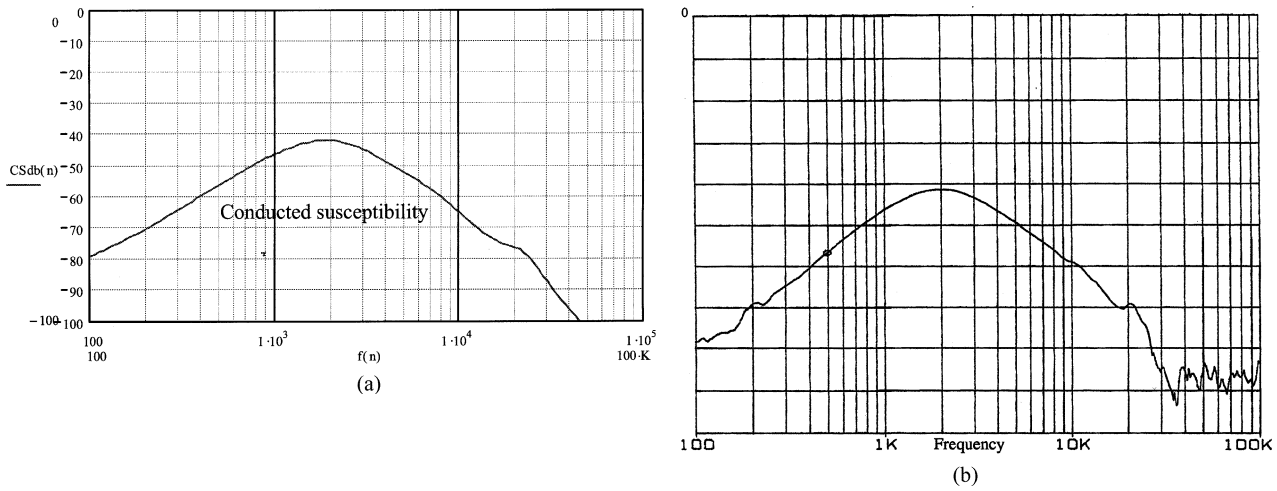


Fig. 3. Conducted susceptibility. (a) Theoretical. (b) Measurement. −10 dB/div.

IV. Conducted Susceptibility

By including the feedforward effect, a different loop gain is given

$$T_{CS}(s) = [EA_1(s) \cdot EA_2(s) \cdot G_{t2}(s) + G_{t1}(s)] \cdot A_e(s) \cdot F_m \cdot G_p(s).$$

The conducted susceptibility is then expressed as

$$CS(s) = \frac{\frac{N_2}{N_1} H(s) \left[\frac{r_1}{Z_s(s)+r_1} \frac{g_2}{\frac{1}{Z_L(s)}+\frac{1}{r_2}+C_1 \cdot s} + F_v \cdot G_p(s) \right]}{1 - T_{CS}(s)}.$$

The theoretical conducted susceptibility Fig. 3(a) matches well the actual measurement, Fig. 3(b).

V. Conclusion

A complete analysis was given for the flyback dc–dc converter with peak-current current-mode control. The power stage transfer functions are derived based on the voltage-mode canonical model given in [6]. However, combinational effects of voltage-loop feedback (F_m) and current-loop feedforward (F_v) make the model valid for the current-mode control. A superb match between the analytical results and the actual measurements supports the viewpoint.

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