A New Flyback Converter with Primary Side Detection and Peak Current Mode Control

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Abstract: A new cycle-by-cycle control flyback converter with primary side detection and peak current mode control is proposed and its dynamic characteristics are analyzed. The control circuit is verified by using the OrCAD simulation. The circuit is suitable for digital control implementation.

Keywords: Flyback converter, Peak current mode, Primary side detection

I. Introduction

A conventional switch-mode power supply with galvanic isolation is provided by an opto-coupler, signal transformer or capacitor for the feedback voltage path. Signal transformer or capacitor isolation schemes complicate the circuit, and opto-coupler is hardly operated at high temperature and radiate environment.

However, the output voltage also exists across the primary side switch when in its off state and all the necessary information for control is available from the primary switch voltage. Previous attempts at implementing primary side control were impeded by the performance and bandwidth of the components available [1]. The other attempts are that the output voltage was extracted within on-switching-cycle and a flyback converter with a cycle-by-cycle control was developed [2]. Because the on-time is not the linear function of input voltage in this control circuit, it needs a complex fast analog multiplier for calculation and three sawtooth waveform generators. In this paper, a new flyback converter with primary side detection and current limiting mode control is proposed, and it is suitable for cycle-by-cycle control.

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II. Circuit and Operation Principe

The flyback converter circuit is shown in Fig .1. The desired information is available from the primary switch voltage, V_{sw}, during the off-time in continuous conduction mode (CCM)

$$V_{sw} = V_{in} + (V_o + V_F)\frac{N_P}{N_s} \qquad (1)$$

Where: V_{in} is the input voltage, V_o is the output voltage, V_F is the forward voltage drop of the output diode, N_P/N_s is the flyback transformer turns ratio. The relationship between V_o and the peak of V_{sw} for both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is also given in Eq.1.So a peak detector is used in circuit for calculate the V_o at the beginning of off-time when the V_{sw} reaches its the highest point. However the initial spike on V_{sw} will be neglected when the V_{sw} is being detected.

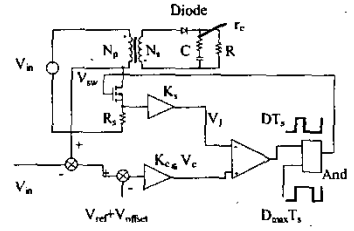

Fig.1 The flyback converter with primary signal detected and peak current control.

The value of V_{sw} must be hold for the complete off-time and a regulation error signal V_E is calculated from output voltage Vo and the reference voltage V_{ref}. In the ideal case V_E is zero. In this case the on-time will be calculated according to the offset voltage, V_{offset}. The reference voltage for current control, V_c is given by:

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$$V_c = (V_{ref} + V_{offset}) - \left[(V_{sw} + V_{in}) \frac{N_s}{N_p} - V_F \right] \quad (2)$$

On the constant voltage control mode, V_{offset} is the nonlinear function of V_{in}, so the control circuit operated and the constant voltage control mode need a fast analog multiplier for solve this problem. But when control circuits operate under peak current control mode, V_c is independence with the V_{in}. When V_c is constant, the limiting current is constant. From the energy point of views, the winding energy storage in on-time of one cycle is constant, even if the V_{in} is variety [3].

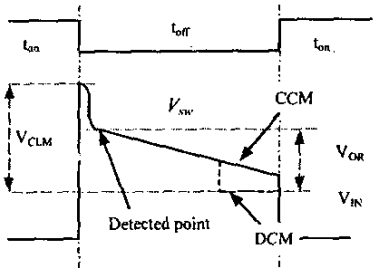

Fig.2 Solution for output voltage detected from V_{sw} waveform for CCM and DCM

The inductor current can be detected from the current sense resistor (R_s) during on-time. The waveform of the inductor current in the peak current control mode for CCM and DCM conditions are shown in Fig.3. The m_1 and m_2 are the rising and falling slopes (with units of volts per second) of the inductor sensed current waveform scaled by R_s. The m_1 for both CCM and DCM is same, and it is given by

$$m_1 = \frac{V_{in}}{L} R_s \quad (3)$$

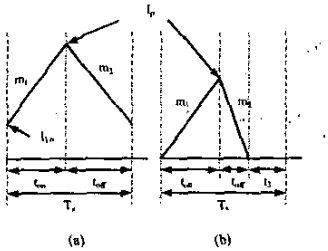

Fig.3 The inductor current in peak current mode control (a) CCM, (b)DCM

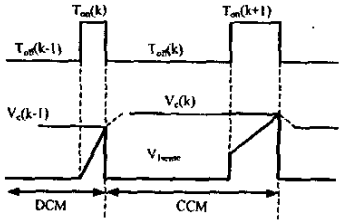

Fig.4 The calculated on-time be for next cycle at CCM and DCM condition.

The output of the peak current detector V_I by the gain of K_s is fed to a comparator, where it is compared with the V_c. The result of the comparison is the nest cycle on-time, and it was shown in Fig.4. In the peak current mode control, duty cycle expressions in CCM and DCM are different. The duty cycle can be calculated as:

$$D = \begin{cases} \dfrac{V_c - I_L R_s}{T_s \dfrac{R_s K_s V_{in}}{2L}} & for \quad CCM \\ \dfrac{V_c}{T_s \dfrac{R_s K_s V_{in}}{L}} & for \quad DCM \end{cases} \quad (4)$$

where: K_s is the gain of current signal amplifier. I_L is average current on primary inductor. T_s is the cycle time. The maximum turn-on time is also has been used by $D_{max}T_s$, shown in Fig.1, to avoid the switch in on-time for longer time.

III. Analysis and Simulation Results

A. dc and small-signal circuit models of the flyback converter

From the steady-state analysis, the dc voltage transfer function of idealized switching part of converter given as.

$$M_v = \frac{V_o}{V_s} = \frac{D}{n(1 - D - \Delta)} \quad (5)$$

Where V_s is the input voltage and $\Delta = t_3/T_s$. When the Δ equates zero, the converter operates on CCM mode. When $\Delta > 0$, it operates on DCM mode.

B. Small-signal characteristics

The small-signal dynamic characteristics of the flyback converter can be derived using the small-signal model. The close-loop transfer function in this converter is:

$$G_{CL}=\frac{G_c(s)G_p(s)G_s(s)}{1+G_c(s)G_p(s)G_s(s)} \qquad (6)$$

where $G_c(s)$ is the error control transfer function, which is decided by error amplifier. $G_p(s)$ and $G_s(s)$ are the PWM transfer function and the transfer function of the flyback converter respectively.

The transfer function $G_p(s)$ is:

$$G_p(s)=\frac{\hat{d}(s)}{\hat{v}_c(s)}=\begin{cases}\dfrac{L}{T_s R_s K_s V_{in}} & for\ \ DCM\\ \dfrac{2L}{T_s R_s K_s V_{in}} & for\ \ CCM\end{cases} \qquad (7)$$

The duty ratio-to output transfer function on CCM in the s-domain is

$$G_s(s)=\frac{\hat{v}_o(s)}{\hat{d}(s)}$$
$$=-\frac{V_o r_c}{[n(1-D)+D](1-D)(R+r_c)}\cdot\frac{(s+\omega_{rc})(s+\omega_{rl})}{s^2+2\xi_l\omega_l s+\omega_l^2} \qquad (8)$$

where:

$$\omega_{tc}=\frac{1}{Cr_c}$$

$$\omega_{rl}=-\frac{1}{L}\left[\frac{n^2(1-D)^2R}{D^2}-1\right]$$

$$\xi_l=\frac{C\left\{\dfrac{n^2(1-D)^2Rr_c}{D[n(1-D)+D]}\right\}}{2\sqrt{LC(R+r_c)\left\{\dfrac{n^2(1-D)^2R}{D[n(1-D)+D]}\right\}}}$$

$$\omega_l=\sqrt{\frac{\dfrac{n^2(1-D)^2R}{D[n(1-D)+D]}}{LC(R+r_c)}}$$

where the forward resistance of diode, transistor on resistance, winding resistance of the primary and secondary of transformer and magnetic core series resistance have been neglected.

C. Simulation Results

A flyback converter in this paper is verified by using OrCAD simulation software. The specification of the converter for the evaluation is as follows: V_{in}=310V, T_s=10μs, L=1.6mH, C=100μ, V_o=3.5V.

A Sample-Hold (S/H) circuit has been used to detect the peak switch voltage of the primary side. During each cycle, a clear control signal reset the S/H circuit at first, then a S/H control signal enable the S/H circuit to sample the primary side switch voltage at fixed time, for avoiding the spike of voltage. The clear control, S/H control and switch control signal are shown in Fig.5.

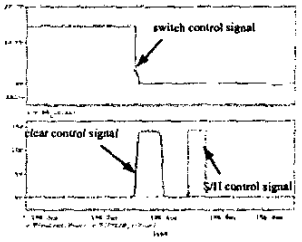

Fig.5 Clear control, S/H control and switch control signal

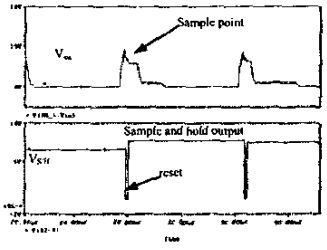

Fig.6 V_{sw} and S/H output of peak detector waveforms on DCM condition.

The V_{sw} and output of S/H circuit are shown in Fig.6. The output voltage of S/H circuit will be hold and used to calculate next cycle on-time until the switch turn off in next cycle.

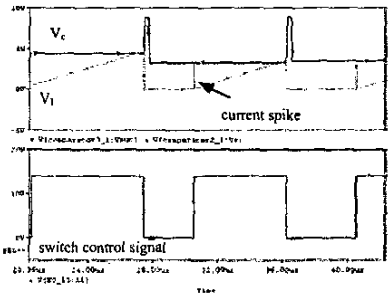

Fig.7 V_1, V_{1Limit} and the switch control signal waveforms.

The error voltage gain for the prototype is K_c= 12. The offset voltage, $V_{offset}+V_{ref}$=10V, is chosen to provide the correct on-time. The V_c and V_1 waveform fed to a comparator are shown in Fig.7. At the beginning of the turn on, a spike current occurs on switch so the spike of current should not be compared with V_c to avoid wrong

comperating results.

The output of the regulator is shown in Fig.8. Due to existence of cycle-by-cycle peak current mode control loop, the output voltage can be rapidly regulated when the load change.

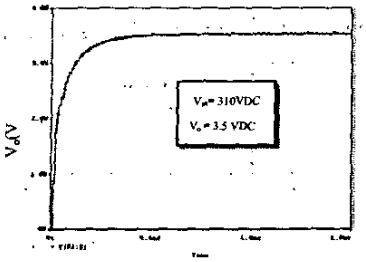

Fig.8 The output voltage of the flyback converter

The output voltage ripple of this flyback converter is shown in Fig.9.The maximum output voltage ripple, at full load in steady-state condition, is around 32.917mV(1%).

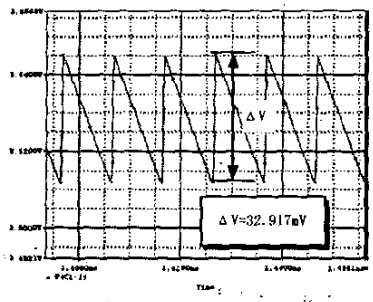

Fig.9 The output voltage Ripple, V_o=3.5V

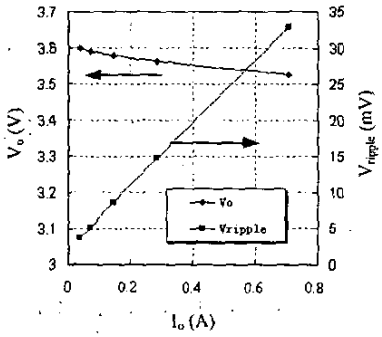

Fig.10 Load regulation and voltage ripple curve for steady state load

The load regulation and voltage ripple curve for steady state load is shown in Fig.10. When load current change from 200mA to 700mA, the output voltage variation is around 800mV, and output voltage ripple increase from 4mV to 35mV. The main advantages of this converter over the convential one are simplicity, size and rapidly regulating. Furthermore because peak current mode control can supplies constant energy when the V_{Ilimit} is constant, this fact allows the use of this converter in wide input voltage range application. This control mode and error voltage detection method can also be used in others known topologies such as forward isolation converter.

IV. Conclusion

A primary side detection method and peak current mode control is applied to an isolated flyback converter without sensing control signals over the isolation barrier. The new control circuit provides cycle-by-cycle control of the flyback converter in CCM and DCM conditions. The dynamic characteristics are analyzed in this paper. The control circuit is verified by using the OrCAD simulation. The circuit is suitable for digital control implementation.

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