SLVP088 20 V to 40 V Adjustable Boost Converter Evaluation Module User's Guide

IMPORTANT NOTICE

Preface

Read This First

About This Manual

This user's guide is a reference manual for the SLVP088 20 V to 40 V Adjustable Boost Converter Evaluation Module. This document provides information to assist managers and hardware engineers in application development.

How to Use This Manual

This manual provides the information and instructions necessary to design, construct, operate, and understand the SLVP088. Chapter 1 describes and lists the hardware requirements; Chapter 2 describes design considerations and procedures; and Appendix A contains the data sheet for the TL5001 Pulse-Width-Modulation Controller.

Related Documentation From Texas Instruments

The following books describe the TL5001 and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924. When ordering, please identify the book by its title and literature number.

TL5001 Pulse-Width-Modulation Control Circuits Data Sheet (Literature number SLVS084C) is included in Appendix A of this book. It contains electrical specifications, available temperature options, general overview of the device, and application information.

Designing with the TL5001C PWM Controller Application Report (Literature number SLVA034).

Examples of Application with the Pulse Width Modulator TL5001 (Literature number SLVAE05).

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Chapter 1

Hardware

The SLVP088 20 V to 40 V Adjustable Boost Converter Evaluation Module (SLVP088) provides a method for evaluating the performance of the TL5001 Pulse-Width-Modulation Controller (TL5001). The TL5001 uses pulse-width-modulation (PWM) circuits to control a switch-mode power supply in a voltage-mode configuration. This manual explains how to construct basic power conversion circuits, including the design of control circuits and basic power stage components. This chapter includes the following topics:

Topic **Page**

1.1 Introduction

The SLVP088 supplies a constant dc output voltage that is adjustable from 20 V to 40 V. The SLVP088 can supply output power from no load to 2 W. Using a dc input voltage of 4.5 V to 7 V, full load efficiency varies from 73 percent to 86 percent depending on input voltage and output voltage.

The SLVP088 is a boost converter, also known as a step-up converter. This type of converter converts an unregulated input voltage to a regulated output voltage that is always higher than the input voltage.

The control method used in the SLVP088 is fixed frequency, variable on-time pulse-width-modulation. The feedback method used is voltage-mode control. Other features of the SLVP088 include undervoltage lockout (UVLO), short-circuit protection (SCP), and soft-start.

CAUTION

Short circuit protection

Short circuit protection protects against short circuits only. If the output load current is increased beyond the rated value, damage may occur to the power supply. Short circuit protection does not imply overload protection. This EVM shuts down when a short circuit is encountered. Input power must be recycled to restart the module.

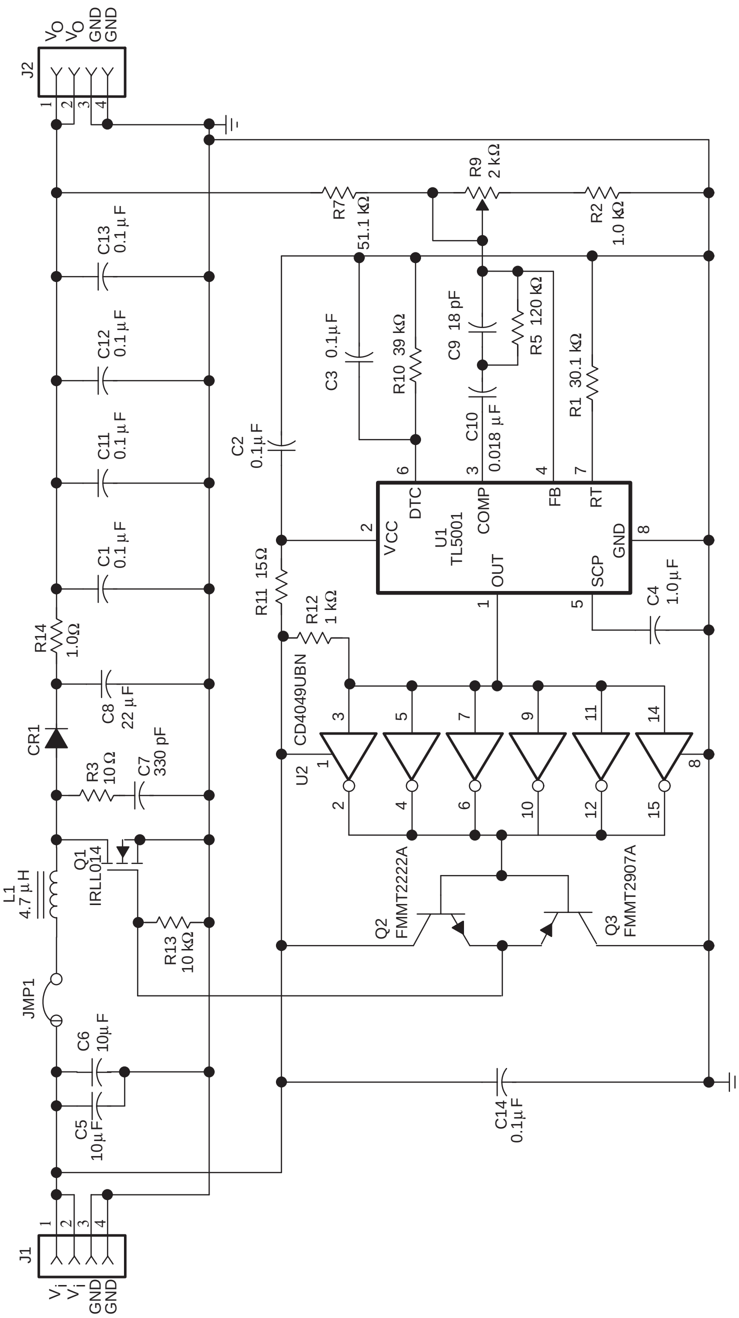
1.2 Schematic

Figure 1–1 shows the schematic diagram for the SLVP088.

The TL5001 (U1) incorporates all functions required for a PWM control circuit. The TL5001 contains an error amplifier, a reference regulator, an oscillator, a PWM comparator with a dead-time-control input, a UVLO circuit, an SCP circuit, and an open-collector output transistor. For a complete description and operational details of the TL5001, see the data sheet in Appendix A.

The power components consist of L1, Q1, CR1, and C8. Power is transferred from the input to the output by turning on the main switch, Q1, and storing energy in L1. When Q1 is turned off, L1 delivers the stored energy to the load and output filter capacitance through CR1. The main switch is turned on and off at the converter switching frequency. The control circuit adjusts the duty cycle (the ratio of switch on-time to total switching period) to regulate the output voltage to the desired value.

Figure 1–1. SLVP088 Schematic Diagram



Notes:

1) Output voltage is set by adjusting R9
2) This unit and the components are thermally rated to 2 W output power. The output power should not exceed 2 W unless proper thermal management is put in place.
3) Switching frequency is set to 250 kHz by R1. See TL5001 Data Sheet, literature number SLVS084C for design equations.

1.3 Test Setup

Do the following steps for initial power-up of the SLVP088:

1) This EVM output voltage is adjustable with a potentiometer, R9. For initial power-up, adjust R9 for approximately the mid-point. This produces an output voltage of approximately 30 V.

2) Connect an electronic load adjusted to draw approximately 50 mA at 30 V. The exact current is not critical; any nominal current is sufficient. A fixed resistor can also be used in place of the electronic load. The output current drawn by the resistor is $I_O = \frac{V_O}{R}$ where R is the value of the load resistor. The power rating if the resistor, P_R, should be at least $P_R = \frac{V_O^2}{R} \times 2$.

3) Connect a lab power supply to the input of the SLVP088. Make sure that the current limit is set for at least 0.5 A. Turn the voltage up to 5 V.

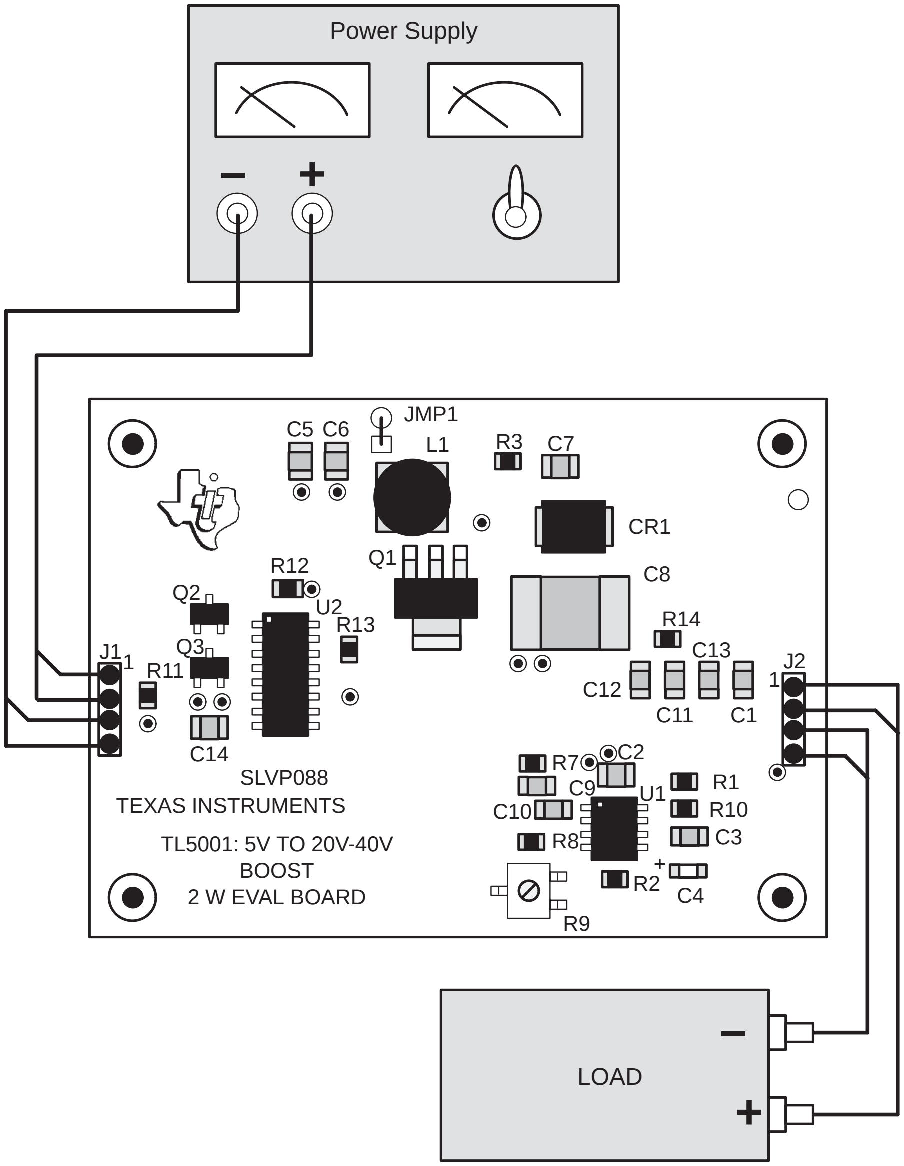
4) Verify that the SLVP088 output voltage is approximately 30 V.

5) For subsequent testing, make sure the lab supply output current capacity and current limit are at least 2 A, so that the SLVP088 can be operated at a maximum load of 2 W.

6) Refer to section 1.6 for selected typical waveforms and operating conditions for verification of proper module operation.

Figure 1–2 shows the test setup for the SLVP088.

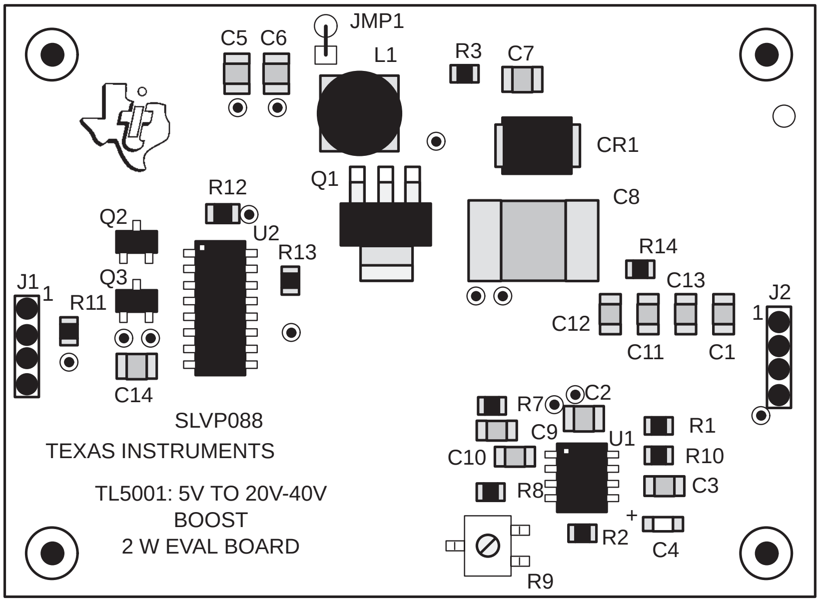
Figure 1–2. Test Setup



1.4 Board Layout

Figure 1–3 shows the board layout for the SLVP088.

Figure 1–3. Board Layout



1.5 Bill of Materials

Table 1–1 lists materials required for the SLVP088.

Table 1–1. Bill of Materials

Qty	Reference	Part Number	Mfr	Description
1	CR1	SS16	GI	Diode, Schottky, 1 A, 60 V, DO–214AC
7	C1, C2, C3, C11, C12, C13, C14	Standard		Capacitor, 0.1 μF, 10%, X7R, 1206
1	C4	ECS–T1CY105R	Panasonic	Capacitor, Tant, 1.0 μF, 20%, A-Case
2	C5, C6	C3225Y5V1C106Z	TDK	Capacitor, 10 μF, 10 V, Z5U, 1210
1	C7	Standard		Capacitor, 330 pF, NPO, 5%, 0805
1	C8	THCR70E1H226ZT	Marcon	Capacitor, 22 μF, 50 V, Z5U, .3”×.252”
1	C9	Standard		Capacitor, 18 pF, NPO, 5%, 0805
1	C10	Standard		Capacitor, 0.018 μF, X7R, 10%, 0805
2	J1, J2	TSW-104-14-G-S	Samtec	Connector, 4-pin header, 25 Mil, 0.1” Sp. Gold
1	L1	CD43-4R7MC	Sumida	Inductor, 4.7 μH, 20%, 0.094 Ω, 1.7 A
1	Q1	IRLL014	I.R.	Transistor, N-CH, 60 V, 0.2 Ω, 2.7 A, SOT-223
1	Q2	FMMT2222ACT	Zetex	Transistor, NPN, 40 V, 0.8 A, SOT-23
1	Q3	FMMT2907ACT	Zetex	Transistor, PNP, 60 V, 0.8 A, SOT-23
1	R1	Standard		Resistor, 30.1 kΩ, 1%, 0805
1	R2	Standard		Resistor, 1.00 kΩ, 1%, 0805
1	R3	Standard		Resistor, 10 Ω, 5%, 0805
1	R7	Standard		Resistor, 51.1 kΩ, 1%, 0805
1	R8	Standard		Resistor, 120 kΩ, 5%, 0805
1	R9	ST4B202CT		Resistor, variable, 2 kΩ, 20%, Cermet
1	R10	Standard		Resistor, 39 kΩ, 5%, 0805
1	R11	Standard		Resistor, 15 Ω, 5%, 0805
1	R12	Standard		Resistor, 1.0 kΩ, 5%, 0805
1	R13	Standard		Resistor, 10 kΩ, 5%, 0805
1	U1	TL5001CD	TI	IC, PWM, SO-8
1	U2	CD4049UBM	National	IC, CMOS hex inverter, SO-16
1		SLVP088		PWB

1.6 Test Results

Figures 1–4 through 1–13 and Tables 1–2 and 1–3, show the test results for the SLVP088.

Figure 1–4. Output Voltage Ripple

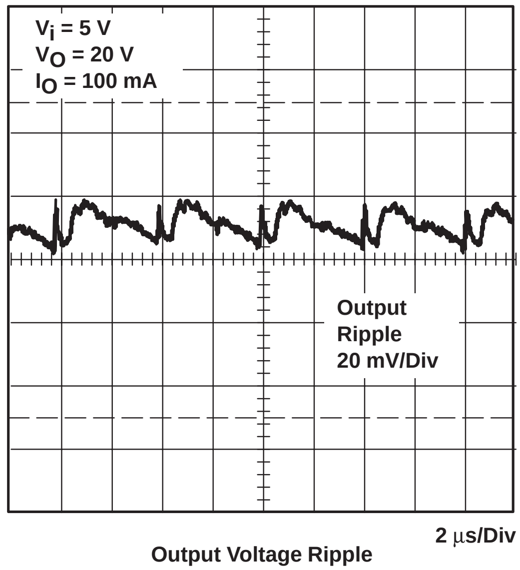


Figure 1–5. Output Voltage Ripple

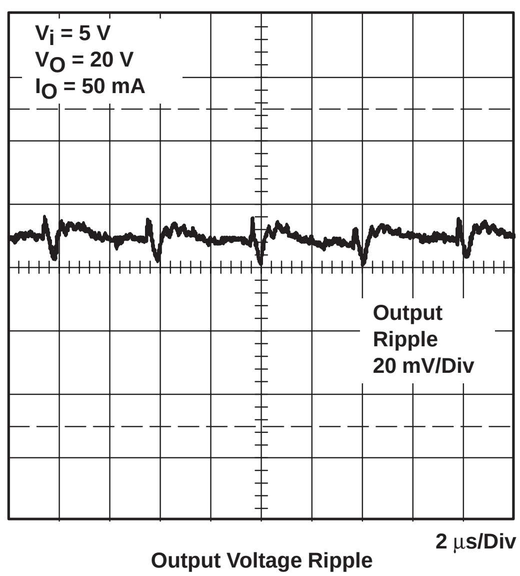
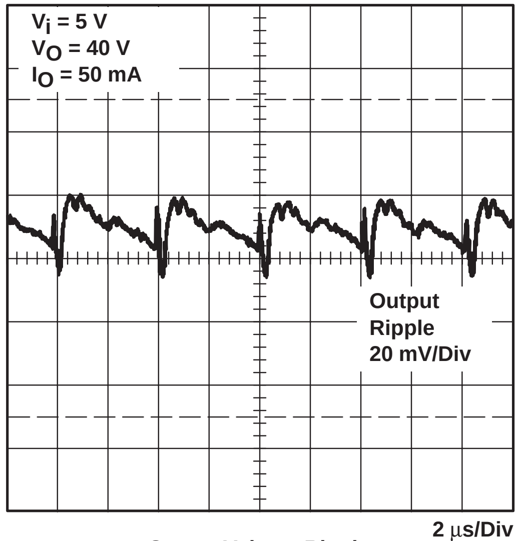
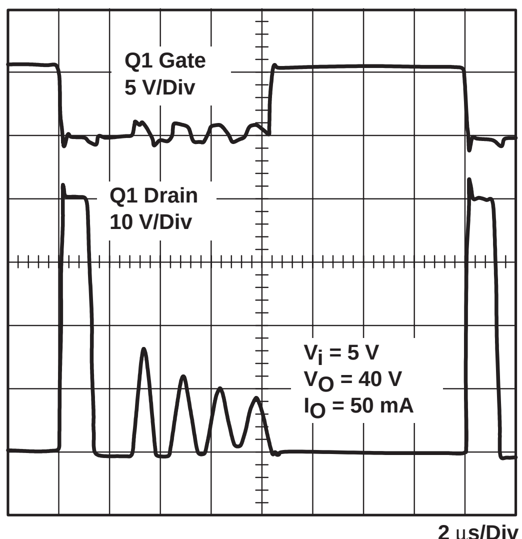


Figure 1–6. Output Voltage Ripple



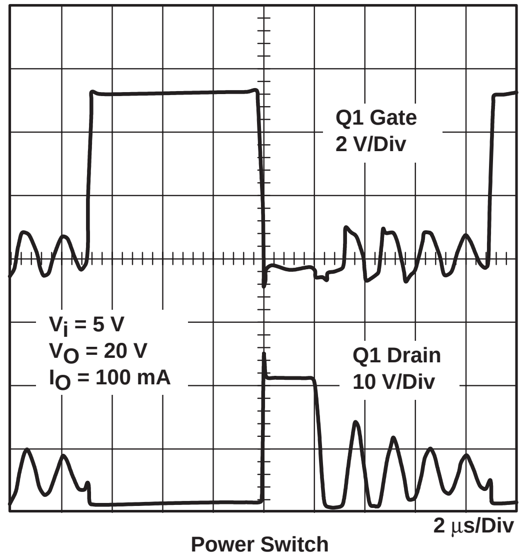
Output Voltage Ripple

Figure 1–7. Power Switch Drain Voltage and Gate Voltage



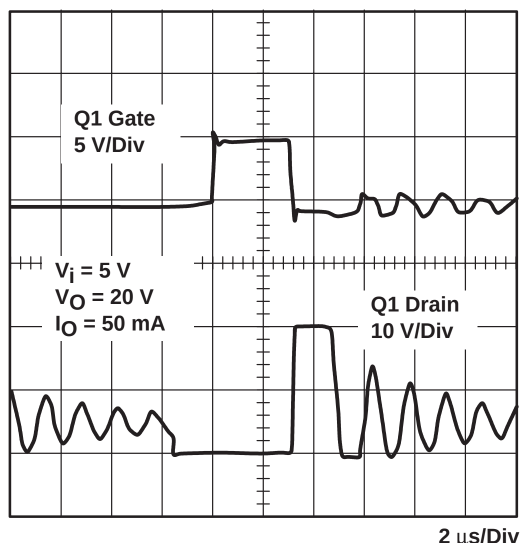
Power Switch
Drain Voltage and Gate Voltage

Figure 1–8. Power Switch Drain Voltage and Gate Voltage



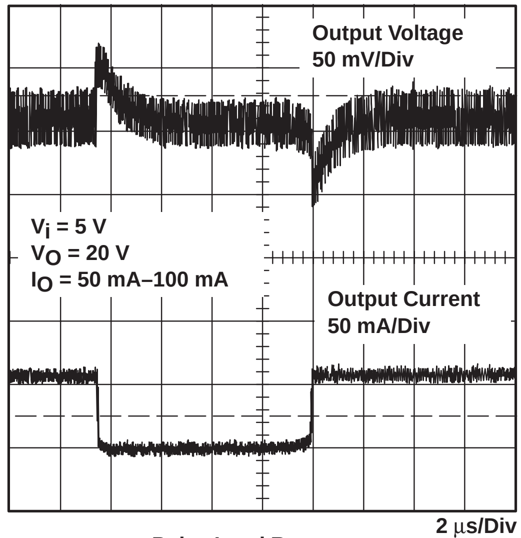
Power Switch
Drain Voltage and Gate Voltage

Figure 1–9. Power Switch Drain Voltage and Gate Voltage



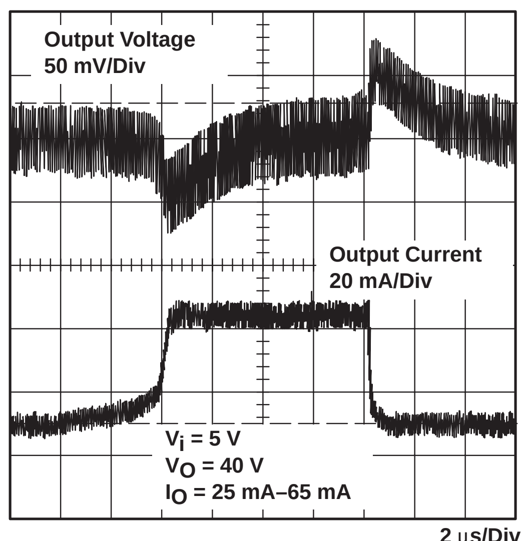
Power Switch
Drain Voltage and Gate Voltage

Figure 1–10. Pulse Load Response 50 mA to 100 mA



Pulse Load Response
50 mA to 100 mA

Figure 1–11. Pulse Load Response 25 mA to 65 mA



Pulse Load Response
25 mA to 65 mA

Figure 1–12. Efficiency vs Load 20-V Output

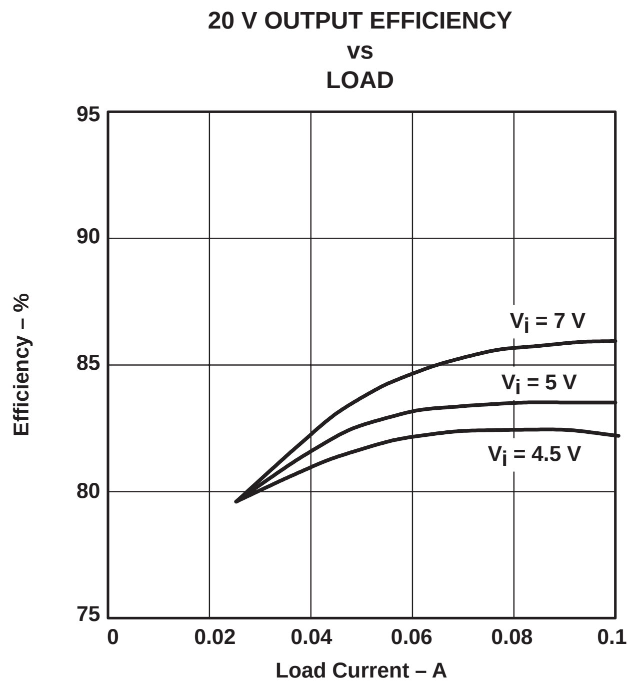


Figure 1–13. Efficiency vs Load 40-V Output

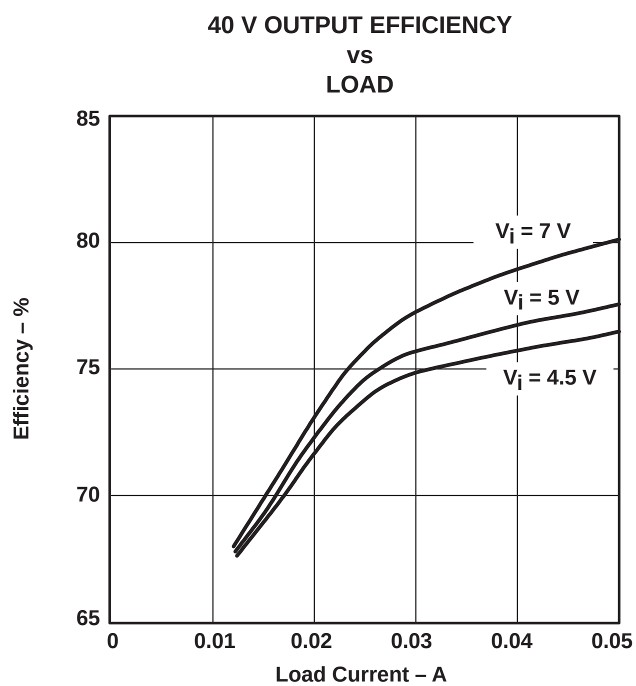


Table 1–2. Line/Load Regulation, 20 V

Line/Load	12.5 mA	25 mA	37.5 mA	50 mA	Load Reg.
4.5 V Vo(V)	20.010	20.010	20.010	20.010	0.00%
5.0 V Vo(V)	20.010	20.010	20.010	20.010	0.00%
5.5 V Vo(V)	20.010	20.010	20.010	20.010	0.00%
6.0 V Vo(V)	20.010	20.010	20.010	20.010	0.00%
6.5 V Vo(V)	20.010	20.010	20.010	20.010	0.00%
7.0 V Vo(V)	20.010	20.010	20.010	20.010	0.00%
Line Reg.	0.00%	0.00%	0.00%	0.00%	

Table 1–3. Line/Load Regulation, 40 V

Line/Load	12.5 mA	25 mA	37.5 mA	50 mA	Load Reg.
4.5 V Vo(V)	40.070	40.070	40.070	40.070	0.00%
5.0 V Vo(V)	40.070	40.080	40.080	40.070	0.02%
5.5 V Vo(V)	40.080	40.080	40.070	40.070	0.02%
6.0 V Vo(V)	40.080	40.080	40.080	40.070	0.02%
6.5 V Vo(V)	40.080	40.080	40.080	40.080	0.00%
7.0V Vo(V)	40.080	40.080	40.080	40.080	0.00%
Line Reg.	0.02%	0.02%	0.02%	0.02%	

Chapter 2

Design Procedure

There are many ways to design power supplies. This chapter shows the procedure and equations used in designing the SLVP088. Besides verifying the SLVP088 design, the equations can also be used to design circuits with different output voltages and/or different output power capacities. The chapter includes the following topics:

Topic **Page**

2.1 Introduction

The SLVP088 is a dc-to-dc step-up (boost) converter module that provides a constant dc output voltage that is adjustable from 20 V to 40 V. The module provides up to 100 mA at 20 V out, or up to 50 mA at 40 V out. The controller IC is a TL5001.

2.2 Operating Specifications

Table 2–1 lists the operating specifications for the SLVP088.

Table 2–1. Operating Specifications

Specification	Min	Typ	Max	Units
Input Voltage Range	4.5	5	7	V
Output Voltage Range	20	N/A	40	V
Output Power Range	0	N/A	2	W
Output Current Range	0	N/A	100†	mA
Operating Frequency		250		kHz
Output Ripple			50	mV
Efficiency‡	73	80	86	%

† Maximum output current when the output voltage is adjusted to 20 V.
‡ This is for loads of at least 1 W.

2.3 Design Procedures

This section describes the steps to design a discontinuous-mode boost converter. Example calculations accompany the design equations. Since this is an adjustable output converter, all example calculations apply to the converter with output voltage adjusted to 20 V and input voltage set to 5 V, unless specified otherwise. The first two quantities to be determined are the converter switching frequency and the boost inductor value.

2.3.1 Converter Switching Frequency

For relatively low output power converters such as this, the switching frequency should be chosen as high as practical to minimize the size and weight of the converter. A switching frequency of 250 kHz was chosen. The high switching frequency is possible in part because of the small size required for the main switch, Q1, and the ability to use a Schottky rectifier for CR1. A low-power MOSFET implies that the junction capacitances are small, which allows fast switching without large peak currents to charge and discharge the capacitances. For lower frequencies, the size of boost inductor L1 and main output capacitor C8 increase. For higher frequencies, switching losses become significant compared to the output power level, and losses represent extra heat that must be removed from the module.

2.3.2 Boost Inductor Selection

The boost inductor, converter switching frequency, input and output voltages, and output power determine a boost converter’s operating mode. This converter operates in the discontinuous-conduction mode (discontinuous mode). In discontinuous mode, the current in the inductor starts at zero current and returns to zero current in each switching cycle. To keep the converter in discontinuous mode, the inductor must be less than a computed maximum value. However, for a specified output power level, the smaller the inductance, the higher the peak and rms current in Q1 and CR1. Therefore, the value of inductance is not critical and can be left to the discretion of the designer.

Discontinuous mode is desirable because the power-stage frequency response is well behaved, being comprised of a dc gain and a single pole. Continuous-mode boost converters on the other hand, have a dc gain, a complex pole pair, and a right-half-plane zero, making feedback loop stabilization difficult.

As a starting point, define M as the converter voltage gain as follows:

$$M = \frac{V_O}{V_i}$$

Where Vo is the output voltage and Vi is the input voltage. For this example, choosing the maximum steady state value possible,

$$M = \frac{40\ V}{4.5\ V} = 8.9$$

However, the value of M used to determine the inductance value should be smaller to allow for startup transients where M can be as low as 1 – 1.5.

Therefore, the maximum value of inductance, L, can be calculated as a function of M, R, and t_S where M is defined above, R is the load resistance and t_S is the period of one switching cycle.

$$L \leq \frac{R \times t_S}{2} \times \frac{(M-1)}{M^3}$$

For this example, with M = 8.9, Vo = 40 V, V_i = 4.5 V, and R = 800 Ω, the calculated value of L is:

$$L \leq \frac{800\ \Omega \times 4\ \mu s}{2} \times \frac{(8.9-1)}{8.9^3}$$

or,

$$L \leq 17.9\ \mu H$$

Allowing for startup transients and additional output current to charge the output filter capacitor, a standard-value inductor can be used:

$$L = 4.7\ \mu H$$

2.3.3 Duty Cycle Estimate

The duty cycle, D, is the ratio of the power switch conduction time to the period of one switching cycle. An estimate of the duty cycle is used frequently in the following sections.

Now, defining K as:

$$K = \frac{2 \times L}{R \times t_S}$$

a simplified expression for the duty cycle, D, is:

$$D = \sqrt{K \times M \times (M-1)}$$

For this example, (assuming V_i = 5 V, Vo = 20 V, R = 200 Ω, corresponding to 2 W output power), we get a duty cycle estimate of:

$$D = \sqrt{\frac{2 \times 4.7\ \mu H}{200 \times 4 \mu s} \times \frac{20}{5} \times \left(\frac{20}{5} - 1\right)} = 0.375$$

For Vi = 5 V, Vo = 40 V, R = 16000 Ω (corresponding to 0.1 W output power), we get a duty cycle estimate of:

$$D = \sqrt{0.000147 \times 8 \times 7} = 0.0907$$

2.3.4 Output Filter Capacitance

The peak inductor current must be calculated to determine the amount of output capacitance needed. The expression for the peak inductor current, I_{pk}, is:

$$I_{pk} = \frac{V_i}{L} \times D \times t_S$$

The peak inductor current occurs when the converter is driving its maximum 2-watt load. Using the duty cycle calculated above for a 2-W load gives:

$$I_{pk} = \frac{5\ V}{4.7\ \mu H} \times 0.375 \times 4\ \mu s = 1.6\ A$$

The two criteria for selecting the output capacitor are the amount of capacitance needed and the capacitor’s equivalent series resistance (ESR). After the capacitance and ESR requirements are determined, the capacitor can be selected.

The voltage variation due to the inductor current flow in the output capacitor is approximately:

$$\Delta V_O = \frac{I_{pk}^2 \times L}{2 \times C \times (V_O - V_i)}$$

The above equation is based on the assumption that all inductor ripple current flows through the capacitor and the ESR is zero. If the desired output ripple voltage is 50 mV, then the capacitance needed is:

$$C = \frac{(1.6\ A)^2 \times 4.7\ \mu H}{2 \times 0.05\ V \times (20 - 5)} = 8\ \mu F$$

Now, assuming that the capacitance is very large, the ESR needed to limit the ripple to 50 mV is:

$$ESR = \frac{\Delta V_O}{\Delta I_O} = \frac{0.05\ V}{1.6\ A} = 31.3\ m\Omega$$

The output filter capacitor should be rated at least two to three times the calculated capacitance and 30 to 50 percent lower than the calculated ESR. This design used one 22 µF multilayer ceramic capacitor. With a ceramic capacitor, the ESR is much less than the ESR requirement.

2.3.5 Power Switch

Power-switch design requires selecting the power switch, calculating power dissipation, and ensuring the semiconductors have proper heat sinking.

The peak inductor current, which also flows in the power switch during the on time, is given above as 1.6 A. The duty cycle for Vi = 5 V is 0.375. Thus, the rms value of the power switch current is:

$$I_{RMS} = I_{pk} \times \sqrt{\frac{D}{3}}$$

So, the rms current in the power switch is:

$$I_{RMS} = 1.6\ A \times \sqrt{\frac{0.375}{3}} = 0.566\ A$$

The design uses an n-channel power MOSFET to simplify the drive-circuit design and minimize component count. Based on these calculations, the drain current rating should be chosen for 1.6 A peak and 0.566 A rms. The drain-to-source breakdown rating should be appropriate for the 40 V applied to the device during the off time. Surface mount packaging is also recommended.

The IRLL014 power MOSFET is a 60-V n-channel MOSFET in a power surface mount package with an $I_{D\ MAX}$ rating of 1.7 A continuous at a case temperature of 100°C.

Power dissipation, P_D, which includes both conduction and switching losses can be approximated by:

$$P_D = \left(I^2_{RMS} \times r_{DS(on)}\right) + \left(0.5 \times V_O \times I_{PK} \times t_{r+f} \times f\right)$$

where t_{r+f} is the total MOSFET switching time and $r_{DS(on)}$ is adjusted for temperature. However, in a discontinuous-mode boost converter, there is no switching loss at turn-on, because the current starts at zero.

Assuming the drive circuit is adequate for t_f = 100 ns and the junction temperature is 125°C with a 55°C ambient, the $r_{DS(on)}$ adjustment factor is 1.8 (given in the IRLL014 data sheet).

$$\begin{aligned} P_D \ &= \left(0.566^2 \times 0.28 \times 1.8\right) \\ &+ (0.5 \times 20 \times 1.6 \times 100\ ns \times 250\ kHz) = 0.56\ W \end{aligned}$$

Switching losses are dominant in this application but may not be in others. Check dissipation at the limits of input and output voltages to find the worst case.

The thermal impedance given in the component data sheet is $R_{\theta JA}$ = 60°C/W for FR-4 PWB material with 2-oz. copper and a one-inch-square pattern. The junction temperature of the power switch can be calculated as follows:

$$T_J = T_A + \left(R_{\theta JA} \times P_D\right) = 55 + (60 \times 0.56) = 88.6°\text{C}$$

2.3.6 Snubber Network

A snubber network suppresses the ringing at the node where the power switch drain, boost inductor, and output diode anode connect. This ringing results from driving parasitic inductance and capacitance with fast rise time waveforms. An RC snubber-damping network in parallel with the power switch is by far the simplest way to minimize or eliminate the problem.

The initial design is straightforward, but the PCB layout may necessitate component value adjustments during the prototype phase. The capacitor value chosen is normally 4 to 10 times greater than the power switch drain-to-source capacitance; higher values improve the snubbing but dissipate more power. The IRLL014 has a typical output capacitance of 170 pF. Due to the relatively high switching frequency and low output power, the snubber capacitor value is chosen to be 330 pF to keep the power dissipation low. The snubber capacitor should be fully charged and discharged in the course of one switching cycle. This determines a maximum value for the snubber resistor value. Determination of the resistor value is largely empirical as long as it is less than the maximum value imposed by the capacitor. In this example, a value of 10 Ω was chosen.

Since the capacitor is charged and discharged each cycle, the power dissipation is:

$$P_D = 2 \times \frac{1}{2} \times C \times V_O^2 \times f = 330\ pF \times 20^2 \times 250\ kHz = 0.033\ W$$

where V_O = 20 V.

2.3.7 Output Rectifier

The output rectifier conducts when the power switch turns off and provides a path for the inductor current. Important criteria for selecting the rectifier include: fast switching, appropriate breakdown voltage, current rating, low forward voltage drop to minimize power dissipation, and appropriate packaging. Unless the application justifies the expense and complexity of a synchronous rectifier, the best solution for low voltage outputs is usually a Schottky rectifier.

The breakdown voltage must be 40 V or greater to block the maximum output voltage during the power switch on time. The rectifier's average current rating must be at least 1 A. Generally, the current rating will be much higher than the actual output current because the rectifier's power dissipation and junction temperature ratings are usually the prevailing factors in device selection.

The SS16 is a 1-A, 60-V Schottky rectifier in a DO-214AC surface mount package. Care must be taken to ensure that the rectifier maximum junction temperature is not exceeded. The first step in determining the rectifier junction temperature is to estimate worst-case power dissipation. Neglecting leakage current and assuming there are no switching losses, the power dissipation in the output rectifier is:

$$P_D = I_D \times V_D = 0.1\ A \times 0.4\ V = 0.04\ W$$

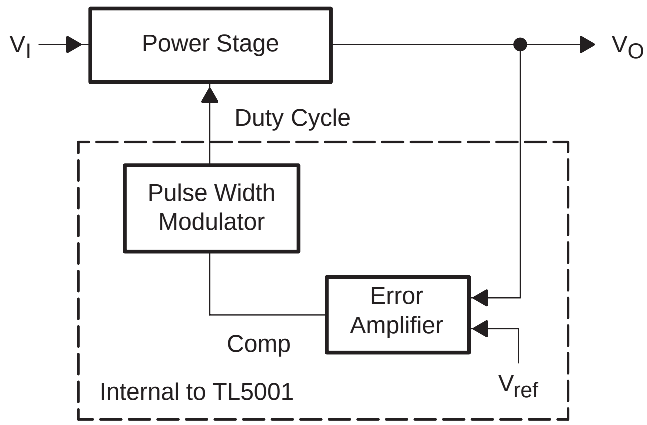
The thermal impedance given in the component data sheet is $R_{\theta JA}$ = 88°C/W for PCB mounting and a 0.2-inch-square pattern. The junction temperature of the output rectifier can be calculated as follows:

$$T_J = T_A + \left(R_{\theta JA} \times P_D\right) = 55 + (88 \times 0.04) = 58.5°C$$

2.3.8 Loop Compensation

The control loop for this converter consists of three gains: the power stage (G_{PS}), the error amplifier ($G_{E/A}$), and the internal TL5001 PWM modulator (G_{PWM}). Figure 2–1 shows a simplified block diagram of the control loop. Negative feedback stabilizes the output voltage against changes in line or load without destroying the control-loop's ability to respond to line and/or load transients. To maintain good performance and stability, it is necessary to tailor the open-loop frequency response of the converter. The frequency response of the error amplifier is shaped to obtain a desired overall open-loop response. This tailoring of the converter frequency response is called loop compensation.

Figure 2–1. Control Loop Simplified Block Diagram



The loop-compensation design procedure consists of shaping the error-amplifier frequency response with external components to stabilize the dc-to-dc converter. A detailed treatment of dc-to-dc converter stability analysis and design is beyond the scope of this report; however, several references on the subject are available. The following is a simplified approach to designing networks to stabilize discontinuous mode boost converters that works well when the open-loop gain is below unity at a frequency much lower than the frequency of operation.

The first step in the design of the loop-compensation network is the design of the output sense divider. This sets the output voltage, and the top resistor, R7, determines the relative impedance of the rest of the compensation design. Since the TL5001 input bias current is 0.5 µA (worst case from the TL5001 data sheet), the divider current should be 500 to 1000 times this amount in order to minimize errors due to input bias currents. A 51.1 KΩ resistor for the top of the divider gives a minimum divider current of 370 µA for an output setting of 20 V. The bottom of the divider is calculated as:

$$R = V_{ref} \times \frac{R7}{V_O - V_{ref}} = 1\ V \times \frac{51.1\ k\Omega}{V_O - 1}$$

This resistance will vary depending on the output voltage setting.

The response of the boost power stage operating in discontinuous mode can be modeled as a simple gain block with a single real pole. The magnitude of the gain is the change in output voltage divided by the change in the duty cycle. Without going through the detailed derivation, the gain of the discontinuous boost power stage is:

$$G_{PS}(s) = \frac{\Delta V_O}{\Delta D} = G_{OD} \times \frac{1}{1 + \frac{s}{\omega_P}}$$

where,

$$G_{OD} = \frac{2 \times V_O}{(2 \times M)-1} \times \sqrt{\frac{M-1}{K \times M}}$$

$$\omega_P = \frac{(2 \times M)-1}{M-1} \times \frac{1}{R \times C}$$

and K and M are the same as previously defined. For this example, the dc gain, G_{OD} , is given by:

$$G_{OD} = \frac{2 \times 20}{(2 \times 4)-1} \times \sqrt{\frac{4-1}{0.0117 \times 4}} = 45.8$$

Since gain is usually expressed in dB,

$$G_{OD} = 33.2 \ dB$$

and, the single real pole is given by:

$$\omega_P = \frac{(2 \times 4)-1}{4-1} \times \frac{1}{200 \ \Omega \times 22 \ \mu F} = 530 \ Radians$$

Since frequency is usually expressed in Hertz,

$$\omega_P = 84.4 \ Hz$$

This power stage gain is dependent on input voltage, output voltage, and output load resistance. For this circuit, the worst case is when the input voltage is at its maximum of 7 V, the output voltage is at its minimum of 20 V, and its maximum load of 2 W. This condition gives a minimum phase margin. It is good design practice to check for stability at the line voltage extremes, and limits of output voltage settings and loads to ensure that gain and phase variations do not cause problems.

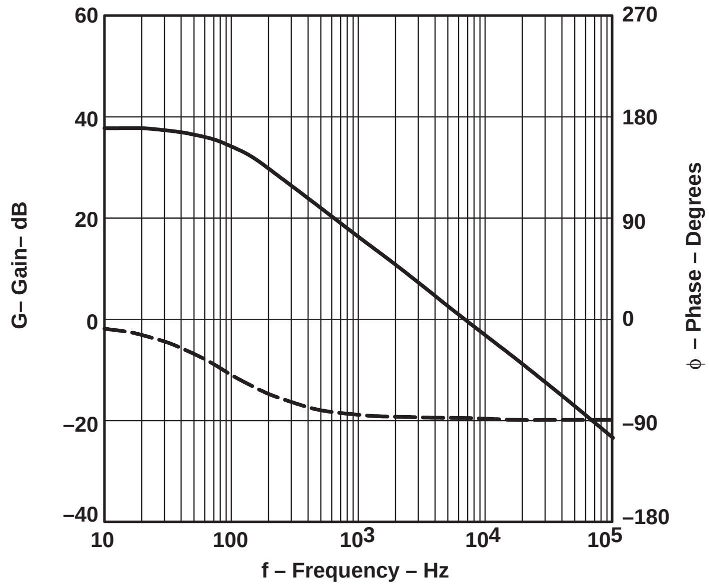
The response of the pulse-width modulator can be modeled as a simple gain block. The magnitude of the gain is the change in PWM output duty cycle for a change in the pulse-width-modulator input voltage (error-amplifier COMP voltage). Typically, increasing the COMP voltage from 0.6 V to 1.4 V increases the duty cycle from 0 to 100%.

The gain, G_{PWM}, is:

$$G_{PWM} = \frac{\Delta D}{\Delta V_{O(COMP)}} = \frac{1-0}{1.4-0.6} = 1.25 \Rightarrow 1.9 \ dB$$

The product (sum in dB) of the gains of the power stage, G_{PS}, and the pulsewidth-modulator, G_{PWM} makes up the uncompensated open loop response. Figure 2–2 is a gain (solid line) and phase (dashed line) plot of the uncompensated open loop response of the converter obtained from a MathCad analysis.

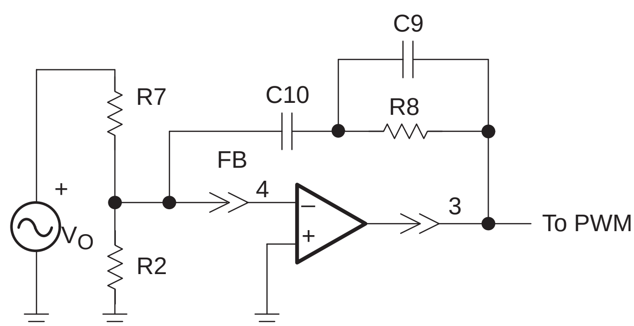
Figure 2–2. Uncompensated Open-Loop Response



The presence of the single real pole is evident from the phase in the vicinity of 84 Hz and the fact that the total phase shift is only 90 degrees.

Unless the designer is trying to meet an unusual requirement, such as very wideband response, many of the decisions regarding gains, compensation pole and zero locations, and unity-gain bandwidth are largely arbitrary. Generally, the gain at low frequencies is very high to minimize error in the output voltage. Compensation zero(s) are added near the filter pole(s) to correct for the phase shift due to the power stage frequency response. Finally, an open-loop unity gain frequency is selected well beyond the power stage pole but at 5 to 10 percent of the converter operating frequency. Figure 2–3 shows a standard compensation network chosen for this example.

Figure 2–3. Compensation Network



Assuming an ideal amplifier, the error amplifier transfer function is:

$$G_{E/A} = \frac{\Delta V_{O(COMP)}}{\Delta V_{OUT}} = \frac{-1}{s \times R7 \times C10} \times \frac{1 + s \times R8 \times (C9 + C10)}{1 + s \times R8 \times C9}$$

This amplifier has a pole at dc, a zero positioned to approximately cancel the pole from the power stage, and a high frequency pole to prevent noise from upsetting the control loop.

The unity gain frequency is selected to be approximately 12 kHz. From the gain-phase plot of the uncompensated open loop response of the converter (Figure 2–2), the gain is seen to be about –7 dB, and the phase is –90 degrees at 12 kHz. Therefore, the amplifier needs to provide a gain of +7 dB at 12 kHz. This gain is determined approximately by the ratio of R8 to R7 because the zero provided by R8 and C9 is located much lower in frequency than the desired crossover frequency.

Resistor R8 is chosen to be 120 kΩ. This value produces the desired gain shown by the following:

$$G = 20 \times log_{10}\left[\frac{R8}{R7}\right] = 7.41 \ dB$$

The frequency of the zero to cancel the power stage pole is given by:

$$f_Z = \frac{1}{2\pi \times R8 \times C10}$$

Solving for C10, we get:

$$C10 = \frac{1}{2\pi \times R8 \times f_Z} = \frac{1}{2\pi \times 120 \ k\Omega \times 84} = 0.016 \ \mu F \Rightarrow 0.018 \ \mu F$$

The high frequency pole at 75 kHz is given by:

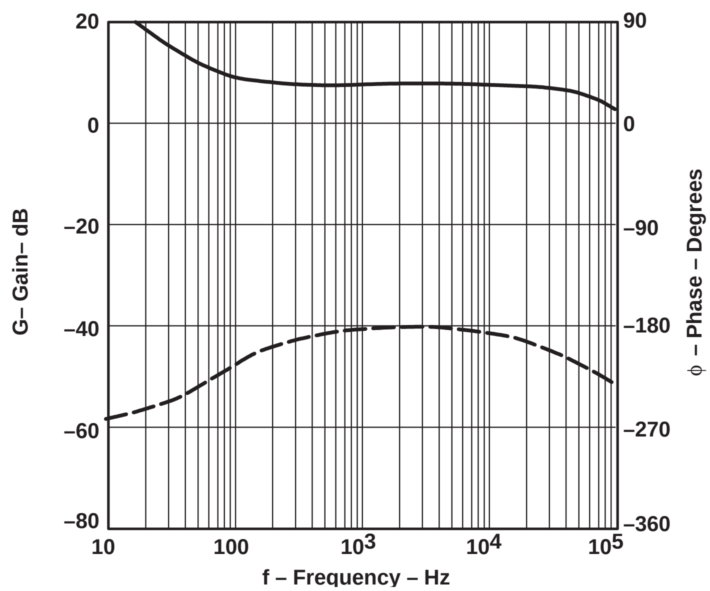
$$f_P = \frac{1}{2\pi \times R8 \times C9}$$

Solving for C9, we get:

$$C9 = \frac{1}{2\pi \times R8 \times f_P} = \frac{1}{2\pi \times 120 \ k\Omega \times 75 \ kHz} = 17.7 \ pF \Rightarrow 18 \ pF$$

Figure 2–4 is a gain (solid line) and phase (dashed line) plot of the error amplifier frequency response obtained from a MathCad analysis.

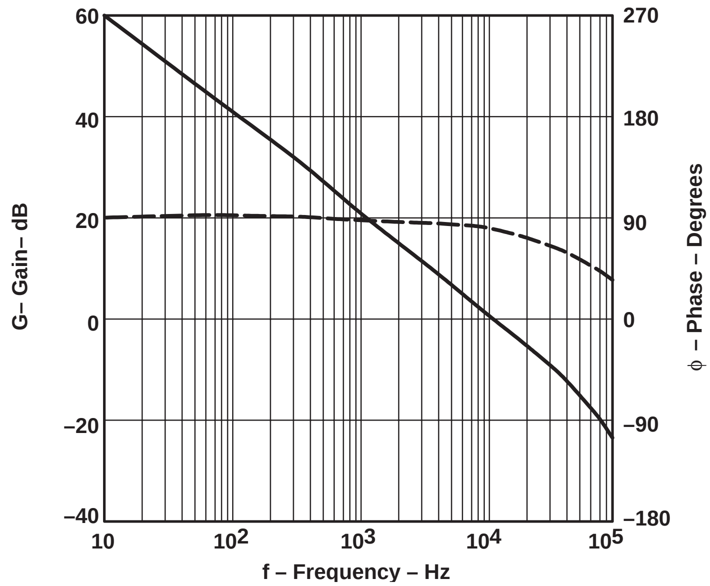
Figure 2–4. Error Amplifier Frequency Response



The overall open loop frequency response of the converter is the product of the uncompensated open loop response and the error amplifier response. A

Bode plot of the overall open loop frequency response of the converter is shown below in Figure 2–5. The gain crosses 0 dB in the vicinity of 12 kHz and the phase margin is approximately 78 degrees.

Figure 2–5. Overall Open Loop Response

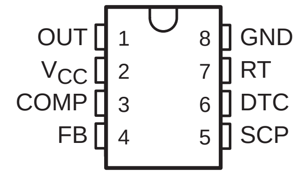


Appendix A

TL5001 Data Sheet

- **Complete PWM Power Control**
- **3.6-V to 40-V Operation**
- **Internal Undervoltage-Lockout Circuit**
- **Internal Short-Circuit Protection**
- **Oscillator Frequency . . . 40 kHz to 400 kHz**
- **Variable Dead Time Provides Control Over Total Range**

D OR P PACKAGE
(TOP VIEW)



description

The TL5001 incorporates on a single monolithic chip all the functions required for a pulse-width-modulation (PWM) control circuit. Designed primarily for power-supply control, the TL5001 contains an error amplifier, a regulator, an oscillator, a PWM comparator with a dead-time-control input, undervoltage lockout (UVLO), short-circuit protection (SCP), and an open-collector output transistor.

The error-amplifier common-mode voltage ranges from 0 V to 1.5 V. The noninverting input of the error amplifier is connected to a 1-V reference. Dead-time control (DTC) can be set to provide 0% to 100% dead time by connecting an external resistor between DTC and GND. The oscillator frequency is set by terminating RT with an external resistor to GND. During low V_{CC} conditions, the UVLO circuit turns the output off until V_{CC} recovers to its normal operating range.

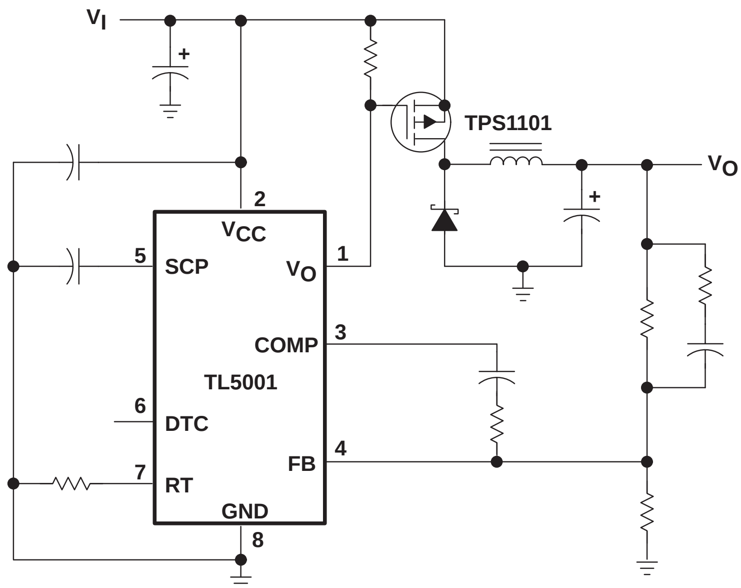
The TL5001C is characterized for operation from –20°C to 85°C. The TL5001I is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

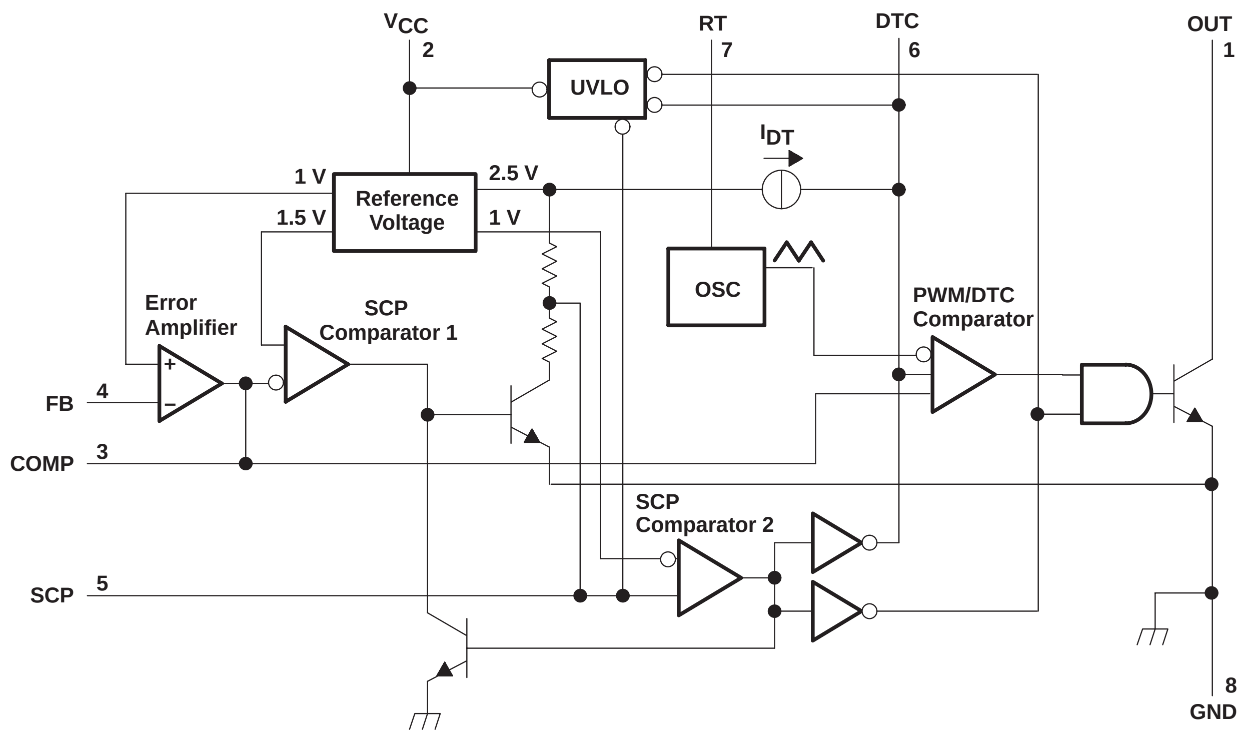
T_A	PACKAGED DEVICES		
	SMALL OUTLINE (D)	PLASTIC DIP (P)	CHIP FORM (Y)
–20°C to 85°C	TL5001CD	TL5001CP	TL5001Y
–40°C to 85°C	TL5001ID	TL5001IP	—

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TL5001CDR). Chip forms are tested at T_A = 25°C.

schematic for typical application

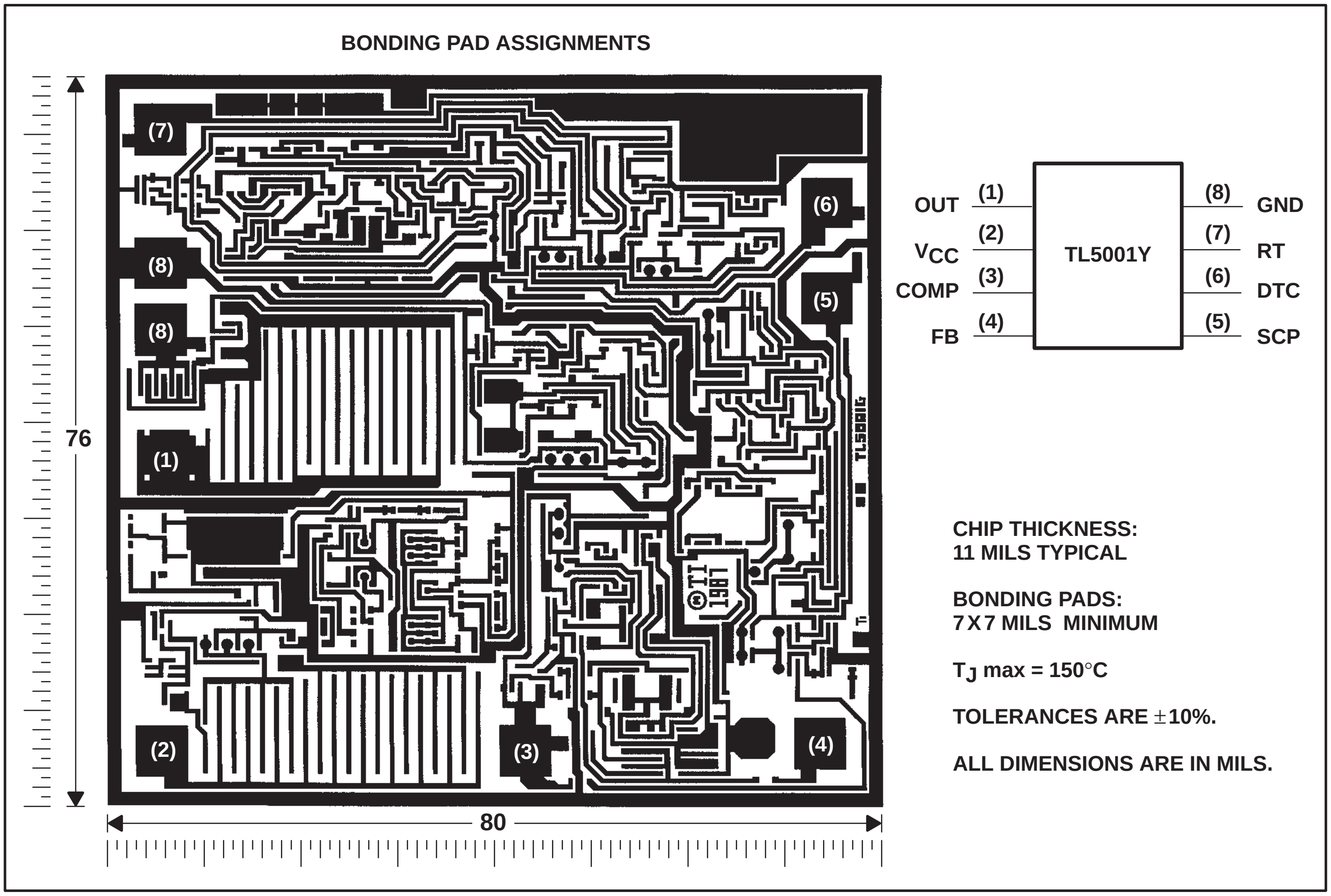


functional block diagram



TL5001Y chip information

This chip, when properly assembled, displays characteristics similar to the TL5001C. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. The chips may be mounted with conductive epoxy or a gold-silicon preform.



detailed description

voltage reference

A 2.5-V regulator operating from V_{CC} is used to power the internal circuitry of the TL5001 and as a reference for the error amplifier and SCP circuits. A resistive divider provides a 1-V reference for the error amplifier noninverting input. The 1-V reference remains within 5% of nominal over the operating temperature range.

error amplifier

The error amplifier compares a sample of the dc-to-dc converter output voltage to the 1-V reference and generates an error signal for the PWM comparator. The dc-to-dc converter output voltage is set by selecting the error-amplifier gain (see Figure 1), using the following expression:

$$V_O = (1 + R1/R2)\ (1\ V)$$

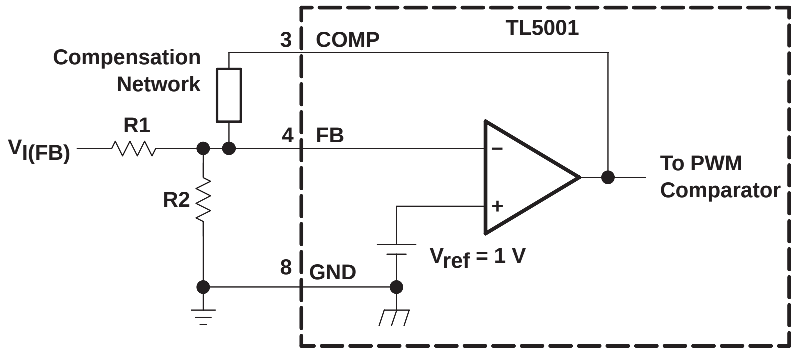


Figure 1. Error-Amplifier Gain Setting

The error-amplifier output is brought out as COMP for use in compensating the dc-to-dc converter control loop for stability. Because the amplifier can only source 45 µA, the total dc load resistance should be 100 kΩ or more.

oscillator/PWM

The oscillator frequency (f_{osc}) can be set between 40 kHz and 400 kHz by connecting a resistor between RT and GND. Acceptable resistor values range from 15 kΩ to 250 kΩ. The oscillator frequency can be determined by using the graph shown in Figure 5.

The oscillator output is a triangular wave with a minimum value of approximately 0.7 V and a maximum value of approximately 1.3 V. The PWM comparator compares the error-amplifier output voltage and the DTC input voltage to the triangular wave and turns the output transistor off whenever the triangular wave is greater than the lesser of the two inputs.

dead-time control (DTC)

DTC provides a means of limiting the output-switch duty cycle to a value less than 100%, which is critical for boost and flyback converters. A current source generates a reference current (I_{DT}) at DTC that is nominally equal to the current at the oscillator timing terminal, RT. Connecting a resistor between DTC and GND generates a dead-time reference voltage (V_{DT}), which the PWM/DTC comparator compares to the oscillator triangle wave as described in the previous section. Nominally, the maximum duty cycle is 0% when V_{DT} is 0.7 V or less and 100% when V_{DT} is 1.3 V or greater. Because the triangle wave amplitude is a function of frequency and the source impedance of RT is relatively high (1250 Ω), choosing R_{DT} for a specific maximum duty cycle, D, is accomplished using the following equation and the voltage limits for the frequency in question as found in Figure 11 (V_{osc}max and V_{osc}min are the maximum and minimum oscillator levels):

$$R_{DT} = \left(R_t + 1250\right)\left[D\left(V_{osc}\text{max} - V_{osc}\text{min}\right) + V_{osc}\text{min}\right]$$

where

R_{DT} and R_t are in ohms, D in decimal

Soft start can be implemented by paralleling the DTC resistor with a capacitor (C_{DT}) as shown in Figure 2. During soft start, the voltage at DTC is derived by the following equation:

$$V_{DT} \approx I_{DT}R_{DT}\left(1 - e^{\left(-t/R_{DT}C_{DT}\right)}\right)$$

dead-time control (DTC) (continued)

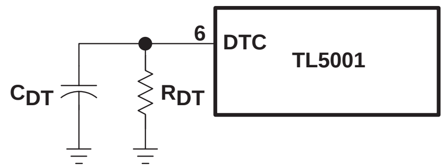


Figure 2. Soft-Start Circuit

If the dc-to-dc converter must be in regulation within a specified period of time, the time constant, $R_{DT}C_{DT}$, should be $t_0/3$ to $t_0/5$. The TL5001 remains off until $V_{DT} \approx 0.7$ V, the minimum ramp value. C_{DT} is discharged every time UVLO or SCP becomes active.

undervoltage-lockout (UVLO) protection

The undervoltage-lockout circuit turns the output transistor off and resets the SCP latch whenever the supply voltage drops too low (approximately 3 V) for proper operation. A hysteresis voltage of 200 mV eliminates false triggering on noise and chattering.

short-circuit protection (SCP)

The TL5001 includes short-circuit protection (see Figure 3), which turns the power switch off to prevent damage when the converter output is shorted. When activated, the SCP prevents the switch from being turned on until the internal latching circuit is reset. The circuit is reset by reducing the input voltage until UVLO becomes active or until the SCP terminal is pulled to ground externally.

When a short circuit occurs, the error-amplifier output at COMP rises to increase the power-switch duty cycle in an attempt to maintain the output voltage. SCP comparator 1 starts an RC timing circuit when COMP exceeds 1.5 V. If the short is removed and the error-amplifier output drops below 1.5 V before time out, normal converter operation continues. If the fault is still present at the end of the time-out period, the timer sets the latching circuit and turns off the TL5001 output transistor.

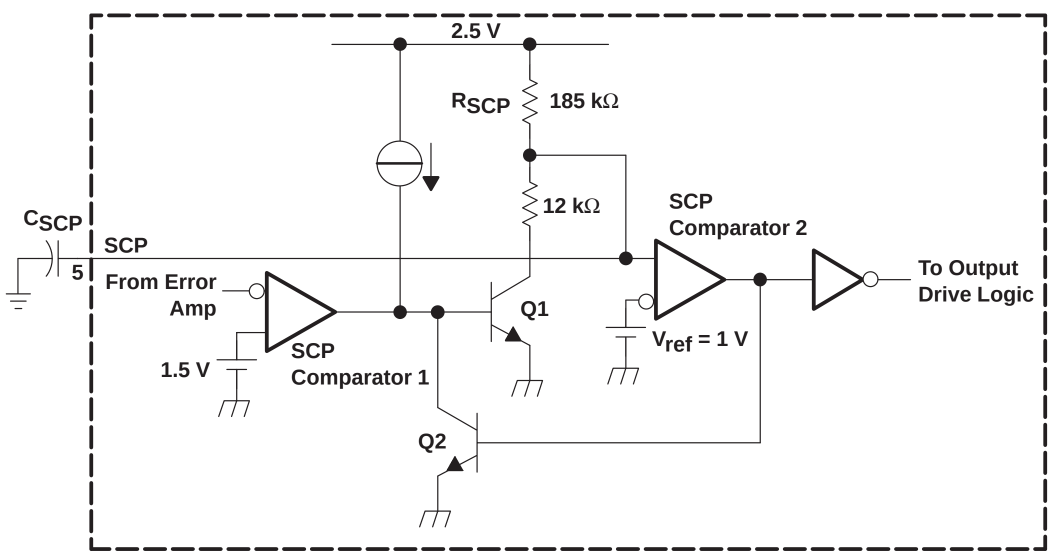


Figure 3. SCP Circuit

short-circuit protection (SCP) (continued)

The timer operates by charging an external capacitor (C_{SCP}), connected between the SCP terminal and ground, towards 2.5 V through a 185-kΩ resistor (R_{SCP}). The circuit begins charging from an initial voltage of approximately 185 mV and times out when the capacitor voltage reaches 1 V. The output of SCP comparator 2 then goes high, turns on Q2, and latches the timer circuit. The expression for setting the SCP time period is derived from the following equation:

$$V_{SCP} = (2.5 - 0.185)\left(1 - e^{-t/\tau}\right) + 0.185$$

where

$$\tau = R_{SCP}C_{SCP}$$

The end of the time-out period, t_{SCP}, occurs when V_{SCP} = 1 V. Solving for C_{SCP} yields:

$$C_{SCP} = 12.46 \times t_{SCP}$$

where

t is in seconds, C in µF.

t_{SCP} must be much longer (generally 10 to 15 times) than the converter start-up period or the converter will not start.

output transistor

The output of the TL5001 is an open-collector transistor with a maximum collector current rating of 21 mA and a voltage rating of 51 V. The output is turned on under the following conditions: the oscillator triangle wave is lower than both the DTC voltage and the error-amplifier output voltage, the UVLO circuit is inactive, and the short-circuit protection circuit is inactive.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . 41 V
Amplifier input voltage, $V_{I(FB)}$ . . . . 20 V
Output voltage, V_O, OUT . . . . 51 V
Output current, I_O, OUT . . . . 21 mA
Output peak current, $I_{O(peak)}$, OUT . . . . 100 mA
Continuous total power dissipation . . . . See Dissipation Rating Table
Operating ambient temperature range, T_A: TL5001C . . . . –20°C to 85°C
TL5001I . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		3.6	40	V
Amplifier input voltage, $V_{I(FB)}$		0	1.5	V
Output voltage, V_O, OUT			50	V
Output current, I_O, OUT			20	mA
COMP source current			45	µA
COMP dc load resistance		100		kΩ
Oscillator timing resistor, R_t		15	250	kΩ
Oscillator frequency, f_{osc}		40	400	kHz
Operating ambient temperature, T_A	TL5001C	–20	85	°C
	TL5001I	–40	85	

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted)

reference

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			UNIT
		MIN	TYP†	MAX	
Output voltage	COMP connected to FB	0.95	1	1.05	V
Input regulation	V_{CC} = 3.6 V to 40 V		2	12.5	mV
Output voltage change with temperature	T_A = –20°C to 25°C (TL5001C)	–10	–1	10	mV/V
	T_A = –40°C to 25°C (TL5001I)	–10	–1	10	
	T_A = 25°C to 85°C	–10	–2	10	

† All typical values are at T_A = 25°C.

undervoltage lockout

PARAMETER	TL5001C, TL5001I			UNIT
	MIN	TYP†	MAX	
Upper threshold voltage		3		V
Lower threshold voltage		2.8		V
Hysteresis	100	200		mV

† All typical values are at T_A = 25°C.

short-circuit protection

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			UNIT
		MIN	TYP†	MAX	
SCP threshold voltage	T_A = 25°C	0.95	1.00	1.05	V
SCP voltage, latched	No pullup	140	185	230	mV
SCP voltage, UVLO standby	No pullup		60	120	mV
Timing resistance			185		kΩ
SCP comparator 1 threshold voltage			1.5		V

† All typical values are at T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted) (continued)

oscillator

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			UNIT
		MIN	TYP†	MAX	
Frequency	R_t = 100 kΩ		97		kHz
Standard deviation of frequency			15		kHz
Frequency change with voltage	V_{CC} = 3.6 V to 40 V		1		kHz
Frequency change with temperature	T_A = –20°C to 25°C	–4	–0.4	4	kHz
	T_A = 25°C to 85°C	–4	–0.2	4	
Voltage at RT			1		V

† All typical values are at T_A = 25°C.

dead-time control

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			UNIT
		MIN	TYP†	MAX	
Output (source) current		$0.9 \times I_{RT}$‡		$1.1 \times I_{RT}$	µA
Input threshold voltage	Duty cycle = 0%	0.5	0.7		V
	Duty cycle = 100%		1.3	1.5	

† All typical values are at T_A = 25°C.
‡ Output source current at RT

error amplifier

PARAMETER		TEST CONDITIONS	TL5001C, TL5001I			UNIT
			MIN	TYP†	MAX	
Input voltage		V_{CC} = 3.6 V to 40 V	0		1.5	V
Input bias current				–160	–500	nA
Output voltage swing	Positive		1.5	2.3		V
	Negative			0.3	0.4	V
Open-loop voltage amplification				80		dB
Unity-gain bandwidth				1.5		MHz
Output (sink) current		$V_{I(FB)}$ = 1.2 V, COMP = 1 V	100	600		µA
Output (source) current		$V_{I(FB)}$ = 0.8 V, COMP = 1 V	–45	–90		µA

† All typical values are at T_A = 25°C.

output

PARAMETER	TEST CONDITIONS	TL5001C, TL5001I			UNIT
		MIN	TYP†	MAX	
Output saturation voltage	I_O = 10 mA		1.5	2	V
Off-state current	V_O = 50 V, V_{CC} = 0			10	µA
	V_O = 50 V			10	
Short-circuit output current	V_O = 6 V		40		mA

† All typical values are at T_A = 25°C.

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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V, f_{osc} = 100 kHz (unless otherwise noted) (continued)

total device

PARAMETER		TEST CONDITIONS	TL5001C, TL5001I			UNIT
			MIN	TYP†	MAX	
Standby supply current	Off state			1	1.5	mA
Average supply current		R_t = 100 kΩ		1.1	2.1	mA

† All typical values are at T_A = 25°C.

electrical characteristics, V_{CC} = 6 V, f_{osc} = 100 kHz, T_A = 25°C (unless otherwise noted)

reference

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
Output voltage	COMP connected to FB		1		V
Input regulation	V_{CC} = 3.6 V to 40 V		2		mV
Output voltage change with temperature			–2		mV/V

undervoltage lockout

PARAMETER	TL5001Y			UNIT
	MIN	TYP	MAX	
Upper threshold voltage		3		V
Lower threshold voltage		2.8		V
Hysteresis		200		mV

short-circuit protection

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
SCP threshold voltage			1		V
SCP voltage, latched	No pullup		185		mV
SCP voltage, UVLO standby	No pullup		60		mV
Timing resistance			185		kΩ
SCP comparator 1 threshold voltage			1.5		V

oscillator

PARAMETER	TEST CONDITIONS	TL5001Y			UNIT
		MIN	TYP	MAX	
Frequency	R_t = 100 kΩ		97		kHz
Standard deviation of frequency			15		kHz
Frequency change with voltage	V_{CC} = 3.6 V to 40 V		1		kHz
Frequency change with temperature			–0.4		kHz
			–0.2		
Voltage at RT			1		V

electrical characteristics, V_{CC} = 6 V, f_{osc} = 100 kHz, T_A = 25°C (unless otherwise noted) (continued)

dead-time control

PARAMETER	TEST CONDITIONS	TL5001Y MIN	TL5001Y TYP	TL5001Y MAX	UNIT
Input threshold voltage	Duty cycle = 0%		0.7		V
	Duty cycle = 100%		1.3		

error amplifier

PARAMETER		TEST CONDITIONS	TL5001Y MIN	TL5001Y TYP	TL5001Y MAX	UNIT
Input bias current				–160		nA
Output voltage swing	Positive			2.3		V
	Negative			0.3		V
Open-loop voltage amplification				80		dB
Unity-gain bandwidth				1.5		MHz
Output (sink) current		$V_{I(FB)}$ = 1.2 V, COMP = 1 V		600		µA
Output (source) current		$V_{I(FB)}$ = 0.8 V, COMP = 1 V		–90		µA

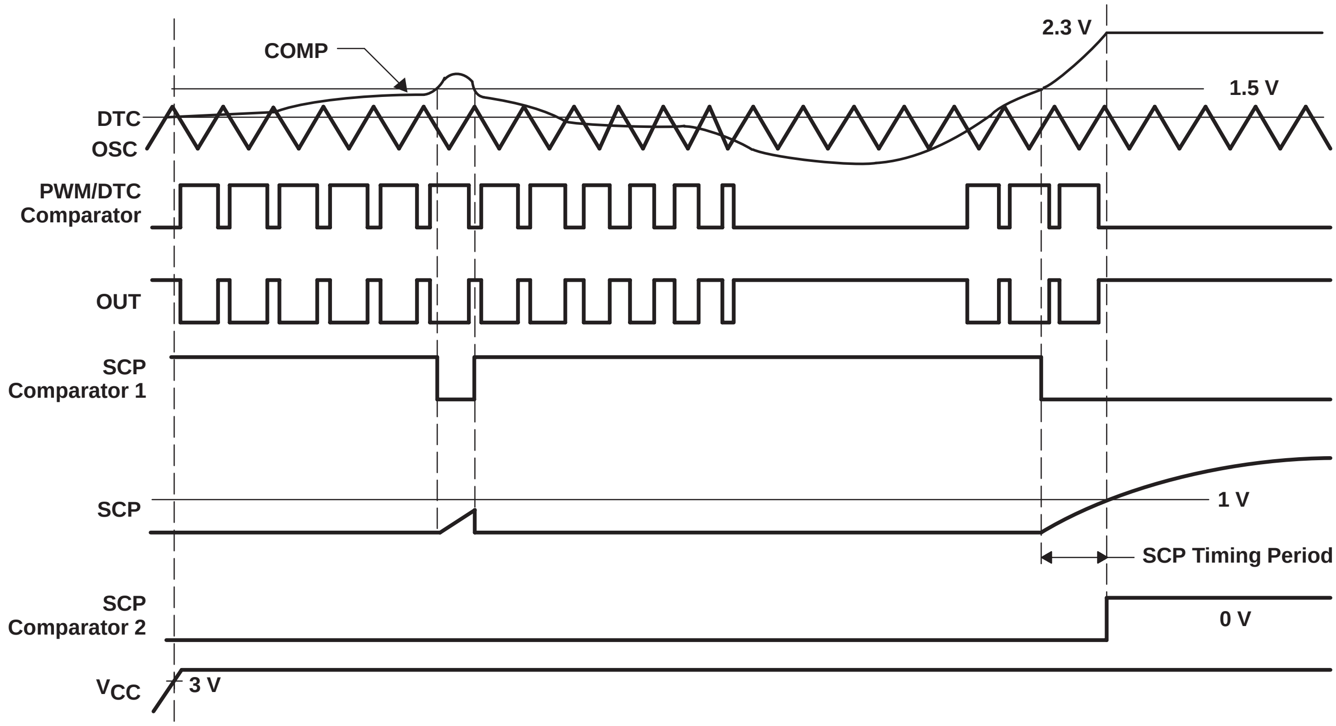
output

PARAMETER	TEST CONDITIONS	TL5001Y MIN	TL5001Y TYP	TL5001Y MAX	UNIT
Output saturation voltage	I_O = 10 mA		1.5	2	V
Short-circuit output current	V_O = 6 V		40		mA

total device

PARAMETER		TEST CONDITIONS	TL5001Y MIN	TL5001Y TYP	TL5001Y MAX	UNIT
Standby supply current	Off state			1		mA
Average supply current		R_t = 100 kΩ		1.1		mA

PARAMETER MEASUREMENT INFORMATION



NOTE A: The waveforms show timing characteristics for an intermittent short circuit and a longer short circuit that is sufficient to activate SCP.

Figure 4. PWM Timing Diagram

TYPICAL CHARACTERISTICS

OSCILLATOR FREQUENCY vs TIMING RESISTANCE

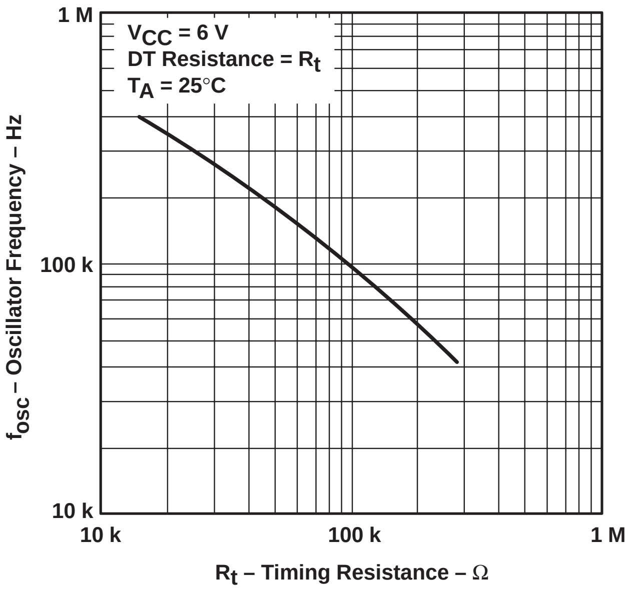


Figure 5

OSCILLATION FREQUENCY vs AMBIENT TEMPERATURE

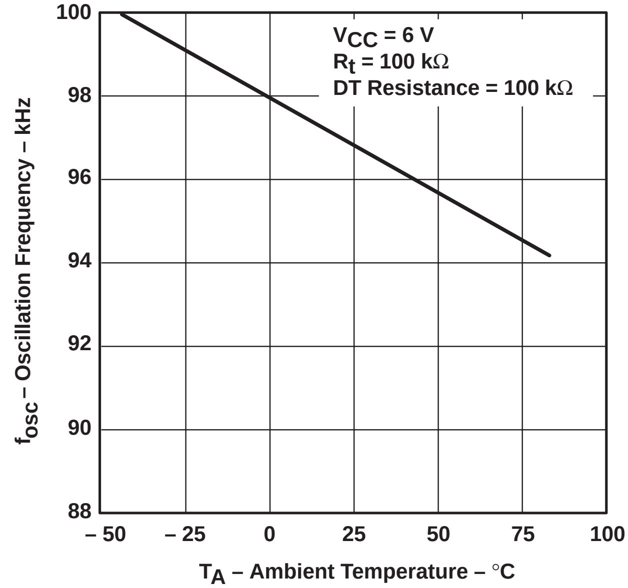


Figure 6

REFERENCE OUTPUT VOLTAGE vs POWER-SUPPLY VOLTAGE

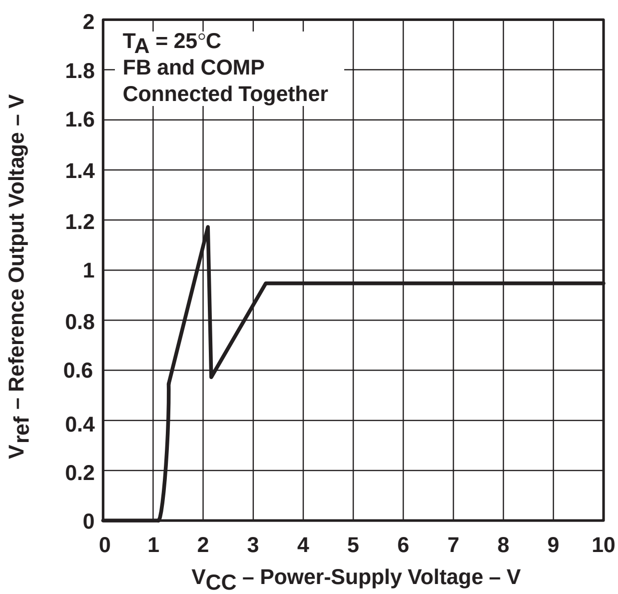


Figure 7

REFERENCE OUTPUT VOLTAGE FLUCTUATION vs AMBIENT TEMPERATURE

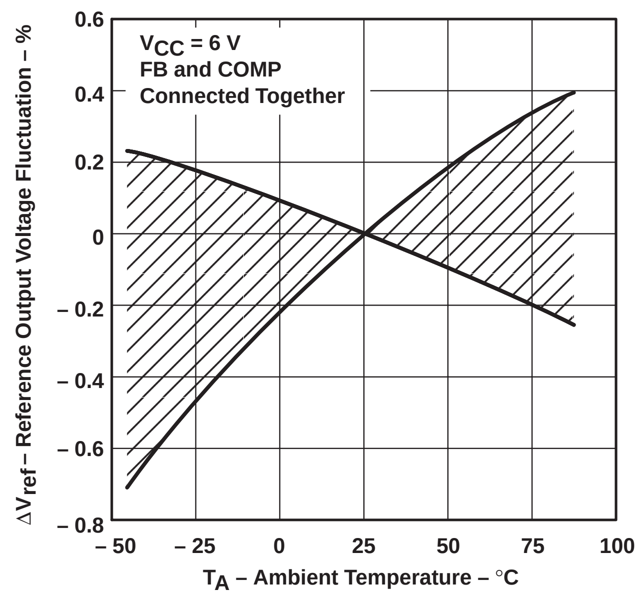


Figure 8

TYPICAL CHARACTERISTICS

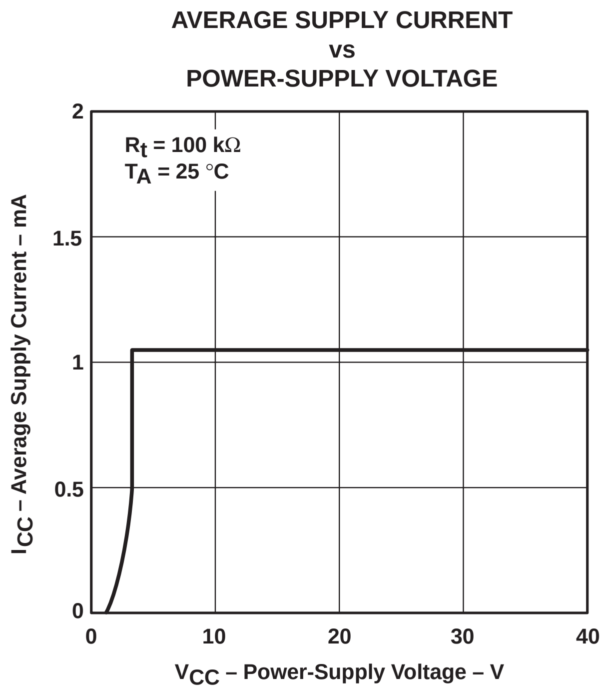


Figure 9

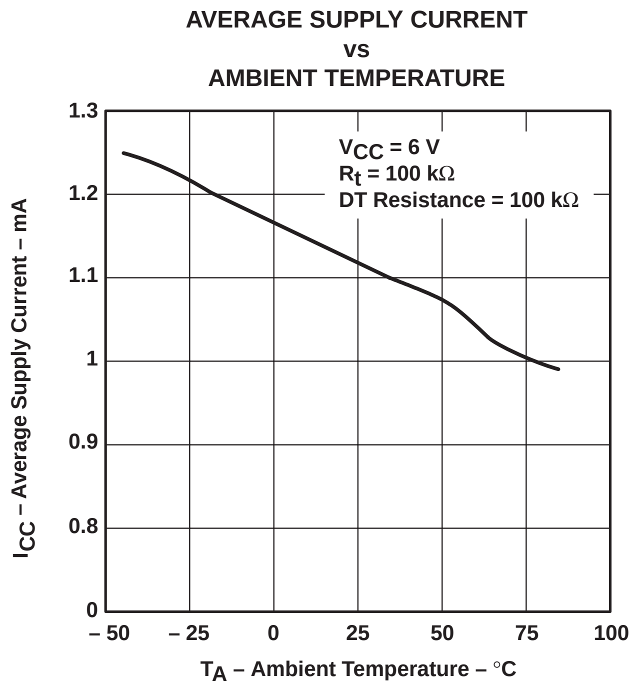


Figure 10

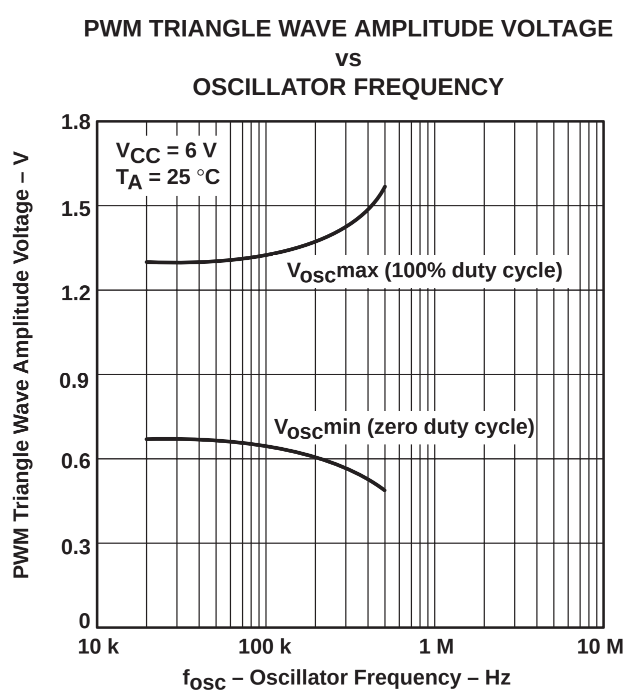


Figure 11

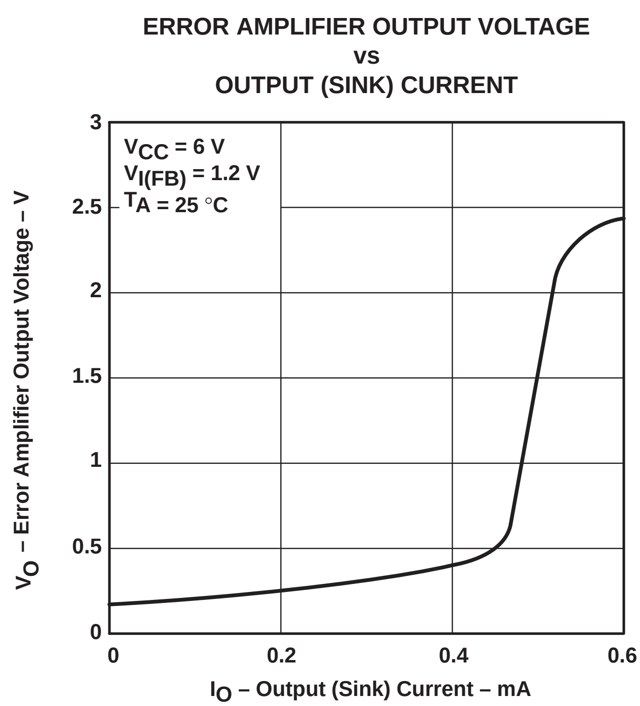


Figure 12

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER OUTPUT VOLTAGE vs OUTPUT (SOURCE) CURRENT

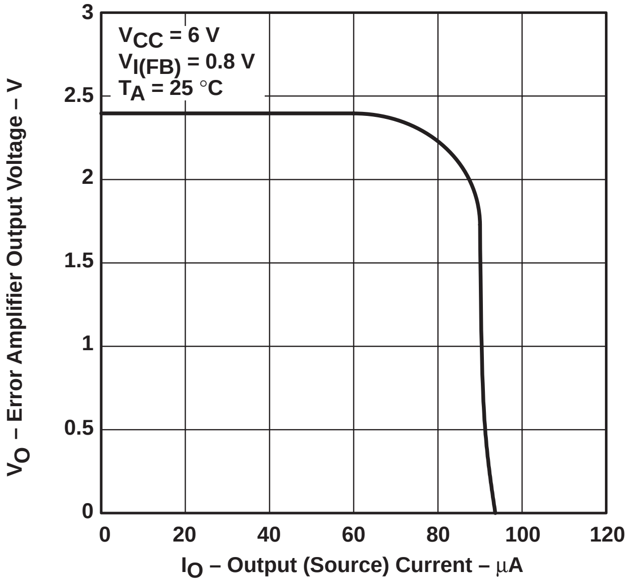


Figure 13

ERROR AMPLIFIER OUTPUT VOLTAGE vs AMBIENT TEMPERATURE

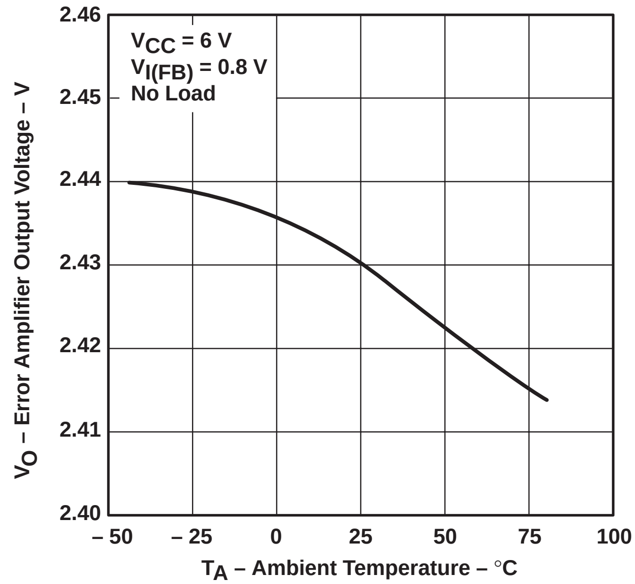


Figure 14

ERROR AMPLIFIER OUTPUT VOLTAGE vs AMBIENT TEMPERATURE

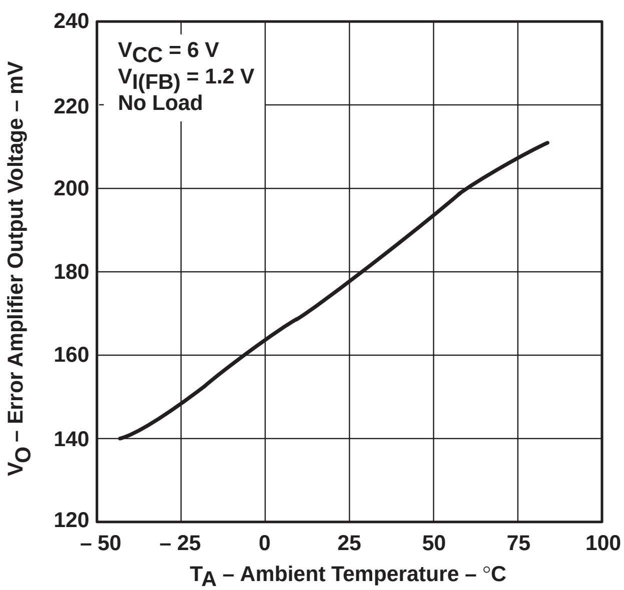


Figure 15

ERROR AMPLIFIER CLOSED-LOOP GAIN AND PHASE SHIFT vs OSCILLATOR FREQUENCY

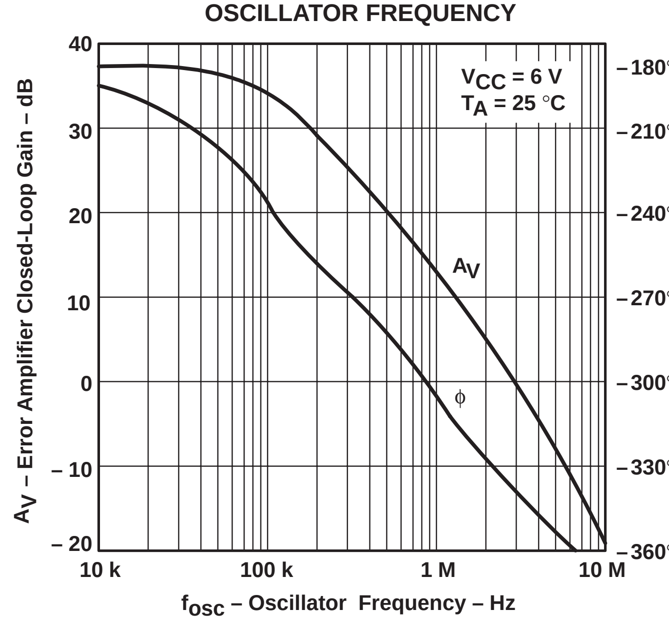


Figure 16

TYPICAL CHARACTERISTICS

OUTPUT DUTY CYCLE vs DTC VOLTAGE

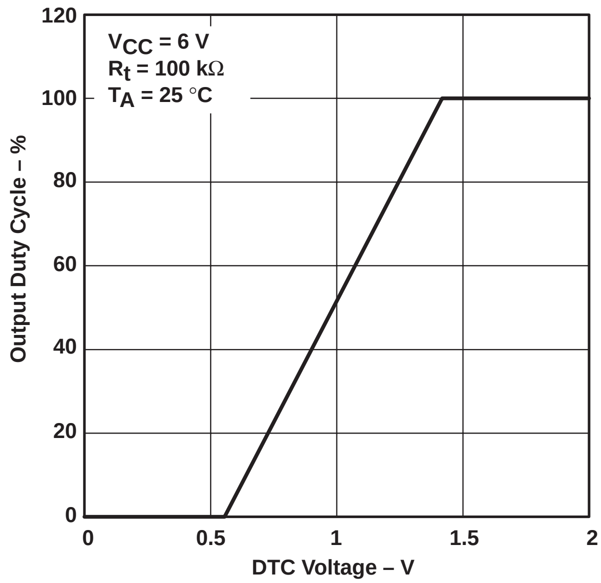


Figure 17

SCP TIME-OUT PERIOD vs SCP CAPACITANCE

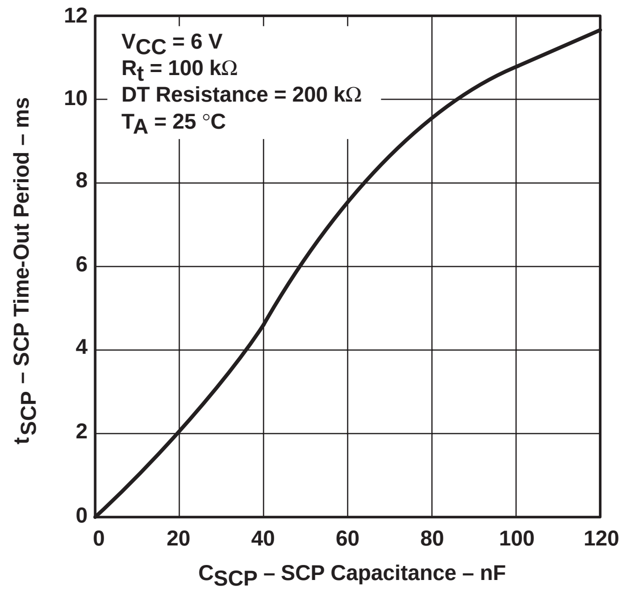


Figure 18

DTC OUTPUT CURRENT vs RT OUTPUT CURRENT

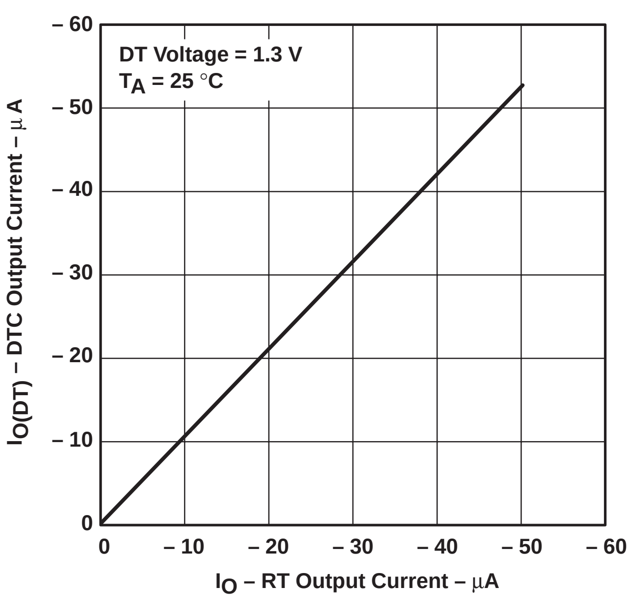


Figure 19

OUTPUT SATURATION VOLTAGE vs OUTPUT (SINK) CURRENT

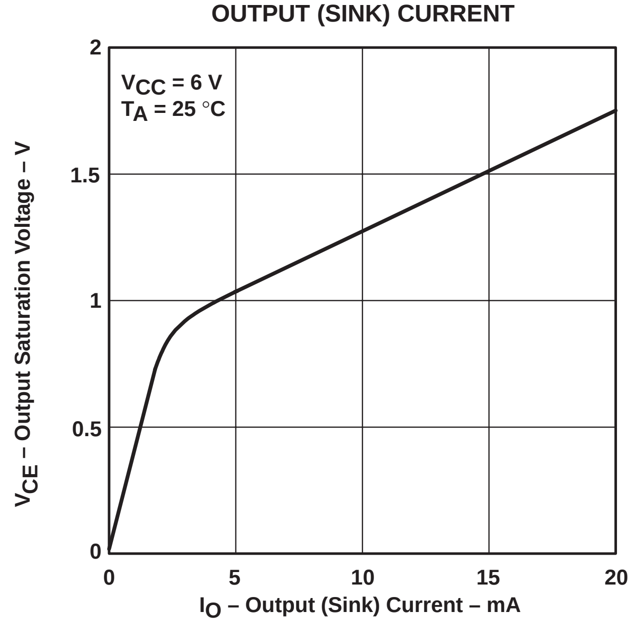
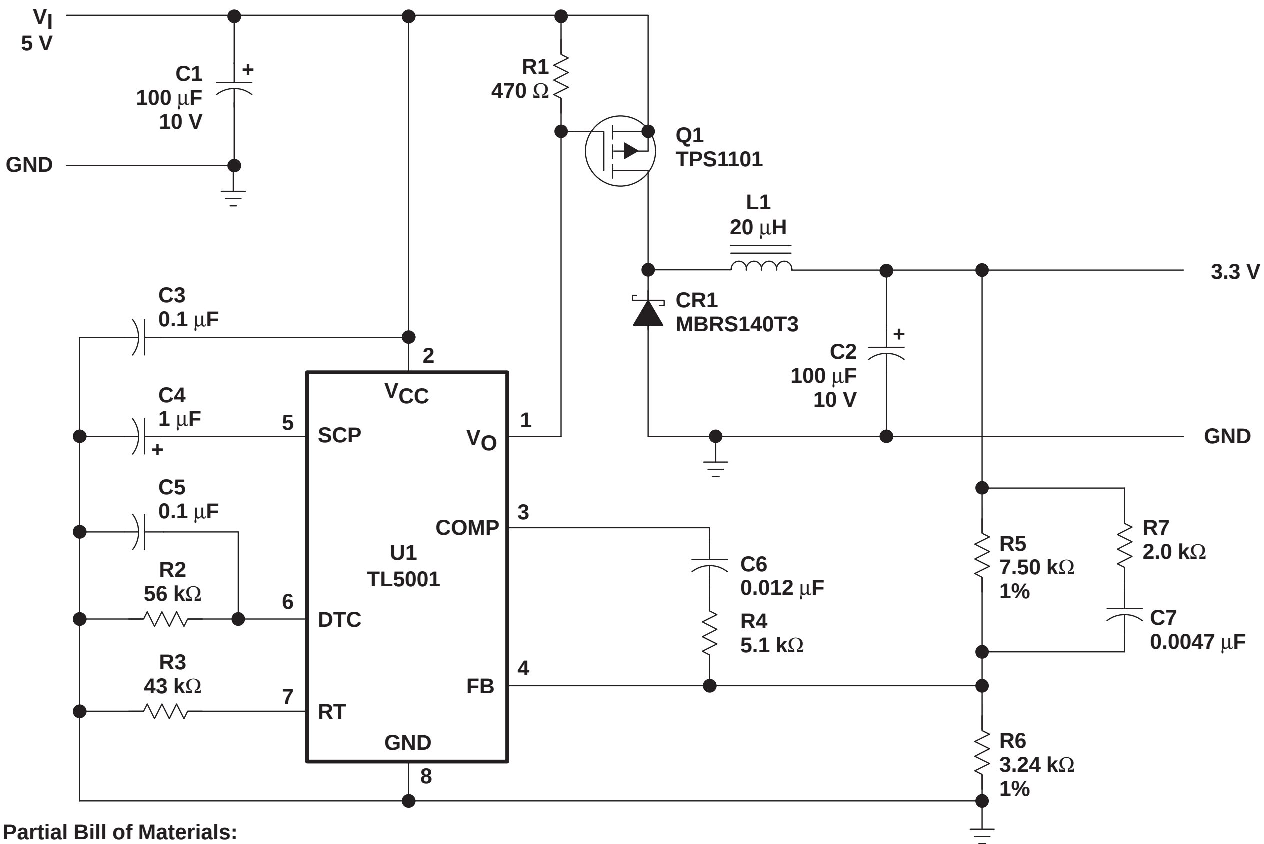


Figure 20

APPLICATION INFORMATION



Partial Bill of Materials:

U1	TL5001	Texas Instruments
Q1	TPS1101	Texas Instruments
LI	CTX20-1 or 23 turns of #28 wire on Micrometals No. T50-26B core	Coiltronics
C1	TPSD107M010R0100	AVX
C2	TPSD107M010R0100	AVX
CR1	MBRS140T3	Motorola

NOTES: A. Frequency = 200 kHz
B. Duty cycle = 90% max
C. Soft-start time constant (TC) = 5.6 ms
D. SCP TC = 70 msA

Figure 21. Step-Down Converter