Modeling of Control Loop Behavior of Magamp Post Regulators

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Abstract—**Small signal control models are presented for a magamp switching-mode post regulator. Two commonly used current reset schemes are considered; an external reset scheme and a self reset scheme. Models for both continuous mode and discontinuous modes of operation are presented. These models provide designers with useful tools for designing compensation network for the feedback error amplifier.**

I. INTRODUCTION

IN RECENT years, magamp post regulators have received growing interest from switching mode power supply manufacturers and university research personnel. A large number of recent papers [1]–[9] reflect new interest in the use of magamp in multiple-output power supply applications. There are numerous advantages of using magamp techniques: simple circuit, small electromagnetic interference (EMI), rugged, and efficient.

One of the main tasks in the design of a magamp regulator is to stabilize the control loop. It has been shown in [1] that the control loop behavior is quite different for the two commonly used reset circuits: Type A circuit (self reset from magamp output voltage) and Type B circuit (reset from an external fixed voltage source). A control loop pole shifting phenomenon in a self-reset type was uncovered. The shifting in control loop poles requires a corresponding change in the error amplifier compensation to achieve a desirable loop response. Reference [1] provides a detailed explanation of the phenomenon and a procedure for compensating the regulator for continuous mode of operation. However, the model presented in [1] is limited to continuous mode of operation in a voltage mode magamp control.

In the present paper, models are developed to predict the small signal control loop behavior of a magamp post regulator for both the continuous mode and the discontinuous mode of operation in a voltage mode feedback. These models also lay the foundation for a more sophisticated control such as current mode magamp control.

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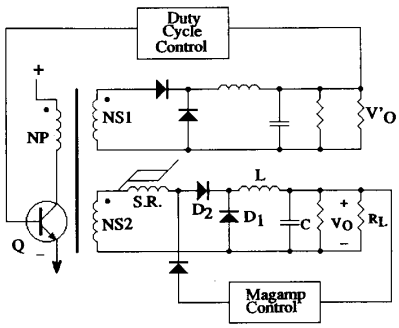

Fig. 1. PWM—controlled forward converter with magamp output.

In the paper, a description of magamp control loop behavior is given first from a circuit level point of view. Then the focus is shifted to look at the same issue from the block diagram point of view. The block diagrams presented are arranged such that they are compatible with the state averaging model for dc-dc converters which became so popular in recent years [12], [13]. In doing so, a body of knowledge already existing in dc converter circuit can be applied to the modeling of magamp control behavior.

II. REVIEW OF MAGAMP CIRCUIT OPERATION AND CONTROL LOOP BEHAVIOR

Before a detailed mathematical modeling of control loop behavior, a brief review of the magamp control is desirable. From this review, control block diagrams will be described, which leads to the modeling of loop behavior.

Fig. 1 shows a PWM-controlled forward converter with a magamp output. The main output voltage V_O is regulated through duty cycle control of the transistor switch Q. Magamp output voltage V_O is post regulated through controlling the reset time of the saturable reactor S.R. The detail of the control action is described next.

PWM MAGNETIC SWITCH

The saturable reactor (SR) in the circuit works as a pulsewidth modulated (PWM) switch. Referring to Fig. 2, when the switch Q conducts and core operates in between t_1 and t_2 of the idealized B-H loop, essentially all of the voltage across secondary winding N_{S2} is blocked by the saturable reactor because of very high inductance

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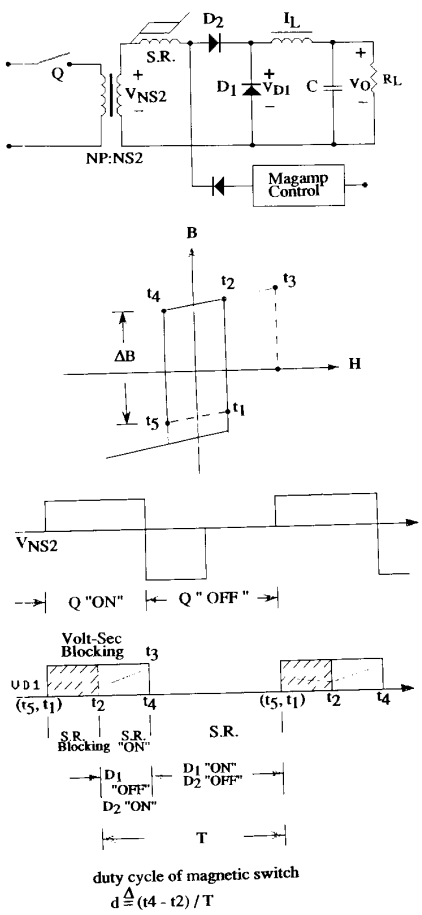

Fig. 2. Magamp operating waveforms. Duty cycle of magnetic switch: $d \triangleq (t4 - t2)/T$.

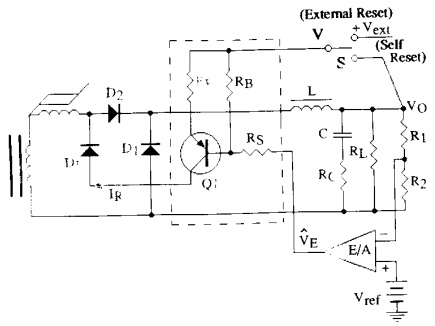

Fig. 3. Magamp control circuit. External reset is used if switch S is connected to V_{ext}. Self reset is used if S is connected to V_O.

associated with this portion of operation. During this period of time, output inductor current is freewheeling through diode D_1 and D_2 is conducting the magnetizing current of the SR, which is ideally zero and practically very small. This corresponds to OFF state of the magnetic switch. When the core saturates, i.e.; between t_2 and t_3, S R presents very little impedance and blocks little voltage. D_1 is off and V_{NS2} is driving filter inductor current through S R and D_2. This corresponds to the ON state of the switch. When V_{NS2} reverses polarity, the SR flux moves from t_3 to t_4 in a very short period of time and D_2 is cut off. Feedback control circuit then determines the amount of flux reset ΔB, which indirectly controls the duration Δt ($\triangleq t_2 - t_1$) of the voltage blocking state, according to Faraday's Law. The leading edge of the V_{D1} waveform is therefore pulsewidth modulated according to reset. This PWM waveform is then filtered by output LC to give a regulated dc output voltage.

Feedback Control and Reset Circuits

Two schemes of resetting core have been reported [4], voltage reset scheme and current reset scheme. Current reset is the most commonly used scheme and is the focus of the present paper. Fig. 3 shows the feedback network and the current reset circuit. There are two types of current reset circuit considered in this paper. Referring to the figure, the self-reset type (Type A) provides reset current by using output voltage V_O and the external-reset type (Type B) provides reset current by using an external voltage source V_{ext}. Both types are in use practically. Self reset type requires no external power supply and is, in general, difficult for the implementation of output short circuit protection. External reset type is just the opposite. The function of the reset circuit is to convert the error voltage V_E into a reset current I_R which resets the saturable reactor to the left half plane of the B-H loop. As explained earlier in the subsection PWM magnetic switch, during the reset period, D_2 is OFF and the reset current I_R is in proportion to the H field of the B-H loop. The larger the I_R, the more to the left is the core reset, which means the longer the voltage blocking duration (Δt) of the next cycle will be. This reduces the pulse width of the V_{D1} waveform. Take one example to see how the control circuit works. The description to follow applies to either types of reset circuits. If V_O exceeds the desirable voltage level, the error V_E becomes more negative. This causes higher voltage across R_B which implies larger voltage across R_E and larger reset current I_R. Transistor Q_1 is operated in the active mode. Larger I_R causes narrowing of the PWM waveform across V_{D1}, as explained earlier. This pulls the output voltage back to the desirable level and achieves regulation.

III. Control Block Diagram and Transfer Function

From the above discussion, control block diagrams are formulated as shown in Fig. 4. It is to be noted that these diagrams are arranged such that they are compatible with the dc converter small signal control models which becomes popular in recent years. A body of knowledge obtained in dc converter modeling can be applicable to the modeling of magamp regulators discussed in the present paper. Referring to Fig. 4, 4(a) shows the diagram for the external reset type and 4(b) shows the diagram for the self

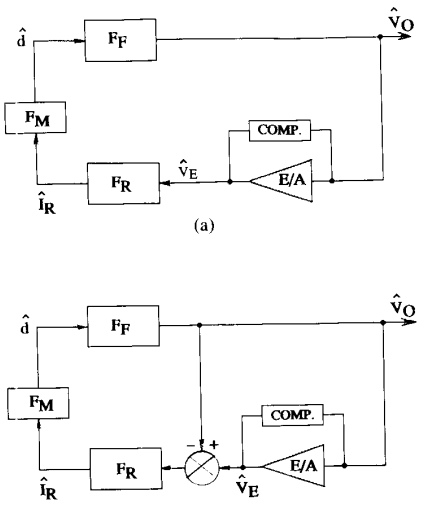

Fig. 4. Control block diagrams for magamp post regulator. (a) External Reset Type. (b) Self-Reset Type. $F_F \triangleq \hat{V}_o/\hat{d}$ duty cycle-to-output transfer function. $F_M \triangleq \hat{d}/\hat{I}_R$ reset current-to-duty cycle transfer function. $F_R \triangleq \hat{I}_R/\hat{V}_E$ control voltage-to-reset current transfer function.

reset type. The definition of the transfer function of each of the blocks is also shown. The transfer functions of each of the blocks is derived as follows.

Transfer Functions

Error Amplifier and Compensator E/A: The main task about feedback control in this instance is to design a compensator network which stabilizes the system and gives an optimized regulator response. Compensator design depends very much on loop transfer functions to be discussed below.

Reset Circuit Transfer Function F_R: As defined, F_R is the error voltage-to-reset current transfer function. Referring to the reset circuit in Fig. 3, reset current I_R can be represented in terms of error voltage V_E, voltage V_{ext} or V_O depending upon the type of reset used, and resistor values R_B, R_S, and R_E by (1):

$$I_R = \left[\frac{(V - V_E)R_B}{(R_B + R_S)} - V_{BE}\right] \cdot \frac{1}{R_E}, \tag{1}$$

where

$$V = V_O \quad \text{for self reset type,}$$

and

$$V = V_{\text{ext}} \quad \text{for external reset type.}$$

The small signal transfer function F_R can be derived from (1) by perturbation method as described next.

External Reset Type

Perturbing (1) by the following substitution:

$$I_R = \langle I_R \rangle + \hat{I}_R;$$

$$V_E = \langle V_E \rangle + \hat{V}_E;$$

$$V = \langle V_{\text{ext}} \rangle + \hat{V}_{\text{ext}} = \langle V_{\text{ext}} \rangle$$

$$V_{BE} = \langle V_{BE} \rangle + \hat{V}_{BE} = \langle V_{BE} \rangle,$$

where $\langle\ \rangle$ sign represents dc quantity and $\hat{}$ sign represents small signal ac quantity. By equating the small signal quantities after the perturbation, (2) is obtained:

$$F_R \triangleq \frac{\hat{I}_R}{\hat{V}_E} = \frac{-R_B}{(R_B + R_S)R_E}. \tag{2}$$

In this derivation, it is assumed that transistor V_{BE} is a constant.

Self Reset Type

Using similar procedure and (2) leads to (3):

$$I_R \triangleq \frac{-R_B}{(R_B + R_S)R_E} \cdot (\hat{V}_E - \hat{V}_O)$$

$$= F_R(\hat{V}_E - V_O). \tag{3}$$

Equation (3) explains the addition of an inner feedback path from V_O in the block diagram in Fig. 4(b) for self reset type.

Magnetic Modulator Transfer Function F_M: F_M is defined as the change of magnetic switch duty cycle ($d \triangleq (t_4 - t_2)/T$; see Fig. 2) to the change of reset current I_R. F_M is strongly affected by the saturable reactor design parameters and the dc operating condition of the magamp circuit. (4) shows the following relationship:

$$F_M \triangleq \frac{\hat{d}}{\hat{I}_R} = \frac{-0.4\pi \cdot \mu_M \cdot N^2 \cdot Ae \cdot F_s}{l_e \cdot V_x \cdot 10^8}, \tag{4}$$

where N is the number of turns, Ae is the core cross section area (cm^2), l_e is the core mean length (cm), V_x is the voltage across transformer secondary winding when the SR is at blocking state, and μ_M is the average permeability defined in (5). The detail of the derivation of (4) is given in the Appendix. There is a phase delay associated with F_M [10], but it is ignored in this paper because the phase delay is insignificant at low frequency in which this paper is focused on.

Average Permeability μ_M

μ_M is approximated by an empirical formula shown in (5), [2]:

$$\mu_M = \frac{(\Delta B)^2 Fs}{K_c \cdot P_L \cdot 10^6}, \tag{5}$$

where $K_c = 1.2$ for square 80 permalloy core and $K_c = 1.08$ for mag. Inc. 2704A metglas core. P_L is core loss density (W/Ib) and Fs is switching frequency. ΔB is the total flux density transversed from t_1 and t_2 as shown in Fig. 2. μ_M value depends on core material used, switching frequency, S.R. design parameter and dc operation conditions.

Continuous MMF Mode Versus Discontinuous MMF Mode

It can be seen from (5) that if P_L were proportional to $(\Delta B)^2 Fs$, then μ_M would have been a constant. But for the two commonly used two materials, Square 80 permalloy and Mag. Inc. 2704A Metglass, μ_M increases with ΔB and increases with Fs. For the same reactor design, ΔB increases when the output choke L operates in the discontinuous mode. From the above discussion, μ_M value increases as converter operates in discontinuous mode.

Duty Cycle to Output Voltage Transfer Function F_F

F_F can be derived by using state space averaging technique [12], [13]. However, the results obtained in [12], [13] are applicable to the magamp power stage. The operation of a magamp power stage is identical to that of a buck converter power stage except that the former uses a magnetic switch and the later uses a semiconductor switch for pulse width modulation. The mathematics to derive the small signal transfer function F_F can therefore be avoided. Results obtained for Buck converter in the earlier literature [10], [11] are applicable to the magamp circuit and are shown in (6) and (7).

Continuous MMF Mode

$$F_{Fc} \triangleq \frac{\hat{V}_O}{\hat{d}} = \frac{V_O}{d}\left[\frac{1 + SR_CC}{1 + S(R_CC + L/R_L) + S^2LC}\right]. \tag{6}$$

Discontinuous MMF Mode

$$F_{Fd} \triangleq \frac{\hat{V}_O}{\hat{d}} = \frac{2V_O(1 - M)^{3/2}}{K^{1/2}M(2 - M)} \cdot \frac{1}{1 + S/\omega_p d}, \tag{7}$$

where

$$M \triangleq V_O/V_x$$

$$K \triangleq 2LFs/R_L$$

$$\omega_{pd} = (2 - M)/[(1 - M)R_LC].$$

IV. Open Loop Transfer Function $G(s)$

Using the results presented in Section III, the open loop transfer function G ($\triangleq \hat{V}_O/\hat{V}_E$) can be obtained. G function is the focus of control loop design. Based on this open loop transfer function, error amplifier compensation network can be designed to achieve certain desirable control characteristics.

External Reset Type

Referring to Fig. 4(a), the open loop transfer function for the external reset type G_{ext} is expressed by (8):

$$G_{\text{ext}}(S) = F_R \cdot F_M \cdot F_F(S). \tag{8}$$

From (2) and (4)–(6), G_{ext} can be obtained for the continuous MMF mode. G_{ext} for the continuous mode can be obtained from (2), (4), (5), and (7).

Continuous MMF Mode Versus Discontinuous MMF Mode

F_R is independent of mode of operation, independent of frequency but F_M and F_F are not. It was concluded in the section magnetic transfer function F_M that under the same line condition $|F_M|$ increases as the magamp enters discontinuous mode. From (6) and (7), it can be seen that F_F changes even more dramatically between continuous mode and discontinuous mode. F_F is a single-pole transfer function in a discontinuous mode and is a two-pole transfer function in a continuous mode.

Continuous Mode:

$$G_{c,\text{ext}(S)} = F_R \cdot F_M \cdot F_{Fc}(S) \tag{9}$$

Discontinuous Mode:

$$G_{d,\text{ext}(S)} = F_R \cdot F_M \cdot F_{Fd}(S). \tag{10}$$

Self Reset Type

Referring to Fig. 4(b), the open loop transfer function (open at the output of error amplifier E/A) $\hat{V}_O/\hat{V}_E$ is different from the external reset type. Because of the inner feedback path from V_O, the transfer function can be expressed as in (11):

$$G_{\text{self}}(S) \triangleq \frac{\hat{V}_O}{\hat{V}_E} = \frac{F_R \cdot F_M \cdot F_F(S)}{1 + F_R \cdot F_M \cdot F_F(S)}. \tag{11}$$

The name of the transfer function G_{self} is different from that of the transfer function G_{ext} shown in (8). This implies that the compensation network design is different for the two different reset circuits. It can be seen from (11) that low frequency gain G_{self} is always less than unity. The pole frequency of $G_{\text{self}}(S)$ is shifted to that of G_{ext}. The amount of shifting depends on magamp mode of operation as expressed by (12)–(14).

Continuous MMF Mode

It can be proved, through the reasoning of $F_{Fc}(S)$ characteristics, that $G_{c,\text{self}}$ is a two-pole transfer function with pole frequency expressed by (12), [1]:

$$G_{d,\text{self}}(S) = \frac{F_RF_MF_{Fc}(S)}{1 + F_RF_MF_{Fc}(S)}$$

$$\mu_{Pc,\text{self}} = \frac{1}{(LC)^{1/2}}\left[1 + F_RF_MF_{Fc}(0)\right]^{1/2} \tag{12}$$

$$\omega_{Pc,\text{ext}} = 1/(LC)^{1/2}. \tag{13}$$

Discontinuous MMF Mode

It can be proved that open loop gain $G_{d,\text{self}}$ can be expressed as (14):

$$G_{d,\text{self}} = \frac{\alpha}{1 + \alpha} \cdot \frac{1}{1 + S/\omega_{Pd,\text{self}}}, \tag{14}$$

TABLE I
THE TRANSFER FUNCTIONS OF CONTINUOUS MODE AND DISCONTINUOUS MODE ON BOTH TYPES RESETS

Trans. Function \ Types / Mode		External Reset Type (Type B)	Self Reset Type (Type A)
$F_R \triangleq \frac{\hat{I}_R}{\hat{V}_E}$	Continuous Mode / Discontinuous Mode	$\frac{-R_B}{(R_B + R_S)R_E}$	$\frac{-R_B}{(R_B + R_S)R_E}$
$F_M \triangleq \frac{\hat{d}}{\hat{I}_R}$	Continuous Mode / Discontinuous Mode	$\frac{-0.4\pi \cdot \mu_M \cdot N^2 \cdot Ae \cdot Fs}{le \cdot V_x \cdot 10^8}$	$\frac{-0.4\pi \mu_M \cdot N^2 \cdot Ae \cdot Fs}{le \cdot V_x \cdot 10^8}$
$F_F \triangleq \frac{\hat{V}_o}{\hat{d}}$	Continuous Mode (F_{Fc})	$\frac{V_O}{d}[\frac{1 + SR_CC}{1 + S(R_CC + L/R_L) + S^2LC}]$	$\frac{V_O}{d}[\frac{1 + SR_CC}{1 + S(R_CC + L/R_L) + S^2LC}]$
	Discontinuous Mode (F_{Fd})	$\frac{2V_O(1 - M)^{3/2}}{K^{1/2}M(2 - M)(1 + S/\omega p)}$	$\frac{2V_O(1 - M)^{3/2}}{K^{1/2}M(2 - M)(1 + S/\omega p)}$
Open Loop Gain (G) and Freq. Pole (ωp)	Continuous Mode	low freq. gain $G_{c,ext}(0)$: $F_RF_MF_{Fc}(0)$	low freq. gain $G_{c,self}$: $\frac{G_{c,ext}(0)}{1 + G_{c,ext}(0)}$
		freq. pole $\omega_{P1c,ext}$ $\omega_{P2c,ext}$: $\frac{1}{(LC)^{1/2}}$	freq. pole $\omega_{P1c,self}$ $\omega_{P2c,self}$: $\frac{[1 + G_{c,ext}(0)]^{1/2}}{(LC)^{1/2}}$
	Discontinuous Mode	low freq. gain $G_{d,ext}$: $F_RF_MF_{Fd}(0)$	low freq. gain $G_{d,self}$: $\frac{G_{d,ext}(0)}{1 + G_{d,ext}(0)}$
		freq. pole $\omega_{Pd,ext}$: $\frac{(2 - M)}{(1 - M)} \cdot \frac{1}{R_LC}$	freq. pole $\omega_{Pd,self}$: $[1 + G_{d,ext}(0)] \cdot \omega_{Pd,ext}$

$$\Delta B = \frac{V_xT \cdot 10^8}{NAe}\left(\frac{t_{on}}{T} - \frac{V_O + V_D}{V_x}\right) + \frac{(V_x - V_O - V_D)x10^8}{NAe}\left[\frac{(V_O + V_D)T}{V_x} - \left[\frac{2LT(P_O + P_B)(V_O + V_D)}{V_O(V_x - V_O - V_D)V_x}\right]^{1/2}\right]$$

$$\mu_M = \frac{(\Delta B)^2 Fs}{K_c \cdot P_L \cdot 10^6} \qquad M \triangleq V_O/V_x, \quad K \triangleq 2LFs/R_L$$

where

$$\alpha = F_R \cdot F_M \cdot F_{Fd}(S = 0)$$

$$\omega_{Pd,self} = (1 + \alpha)\omega_{Pd,ext} = (1 + \alpha) \cdot \frac{2 - M}{1 - M} \cdot \frac{1}{R_LC}$$

The details of the derivation are given in the Appendix. It is seen from (14) that $|G_{d,self}|$ is less than unity and the pole frequency of $G_{d,self}$ is shifted upward by a factor of $(1 + \alpha)$ when compared to the pole frequency of $G_{d,ext}$.

Table I summarizes the transfer functions for both types of reset circuit for both continuous mode and discontinuous mode.

V. EXPERIMENTAL VERIFICATION

To verify the model described, an experimental circuit shown in Fig. 5 was used. Both types of reset circuit can be tested. To make open loop gain measurement under close loop condition, a perturbing signal $\hat{V}_E$ is injected at Node A. Open loop gain G ($\triangleq \hat{V}_O/\hat{V}_E$) is then measured and plotted. Fig. 6 shows the open loop gain plot for both modes of operation. Fig. 7 shows V/F characteristics of the technique. The theoretical prediction agrees well with the measured results. A step-by-step procedure for using the equation formulated in this paper is presented in the following example.

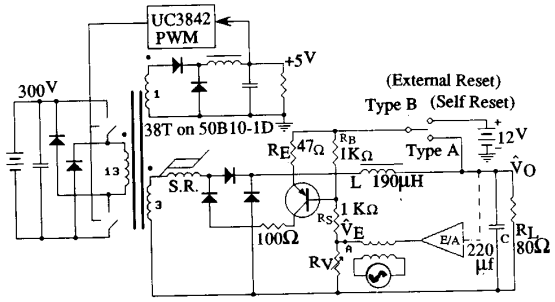

Fig. 5. Experiment circuit for loop gain measurement. Load resistor R_L is adjusted to have discontinuous mode of operation.

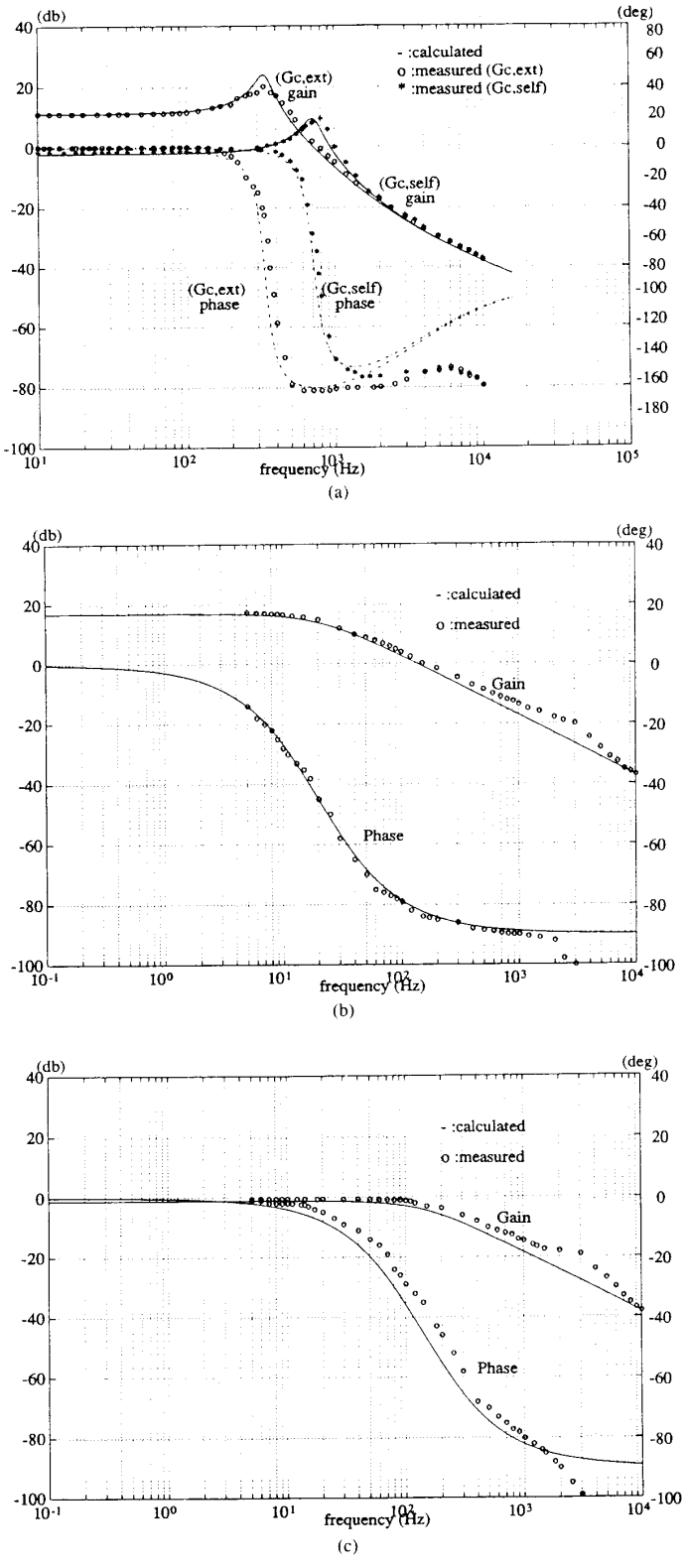

Fig. 6. Bode plots of open loop transfer functions. (a) Continuous mode, external reset, and self reset. (b) Discontinuous mode, external reset. (c) Discontinuous mode, self reset.

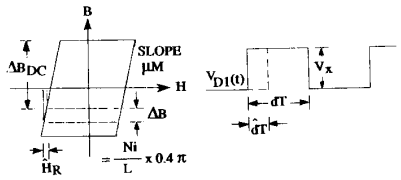

Fig. 7. *B-H* characteristics and waveform.

Model Parameters Calculation for Discontinuous Mode

Magamp power circuit and reset circuit parameters are as follows.

$Fs = 50$ kHz, $L = 190$ uh, $C = 220$ uf, $R_B = 1$ kΩ

$Rs = 1$ kΩ, $R_E = 47$ Ω, $V_x = 72$ V, $Vo = 12$ V

$R_L = 80$ Ω, transistor Q duty cycle = 25%.

Saturable reactor parameters are as follows.

$N = 38$, $A_e = 7.6 \cdot 10^{-6}$ m^2, $le = 6.18 \cdot 10^{-2}$ m,

Material: Square 80 Permalloy (Mag. Inc. 50B10-1D).

Find: Open loop gain transfer function.

Step I: Calculation of F_R: Using (2), $F_R = -1/(1 + 1) \cdot 47 = -0.0106383$.

Step II: Calculation of F_M: To find out F_M, μ_M must be determined.

a) Find ΔB for a discontinuous mode of operation. ΔB is expressed as follows [3]:

$$\Delta B = \frac{V_x T \cdot 10^8}{NAe}\left(\frac{t_{on}}{T} - \frac{V_O + V_D}{V_x}\right) + \frac{(V_x - V_O - V_D)x\ 10^8}{NAe} \cdot \left[\frac{(V_O + V_D)T}{V_x} - \left[\frac{2LT(P_O + P_B)(V_O + V_D)}{V_O(V_x - V_O - V_D)V_x}\right]^{1/2}\right].$$

Using $V_D = 1$ V, $P_O + P_B = (12)^2/80$.

ΔB discon = 3560.95 G is larger than 1

ΔB = 3462.6 G (cont.) + 3560.95 G (discont.)
= 7023.55 G.

b) Find core losses at $\Delta B/2 = 3511.78$ G and 50 kHz using core catalog, $P_L = 59.72$ W/lb.

c) Calculate μ_M using (5), $\mu_M = 34417.74$.

d) Find F_M using (4), $F_M = 5.34$.

Step III: Determination of F_F: From (7), $M = 12/72 = 0.1667$, $K = 0.2375$

$$F_{Fd} = \frac{2 \cdot 12 \cdot (1 - 0.1667)^{3/2}}{0.2375^{1/2} \cdot 0.1667 \cdot (2 - 0.1667)} \cdot \frac{1}{1 + S/\omega_{Pd}} = 122.61/(1 + S/\omega_{Pd})$$

$$\omega_{Pd} = (2 - 0.1667)/[(1 - 0.1667) \cdot 80 \cdot 220 \cdot 10^{-6}] = 125 \text{ rad/s } (19.90 \text{ Hz})$$

Step IV: Determination of open loop gain transfer functions:

a) External reset type: From (10), (7), (4) and (2):

$$G_{d,\text{ext}}(S) = F_R F_M F_{Fd}(0)/(1 + S/\omega_{Pd,\text{ext}}) = 6.96/(1 + S/125)$$

b) Self reset type: From (14),

$$G_{d,\text{self}}(S) = 6.96/(1 + 6.96)\,[1/(1 + \omega_{Pd,\text{self}})] = 0.85/(1 + S/995)$$

$$\omega_{Pd,\text{self}} = (1 + 6.96) \cdot \omega_{Pd,\text{ext}} = 995 \text{ rad/s } (158.4 \text{ Hz}).$$

VI. Conclusion

The models developed can be used to predict the small signal control loop behavior of a voltage mode magamp post regulator for both the continuous mode and the discontinuous mode of operation. Two commonly used reset schemes—an external reset type and a self-reset type are considered. It is mathematically shown that the open loop gain is a two-pole, single-zero transfer function for continuous mode operation and is a single pole transfer function for discontinuous mode operation.

The equations for predicting the open loop gains for both types of reset circuits are derived and verified experimentally. It is shown that the open loop gain characteristics of a magamp regulator depends on power circuit parameters, the reset circuit parameters, and the saturable reactor parameters. Therefore, in a normal design procedure of a magamp, if the design parameters of the saturable reactor are changed, a corresponding change of the compensation network must be made to optimize the control performance.

The models presented provide the deisgner with a tool to facilitate the feedback loop design of a voltage mode magamp post regulator. This work also lays the foundation for modeling the control behavior of a magamp regulator with a more sophisticated control scheme such as a current-mode multiple feedback control.

VII. Appendix
Derivation of (4) and (14)

Derivation of (4)

From definition, $F_M \triangleq \hat{d}/\hat{I}_R$

from Ampere's law, $\hat{I}_R = l_e \cdot \hat{H}_R/N \cdot 0.4\pi$ (15)

from *B-H* characteristics, $\hat{H}_R = \Delta\hat{B}/\mu_M$ (16)

from Faraday's Law, $V_x = N \cdot Ae \cdot (\Delta B) \cdot 10^{-8}/\Delta t$, (17)

perturbing (17) by a small ac signal,

$$\Delta B = \Delta B_{dc} + \Delta \hat{B} \text{ and } \Delta t = dT - \hat{d}T,$$

and eliminating dc quantity,

$$-V_x \cdot \hat{d}T = N \cdot Ae \cdot \Delta B \times 10^{-8}. \tag{18}$$

Using (15), (16), and (18):

$$\hat{I}_R = \frac{-le \cdot \dfrac{\Delta \hat{B}}{\mu_M}}{N \cdot 0.4\pi} = \frac{\dfrac{l_e}{\mu_M} \cdot \dfrac{V_x \cdot \hat{d}T \cdot 10^8}{N \cdot Ae}}{N \cdot 0.4\pi},$$

so that

$$\frac{\hat{d}}{\hat{I}_R} = \frac{-0.4\pi \cdot \mu_M N^2 \cdot Ae \cdot Fs}{l_e \cdot V_x \cdot 10^8}.$$

μ_M is an average permeability, which depends on operating dc flux density and frequency. The empirical relationship is given by (5), [1].

Derivation of (14)

From (11),

$$G_{self(S)} = \frac{F_R F_M F_F(S)}{1 + F_R F_M F_F(S)}. \tag{19}$$

From (7),

$$F_F(S) = \frac{2V_O(1 - M)^{3/2}}{K^{1/2}M(2 - M)} \cdot \frac{1}{1 + S/\omega_p}. \tag{20}$$

Remove (20),

$$F_F(S) = F_F(0) \cdot \frac{1}{1 + S/\omega_p}. \tag{21}$$

Substituting (21) into (19),

$$G_{self}(S) = \frac{F_R F_M F_F(0)\,(1 + S/W_p)^{-1}}{1 + F_R F_M F_F(0)\,(1 + S/W_p)^{-1}},$$

defining $\alpha = F_R F_M F_F(0)$

$$G_{self} = \frac{\alpha \cdot (1/1 + S/\omega_p)}{1 + \alpha \cdot \dfrac{1}{1 + S/\omega_p}} = \frac{\alpha}{1 + S/\omega_p + \alpha}$$

$$= \frac{\alpha/1 + \alpha}{1 + \dfrac{S}{(1 + \alpha)\omega_p}}.$$

defining $\omega_p \text{self} = (1 + \alpha)\omega_p$

$$G_{self} = \frac{\alpha}{1 + \alpha} \cdot \frac{1}{1 + S/\omega_p \text{self}}.$$

References

[1] D. Chen, J. Lee, and C. Jamerson, "A simple model predicts small signal control loop behavior of magamp post regulator," *Rec. High Frequency Conf.*, 1988.

[2] C. Jamerson, "Calculation of magnetic amplifier post regulator voltage control loop parameters," in *High Frequency Power Conversion Conf. Rec.*, 1988.

[3] J. Lee, D. Chen, and C. Jamerson, "Magamp post regulators—practical considerations to allow operation under extreme loading conditions," in *IEEE APEC Rec.*, 1988.

[4] R. M. Tedder, "Limitations of the magamp regulator and an improved magamp choke design procedure," in *IEEE APEC Conf. Rec.*, Feb. 1988.

[5] T. Koyashiki and T. Ogata, "Design considerations in multi-output dc converter with magnetic amplifiers," in *Fifth International Telecommunications Energy Conf. Rec.*, 83CH1855-6, paper 12-3, pp. 388-394, Oct. 1983.

[6] K. Harada, T. Nabeshima, R. Hirmatsu, and I. Morigoe, "A dc converter controlled by magnetic amplifiers with 1 Mhz switching," in *IEEE Power Electronics Specialists Conf. Rec.*, 85CH2000-8, pp. 382-387, June 1984.

[7] A. Urling, T. Wilson, H. Owen, G. Gromwell, and J. Paulakonis," Modeling the frequency domain behavior of magnetic amplifier controlled high frequency switched mode power supplies," in *IEEE APEC Rec.*, 1987.

[8] "Using an integrated controller in the design of magamp output regulators," *Unitrode Applications Note* U-109.

[9] R. Hiramatsu and C. Mullet, "Using saturable reactor control in 500 kHz converter design," in *Proc. Tenth International Solid State Power Conversion Conf.*, paper F2, pp. 1-10, Mar. 1983.

[10] R. D. Middlebrook, "Describing function properties of a magnetic pulsewidth modulator," in *IEEE PESC Rec.*, 1972.

[11] Bulletin No. SR-4, Technical Bulletin, *Magnetics, Inc.*

[12] S. Ćuk and R. D. Middlebrook, "A general unified approach to modelling switching dc to dc converters in discontinuous mode," in *IEEE PESC Rec.*, 1977, pp. 36-57.

[13] R. D. Middlebrook and S. Ćuk, "A general switching—converter power stages," in *IEEE PESC Conf. Rec.*, 1976, pp. 18-34.

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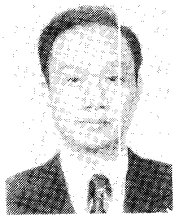

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