Design Example Report

Title	***3W Wide Range Flyback Power Supply using LNK304P***
Specification	Input: 57-580VAC Output: 12V / 250mA
Application	Utility Meter
Author	Power Integrations Applications Department
Document Number	DER-58
Date	May 4, 2005
Revision	1.0

Summary and Features

- StackFET^{TM} Flyback Topology delivers full load over extremely wide input AC voltage range
- LinkSwitch-TN feedback simplifies non-isolated voltage regulation – 2 resistors precisely set the output voltage
- E-SHIELD^{TM} Transformer Construction for reduced common-mode EMI (>10dB margin)
- 66kHz Switching Frequency with jitter to reduce conducted EMI
- Simple ON/OFF controller – no feedback compensation required
- Auto-restart function for automatic and self-resetting open-loop, overload and short-circuit protection
- Built-in Hysteretic thermal shutdown at 135C
- EcoSmart for extremely low standby power consumption <200mW at 265VAC

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5245 Hellyer Avenue, San Jose, CA 95138 USA.
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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

Design Reports contain a power supply design specification, schematic, bill of materials, and transformer documentation. Performance data and typical operation characteristics are included. Typically only a single prototype has been built.

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1. Introduction

This document is an engineering report describing a wide-range non-isolated StackFET® Flyback converter employing the LNK304P.

The document contains the power supply specification, schematic, bill-of-materials, transformer documentation, printed circuit layout, and performance data.

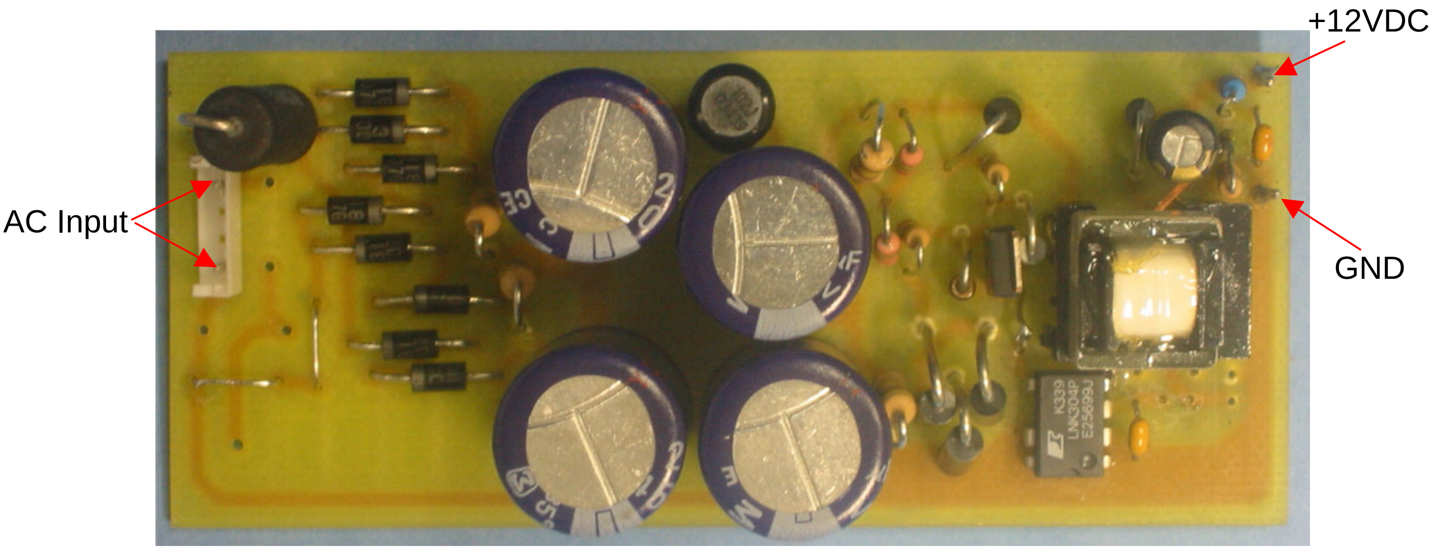

Figure 1 – Populated Circuit Board Photograph

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2. Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	57		580	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (240 VAC)				0.2	W	
Output						
Output Voltage 1	V_{OUT1}		12		V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$				mV	20 MHz Bandwidth
Output Current 1	I_{OUT1}			0.25	A	
Total Output Power						
Continuous Output Power	P_{OUT}			3	W	
Efficiency	η	45			%	Measured at P_{OUT} (3 W), 25 ^{o}C
Environmental						
Conducted EMI		Meets CISPR22B / EN55022B				
Safety		Class I (non-Isolated)				
Ambient Temperature	T_{AMB}	0		60	^{o}C	Free convection, sea level

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3. Schematic

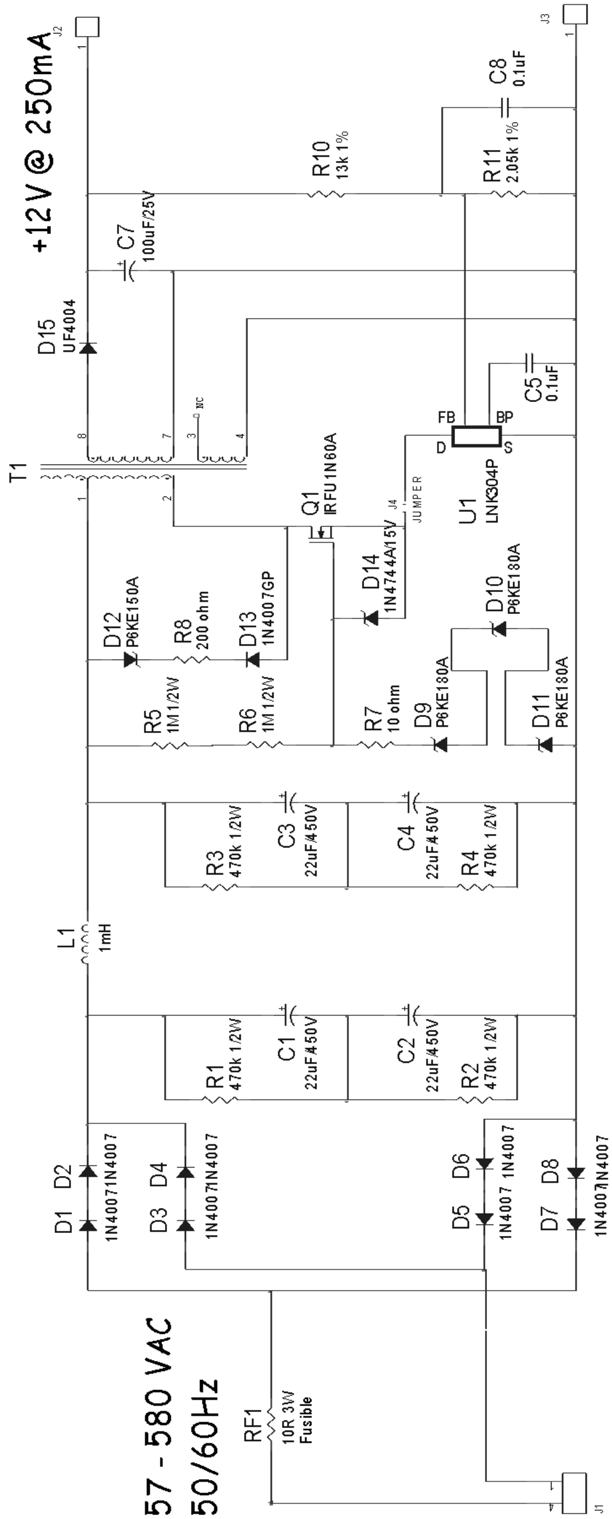

Figure 2 –Schematic

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4. Circuit Description

RF1 is a fusible link resistor, which limits inrush current through the full-bridge rectifier comprised of D1 to D8. This resistor also complies with safety agency requirements to blow open in the event of a catastrophic failure in the power supply.

AC voltage is rectified through the full-bridge rectifier stage and filtered to produce a DC voltage across the series stacked high voltage electrolytic capacitors C1-C4. R1, R2 and R3, R4 help maintain voltage equalization across the series connected capacitors C1, C2 and C3, C5 respectively. L1, C1-C4 forms an input pi filter to reduce components of the switching frequency and its harmonics on the input line.

The rectified high voltage DC is applied to the transformer (T1) primary. The other end of the transformer primary winding is connected to a high-voltage (600V) MOSFET (Q1) that is cascode connected to the Drain of the LinkSwitch-TN Switch (U1). In this configuration the effective Drain-Source voltage rating of the primary is 1300Vpk.

D9-D11 clamps the maximum drain-source voltage across the LinkSwitch-TN (U1) to below 600V. D14 ensures that the maximum gate-source voltage of Q1 does not exceed 15V. R5 and R6 provide bias to enhance the gate of Q1 when its source is switched low by the drain of U1.

D12, D13 and R8 clamp the leakage inductance spike to limit the effective VDS (voltage across Q1 and U1) to about 980Vpk at high line (580VAC) input. C5 is the VCC storage capacitor for U1; this capacitor is charged to 5.8V from the internal high voltage current source, U1 derives its bias from this capacitor.

D15 and C7 rectify and filter the AC waveform produced from the transformer secondary winding to produce the desired DC voltage level. R10 and R11 form a potential divider that controls the output voltage. The midpoint of this divider is connected to the EN pin of U1 that is internally set at 1.63VDC. The simple ON/OFF controller integrated in the LinkSwitch-TN series switches the internal 700V MOSFET at 66kHz to maintain the output voltage set point. C8 is added across R11 to increase noise immunity in the event of transients caused by the load.

The transformer was wound with shields to counteract common-mode displacement currents generated by the windings in the transformer (ESHIELD™). This technique helps reduce conducted EMI and the burden on the input EMI filter. The primary winding was also wound with a Z-winding technique to reduce its self-capacitance and switching losses in the converter.

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5. PCB Layout

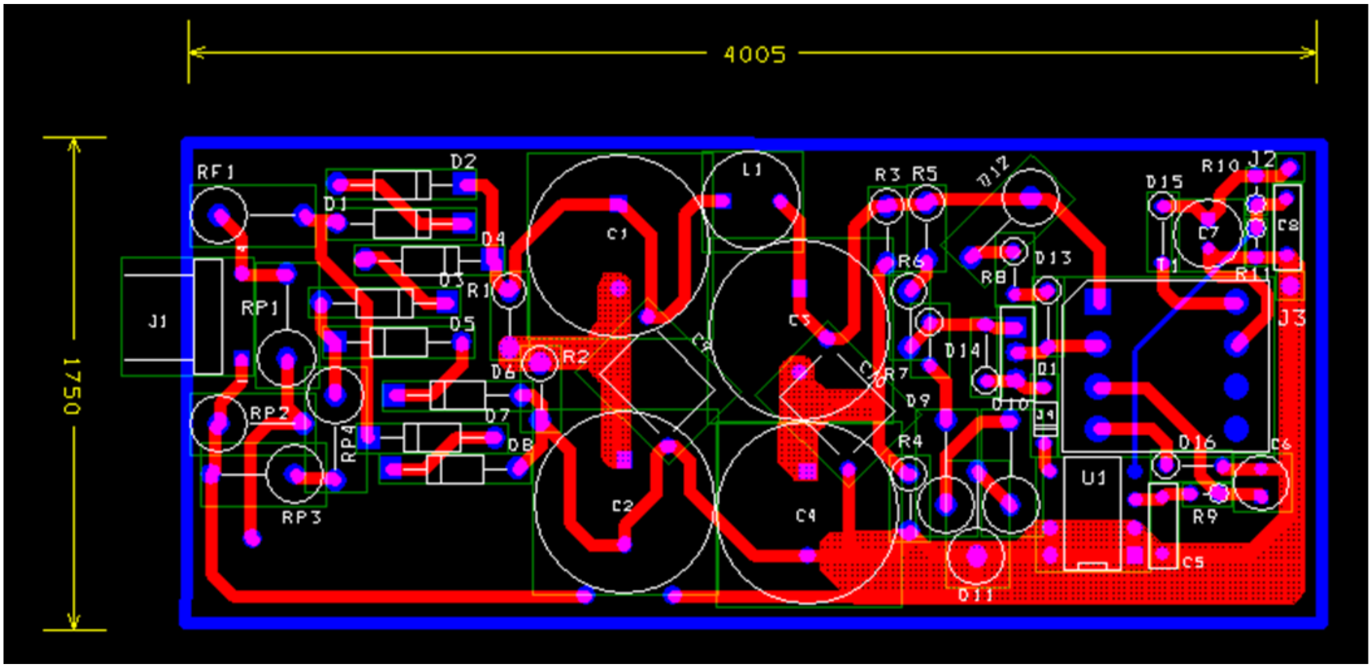

Figure 3 – Printed Circuit Layout

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6. Bill Of Materials

Item	*QTY*	*Ref Des*	*Value*	*Manufacturer*	*Part Number*
1	4	C1, C2, C3, C4	22uF/450V		
2	2	C5, C8	0.1uF		
3	1	C7	100uF/25V		
4	9	D1, D2, D3, D4, D5, D6, D7, D8, D13	Stand. Rec. 1A/1000V		1N4007GP
5	3	D9, D10, D11	TVS 180V		P6KE180A
6	1	D12	TVS 150V		P6KE150A
7	1	D14	Zener 15V		1N4744A
8	1	D15	Ultrafast 1A/200V		UF4004
9	1	J4	JUMPER		
10	1	L1	1mH	Toko	8RB-102Y
11	1	Q1	N-Chan. MOSFET 1A/600V	International Rectifier	IRFU1N60A
12	4	R1, R2, R3, R4	470k 1/2W		
13	2	R5, R6	1M 1/2W		
14	1	R7	10 ohm		
15	1	R8	200 ohm		
16	1	R10	13k 1%		
17	1	R11	2.05k 1%		
18	1	RF1	10R 3W		
19	1	T1	EE13 Transformer		
20	1	U1	PWM + MOSFET	Power Integrations	LNK304P

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7. Transformer Specification

7.1. *Transformer Electrical Diagram*

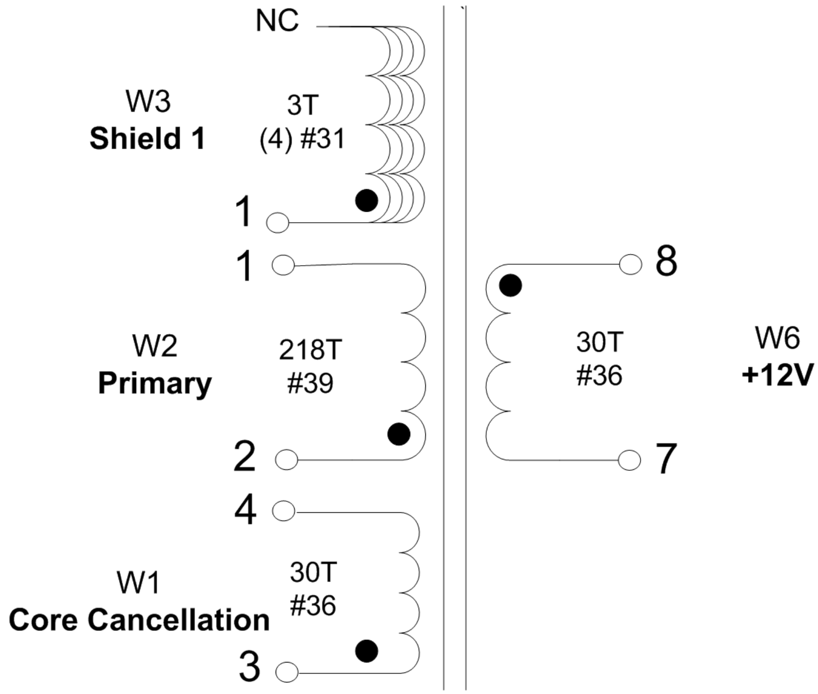

Figure 4 –Transformer Electrical Diagram

7.2. *Electrical Specifications*

Electrical Strength	60Hz 1minute, from Pins 1-4 to Pins 7-8	N/A
Primary Inductance (Pin 1 to Pin 2)	All windings open	2.7mH +/- 10%
Resonant Frequency	All windings open	500 kHz min.
Primary Leakage Inductance	L_{12} with pins 7-8 shorted	100μH max.

7.3. *Materials*

Item	Description
[1]	Core: EE13, TDK Gapped for A_L = 57 nH/T^2
[2]	Bobbin: Horizontal 8 pins
[3]	Magnet Wire: #36 AWG
[4]	Magnet Wire: #39 AWG
[5]	Magnet Wire: #31 AWG
[6]	Tape: 3M 1298 Polyester Film (white) 0.311” x 2 mils
[7]	Varnish

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7.4 Transformer Build Diagram

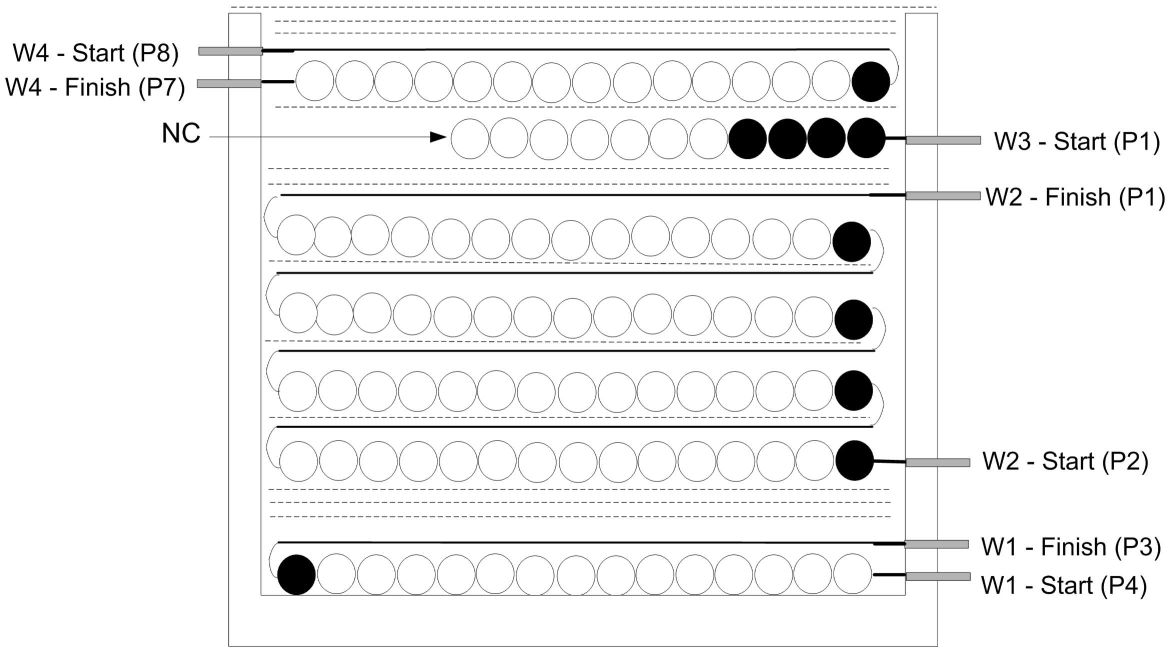

Figure 5 – Transformer Build Diagram

7.5 Transformer Construction

W1 (Core Cancellation Winding)	Start at pin 6 temporarily. Wind 30 turns of item [3] from left to right uniformly without any space between turns, in a single layer across the entire width of the bobbin. Finish on Pin 4. Move the start end from pin 6 to pin 3.
Insulation	Add 4 layers of tape [6] for insulation.
W2 (Primary Winding)	Start at pin 2. Wind 55 turns of item [4] from right to left. After finishing the first layer, return to the right and add one layer of tape [6]. Then wind 55 turns of item [4] from right to left, after finishing the second layer, return to the right and add one layer of tape [6]. Then wind 54 turns of item [4] from right to left, after finishing the second layer, return to the right and add one layer of tape [6]. Again, wind 54 turns of item [4] from right to left, after finishing the fourth layer, return to the right and finish on Pin 1. Wind all layers uniformly without any spaces between the turns.
Insulation	Add 3 layers of tape [6] for insulation.
W3 (Shield Winding)	Start of pin 1, wind 3 turns of quadfilar item [5]. Wind from right to left in a single layer across 60% of the bobbin width. Cut the wires after finishing the third turn.
Insulation	Add 1 layer of tape [6] for insulation.
W4 (Secondary Winding)	Temporarily start at pin 3. Wind 30T of item [3] from right to left in a single layer without any spaces between adjacent turns, across the entire width of the bobbin, finish on pin 7. Then move the Start lead to pin 8.
Outer Insulation	Add 2 layers of tape [6] for insulation.
Final Assembly	Use guidelines specified in AN-24 for audio noise suppression techniques in the transformer construction.

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7.6 Design Notes

Power Integrations Device	LNK304P
Frequency of Operation	66 KHz
Mode	Continuous/ discontinuous
Peak Current	0.23 A
Reflected Voltage (Secondary to Primary)	92V
Maximum AC Input Voltage	580 V
Minimum AC Input Voltage	57 V

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8. Transformer Spreadsheets

Rev 1.0	INPUT		OUTPUT		TinySwitch-II_022001.xls: TINYSwitch-II Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					
VACMIN	57			Volts	Minimum AC Input Voltage
VACMAX	580			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	12			Volts	Output Voltage
PO	3			Watts	Output Power
n	0.6				Efficiency Estimate
Z	0.5				Loss Allocation Factor
VB	12			Volts	Bias Voltage
tC	3			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	22			uFarads	Input Filter Capacitor
ENTER TinySwitch-II VARIABLES					
TNY-II	lnk304			*Universal*	*115/230V*
Chosen Device	*LNK304*		*Power Out*	*5.5W*	*8W*
ILIMITMIN			*0.233*	Amps	
ILIMITMAX			*0.267*	Amps	
fS	66000			Hertz	Typical Switching Frequency
fSmin			57000	Hertz	Minimum Switching Frequency (inc jitter deviation)
fSmax			74000	Hertz	Maximum Switching Frequency (inc jitter deviation)
VOR	92.1			Volts	Reflected Output Voltage
VDS	10			Volts	TOPSwitch on-state Drain to Source Voltage
VD	0.7			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.7			Volts	Bias Winding Diode Forward Voltage Drop
KP	**0.86**				Bias Winding Diode Forward Voltage Drop
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	ee13				
Core		*#N/A*		*P/N:*	*#N/A*
Bobbin		*#N/A*		*P/N:*	*#N/A*
AE		0.171		cm^2	Core Effective Cross Sectional Area
LE		3.02		cm	Core Effective Path Length
AL		1130		nH/T^2	Ungapped Core Effective Inductance
BW		7.4		mm	Bobbin Physical Winding Width
M	0			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	**4**				Number of Primary Layers
NS	**30**				Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			58	Volts	Minimum DC Input Voltage
VMAX			820	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.66		Maximum Duty Cycle
IAVG			0.09	Amps	Average Primary Current
IP			0.23	Amps	Peak Primary Current
IP Effective			0.23		
IP Actual			0.233		Actual IP figure = Device I_LIMIT
fSact					Actual Effective Switching Frequency
IR			0.20	Amps	Primary Ripple Current
IRMS			0.12	Amps	Primary RMS Current
TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			2682	uHenries	Primary Inductance
NP			218		Primary Winding Number of Turns
NB			30		Bias Winding Number of Turns
ALG		57		nH/T^2	Gapped Core Effective Inductance
BM			**1666**	Gauss	Maximum Flux Density at PO, VMIN (BM<3000)
BP			**1925**	Gauss	Peak Flux Density (BP<4200)
BAC		716		Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		1588			Relative Permeability of Ungapped Core
LG			**0.36**	mm	Gap Length (Lg > 0.1 mm)
BWE		29.6		mm	Effective Bobbin Width
OD			0.14	mm	Maximum Primary Wire Diameter including insulation
INS		0.03		mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.10	mm	Bare conductor diameter
AWG			38	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		16		Cmils	Bare conductor effective area in circular mils
CMA	Warning		**137**	Cmils/Amp	!!!!!!!!! INCREASE CMA>200 (increase L(primary layers),decrease NS,larger Cor
TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT / SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			1.68	Amps	Peak Secondary Current
ISRMS			0.61	Amps	Secondary RMS Current
IO			0.25	Amps	Power Supply Output Current
IRIPPLE			0.55	Amps	Output Capacitor RMS Ripple Current
CMS		122		Cmils	Secondary Bare Conductor minimum circular mils
AWGS			29	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.29	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.25	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS			-0.02	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS					
VDRAIN	Warning		1034	Volts	!!!!!!!!! REDUCE DRAIN VOLTAGE Vdrain<680
PIVS			125	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			125	Volts	Bias Rectifier Maximum Peak Inverse Voltage

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9. Performance Data

9.1. Efficiency and Standby Power Consumption

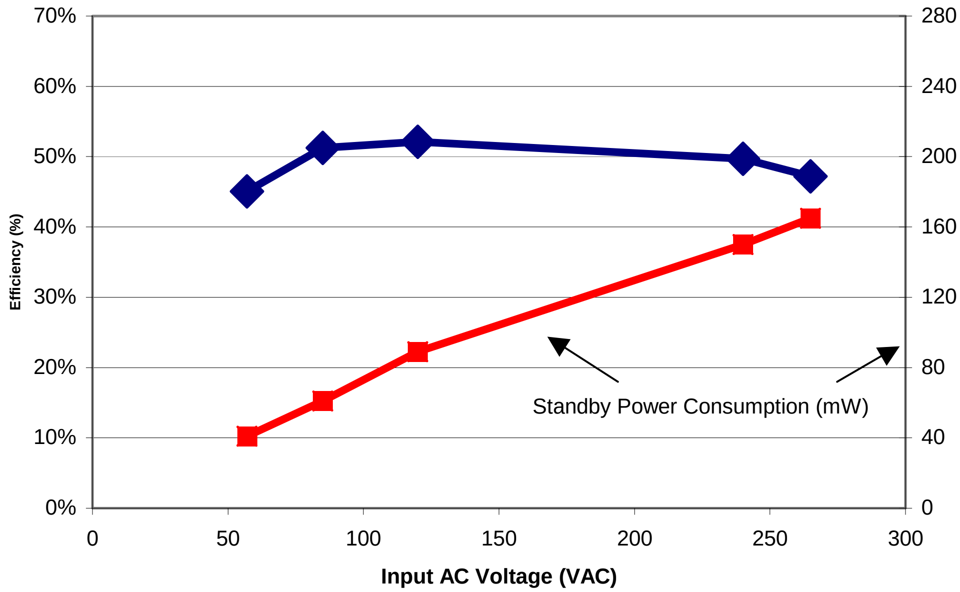

Figure 6 - Efficiency and Standby Power Consumption vs. Input Voltage, Room Temperature, 60 Hz

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9.2. Regulation

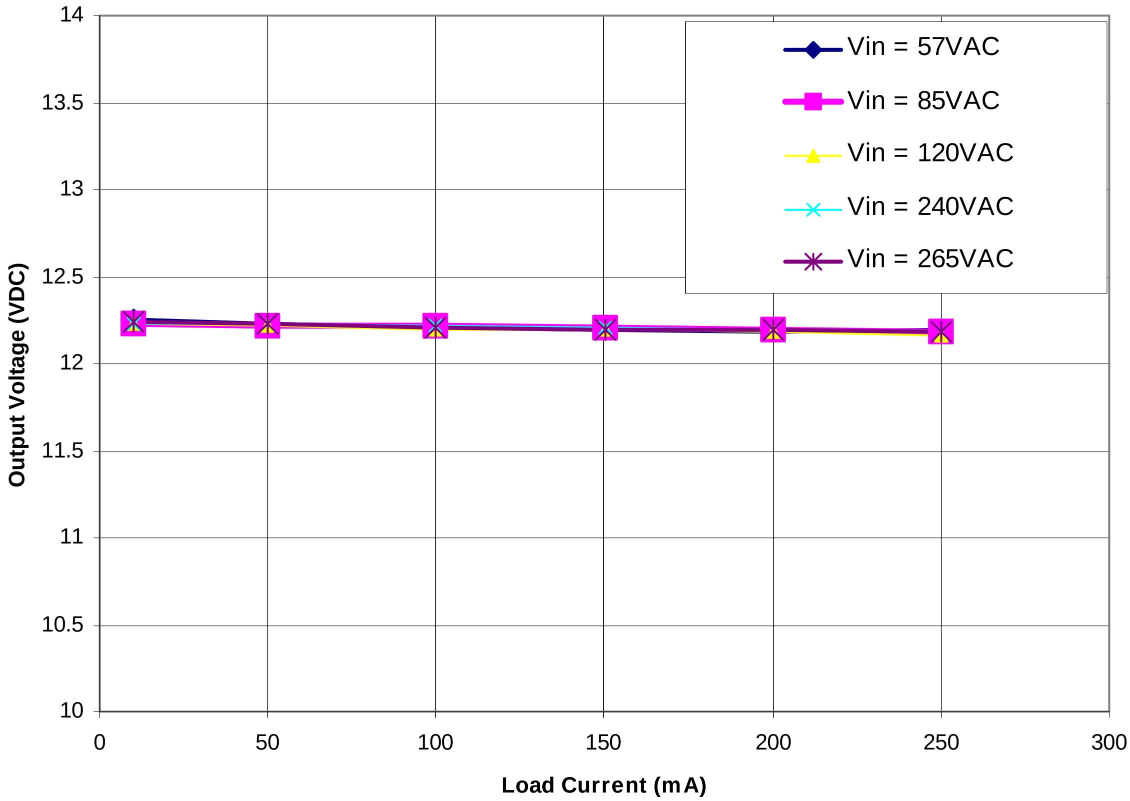

Figure 7 –Load Regulation, Room Temperature.

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10. Waveforms

10.1. Drain Voltage and Current, Normal Operation

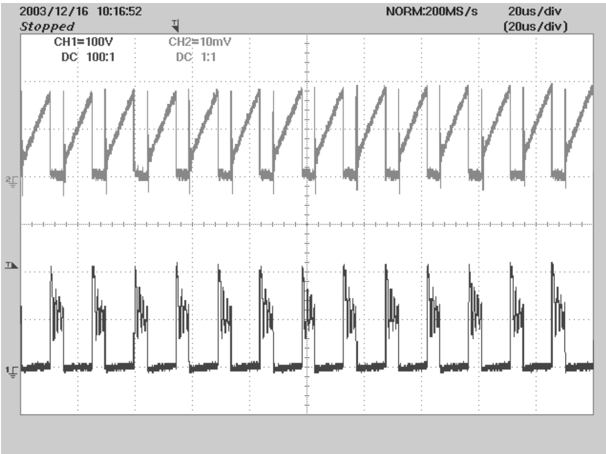

Figure 8 - 57VAC, Full Load *(LNK304)*
Upper: I_{DRAIN}, 0.1 A / div
Lower: V_{DRAIN}, 100 V, 20 μs/div

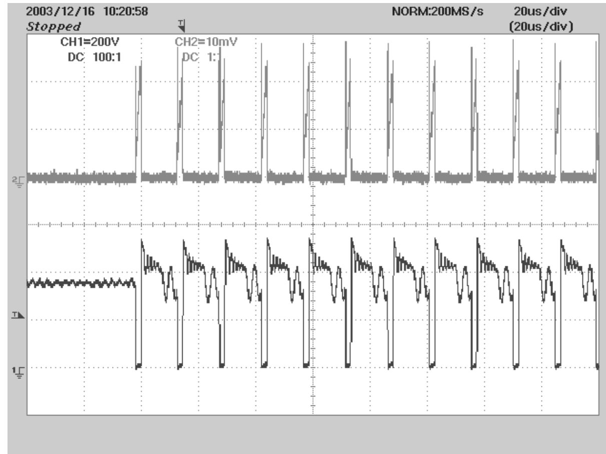

Figure 9 - 265VAC, Full Load *(LNK304)*
Upper: I_{DRAIN}, 0.1 A / div
Lower: V_{DRAIN}, 200 V / div, 20 μs/div

10.2. Output Voltage Start-up Profile at Full Load

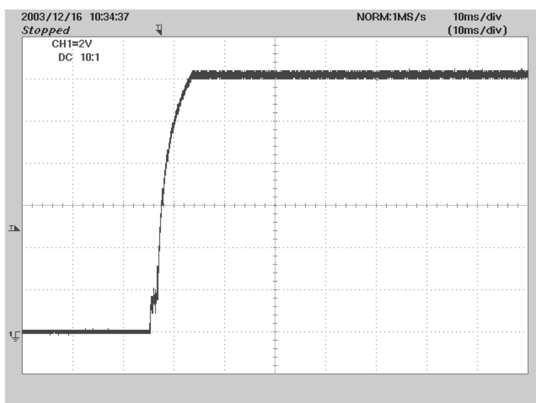

Figure 10 - Start-up Profile +12V @ 250mA 120VAC/60Hz
2V/div, 10msec/div.

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10.3. Drain Voltage and Current Start-up Profile

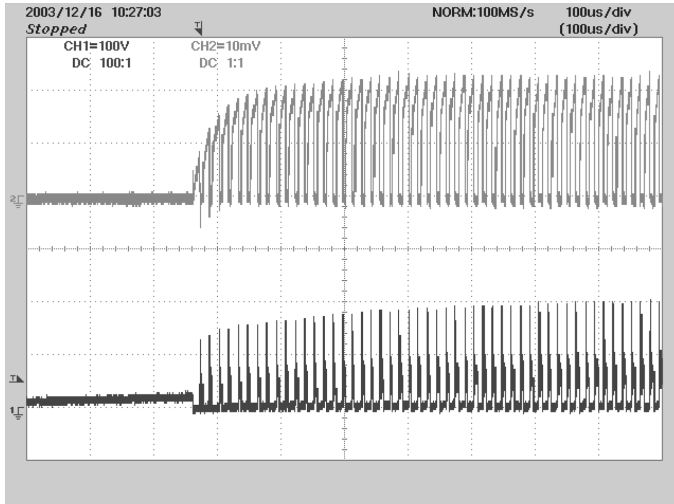

Figure 11 - 57 VAC Input and Maximum Load. Upper: I_{DRAIN}, 0.1 A / div *(LNK304)*
Lower: V_{DRAIN}, 100 V & 1 ms / div.

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10.4. Load Transient Response at 120VAC (50% to 100% Load Step)

In the figures shown below, signal averaging was used to better enable viewing the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving the contribution only from the load step response.

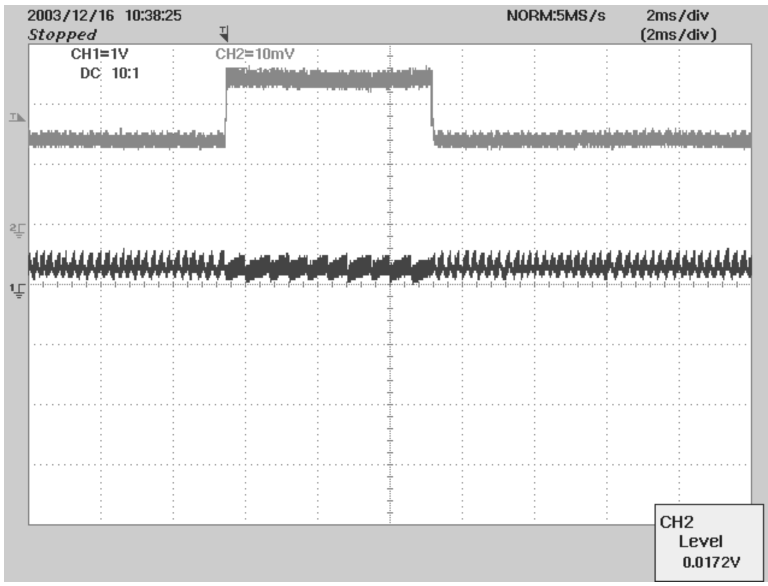

Figure 12 – Transient Response +5V, 50%-100%-50% Load Step.
Load Current, 100mA/div.
Output Voltage
1V, 2ms / div. (+12V Offset)

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10.5. Output Ripple Measurements

10.5.1. Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 13 and Figure 14.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. ***The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).***

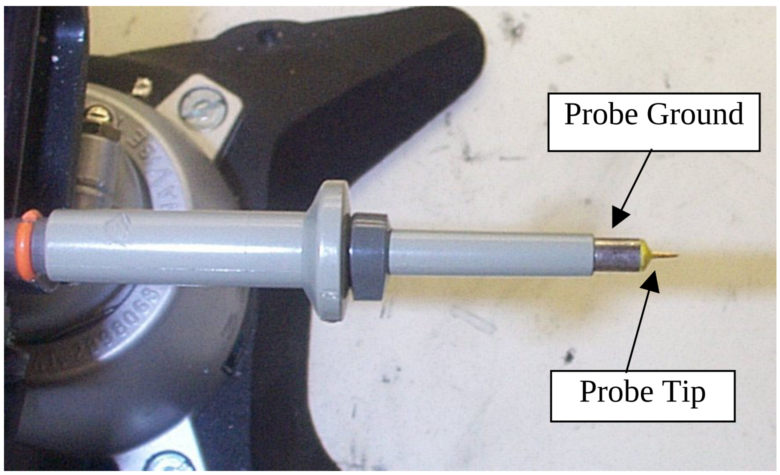

Figure 13 - Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

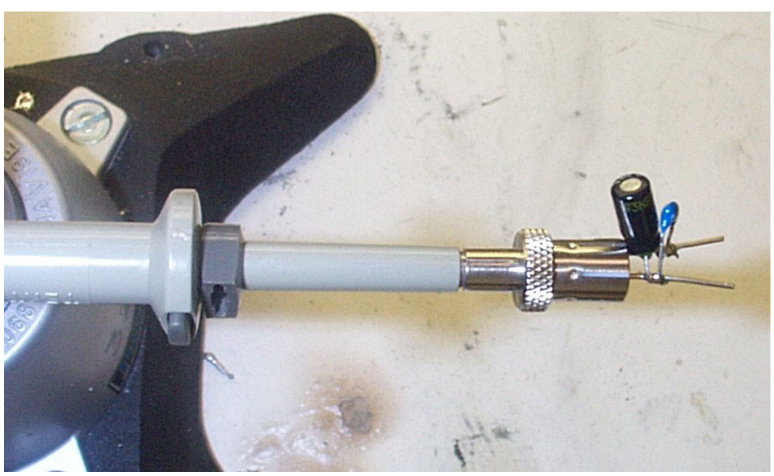

Figure 14 - Oscilloscope Probe with Probe Master 5125BA BNC Adapter. (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added)

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10.5.2. Measurement Results at Full Load

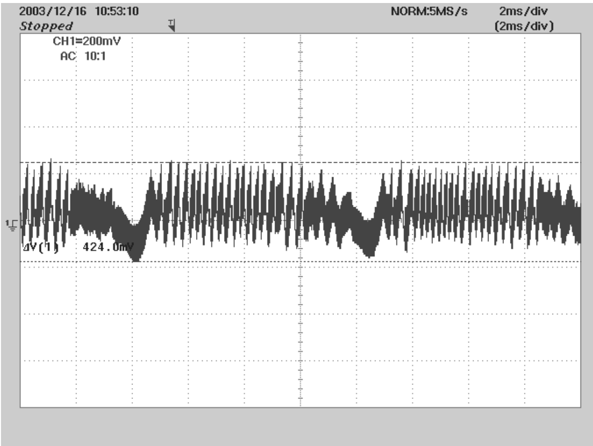

Figure 15 +12V Ripple @ 57VAC
2ms, 200 mV / div

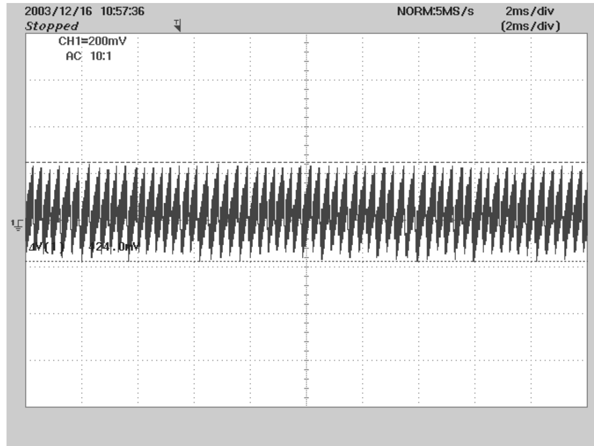

Figure 16 +12 V Ripple @ 265VAC
2 ms, 200 mV / div

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11. Conducted EMI

A conducted EMI scan of the prototype was taken to determine the effectiveness of the input pi-filter and transformer ESHIELD™ construction. The following plots show the peak performance of the converter against quasi-peak (QP) and average (AVG) limits of EN55022 Class B. Both scans were taken at 120VAC/60Hz input with maximum load applied to the output (250mA). Since the peak scan is below the average limits, it is expected that the QP and Average scans would have greater than 10db of margin below the limits.

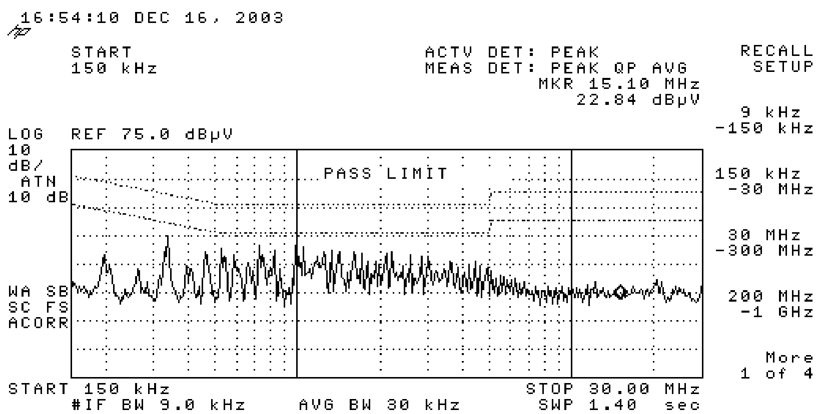

Figure 17 - Conducted EMI (Neutral)

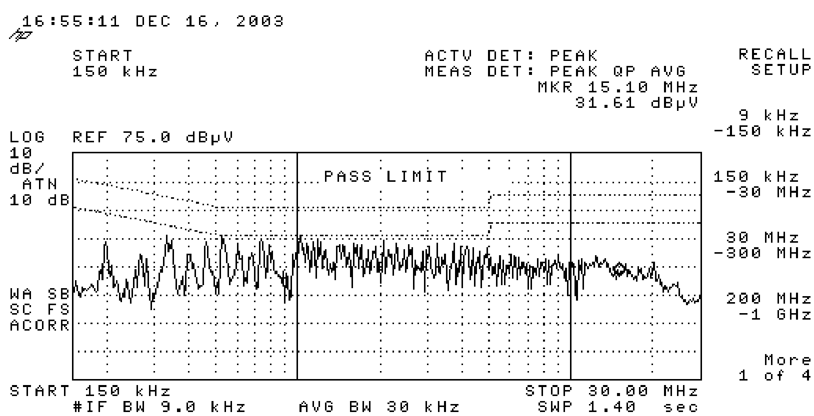

Figure 18- Conducted EMI (LINE)

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Revision History

Date	Author	Revision	Description & changes	Reviewed
May 4, 2005	RSP	1.0	Initial Release	VC /JC / AM

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PATENT INFORMATION

The products and applications illustrated herein (including circuits external to the products and transformer construction) may be covered by one or more U.S. and foreign patents or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at *www.powerint.com*.

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WORLD HEADQUARTERS
5245 Hellyer Avenue,
San Jose, CA 95138, USA
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

GERMANY
Rueckertstrasse 3,
D-80336, Munich, Germany
Phone: +49-895-527-3910
Fax: +49-895-527-3920
e-mail: eurosales@powerint.com

JAPAN
Keihin-Tatemono 1st Bldg.
12-20 Shin-Yokohama,
2-Chome,
Kohoku-ku, Yokohama-shi,
Kanagawa 222-0033, Japan
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

TAIWAN
17F-3, No. 510,
Chung Hsiao E. Rd., Sec. 5,
Taipei, Taiwan 110, R.O.C.
Phone: +886-2-2727-1221
Fax: +886-2-2727-1223
e-mail: taiwansales@powerint.com

CHINA (SHANGHAI)
Rm 807, Pacheer,
Commercial Centre,
555 Nanjing West Road,
Shanghai, 200041, China
Phone: +86-21-6215-5548
Fax: +86-21-6215-2468
e-mail: chinasales@powerint.com

INDIA (TECHNICAL SUPPORT)
Innovatech
261/A, Ground Floor
7th Main, 17th Cross,
Sadashivanagar
Bangalore, India, 560080
Phone: +91-80-5113-8020
Fax: +91-80-5113-8023
e-mail: indiasales@powerint.com

KOREA
8th Floor, DongSung Bldg.
17-8 Yoido-dong,
Youngdeungpo-gu,
Seoul, 150-874, Korea
Phone: +82-2-782-2840
Fax: +82-2-782-4427
e-mail: koreasales@powerint.com

UK (EUROPE & AFRICA HEADQUARTERS)
1st Floor, St. James's House
East Street
Farnham, Surrey GU9 7TJ
United Kingdom
Phone: +44-1252-730-140
Fax: +44-1252-727-689
e-mail: eurosales@powerint.com

CHINA (SHENZHEN)
Rm# 1705, Bao Hua Bldg.
1016 Hua Qiang Bei Lu,
Shenzhen, Guangdong,
518031, China
Phone: +86-755-8367-5143
Fax: +86-755-8377-9610
e-mail: chinasales@powerint.com

ITALY
Via Vittorio Veneto 12, Bresso,
Milano,
20091, Italy
Phone: +39-028-928-6001
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

SINGAPORE
51 Newton Road,
#15-08/10 Goldhill Plaza,
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

APPLICATIONS HOTLINE
World Wide +1-408-414-9660

APPLICATIONS FAX
World Wide +1-408-414-9760

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Power Integrations, Inc.
Tel: +1 408 414 9200 Fax: +1 408 414 9201
www.powerint.com