SGD
Display the World

Specifications for Approval

Customer : _____

Model name : __GG1306B5SAN6T_____ __REV: A_____

Description : __LIQUID CRYSRAL DISPLAY MODULE_____

DESIGN	CHECK	APPROVED

Customer Approval	☐ **Accept** ☐ **Reject** **Comment:** **Approved by:** _____

CONTENTS

MODEL	GG1306B5SAN6T	1/22	PRODUCT SPECIFICATIONS	REV: A

1. FEATURES

The features of LCD are as follows

* Display mode   : STN, Positive, Reflective

* Color   : Display dot : Dark Blue

                         Background: Yellow-Green

* Display Format   : 132Dots × 64Dots

* IC   : Solomon SSD1815T

* Interface Input Data : 8-Bit Parallel or Serial

* Driving Method   : 1/64 Duty, 1/9 Bias

* Viewing Direction   : 6 O'clock

2. MECHANICAL SPECIFICATIONS

Item	Specification	Unit
Module Size	53.5(W) X 45.5(H) X 2.1MAX(T)	mm
Viewing Area	49.5(W) X 23.5(H)	mm
Effective Display Area	43.53(W) X 21.09(H)	mm
Number of Dots	132 X 64Dots	
Dot Size	0.3(W) X 0.3(H)	mm
Dot Pitch	0.33(W) X 0.33(H)	mm

3. ELECTRICAL SPECIFICATIONS

3-1. Absolute Maximum Ratings (Vss=0V)

Item	Symbol	Standard Value			Unit
		Min.	Typ.	Max.	
Supply Voltage For Logic	V_{DD}-V_{SS}	-0.3	_	+4.0	V
Supply Voltage For LCD Drive	Vlcd	-0.3	_	+16.0	V
Input Voltage	V_{IN}	Vss-0.3	_	V_{DD}+0.3	V
Operating Temp.	T_{OP}	-20	-	+70	°C
Storage Temp.	T_{ST}	-25	-	+75	°C

3. ELECTRICAL SPECIFICATIONS (Continued)

Item		Symbol	Test Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic		$V_{DD} - V_{SS}$	-	2.4	3.0	3.5	V
Supply Voltage For LCD		$V_{DD} - V_0$	Ta=25℃	8.5	9.0	9.5	V
Input Voltage	"H" Level	V_{IH}		$0.8V_{DD}$	_	V_{DD}	V
	"L" Level	V_{IL}		V_{SS}	_	$0.2V_{DD}$	V
Output Voltage	"H" Level	V_{OH}	I_{OH}= -0.1mA	$0.9V_{DD}$	_	V_{DD}	V
	"L" Level	V_{OL}	I_{OL}= 0.1mA	0	_	$0.1V_{DD}$	V
Current Consumption		I_{DD}	V_{DD} = 3.0V	-	0.38	2.0	mA

NOTE: 1)Duty ratio=1/64, Bias=1/9

2).Measured in Dots ON-state

4. POWER SUPPLY

All internal power mode

External V$_{EE}$ with internal regulator and divider mode

Optional for external resistors gain control(IRS=L)

Value of external Capacitance

C1	1.0 uF
C2	0.1uF ~ 0.47uF
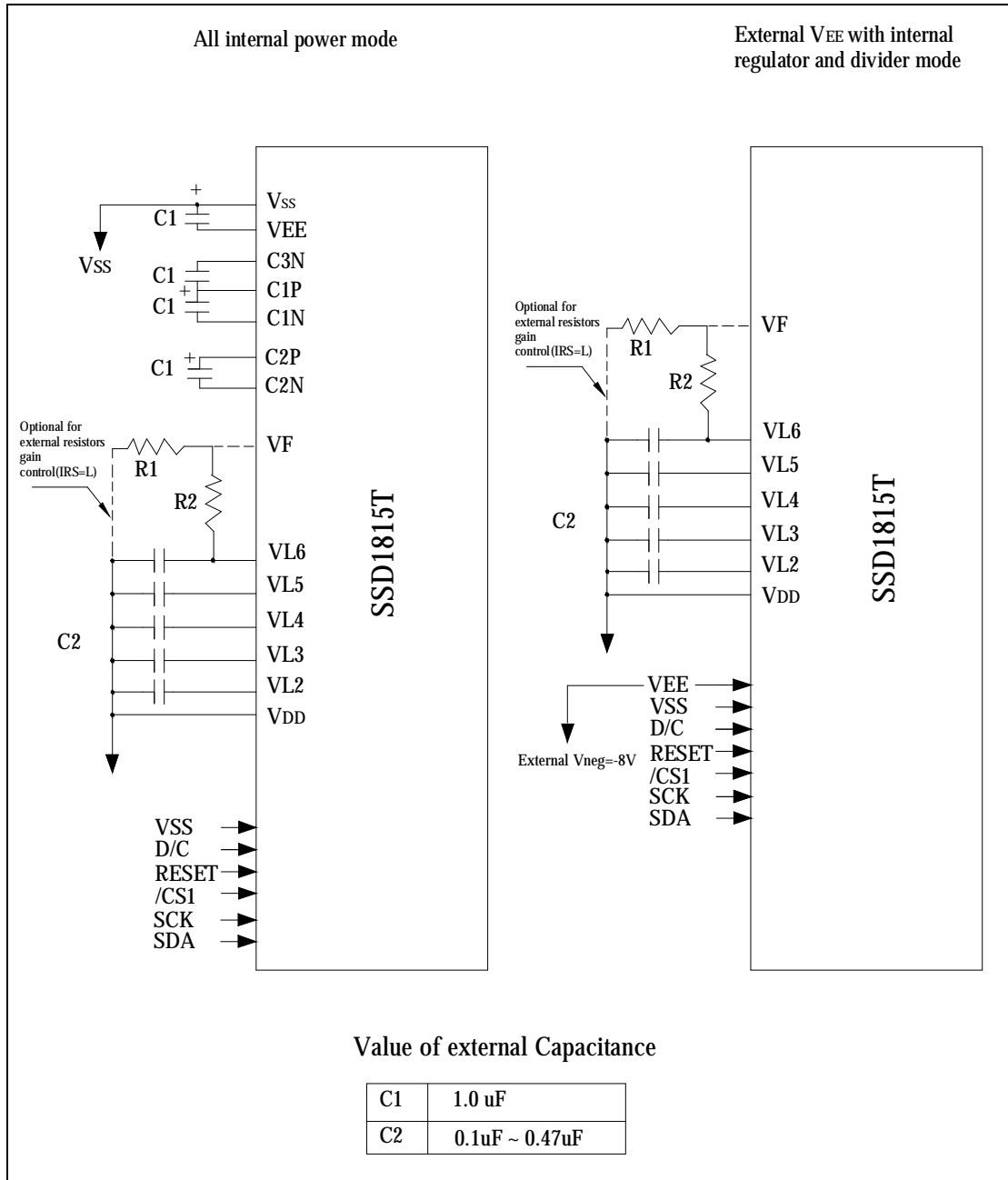
5. ELECTRO – OPTICAL CHARACTERISTICS

Item	Symbol	Temp.	Min.	Typ.	Max.	Unit	Conditions	Note
Viewing Angle	$\Theta2-\Theta1$	25℃	30	80	-	Deg.	-	1,2
	Φ		60	70	-			
Contrast Ratio	Cr	25℃	2	3.9	4.7	-	$\Theta=0°$ $\Phi=0°$	3
Response Time(rise)	Tr	25℃	-	120	250	ms	$\Theta=0°$ $\Phi=0°$	4
		0℃	-	950	1150			
Response Time(fall)	Tf	25℃	-	160	250	ms	$\Theta=0°$ $\Phi=0°$	4
		0℃	-	950	1150			

Note1 . Definition of Angle Θ & Φ
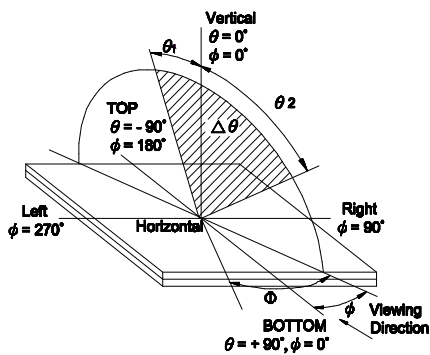
Note2. Definition of Viewing Angle $\Theta1$ & $\Theta1$
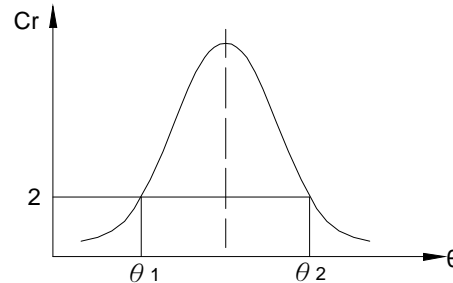
Note3 . Definition of Contrast Cr
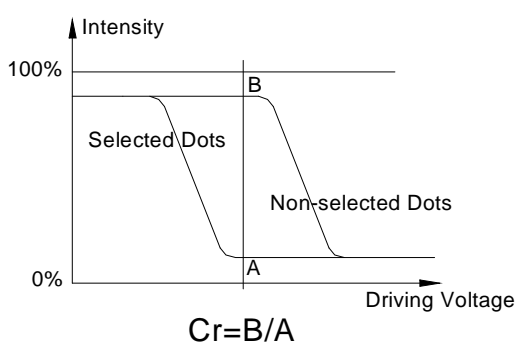
Note4. Definition of Optical Response

Cr=B/A

| MODEL | GG1306B5SAN6T | 5/22 | PRODUCT SPECIFICATIONS | REV: A |
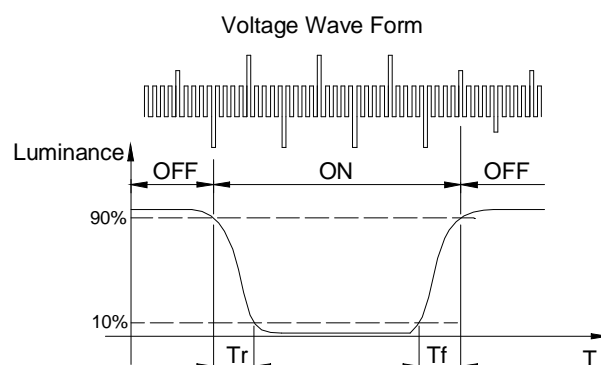
6. Interface Pin Function

Pin	Symbol	I/O	Function
	Dummy		No connected
1	M	I/O	LCD AC signal input /output. When SSD1815 is used in master /slave mode(multi-chip). The M pins must be connected to each other . M/S = " H " : Output M/S = " L " : Input
2	CL	I/0	Display clock input/output . When SSD1815 is used in master / slave mode(multi-chip). The CL pins must be connected to each other .
3	/DOF	I/O	LCD display blanking control input/output. When SSD1815 is used in master/slave mode (multi-chip), the DIPS pins must be connected to each other MS="H": Output MS="L": Input
4	CS1B	I	Chip select inputs pins.
5	CS2	I	Data/instruction I/O is enabled only when CS1B is "L" and CS2 is "H". When chip select is non-active , DB0 to DB7 may be high impedance
6	/RES	I	Reset input pin. When RESETB is "L", initialization is executed.
7	D/C	I	Register Select input D/C = " H " " the data on DB[7~0] is display data D/C = " L " " the data on DB[7~0] is control data
8	RW_WR	I	When interfacing to a 6800 series MPU:Active High. RW_WR="H": Read RW_WR="L": Write When interfacing to an 8080-series MPU , RW_WR is enabled at low.

6. Interface Pin Function (Continue)

9	E/RD	I	When interfacing to a 6800 series MPU : Active High. This is used as an enable clock input in of the 6800-series MPU When interfacing to 8080-series MPU : Active Low This input connects the RD signal of the 8080-series MPU. While this signal is Low , data bus output is enabled.
10	D0	I/O	When the serial interface selected (PS = " L ") D7 : Serial input data (SDA) D6 : Serial input clock (SCK) D5 to D0 : high impedance. When Chip select is not active, DB7 to DB0 will be high impedance.
11	D1		
12	D2		
13	D3		
14	D4		
15	D5		
16	D6_SCK		
17	D7_SDA		
18	VDD	Supply	Power supply .
19	VSS	Supply	Ground.
20	VSS1	I	Reference voltage input for internal DC-DC converter.
21	VEE	Supply	Power supply .
22	C3N	O	When internal DC-DC voltage converter is used, external capacitor is connected between these pin.Different connection will result in different DC-DC converter multiple factor, 2X,3X,or 4X.
23	C1P		
24	C1N		
25	C2N		
26	C2P		
27	VFS	I	This pin provide an external voltage reference for the internal voltage regulator.
28	VDD	Supply	Power supply .
29	VL2	I/O	LCD driving voltages.They can be supplied externally or generated by the internal bias divider. They have the following relationship: $VDD \geqq VL2 \geqq VL3 \geqq VL4 \geqq VL5 \geqq VL6$
30	VL3		
31	VL4		
32	VL5		
33	VL6	I/O	This pin is the most negative LCD driving voltage. It can be supplied externally or generated by the internal regulator.
34	VF	I	This pin is the input of the built-in voltage regulator.
35	VDD	Supply	Power supply .

6. Interface Pin Function (Continue)

36	M/S	I	This pin is the master / slave mode selection input.
37	CLS	I	This pin is the internal clock enable pin.
38	C68/80	I	This pin is microprocessor interface selection input. When the pin is pulled high, 6800 series interface is selected and when the pin pulled low, 8080 series MCU interface is selected.
39	PS	I	This pin is serial /parallel interface selection input. PS="H": Parallel mode PS="L": Serial mode
40	/HPM	I	This pin is the control input of High Power Mode. The function of this pin is only enabled for High Power model which required special ordering
41	IRS	I	This is the input pin to enable the internal resistors network for the voltage regulator.IRS="H": Internal resistors; IRS="L": External resistors.
	Dummy		No connection

7. COMMAND LIST

Bit Pattern	Write Command (D/C=0, R/W(WR)=0, E(RD)=1)	Comment
$0000X_3X_2X_1X_0$	Set Lower Column Address	Set the lower nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b during POR.
$0001X_3X_2X_1X_0$	Set Higher Column Address	Set the higher nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b during POR.
$00100X_2X_1X_0$	Set Internal Regulator Resistor Ratio	Internal regulator gain increases as $X_2X_1X_0$ increased from 000b to 111b. At POR, $X_2X_1X_0$ = 100b.
$00101X_2X_1X_0$	Set Power Control Register	X_0=0 turns off the output op-amp buffer (POR) X_0=1 turns on the output op-amp buffer X_1=0 turns off the internal regulator (POR) X_1=1 turns on the internal regulator X_2=0 turns off the internal voltage booster (POR) X_2=1 turns on the internal voltage booster
$01X_5X_4X_3X_2X_1X_0$	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_4X_3X_2X_1X_0$. Display start line register is reset to 000000 during POR.
$100000C1$ $**X_5X_4X_3X_2X_1X_0$	Set Contrast Control Register	Set Contrast level from 64 contrast steps. Contrast increases (V_{LB} decreases) as $X_5X_4X_3X_2X_1X_0$ is increased. $X_5X_4X_3X_2X_1X_0$ = 100000b (POR)
$1010000X_0$	Set Segment Re-map	X_0=0 column address 00h is mapped to SEG0 (POR) X_0=1 column address 83h is mapped to SEG0 Refer to Figure 5 for example.
$1010001X_0$	Set LCD Bias	X_0=0 1/9 bias (POR) X_0=1 1/7 bias For setting bias ratio to 1/4, 1/5, 1/6 or 1/8, see Extended Command Table
$1010010X_0$	Set Entire Display On/Off	X_0=0 normal display (POR) X_0=1 entire display on
$1010011X_0$	Set Normal/Reverse Display	X_0=0 normal display (POR) X_0=1 reverse display
$1010111X_0$	Set Display On/Off	X_0=0 turns off LCD panel (POR) X_0=1 turns on LCD panel
$1011X_3X_2X_1X_0$	Set Page Address	Set GDDRAM Page Address (0-3) using $X_3X_2X_1X_0$
$1100X_3***$	Set COM Output Scan Direction	X_3=0 normal mode (POR) X_3=1 remapped mode. COM0 to COM[N-1] becomes COM[N-1] to COM0 when Multiplex ratio is equal to N. See Figure 5 as an example for N equal to 64.
11100000	Set Read-Modify-Write Mode	Read-modify-write mode will be entered in which the column address will not be incremented during display data read. At POR, Read-modify-write mode is turned OFF
11100010	Software Reset	Initialize the internal status register.
11101110	Set End of Read-Modify-Write Mode	Exit Read-modify-write mode. Column address before entering the mode will be restored. At POR, Read-modify-write mode is OFF.
$1010110X_0$	Set Indicator On/Off	X_0 = 0: indicator off (POR, no need of second command byte) X_0 = 1: indicator on (second command byte required)
$******X_1X_0$	Indicator Display Mode. This second byte command is required ONLY when "Set Indicator On" command is sent.	X_1X_0 = 00: indicator off X_1X_0 = 01: indicator on and blinking at ~1 second interval X_1X_0 = 10: indicator on and blinking at ~1/2 second interval X_1X_0 = 11: indicator on constantly
11100011	NOP	Command for No Operation
11110000	Test Mode Reset	Reserved for IC testing. Do NOT use.
$111*****$	Set Test Mode	Reserved for IC testing. Do NOT use.
$********$	Set Power Save Mode	Standby or sleep mode will be entered with compound commands

Bit Pattern	Read Command (D/C=0, R/W(WR)=1, E(RD)=0)	Comment
$D_7D_6D_5D_4D_3D_2D_1D_0$ (Data Read Back from the driver)	Status Register Read	D_7=0: indicates an internal operation is completed D_7=1: indicates an internal operation is in progress. D_6=0: indicates reverse segment mapping with column address D_6=1: indicates normal segment mapping with column address D_5=0: indicates the display is ON D_5=1: indicates the display is OFF D_2=0: initialization is not in progress D_2=1: initialization is in progress after RES or software reset $D_3D_2D_1D_0$ = 1010 , these 4-bit is fixed to 1010 which could be used to identify as Solomon Systech Device.

Extended Command Table

Bit Pattern	Command	Comment
10101000 00X5X4X3X2X1X0	$X_5X_4X_3X_2X_1X_0$: Set Multiplex Ratio	To select multiplex ratio N from 2 to 65 [Included Icon Line] N = $X_5X_4X_3X_2X_1X_0$ + 2, eg. N = 111111b + 2 = 65 (POR)
10101001 X7X6X5X4X3X2X1X0	X_1X_0: Set Bias Ratio	X_1X_0 = 00: 1/8, 1/5 X_1X_0 = 01: 1/6, 1/5 X_1X_0 = 10: 1/9, 1/7 (POR) X_1X_0 = 11: Prohibited
	$X_4X_3X_2$: Set TC Value	$X_4X_3X_2$ = 000: -0.01%/C (TC0, POR) $X_4X_3X_2$ = 010: -0.10%/C (TC2) $X_4X_3X_2$ = 100: -0.18%/C (TC4) $X_4X_3X_2$ = 111: -0.25%/C (TC7) $X_4X_3X_2$ = 001, 011, 101, 110: Reserved
	$X_7X_6X_5$: Modify Osc. Freq.	Increase the value of $X_7X_6X_5$ will increase the oscillator frequency and vice versa. This command is not recommended to be used. $X_7X_6X_5$ = 011(POR)
1010101X0	X_0: Set 1/4 Bias Ratio	X_0 = 0: use Normal Setting (POR) X_0 = 1: fixed at 1/4 Bias
11010010 0X6X5000010	X_6X_5: Set Total Frame Phases	The On/Off of the Static Icon is given by 3 phases/1 phase overlapping of the M and MSTAT signals. This command set how many phases of dividing the M/MSTAT signals for each frame The more the phases, the less the overlapping and thus the lower the effective driving voltage. X_6X_5 = 00: 3 phases X_6X_5 = 01: 5 phases X_6X_5 = 10: 7 phases (POR) X_6X_5 = 11: 16 phases
11010011 00X5X4X3X2X1X0	$X_5X_4X_3X_2X_1X_0$: Set Display Offset (for mux ratio has been set less than 64 only)	After POR, $X_5X_4X_3X_2X_1X_0$ = 0 After setting mux ratio less than 64, data will be displayed at Center of matrix. See Table 1. To move display towards Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = L To move display away from Row 0 by L, $X_5X_4X_3X_2X_1X_0$ = 64-L Note: max. value of L = (64 - display mux)/2

Note: Patterns other than that given in Command Table and Extended Command Table are prohibited to enter to the chip as a command. Otherwise, unexpected result will occurs.

MODEL	GG1306B5SAN6T	10/22	PRODUCT SPECIFICATIONS	REV: A

8.TIMING CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300			ns
t_{AS}	Address Setup Time	0	-	-	ns
t_A	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20			ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CS}	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	80	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

MODEL	GG1306B5SAN6T	11/22	PRODUCT SPECIFICATIONS	REV: A

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{H-W}	Write Data Hold Time	15	-	-	ns
t_{D-R}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	120			ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
t_r	Rise Time	-	-	15	ns
t_F	Fall Time			15	ns

MODEL	GG1306B5SAN6T	12/22	PRODUCT SPECIFICATIONS	REV: A

8.TIMING CHARACTERISTICS (Continued)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250			ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150			ns
t_{CSS}	Chip Select Setup Time (for D_n input)	120	-	-	ns
t_{CSH}	Chip Select Hold Time (for D_n input)	60			ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100			ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100			ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time			15	ns

| MODEL | GG1306B5SAN6T | 13/22 | PRODUCT SPECIFICATIONS | REV: A |
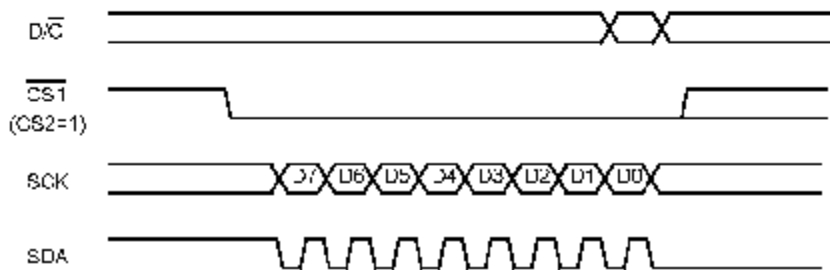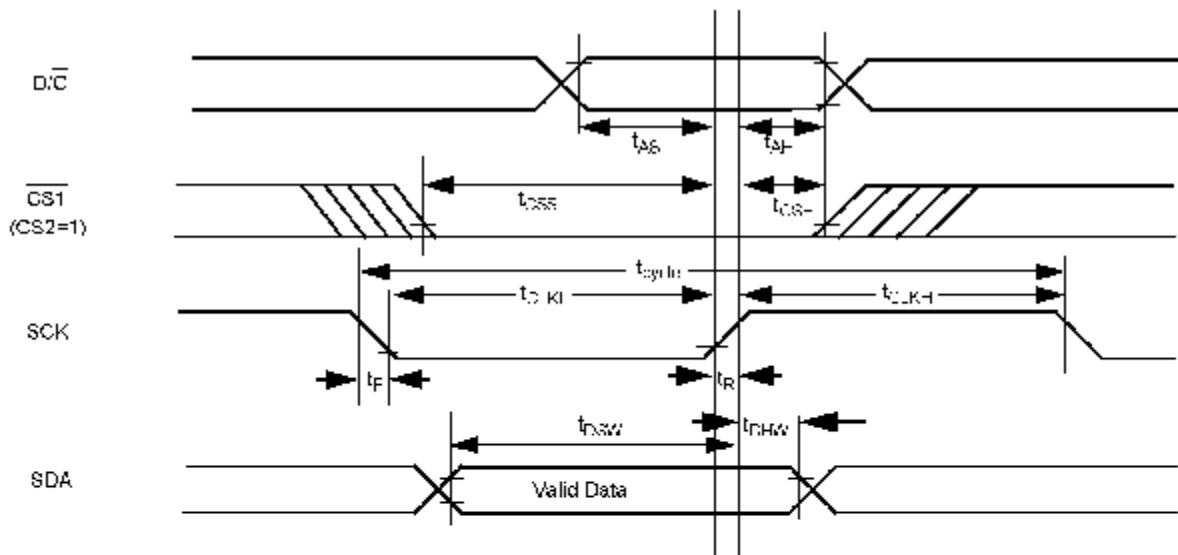
9. QUALITY SPECIFICATION

 9 - 1. LCM Appearance and Electric inspection Condition

   1. Inspection will be done by placing LCM 30cm away from inspector's eyeballs under normal illumination.
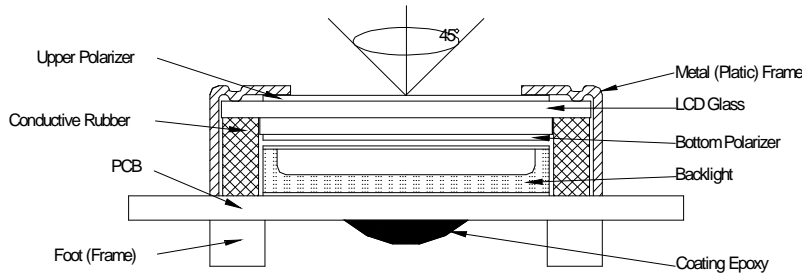
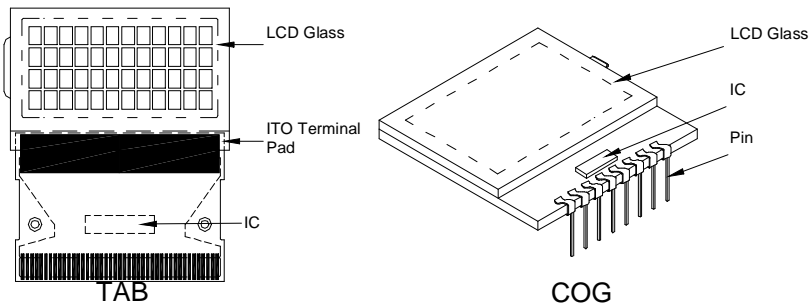   2. View Angle: with in 45° around perpendicular line.

 9 - 2. Definition

   1. COB

   2. Heat Seal

   3. TAB and COG

TAB   COG
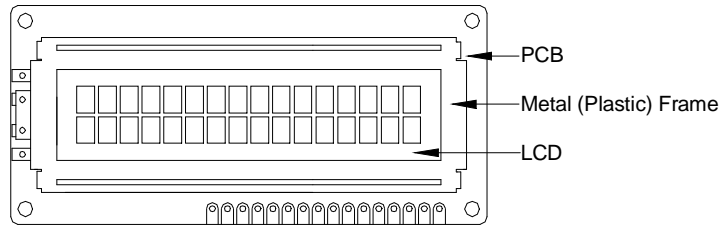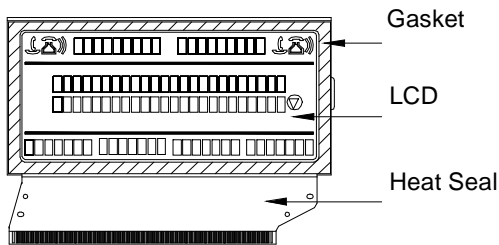
9-3. Sampling Plan and Acceptance

1. Sampling Plan

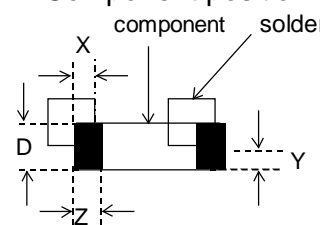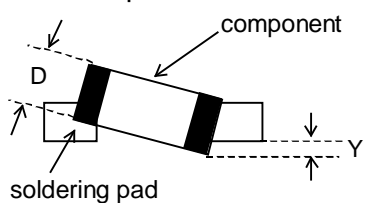MIL - STD - 105E (‖) ordinary single inspection is used.

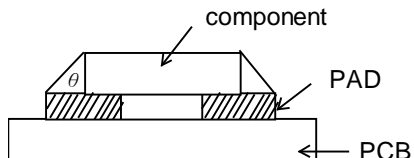2. Acceptance

Major defect: AQL = 0.25%

Minor defect: AQL = 0.65%

9-4. Criteria

1. COB

Defect	Inspection Item	Inspection Standards	
Major	PCB copper flakes peeling off	Any copper flake in viewing Area should be greater than $1.0mm^2$	Reject
Major	Height of coating epoxy	Exceed the dimension of drawing	Reject
Major	Void or hole of coating epoxy	Expose bonding wire or IC	Reject
Major	PCB cutting defect	Exceed the dimension of drawing	Reject

2. SMT

Defect	Inspection Item	Inspection Standards	
Minor	Component marking not readable		Reject
Minor	Component height	Exceed the dimension Of drawing	Reject
Major	Component solder defect (missing , extra, wrong component or wrong orientation		Reject
Minor	Component position shift	$X < 3/4Z$ $Y > 1/3D$	Reject Reject
Minor	Component tilt	$Y > 1/3D$	Reject
Minor	Insufficient solder	$\theta \le 20°$	Reject

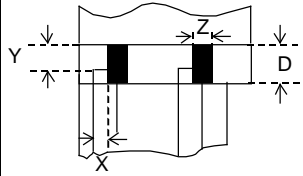| MODEL	GG1306B5SAN6T	15/22	PRODUCT SPECIFICATIONS	REV: A

3. Metal (Plastic) Frame

Defect	Inspection Item	Inspection Standards		
Major	Crack / breakage	Anywhere		Reject
Minor	Frame Scratch	W	L	Acceptable of Scratch
		w<0.1mm	Any	Ignore
		0.1≤w<0.2mm	L≤5.0mm	2
		0.2≤w<0.3mm	L≤3.0mm	1
		w≥0.3mm	Any	0
		Note : 1. Above criteria applicable to scratch lines with distance greater than 5mm.　　　2. Scratch on the back side of frame (not visible) can be ignored .		
Minor	Frame Dent , Prick $\Phi = \dfrac{L + W}{2}$			Acceptable of Dents / Pricks
		$\Phi \leq 1.0$mm		2
		$1.0 < \Phi \leq 1.5$mm		1
		1.5mm$< \Phi$		0
		Note : 1. Above criteria applicable to any two dents / pricks with distance greater than 5mm　　　2. Dent / prick on the back side of frame (not visible) can be ignored		
Minor	Frame Deformation	Exceed the dimension of drawing		
Minor	Metal Frame Oxidation	Any rust		

4. Flexible Film Connector (FFC)

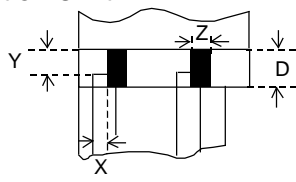| Defect	Inspection Item	Inspection Standards	
Minor	Tilted soldering	Within the angle +5°	Acceptable
Minor	Uneven solder joint /bump		Reject
Minor	Hole　　$\Phi = \dfrac{L + W}{2}$	Expose the conductive line	Reject
		$\Phi > 1.0$mm	Reject
Minor	Position shift	Y > 1/3D	Reject
		X > 1/2Z	Reject

9. QUALITY SPECIFICATION (Continued)

9-4. Criteria (Continued)

5. Screw

Defect	Inspection Item	Inspection Standards	
Major	Screw missing/loosen		Reject
Minor	Screw oxidation	Any rust	Reject
Minor	Screw deformation	Difficult to accept screw　driver	Reject

6. Heatseal 、TCP 、FPC

Defect	Inspection Item	Inspection Standards	
Major	Scratch expose conductive layer		Reject
Minor	HS Hole $\Phi = \dfrac{L + W}{2}$	$\Phi > 0.5mm$	Reject
Major	Adhesion strength	Less than the specification	Reject
Minor	Position shift	$Y > 1/3D$	Reject
		$X > 1/2Z$	Reject
Major	Conductive line break		Reject

7. LED Backing Protective Film and Others

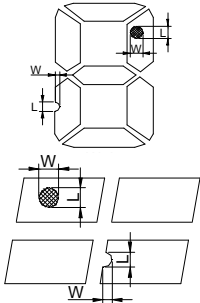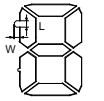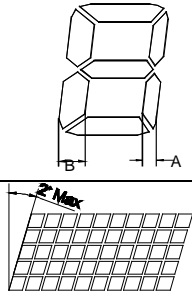| Defect	Inspection Item	Inspection Standards	
Minor	LED dirty, prick	Acceptable number of units	
		$\Phi \leq 0.10mm$	Ignore
		$0.10 < \Phi \leq 0.15mm$	2
		$0.15 < \Phi \leq 0.2mm$	1
		$\Phi > 0.2mm$	0
		The distance between any two spots should be $\geq 5mm$ Any spot/dot/void outside of viewing area is acceptable	
Minor	Protective film tilt	Not fully cover LCD	Reject
Major	COG coating	Not fully cover　ITO circuit	Reject

8. Electric Inspection

Defect	Inspection Item	Inspection Standards	
Major	Short		Reject
Major	Open		Reject

9. QUALITY SPECIFICATION (Continued)

9-4. Criteria (Continued)

9. Inspection Specification of LCD

Defect	Inspect Item		Inspection Standards			
Minor	Linear Defect	∗ Glass Scratch ∗ Polarizer Scratch ∗ Fiber and Linear material	W	W≤0.03	0.03<W≤0.05	W>0.05
			L	L<5	L<3	Any
			ACC. NO.	1	1	Reject
			Note	L is the length and W is the width of the defect		
Minor	Black Spot and Polarizer Pricked	∗ Foreign material between glass and polarizer or glass and glass ∗ Polarizer hole or protuberance by external force	Φ	Φ≤0.1	0.1<Φ≤0.15 / 0.15<Φ≤0.2	Φ>0.2
			ACC. NO.	3EA / 100mm²	2 / 1	0
			Note	Φ is the average diameter of the defect. Distance between two defects > 10mm.		
Minor	White Spot and Bubble in polarizer	∗ Unobvious transparant foreign material between glass and glass or glass and polarizer ∗ Air protuberance between polarizer and glass	Φ	Φ≤0.3	0.3<Φ≤0.5	0.5<Φ
			ACC. NO.	3EA / 100mm²	1	0
			Note	Φ is the average diameter of the defect. Distance between two defects > 10mm.		
Minor	Segment Defect		Φ	Φ≤0.10	0.10<Φ≤0.20 / 0.20<Φ≤0.25	Φ>0.25
			ACC. NO.	3EA / 100mm²	2 / 1	0
			Note	W is more than 1/2 segment width		Reject
				$\Phi = \dfrac{L + W}{2}$ Distance between two defect is 10mm		
Minor	Protuberant Segment	$\Phi = (L + W)/2$	Φ	Φ≤0.10	0.10<Φ≤0.20 / 0.20<Φ≤0.25	Φ>0.25
			W	Glue	W≤1/2 Seg W≤0.2 / W≤1/2 Seg W≤0.2	Ignore
			ACC. NO.	3EA / 100mm²	2 / 1	0
Minor	Assembly Mis-alignment		1. Segment			
			B	B≤0.4mm	0.4<B≤1.0mm	B>1.0mm
			B-A	B-A<1/2B	B-A<0.2	B-A<0.25
			Judge	Acceptable	Acceptable	Acceptable
			2. Dot Matrix			
			Deformation>2°			Reject
Minor	Stain on LCD Panel Surface		Accept when stains can be wiped lightly with a soft cloth or a similar one. Otherwise, judged according to the above items: "Black spot" and "White Spot"			

NO.	Item	Condition	Criterion
1	High Temperature Operating	70℃, 240Hrs	No defect in cosmetic and operational function allowable. Total current Consumption should be below double of initial value.
2	Low Temperature Operating	-20℃, 240Hrs	
3	High Humidity	80℃, 90%RH, 96Hrs	
4	High Temperature Storage	75℃, 240Hrs	
5	Low Temperature Storage	-25℃, 240Hrs	
6	Vibration	Random wave 10 ~ 100Hz Acceleration: 2g 2 Hrs per direction(X,Y,Z)	
7	Thermal Shock	-30℃ to 25℃ to 80℃ (60Min) (5Min) (60Min) 10Cycles	
8	ESD Testing	Contract Discharge Voltage: +1 ~ 5kV and –1 ~ –5kV	There will be discharged ten times at every discharging voltage cycle. The voltage gap is 1kV.
		Air Discharge Voltage: +1 ~ 8kV and –1 ~ -8kV	

Note: 1) Above conditions are suitable for GOLDENTEK standard products.

2) For restrict products, the test conditions listed as above must be revised.

11. HANDLING PRECAUTION

(1) Mounting Method

The panel of the LCD Module consists of two thin glass plates with polarizers which easily get damaged since the Module is fixed by utilizing fitting holes in the printed circuit board. Extreme care should be taken when handling the LCD Modules.

(2) Caution of LCD handling & cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

- Isopropyl alcohol
- Ethyl alcohol
- Trichlorotrifloroethane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

- Water
- Ketone
- Aromatics

(3) Caution against static charge

The LCD Module use C-MOS LSI drivers, so we recommend that you connect any unused input terminal to VDD or VSS, do not input any signals before power is turned on. And ground your body, Work/assembly table. And assembly equipment to protect against static electricity.

(4) Packaging

- Modules use LCD elements, and must be treated as such. Avoid intense shock and falls from a height.

- To prevent modules from degradation. Do not operate or store them exposed directly to sunshine or high temperature/humidity.

(5) Caution for operation

- It is indispensable to drive LCD's within the specified voltage limit since the higher voltage than the limit shorten LCD life. An electrochemical reaction due to direct current causes LCD deterioration, Avoid the use of direct current drive.

| MODEL | GG1306B5SAN6T | 20/22 | PRODUCT SPECIFICATIONS | REV: A |

- Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD's show dark color in them.

However those phenomena do not mean malfunction or out of order with LCD's.

Which will come back in the specified operating temperature range.

- If the display area is pushed hard during operation, some font will be abnormally displayed but it resumes normal condition after turning off once.

- A slight dew depositing on terminals is a cause for electro-chemical reaction resulting in terminal open circuit.

Usage under the relative condition of 40°C, 50%RH or less is required.

(6) Storage

In the case of storing for a long period of time (for instance ,for years) for the purpose or replacement use, The following ways are recommended.

- Storage in a polyethylene bag with sealed so as not to enter fresh air outside in it, And with no desiccant.

- Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping temperature in the specified storage temperature range.

- Storing with no touch on polarizer surface by the anything else. (It is recommended to store them as they have been contained in the inner container at the time of delivery)

(7) Safety

- It is recommendable to crash damaged or unnecessary LCD into pieces and wash off liquid crystal by using solvents such as acetone and ethanol.

Which should be burned up later.

- When any liquid crystal leaked out of a damaged glass cell comes in contact with your hands, please wash it off well with soap and water.

| MODEL | GG1306B5SAN6T | 22/22 | PRODUCT SPECIFICATIONS | REV: A |