International
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DESIGN TIP

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Isolation method for 1-10V controlled ballast based on the IR21592

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The light output of a dimmable ballast based around the IR21592 control IC, is determined from a DC control voltage between 0 and 5V that provides a reference for the closed loop lamp power control. At inputs below 0.5V the output will be at minimum, a preset power level below which the particular lamp that the ballast has been designed for, does not operate satisfactorily. This point will vary considerably between lamp types, depending on the length and diameter of the tube and also the cathode effectiveness. Above this the lamp power will increase linearly from the minimum level to the maximum. The minimum lamp power for which stable output can be achieved is typically 1% when using the IR21592 phase control technique.

REQUIREMENTS OF A COMMERCIAL DESIGN

When designing a circuit for a commercial ballast however, the control voltage used is from 1 to 10Vdc, where voltages below 1V produce minimum output and a linear response is required up to 10V. This control voltage must also be isolated from the off-line parts of the ballast circuitry, including the IR21592, which are at mains potential and would otherwise make the control voltage input terminals live which is hazardous to ballast users and would probably damage the dimming equipment the ballast is connected to. The isolation must be rated to 4kV in order to comply with safety requirements of the European low voltage directive.

The control input must also be sinkable meaning that when no input is applied the control voltage will remain at 10V and the ballast will operate at maximum output. The dimming control must be able to sink this voltage down to below 1V to achieve dimming over the ballast's full range. It is therefore necessary that the voltage can be pulled down below 1V by sinking only a small current in the order of 1mA. This allows many ballast control inputs to be connected to a single dimming control that would typically be rated to be able to sink up to 200mA and therefore could run up to 200 ballasts.

A COMMONLY USED METHOD

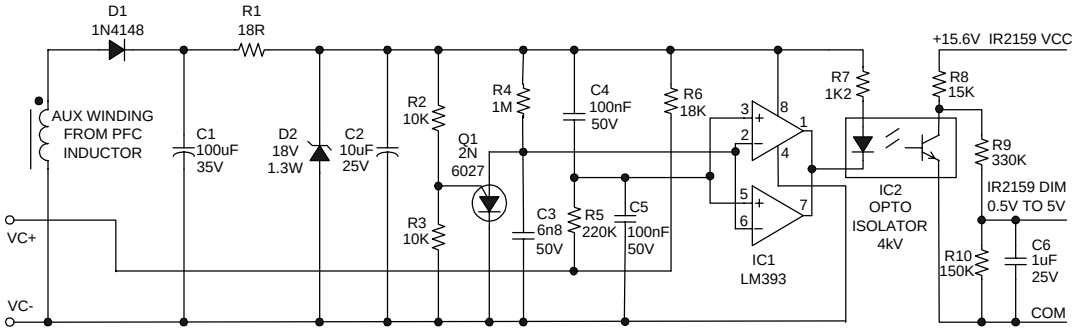
It is possible to achieve isolation by using a small high frequency transformer that has an oscillator on the non-isolated side, applying pulses across the primary which produce 10V pulses at the secondary. These pulses can be peak rectified and thus converted to DC and then an external dimming control used to sink the current reducing the voltage.

This has the effect of reducing the peak level on the primary side of the transformer which can also be peak rectified and used as the IC control voltage. This method is widely used, however it may difficult to achieve a linear relationship between the voltage levels either side of the transformer due to ringing caused by high leakage inductance and other unpredictable effects.

AN EASIER METHOD

The typical linear electronic ballast has a boost converter input section, based around an industry standard low cost power factor correction IC that produces a 400Vdc bus for the IR21592 driven ballast section of the system, whilst maintaining a power factor of better than 0.95. This allows the product to comply with European mains current harmonics standard EN61000-3-2 (class C limits) which impose tight restrictions on all lighting ballasts that require mains power in excess of 25W. The following isolation technique use this input section of the ballast to provide an isolated voltage supply. If there is no active PFC circuit in the ballast it would also be possible to derive the isolated supply from an auxiliary winding on the ballast output inductor.

CIRCUIT DIAGRAM



The circuit shows a simple and reliable method for an isolating 1 to 10Vdc control input that is incorporated into the circuitry.

HOW IT WORKS

Firstly an 18Vdc supply is required to run the isolated section of the circuit. This can be obtained easily by placing an additional winding on the boost inductor. This winding must be isolated from the other two

windings and from the Ferrite cores and be flash tested to 4kV. In order to obtain the correct voltage, the winding will need to have several more turns than the zero current detection winding. It is necessary to ensure that the voltage across the 18V Zener diode does not fall below 18V when the ballast output is dimmed and also over the range of supply voltage.

A bridge rectifier can be used to provide more voltage if a single diode proves to be insufficient over the line / load range.

The next part of the circuit , centred around Q1 programmable unijunction transistor generates an approximate ramp waveform across C3 capacitor which peaks at a little under 10V, guaranteeing maximum output when 10V input is applied at VC+. A trigger voltage provided by a potential divider of 9V is applied to one input of the PJT. C3 charges via R4 until the voltage reaches a point one diode drop above the trigger voltage. Q1 then fires and remains switched on until the current drops below the holding current of the device which is small, discharging the capacitor and then allowing it to charge again, thus a ramp waveform is produced. This signal is fed into the inverting input of a comparator. Note that this circuit uses an LM393 low cost dual comparator but as it requires only a single comparator both have been paralled together, however there is no need for this provided the comparator used is capable of sinking the opto isolator diode current which in this case is around 13mA. The opto isolator diode current should be chosen to be as low as possible to guarantee saturation of the opto transistor when it sinks 1mA and consequently R7 is as large as possible. The non inverting input is connected to the control input via an RC filter circuit and pulled high via R6 which gives a sink current of 1mA. R5 and C5 remove any noise that may be picked up at the comparator input.

The comparator output is open collector providing current to the opto diode when low. The diode will be continuously off when VC+ is at maximum and on when it is zero. Hence the opto isolator transistor will be fully on when the control voltage is minimum and fully off when it is maximum, providing a reasonably linear change in the duty cycle at intermediate levels. It is important to ensure that the opto isolator used is rated to 4kV and has been certified to the necessary safety standards. The transistor side of the opto isolator has the emitter connected to 0V and the collector connected to the IR21592 supply rail of 15.6V via a pull up resistor R8. The collector is then connected via R9 to C6 and R10 to 0V. This averages the PWM signal and provides a DC level to connect to the IR21592 which varies between 0V and 5V. This can be fine tuned, if necessary, by adjusting the value of R10.

A delay is usually incorporated into dimming ballasts to provide a smooth fade from one dimming level to the next. For example, if the control inputs were to be shorted together, the lamp would fade down to minimum brightness over a period determined by the values used. This neatly avoids any flicker that may be caused by sudden changes in load in the boost regulator section. In this case delay is provided via the time constant of R9 and C6. As the frequency of the PWM signal from the opto isolator is only in order of tens of Hertz the delay has been designed to be around 0.33S to ensure minimal ripple on the DC control voltage input to the IC. This can be increased if a longer fade time is desired by making C6 larger.