

The EMI design of the charger without Y Capacitor

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Abstract: Some general knowledge of EMI is introduced in this paper. The basic principle of causing differential mode and common mode current related conducted emissions of EMI in the switch mode power supply is discussed in detail through the relevant circuit theories and the sketch diagrams. The design of the cancellation inside the structure of the transformer is also presented and explained by the sketch diagram. The methods for reducing radiated emissions of EMI are described as well too. In the end the design for common mode inductor is offered.

At present, Y capacitor is widely adopted inside SMPS including the cell phone charger to pass EMI tests. The usage of Y capacitor leads to the leakage current from input lines to output lines. The removal of Y capacitor can pass the leakage current safety test absolutely. On the other hand, the cell phone adopting metal case instead of plastic metal is featured with the metallic sheen and colorful shape. The metal case can offer the better protection the cell phone equipment from electrostatic or magnetic interference outside. But the users of the cell phones with the metal case have the risk of getting an electric shock owing to the existence of Y capacitor. It must require the removal of Y capacitor in this situation.

However, the removal of Y offers the challenge for the EMI design of the charger. So the basic reason of causing EMI and the function of Y capacitor must be known in order to offer the direction of designing the charger without Y capacitor.

1 The basic overview of EMI

Inside SMPS, the operation of the switching devices with high frequency causes rapidly changing current and voltage owing to. The voltage and current waveforms of the mosfet are shown in figure 1. The topology of this converter is fly back in CCM discontinuous conduction mode.

The rapidly changing current of the parasitic inductance can generate the magnetic field and cause high voltage ring:

$$u_L = L di_L / dt$$

The rapidly changing voltage on the parasitic capacitance can form the electric field and cause high current ring:

$$i_C = C du_C / dt$$

It is clear that the electronic and magnetic noises are related with the fast changing current and voltage as well as the coupling paths such as the parasitic inductance and capacitance.

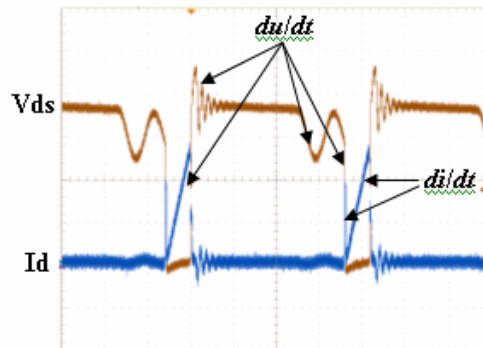


Figure 1: The mosfet voltage and current waveforms

One of the most effective methods to reduce generated EMI should be to slow down the switching transitions, this it, to reduce di/dt and du/dt of the switching device. They can be accomplished to change the gate drive circuit of the power device such as adjusting the resistance in series with the gate in the figure 2 and add the snubber circuits between the switches can do this.

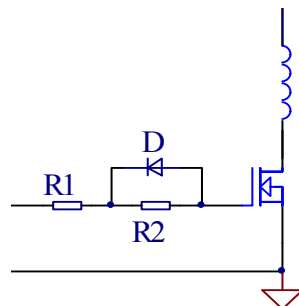


Figure 2: The gate drive circuit for mosfet

In the figure 3, RCD is basic clamp circuit to restrict the spike voltage caused by the leakage inductance. The ferrite beads L1, L2 and L3 can slow down the current transitions during their respective circuits. However, L1 and L2 only decay the signals during some particular frequency bandwidths. L3 only has an effect on the converter in CCM. R1C1, R2C2, R3C3, R4C4 and C5 can slow down the voltage transitions of primary winding, power device, secondary winding, output diode and clamp diode respectively.

They cause some additional power consumption because they are typically dissipative and therefore noticeably reduce the overall efficiency. They also increase the count of the devices with big volume and high cost.

It means that the system size and complexity will increase. In most cases, their usage should be avoided as much as possible except basic clamp circuit RCD.

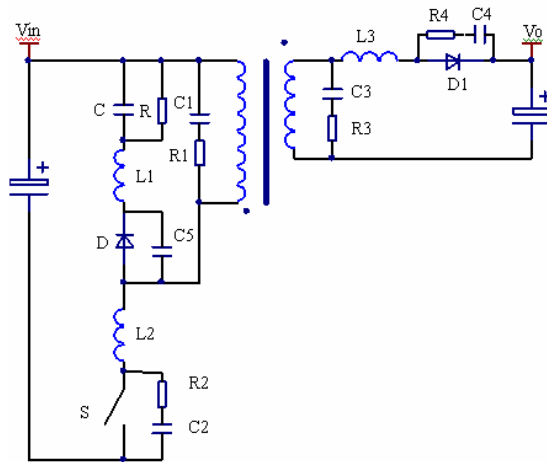


Figure 3: The snubber circuits

It is an unavoidable way to incorporate a line filter at the input or output interface of the system. Normally these filters comprise differential mode and common mode filters, which are composed solely of passive components in a low-pass filter configuration with second order. The design of the filter will be discussed during the following sections.

Another way is to reduce the parasitic inductance and capacitance in the system. The power device is a noise source due to the parasitic package lead inductance which causes high frequency ringing on the voltage waveform across the device and the parasitic capacitance across the device which causes high frequency ringing in the current through the device.

The high frequency voltage across the device from the interaction of the parasitic inductance and rapidly changing current is a source of differential mode noise current from the interaction of components with the switch Miller capacitances. Moreover, it can cause common mode noise currents through the parasitic capacitances inside the transformer.

The transformer is another noise source owing to the leakage inductance and parasitic capacitances. The inter-winding capacitances of primary winding can be minimized by using breadth of bobbin to reduce the number of layers of primary winding and the non disjunction winding or the Faraday shield in the construction of the transformer. Faraday shield is simply an isolated section of copper foil that is wrapped between the primary and secondary windings and then connected to the ground. But they increase leakage inductance due to their loose coupling, which can

also cause high frequency ringing on the voltage waveform across the device. The wound method of separate primary winding into two half windings and sandwiching secondary winding can reduce the leakage inductance and increase the parasitic capacitances

2 Conduction emissions of EMI

2.1 The introduction of LISN

EMI tests consist of CE conducted emissions and RE radiated emissions. Two types of noises are measured and evaluated separately. There are many international standard specifications of EMI. The most important difference between these specifications is the frequency band and the limit. Conducted noise is tested at lower frequencies from 0.15MHz to 30MHz in EU. The starting frequency is usually 450 kHz in US and Canada. In some application for telecom and lighting, it is much lower. Radiated noise is tested at higher frequencies from 30MHz to 1GHz or more. For further information, please read the relevant standard specifications such as FCC, CIRPR, EN, etc.

Conducted noises flow through the input and output lines. The test configuration is shown in figure 4. The AC power source is connected to the EUT equipment under test through the LISN line impedance stabilization network. The purposes of the LISN are as following:

- 1) To insolate the EUT from AC power source and filter the noises coming from the input lines. Make sure that AC power source to the EUT relatively pure.
- 2) To sense the noise signals which go though high pass filter by the common 50 Ω line impedance.

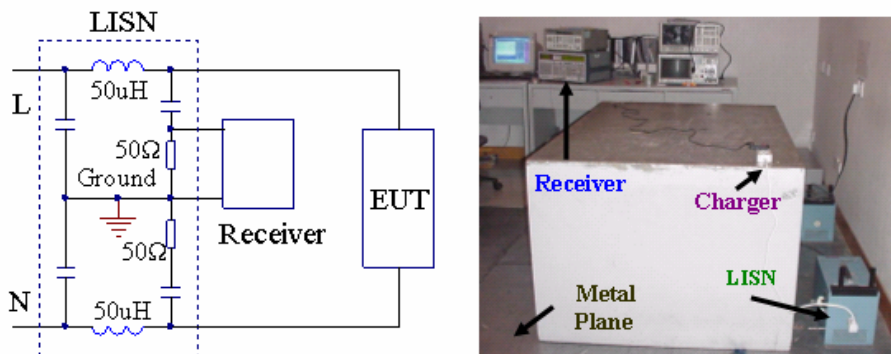


Figure 4: LISN and EUT

The receiver or spectrum analyzer will pick up and deal with test results. In practice, different LISN must be used for different regulations testing. The receiver will analyze the spectrum of a noise voltage of the 50 Ω current shunt. Note that EUT should be put on the test table with the particular size. The non conductive table and LISN must be set on a big metal which is well connected to the earth ground.

The removal of Y capacitor is relevant with CE of EMI. Conducted noises are derived from differential mode current or symmetrical interference or common mode current or asymmetrical interference during input lines of EUT. Differential mode currents and common mode currents are shown in figure 5.

Differential mode currents flow the path between the input feed line and return line in the reverse direction. Common mode currents flow directly through input power feed line and return line in the same direction. They are equal to and in phase with each other and have a circuit path through the earth ground.

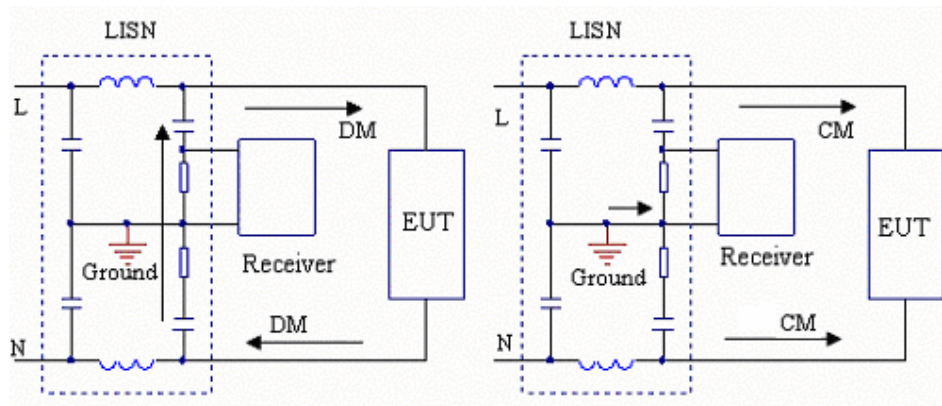


Figure 5: DM and CM current

2.2 The model of the transformer

The parasitic capacitors inside transformer based on circuit model in figure 6 include as following:

- ① C_p : the inter-winding capacitance between the different layers of primary winding. The less the number of layers, the less the C_p .
- ② C_{oe} : the parasitic capacitor from output wires to the earth ground.
- ③ C_{me} : the parasitic capacitor from the magnetic core to the earth ground.
- ④ C_a : the parasitic capacitor from the most outer layer of auxiliary winding of the transformer to the magnetic core.
- ⑤ C_t : the parasitic capacitor from auxiliary winding of the transformer to secondary winding.
- ⑥ C_s : the parasitic capacitor from primary winding of the transformer to secondary winding.

The coupling path is composed of C_s in series with C_{oe} .

- ⑦ C_m : the parasitic capacitor from the most inner layer of primary winding of the transformer to the magnetic core.

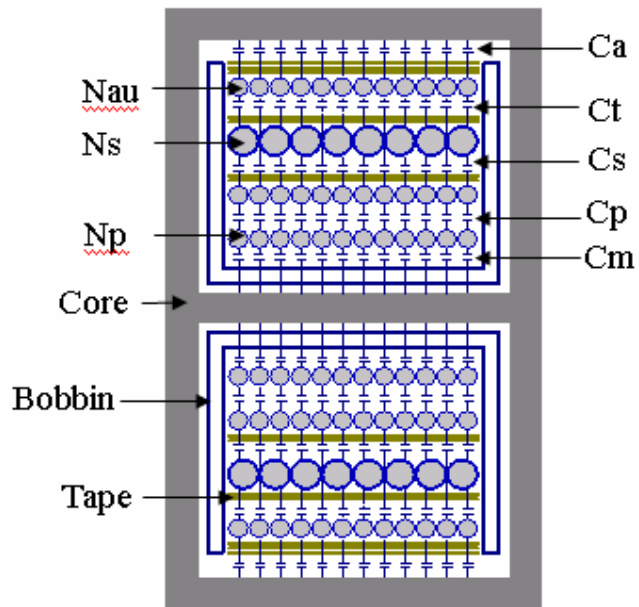


Figure 6: The transformer mode of the parasitic capacitances

2.3 Differential mode currents

Differential mode currents arise mainly in basic switching current of power device. Now we discuss how differential mode current occur.

① the power device is turned on.

Spike current during the instantaneous period of the switch being turned on can be seen in figure 7. The current is composed of three parts:

(1) The charging current of the parasitic capacitance of the primary winding of the transformer.

(2) The discharging current of the parasitic capacitance of drain to source of power MOSFET.

(3) The reverse recovery current of output diode when the converter operates in CCM.

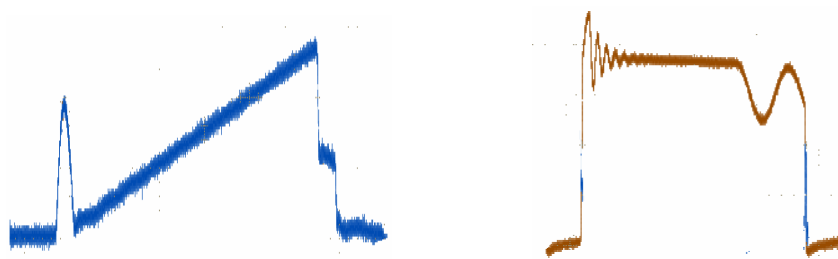


Figure 7: The spike current and voltage during turning on and off

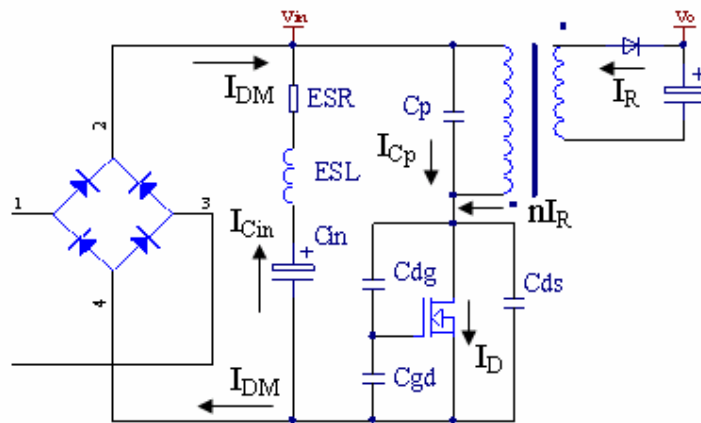


Figure 8: DM currents during turning on

Spike current cannot be bypassed completely the bulk capacitor owing equivalent series resistor ESR and equivalent series inductor ESL when this high frequency current goes through the bus route lines. So part of the current I_{DM} flow through the input lines of the converter. The discharging current of the parasitic capacitance from drain to source of power mosfet does not contribute to I_{DM} .

Hence differential mode current I_{DM} is as following:

$$I_{DM} = I_{Cp} + nI_R - I_{Cin}$$

The currents between different layers flow in the same direction as to the common structure of the transformer as shown in Figure 9. The total sum of the currents is relative high so has a evidently effect on differential mode current.

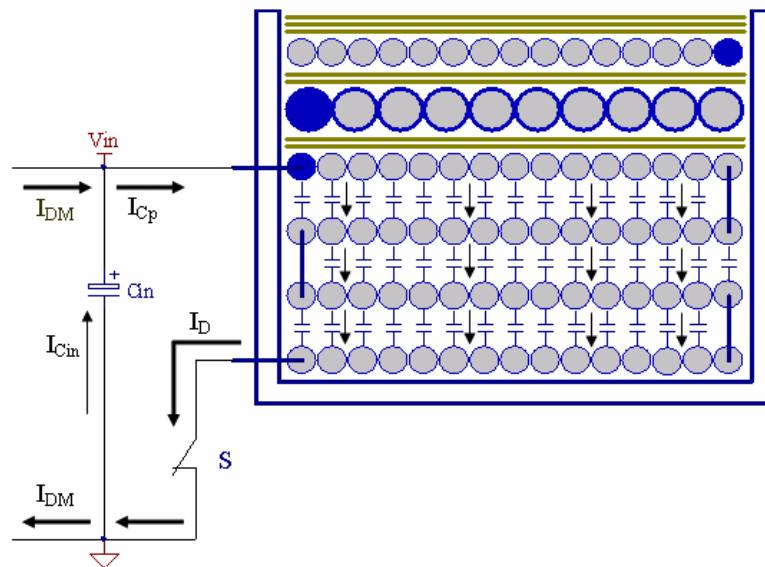


Figure 9: The practical DM currents during turning on

② the power device is turned off.

During the instantaneous period of the switch being turned off, the discharging current of C_p , the charging current of C_{ds} , C_{dg} and C_{gd} will lead to differential mode currents shown in figure 10.

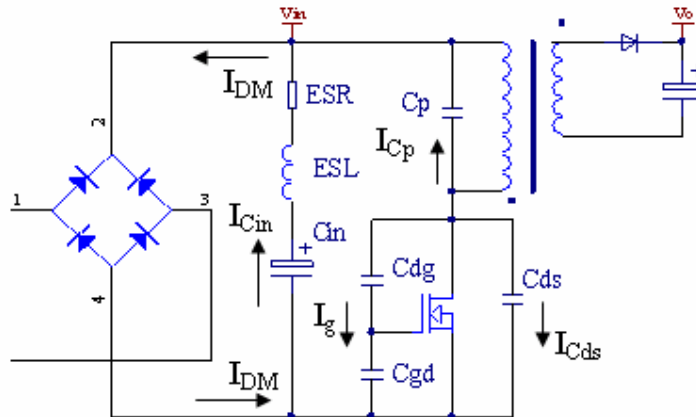


Figure 10: DM current during turning off

Similarly, It cannot be bypassed completely the bulk capacitor owing equivalent series resistor ESR and equivalent series inductor ESL when this high frequency current goes through the bus routes lines. So part of the current I_{DM} is flowing through the input lines of the converter.

So differential mode currents I_{DM} is as following:

$$I_{DM} = I_{Cds} + I_g - I_{Cp} - I_{Cin}.$$

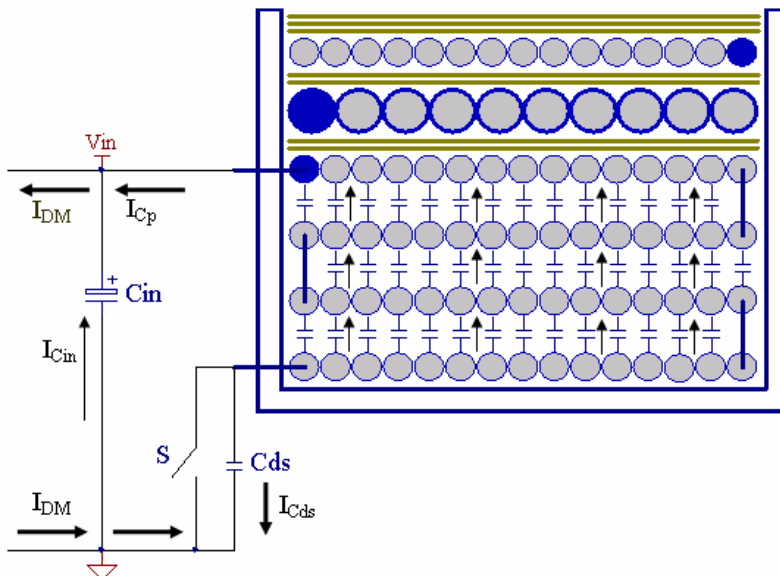


Figure 11: The practical DM currents during turning off

③ High order sub-harmonic components of basic switching current blocked by the ESL and ESR of the bulk capacitor also cause differential mode currents.

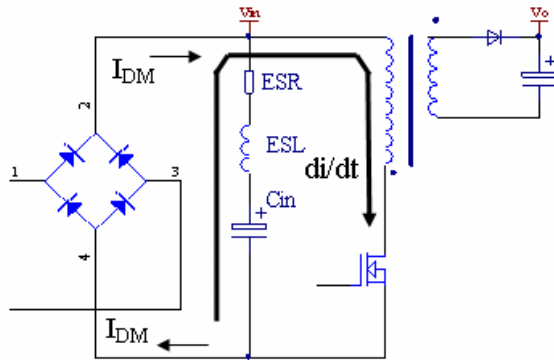


Figure 12: DM currents due to basic switching current

Differential mode current affects the low frequency of CE below 0.1MHz and can be effectively attenuated by balancing noise current path with a DM filter and a high frequency capacitor in parallel with the bulk capacitor.

The high di/dt loop route should be as short and wide as much as possible. The filter with X capacitor and differential mode inductor during the input interface is not adopted in this solution due to low output power, even though it is usually added in some high power converters.

The *actual* filter will include the effects of parasitic capacitance across the inductor and parasitic ESL and ESR in series with the capacitor as shown in figure 13. Paralleling several smaller capacitors instead of using a large one may reduce the parasitic values.

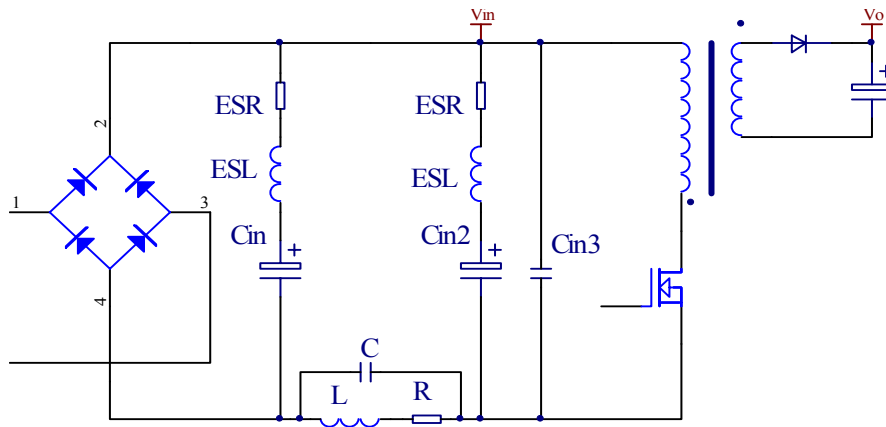


Figure 13: DM inductor

An effective method is to add a small inductor between the paralleled capacitors. This makes the circuit a two-stage or second-order filter yielding a performance gain.

Likewise, parasitic capacitance of the inductor should be reduced as small as possible. Otherwise, high frequency current can pass the inductor through parasitic capacitor.

If the structure of the transformer is changed, primary hot point should be hidden inside as shown in figure 14 and 15.

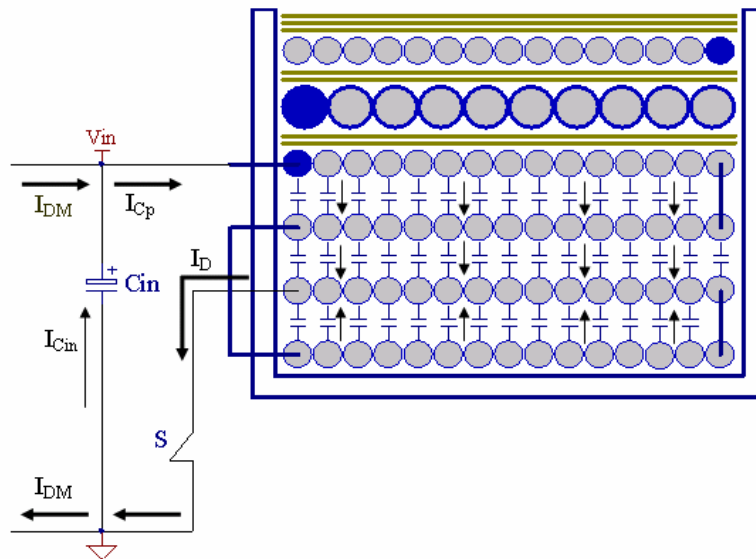


Figure 14: DM currents during turning on

Note that primary winding has three layers. The current flowing directions of each layer of primary winding can be determined by the varying direction of the voltage between each layer. The current flowing directions of the upper three layers of primary winding are reverse with that of the lower two layers. So the current through of different layers of primary winding will be cancelled during turning on as well as turning off.

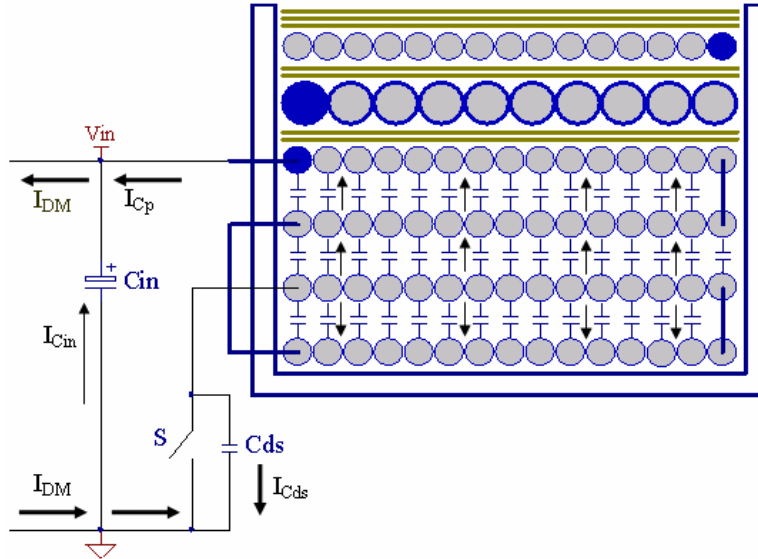


Figure 15: DM currents during turning off

2.4 Common mode current

Common mode current affects the high frequency of CE above 1MHz. Common and differential mode currents both affect together between 0.1MHz and 1MHz. CM noises occur when the transients change from switching voltages are largely coupled to the earth ground or chassis from primary winding of the transformer.

The parasitic capacitor C_{de} from drain area of MOSFET to the earth ground is a coupling path for common mode currents. However, it is usually ignored by the designers. Reducing the copper area of the drain on PCB is helpful to EMI but it leads to the increase of the temperature of the devices. So the engineers should be careful and compromise between the temperature of the devices and EMI. In most cases, much attention should be paid to the temperature because the reliability of the device is much more important. Of course, the substrate inside some devices connected to the source of power mosfet is a better solution.

There are 4 coupling paths for CM currents through from the model of the transformer: $C_m + C_{me}$, $C_a + C_{me}$, $C_t + C_{oe}$ and $C_s + C_{oe}$, among of which $C_s + C_{oe}$ dominates CM currents.

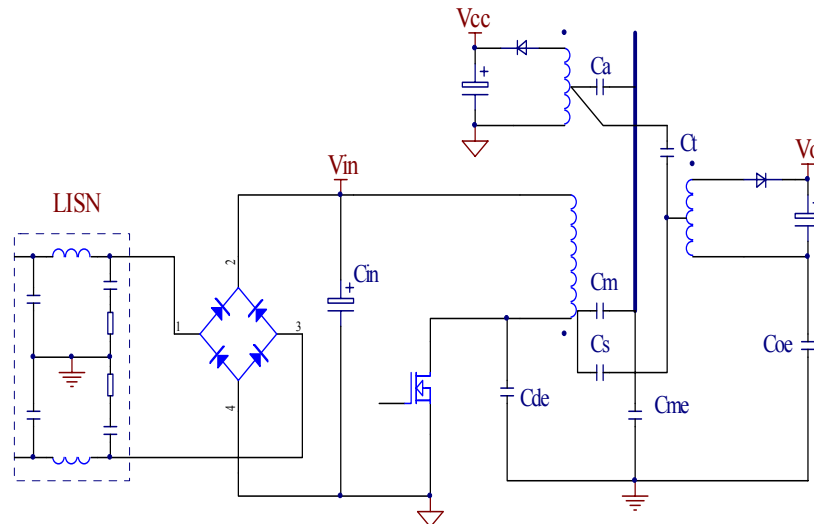


Figure 16: the coupling paths for CM currents

In figure 17, most of the current of C_s is bypassed through Y capacitor to primary the static point because the value of Y_2 is much larger than the stray capacitances C_{oe} so nearly all of the common mode current flow through it. If it is sufficiently larger, then it will have negligible voltage ripple and no longer contain a high frequency component. It can be proved by the voltage waveforms measured by the oscilloscope between primary and secondary cold point. As a result, common mode currents are reduced to a great degree. It can be noted that Y capacitor should be connected directly to the pins of the transformer and they must be cold points at the same time. As a rule of thumb, if the power MOSFET dV/dt is greater at turning on than at turning off, connect Y_2 to the return, but if turnoff is faster, then connect it to the positive rail.

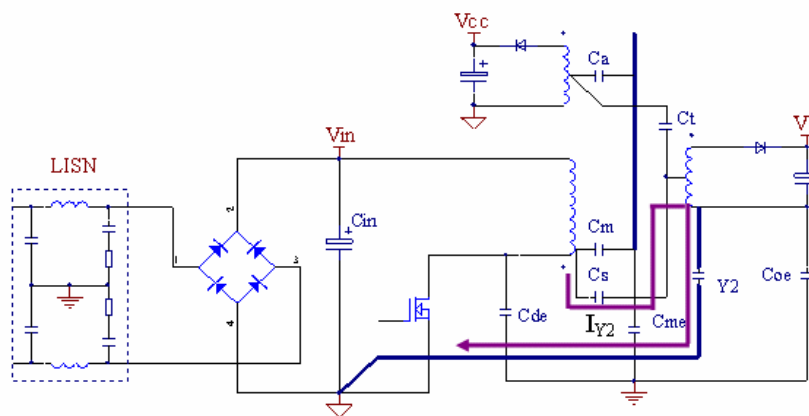


Figure 17: The function of Y capacitor

It should be stressed that points whose voltages do not vary are called cold or static point. Inversely, they are hot or dynamic points. Cold points in the circuit can be changed by changing the positions of the diodes. A, B and V_{in} are cold points and D, B and E are cold points in figure 18. Accordingly, A, V_{cc} V_o , V_{in} are cold points and F, D and G are cold points in figure 19.

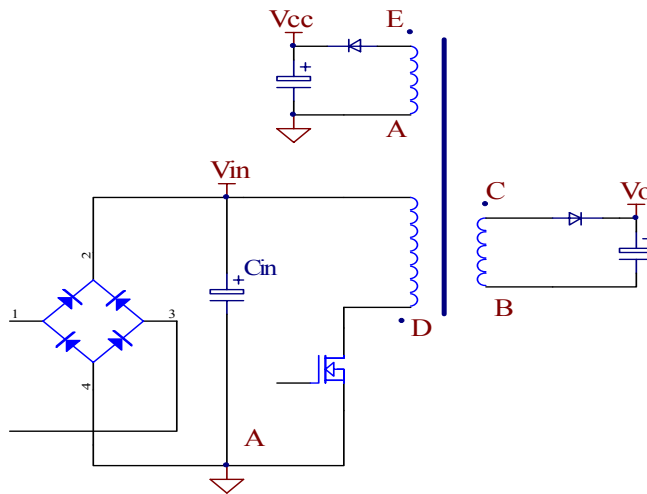


Figure 18: Cold points in the circuit

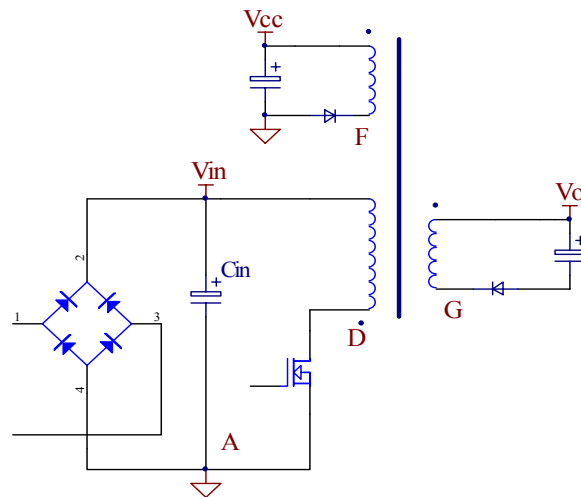


Figure 19: Adjusted cold points in the circuit

It can not be effectively attenuated by only using the CM filter without Y2 capacitor. In this paper, attentions are concentrated on cancellation techniques to reduce the effect of these capacitances by designing the structure of the transformer. We only discuss the instantaneous period during MOSFET turning off below in that the amplitude of the drain to source voltage variation is considerable great during this course.

Bear in mind for ever that rapidly changing voltage and current is the predetermination condition for CM and DM currents through the parasitic capacitances.

Common currents can be caused through $C_m + C_{me}$ and $C_{me} + C_a$ respectively owing to changing voltage of auxiliary winding and the inner layer of primary winding.

Part of the currents between every layer of primary winding is served as DM currents. Rest of them can go through directly to secondary winding through C_s . Changing voltages between primary as well as auxiliary winding and secondary winding can cause common mode current respectively through C_s and C_t . The value of the former is much more than that of the latter because the amplitude of the voltage between primary winding and secondary winding is much higher. Their directions based on their voltage variation each other can be shown in figure 20 if all cold points are placed like that. The dark points are cold points. Common mode currents from primary to secondary side are very high owing to lacked of Y2 capacitor.

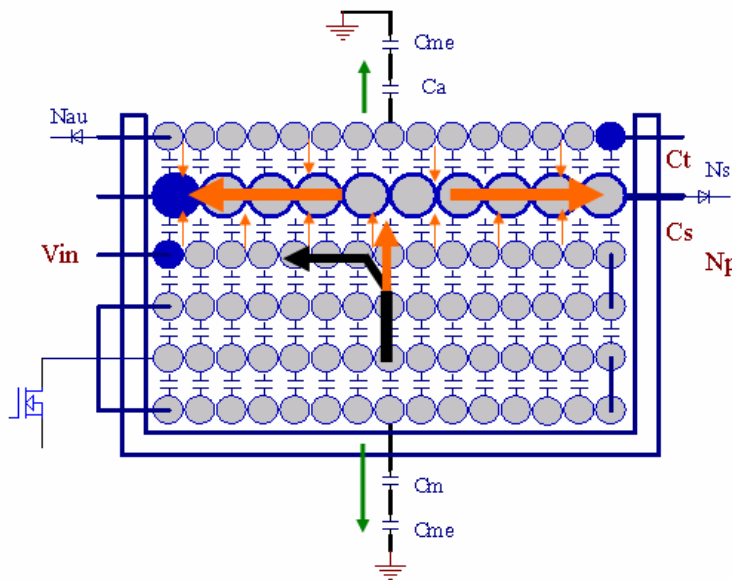


Figure 20: The current flow without changing cold points

If the positions of related cold points are adjusted accordingly, common mode currents can be reduced or cancelled when the direction of the currents through C_t are the same as that through C_s . It can be accomplished if the voltage variations of primary and auxiliary side are ensured to be opposite as shown in figure 21.

Auxiliary winding and secondary winding rectifier should be both chosen on the low sides. So the voltage swings are opposite on the transition. At

the same time, all cold points are wound close to the cold point of secondary winding.

There are not currents through the capacitance without the voltage variation. As a results there are not current between cold points and cold points. The value of the current will be reduced if the amplitude of the voltage variation is reduced.

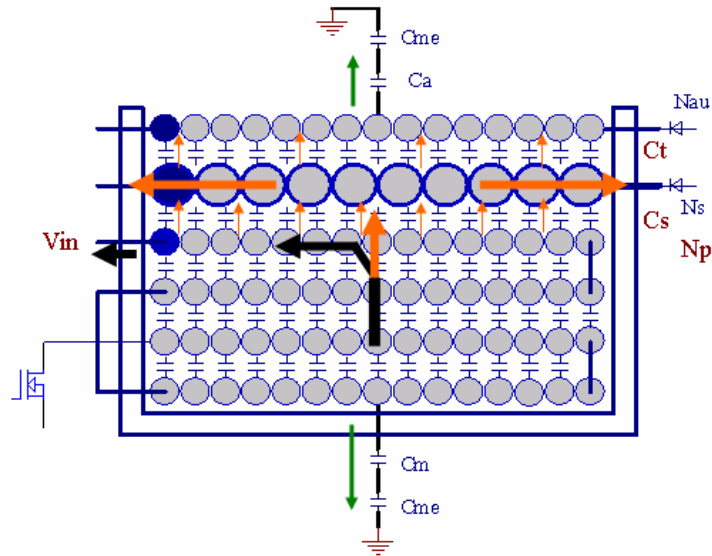


Figure 21: The current flow with changing cold points

To go further step, a copper foil is placed inside the most inner layer covering the breadth of the bobbin and the middle point of the copper is connected to primary cold point by the wire in figure 22.

The voltage of the copper 1 is basically stable so the amplitudes of the voltage variation between the magnetic core and the copper 1 is reduced compared with the voltage between the magnetic core and the most inner layer of primary. The current through C_{mc} and C_{me} is greatly reduced. Similarly, the current through C_{pc1} is also reduced significantly. At the same time, this current goes into primary cold points so that it has no contribution to common mode currents.

Once again, another copper foil is placed between primary and secondary winding. The principle is the same as above. The current between the copper 2 and secondary winding is so small. The current between primary winding and the copper 2 flows into primary cold point so that it has little contribution to common mode currents. Part of the current of interwinding capacitances of primary winding will go into secondary winding without the copper 2 and served as common mode current. The middle point of the copper 2 is also connected to primary cold point by the wire.

Take precaution that two terminals of the copper foil must overlap and not be short circuit. They should be insulated each other by the tape at the point of overlap.

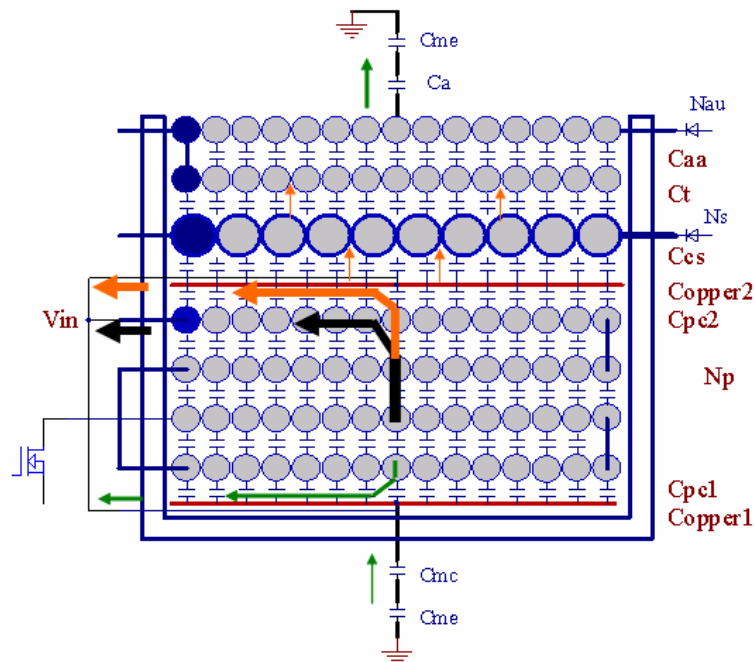


Figure 22: The current flow with further cancellation

The wrapped direction of two copper foils should be same. Otherwise, the reactance inside two coppers will increase due to the interaction of magnetic flux caused by the current inside two coppers.

In this situation, the current between auxiliary and secondary winding is relatively high. There are two ways to compensate it.

① Adding a shielding winding inside auxiliary winding.

The twist direction of shielding winding is the same as that of auxiliary winding. Their same polarity points, one of which is the cold point of auxiliary winding, are connected together as shown in figure 22. Another terminal of auxiliary winding is floating. The amplitudes and directions of their voltage variation are both same so there is not current between them. The induced voltage of shielding winding will resist the current to flow inside it because the terminal of shielding winding is floating. It can also be explained from the polarity of the voltage and the direction of the current in shielding winding.

② Adding the third layer copper foil inside auxiliary winding.

The middle point of the third copper is connected to the middle of auxiliary winding. The flowing directions of the currents between auxiliary winding as well as secondary winding and this copper foil are analyzed as follows. The directions of half of auxiliary on the left is reverse with that on the right owing the voltage of the copper is equal to

the voltage of the middle point of auxiliary. As a result, the circular current flows between the copper and auxiliary winding and be consumed by themselves. Likely, this kind of current can be caused between secondary winding and the copper. What is more, the amplitude of the voltage variation between secondary winding and the copper is reduced owing to incorporation of the copper. Two ends of the copper should also be insulated each other by the tape at the point of overlap.

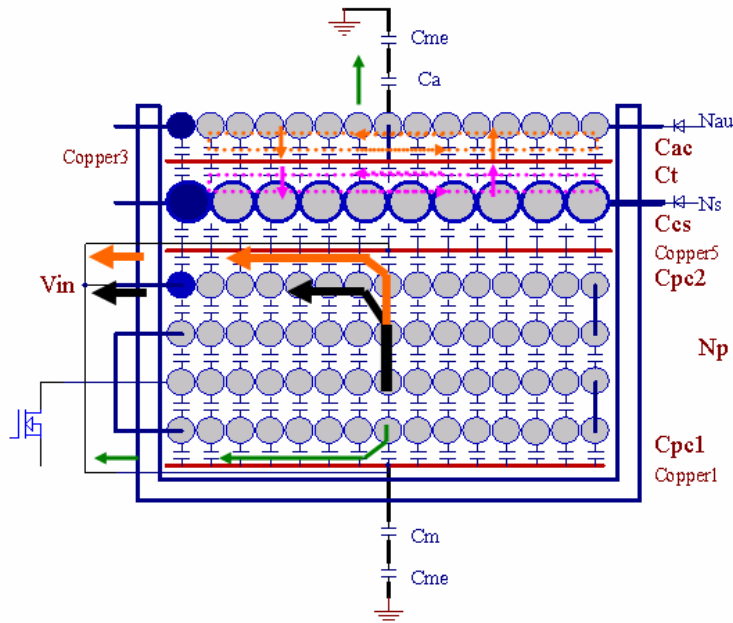


Figure 23: The cancellation for auxiliary winding with the copper

We do not adopt this solution because it needs an additional pin of the transformer during the course of making the transformer. But it can offer you a tip for the cancellation design about the transformer.

The solution in figure 22 is the final structure of the transformer for our No Y Cap charger.

We discuss differential mode and common mode interference separately. In practice, two types of the interferences can commute each other though unbalance noise current path. This topic is outside the content of this paper and not discussed in detail.

3 Radiated emissions of EMI

3.1 The electric and magnetic field radiation

Test for radiated emissions is done in the particular enclosure RF screen room to shield the test setup from any extraneous

RF signals from other generators or reflections. The standard specifications designate the requirement of antenna and its distance and orientation with respect to the EUT.

The EUT is put on the table, which is always rotating during the process of the test. The antenna set at the horizontal and vertical positions respectively is sweeping all radiating angles.

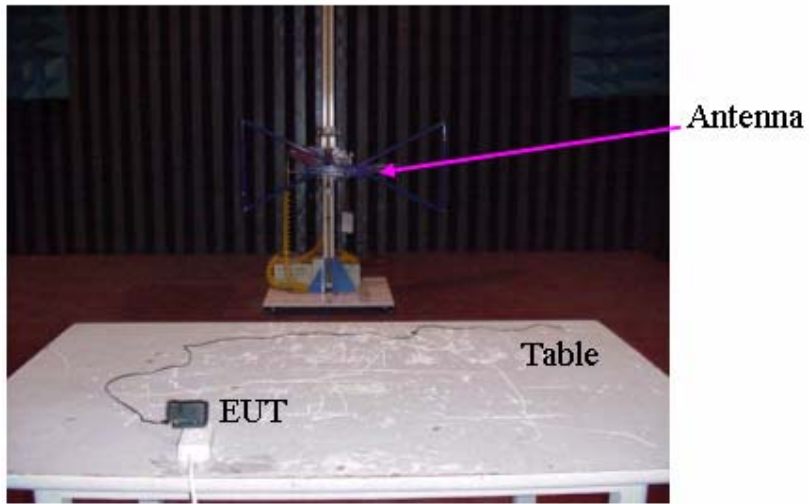


Figure 24: RE test

The radiated EMI can also result from an electric field due to du/dt and a magnetic field due to di/dt . The hot points of the transformer with high du/dt are all the sources for the electric field radiation. So space capacitances as to these points are the contributors of forming an electric field and common mode current for conducted emissions.

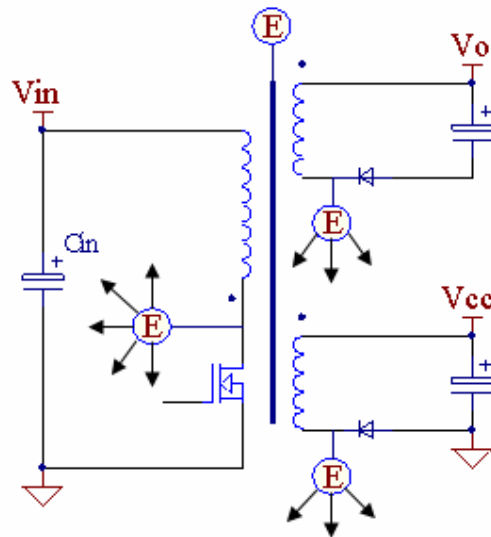
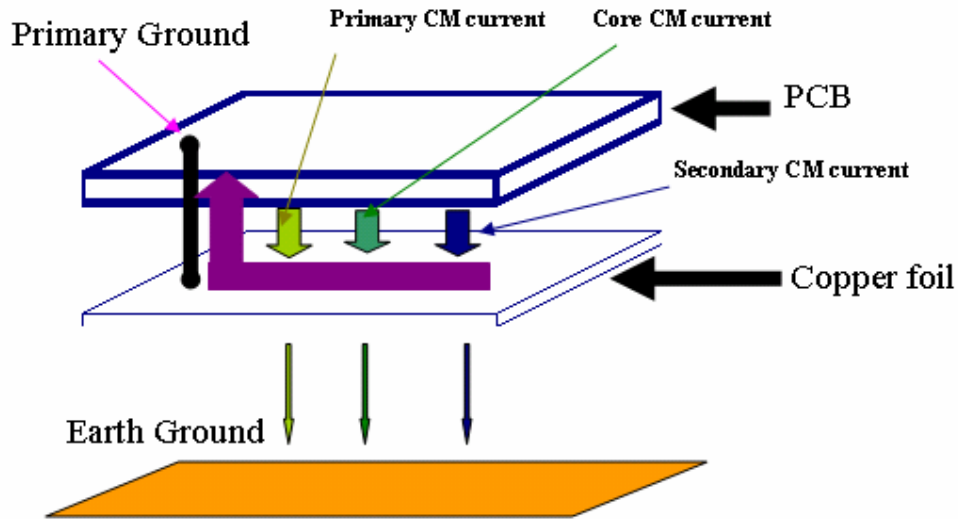


Figure 25: The electric field radiation

It means that common mode inductor is helpful to attenuate the noises not only for radiated emissions but also for conducted emissions. The amplitude of the voltage variation of primary side is much higher to

dominate the electric field radiation. Note that the core with the variation voltage is also a radiation source.

A sheet of copper or another single layer PCB without any device, which is connected to primary ground, is put below the whole PCB of the charger. It can also reduce electric field radiation and conduction emission.



The circular loop with high di/dt can cause the magnetic field radiation though the parasitic inductance of internal wiring. The secondary rectifying loop with much higher di/dt predominate the magnetic field radiation. The directions of magnetic field during these loops caused by di/dt are shown in figure

The inductance of the high di/dt current loop is a function of the area enclosed by the loop. The PCB layout is very critical. These loops, particularly, secondary rectifying loop, should be short and wide as possible because they are the good antennas.

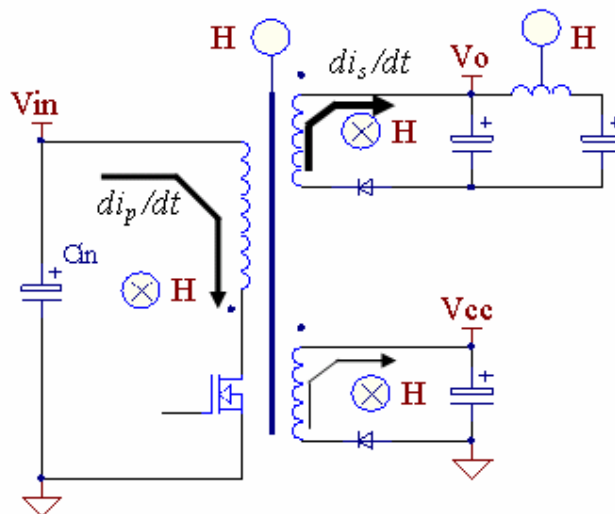


Figure 26: The electric field radiation

The stray magnetic field from the transformer is the source for the magnetic field radiation. It is also caused by the gaps in the core. Opening gaps during both side legs of the core causes much more stray field. Hence the gap should be grind in the center leg.

The transformer structure with interleaved primary winding sandwiched secondary winding can reduce the leakage inductance between primary and secondary windings but increase the capacitance. The usage of the copper covered outside of the transformer is helpful for radiation emissions because the leakage magnetic fields result in the eddy currents in the copper, in turn, which creates an opposing magnetic field to cancel the stray field. So the ends of the copper must be soldered well as a conductive enclosure path to eddy currents.

This kind of rod core for output differential mode inductor is good antenna but poor for radiation emissions. It is also potential generators of stray magnetic fields.

A bead in series with drain of VIPer12A, a capacitor in parallel with the diode of RCD clamp circuit, using 1N4007 instead of the fast diode, RC in parallel with output diode are all helpful for the radiation emissions in figure 3.

Note that the system is valuated with output wire connected to the load resistor. The long output wires become the radiators in that it can amplify the output common mode current, that is, high frequency conducted emissions, to generate an radiation field in the space and increase the total radiated noise. As a result, the usage of the output common inductor is unavoidable difficultly, which can attenuate not only the conducted emission noises but also the radiated emission noises.

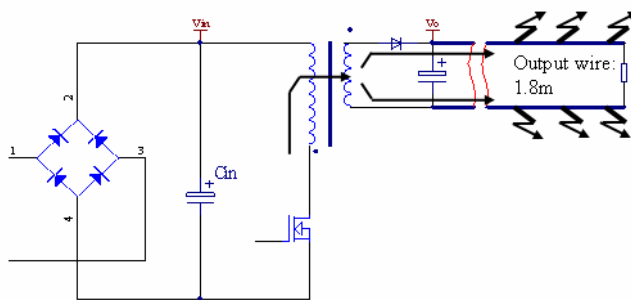


Figure 27: RE from Common Mode Current

In fact, conducted and radiated energy can be transformed back to forth each other. We do not discuss this topic because it is very complicated.

3.2 The design of Common Mode Filter

Each winding of common mode filter is connected in series with one of the output power lines. Magnetic fluxes in the core created by each winding are opposite in phase and cancelled each other when the load current flows through each winding. So it can not attenuate load current except for small losses in the dc resistance of the windings. However it can attenuate common mode currents because common mode currents generate flux in the core.

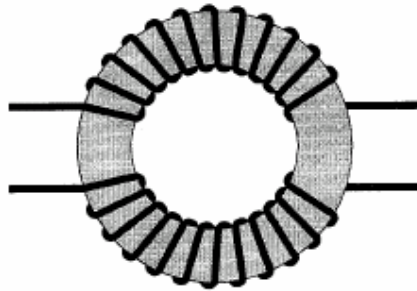


Figure 27: The common mode filter

① Select the core material

The ferrite with high impedance is the most appropriate and cost effective in the frequency band of the unwanted noise.

② Set the inductor impedance

The impedance from 50~100Ω is normally specified as a minimum at a given frequency, Calculating the inductance from following equation:

$$Z = \omega L$$

③ Selecting the shape and size

The inexpensive and low leakage toroids are best for a common mode filter but must be wound by hand.

It is arbitrary to choose the core size based on PCB size. Core's cost and size must be compromised. Of course, it can be selected based on the LI product in the core datasheet.

④ Calculate the number of turns

The number of turns of each winding is determined from the core's AL value as follows:

$$N = (L \times 10^6 A_L)^{0.5}$$

⑤ Calculate the wire diameter

The current determines the wire size. The current density is from 400~800A/cm².

Single layer of the winding can be designed as much as possible to minimize the winding capacitance and prevent core saturation due to asymmetrical windings.

3.3 Jitter or frequency modulation

Before we finish the topic, jitter or frequency modulation should be mentioned. The noise is specified at special frequencies and tested by constant step, such as 10KHz for CE so if the switching frequency is modulated by a low frequency, the noise will be dissipate or spread out wide bandwidth by the random modulation, which can not focus on some high order harmonics of constant basic frequency. It can only greatly reduce the average value instead of the peak value. The principle is shown in figure 27. The jittering range of the frequency is confined to a small value compared with the switching frequency otherwise the system is unstable.

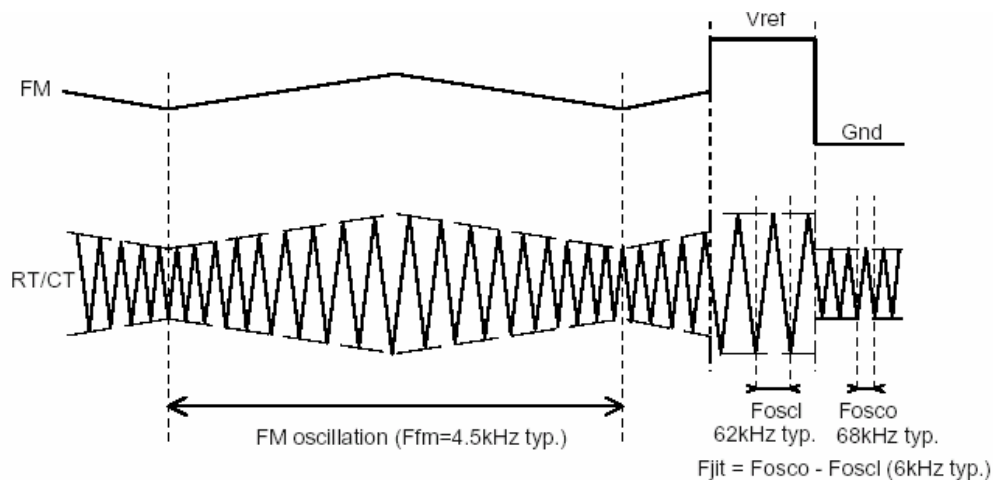
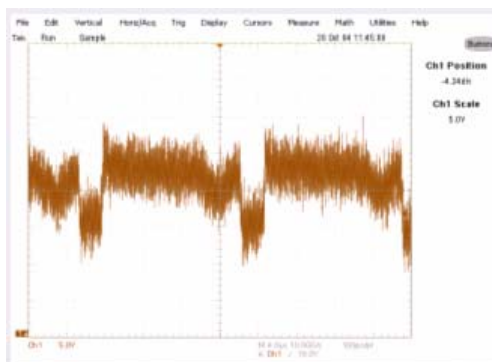


Figure 27: The frequency modulation

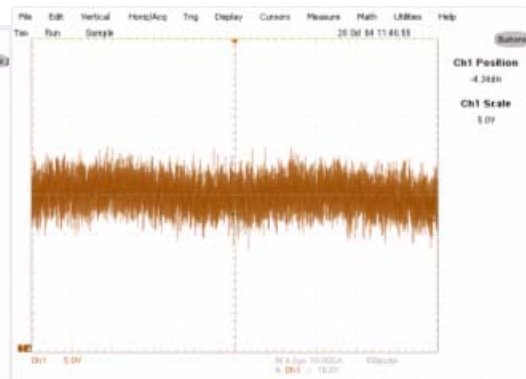
3.4 The floating voltage

3.4.1 The floating voltage waveforms cross primary and secondary cold point (Ch1 scale: 5V, Time: 4us)

► Common structure



► New structure

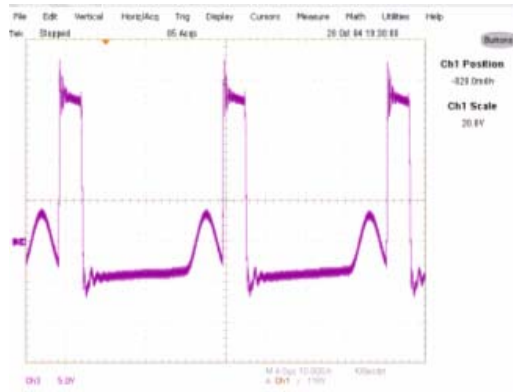


The amplitude of the waveforms of the transformer with common structure is 10V. The waveforms have evident high frequency components.

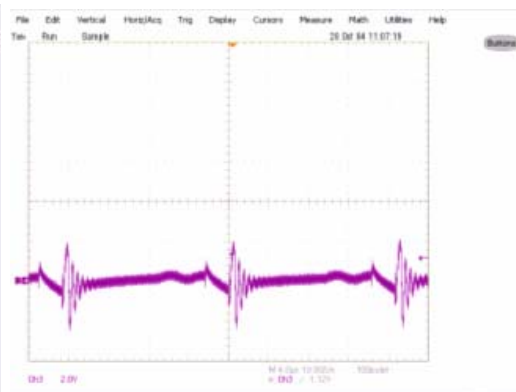
The amplitude of the waveforms of the transformer with new structure is 5V. The waveforms have no evident high frequency components.

3.4.2 The floating voltage waveforms on the core (Ch1 scale: 5V, Time: 4us)

► Common structure



► New structure



The amplitude of the waveforms of the transformer with common structure is 18V. The waveforms have evident high frequency components. The amplitude of the waveforms of the transformer with new structure is 5V. The waveforms have no evident high frequency components.

References

1 MAGNETICS Ferrites 2002

2 Bob Mammano and Bruce Carsten, Understanding and Optimizing Electromagnetic Compatibility in SMPS