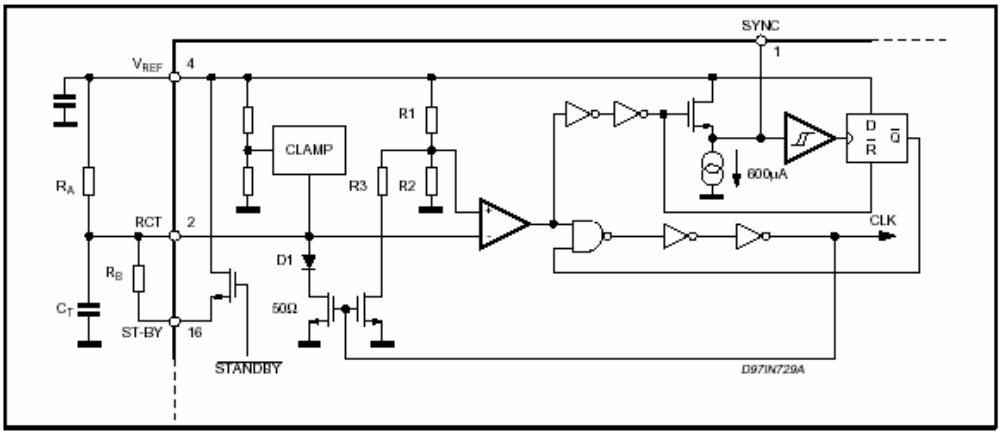
Figure 23. Oscillator and synchronization internal schematic.



The oscillation frequency can be established with the aid of the diagrams of fig. 14, where R_T will be intended as the parallel of R_A and R_B in normal operation and $R_T = R_A$ in standby, or considering the following approximate relationships:

$$f_{osc} \cong \frac{1}{C_T \cdot (0.693 \cdot (R_A \,//\, R_B) + K_T} \quad (1),$$

which gives the normal operating frequency, and:

$$f_{SB} \cong \frac{1}{C_T \cdot (0.693 \cdot R_A + K_T)} \quad (2),$$

which gives the standby frequency, that is the one the converter will operate at when lightly loaded.

In the above expressions, RA // RB means:

$$R_A // R_B = \frac{R_A \cdot R_B}{R_A + R_B},$$

while K_T is defined as:

$$K_T = \begin{cases} 90 & V_{15} = VREF \\ 160 & V_{15} = GND/OPEN \end{cases} \quad (3),$$

and is related to the duration of the falling-edge of the sawtooth:

$$T_d \cong 30 \cdot 10^{-9} + K_T \cdot C_T \quad (4).$$

T_d is also the duration of the sync pulses delivered at pin 1 and defines the upper extreme of the duty cycle range, D_x (see pin 15 for D_X definition and calculation) since the output is held low during the falling edge.

In case V15 is connected to VREF, however, the switching frequency will be a half the values taken from fig. 14 or resulting from (1) and (2).

To prevent the oscillator frequency from switching back and forth from f_{osc} to f_{SB}, the ratio f_{osc} / f_{SB} must not exceed 5.5.

If during normal operation the IC is to be synchronized to an external oscillator, R_A, R_B and C_T should be selected for a f_{osc} lower than the master frequency in any condition (typically, 10-20%), depending also on the tolerance of the parts.

Pin 3. DC (Duty Cycle Control). By biasing this pin with a voltage between 1 and 3 V it is possible to set the maximum duty cycle between 0 and the upper extreme D_x (see pin 15).

If D_{max} is the desired maximum duty cycle, the voltage V3 to be applied to pin 3 is:

$$V_3 = 5 - 2^{(2-Dmax)} \quad (5)$$

D_{max} is determined by internal comparison between V3 and the oscillator ramp (see fig. 24), thus in case the device is synchronized to an external frequency f_{ext} (and therefore the oscillator amplitude is reduced), (5) changes into:

$$V_3 = 5 - 4 \cdot \exp\left(-\frac{D_{max}}{R_T \cdot C_T \cdot f_{ext}}\right) \quad (6)$$

A voltage below 1V will inhibit the driver output stage. This could be used for a not-latched device disable, for example in case of overvoltage protection (see application ideas).

If no limitation on the maximum duty cycle is required (i.e. $D_{MAX} = D_X$), the pin has to be left floating. An internal pull-up (see fig. 24) holds the voltage above 3V. Should the pin pick up noise (e.g.